RL78 Family

Capacitive Touch Sensing Unit (CTSU2L) Operation Explanation

Introduction

This application note explains Capacitive Touch Sensing Unit (CTSU2L).

The number of output channels of the capacitive sensing unit depends on the product.

ROM size	64 to 128 Kbytes								
Pin count	30	32	36	40, 44	48	52	64	80	100
Number of the CTSU2L output channels	2 (TS00, TS01)	3 (TS00 to TS02)	5 (TS00 to TS04)	6 (TS00 to TS05)	8 (TS00 to TS07)	10 (TS00 to TS09)	12 (TS00 to TS11)	(TS00 to TS15, TS20 to TS33)	32 (TS00 to TS15, TS20 to TS35)

ROM size	192 to 768 Kbytes									
Pin count	30	32	36	40	44	48	52	64	80	100, 128
Number of the CTSU2L output channels	6 (TS00, TS01, TS20, TS21, TS26, TS27)	7 (TS00 to TS02, TS20, TS21, TS26, TS27)	11 (TS00 to TS04, TS20 to TS23, TS26, TS27)	13 (TS00 to TS05, TS20 to TS24, TS26, TS27)	14 (TS00 to TS05, TS20 to TS27)	16 (TS00 to TS07, TS20 to TS27)	20 (TS00 to TS09, TS20 to TS29)	22 (TS00 to TS11, TS20 to TS29)	30 (TS00 to TS15, TS20 to TS33)	32 (TS00 to TS15, TS20 to TS35)

The Capacitive Sensing Unit (CTSU2L) measures the electrostatic capacitance of the capacitive sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU2L to detect whether a finger is in contact with the capacitive sensor. The electrode surface of the capacitive sensor is usually enclosed with an electrical conductor so that a finger does not come into direct contact with the electrode.

As shown in Figure 1, electrostatic capacitance (parasitic capacitance) exists between the electrode and the surrounding conductors. Because the human body is an electrical conductor, when a finger is placed close to the electrode, the electrostatic capacitance value increases.

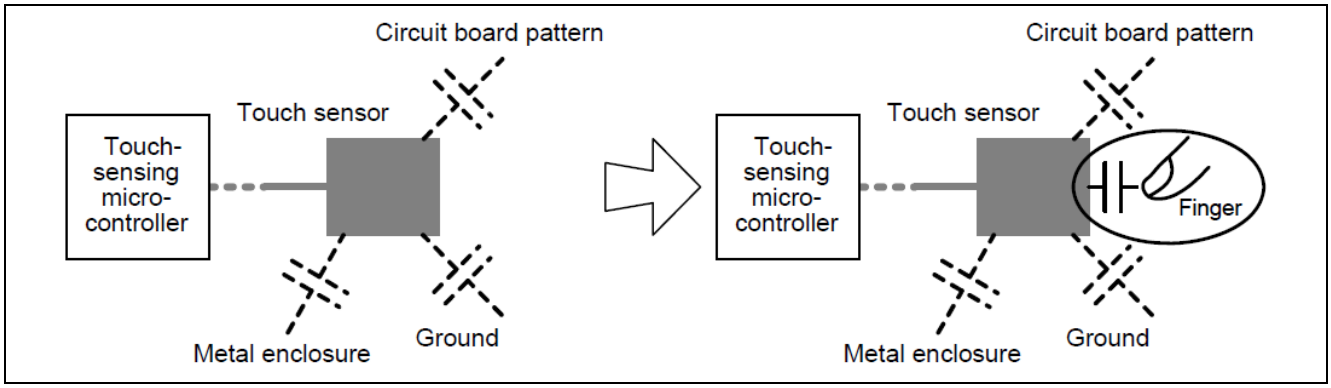

Figure 1 Increased Electrostatic Capacitance Because of the Presence of a Finger

Electrostatic capacitance is detected by the self-capacitance and mutual capacitance methods.

In the self-capacitance method, the CTSU detects electrostatic capacitance generated between a finger and a single electrode. In the mutual capacitance method, two electrodes are used; one electrode is used as a transmit electrode and the other electrode is used as a receive electrode. The CTSU detects a change in the electrostatic capacitance generated between these electrodes when a finger is placed close to them.

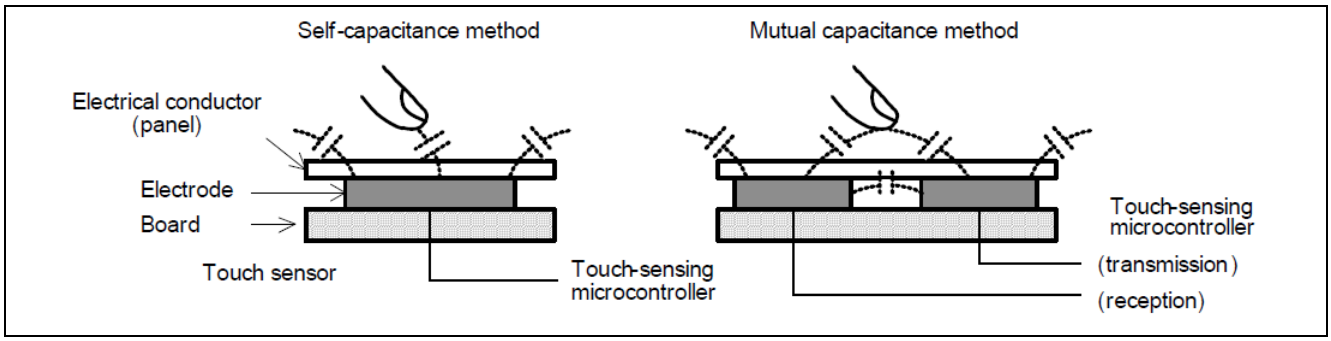

Figure 2 Self-capacitance Method and Mutual Capacitance Method

Electrostatic capacitance is measured by counting clock signal cycles whose frequency changes according to the amount of charged or discharged current for a specified period.

For details of the measurement operation principles, see application note.

Target Device

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Contents

1. Overview 4

2. Operation 6
2.1 Principles of measurement operation 6
2.2 Initial settings flow 9
2.3 Status counter 11
2.4 Measurement methods 12
2.4.1 Self-capacitance method operation 13
2.4.2 Operation of the mutual capacitance method 17
2.5 Scan mode 21
2.5.1 Single scan mode (CTSUCRAL.MD0 = 0) 21
2.5.2 Multi-scan mode (CTSUCRAL.MD0 = 1) 21
2.6 Sensor drive pulse 22
2.6.1 Random pulse mode (CTSUCRAH.SDPSEL = 0) 22
2.6.2 High resolution pulse mode (CTSUCRAH.SDPSEL = 1) 24
2.7 Switching power supply for transmit pins 25
2.8 Multi-clock measurement 28
2.9 Items common to different modes 29
2.9.1 Sensor stabilization wait time and measurement time 29

2.9.2 Measurement start conditions and SNOOZE function 31
2.9.3 Interrupts 34

3. Usage Notes 36
3.1 Measurement result data (CTSUSC register) 36
3.2 Software trigger 36
3.3 External trigger 36
3.4 Notes on forced stop 37
3.5 TSCAP pin 37
3.6 Setting the sampling cycle when applying jitter 37
3.7 Notes on measurement operation (CTSUCRAL.STRT bit = 1) 37
3.8 Prohibiting transmission power switching (TXVSEL and TXVSEL2 bits) after initial settings 38
3.9 Transmit pins in the self-capacitance method 38

Revision History 39

1. Overview

Table 1-1 lists the CTSU functions and Figure 1-1 shows a block diagram of the CTSU. Figure 1-2 shows the sensor drive pulse output clock configuration.

Table 1-1 CTSU Functions

Item		Configuration
CTSU2L operating voltage condition		V_{DD} = 1.8 to 5.5 V
Operating clock		fCLK/2, fCLK/4, or fCLK/8
Pins	Electrostatic capacitance measurement	TSm (m = 00 to 15, 20 to 35) up to 32 channels
	Secondary measurement power capacitor connection pin	TSCAP (10 nF) We recommend connecting a 10-nF capacitor.
Measurement mode	Self-capacitance measurement mode	The charge / discharge current to the electrode for the self-capacitance method is measured.
	Mutual capacitance measurement mode	The charge / discharge current to the capacitance between the transmission / reception electrodes for the mutual capacitance method is measured.
	DC current measurement mode	The current from a measurement pin is measured.
Calibration mode		Characteristic correction function to current control oscillator for measurement
Noise prevention		Countermeasures to synchronous noise Majority decision by multi-frequency measurement using countermeasures to high-pass noise
Adjustment for each pin		Offset current adjustment function Sensor drive pulse frequency specification Measurement time specification
Measurement start conditions		Software trigger External trigger (ELCL)
Low-power function		SNOOZE function supported
Requests	Data transfer request	Channel measurement setting write request Measurement result read request
	Interrupt request	Measurement end interrupt request
Transmission power switching of mutual capacitance method		The power for transmission in the mutual capacitance method can be switched among V_{DD} (REGC), V_{DD} (GPIO), and V_{DD} (dedicated).

As shown in Figure 1-1, the CTSU consists of a status control block, a trigger control block, a clock control block, a channel control block, a port control block, a sensor drive pulse generator, a measurement block, an interrupt block, I/O register control block, a SNOOZE control block, and SFRs.

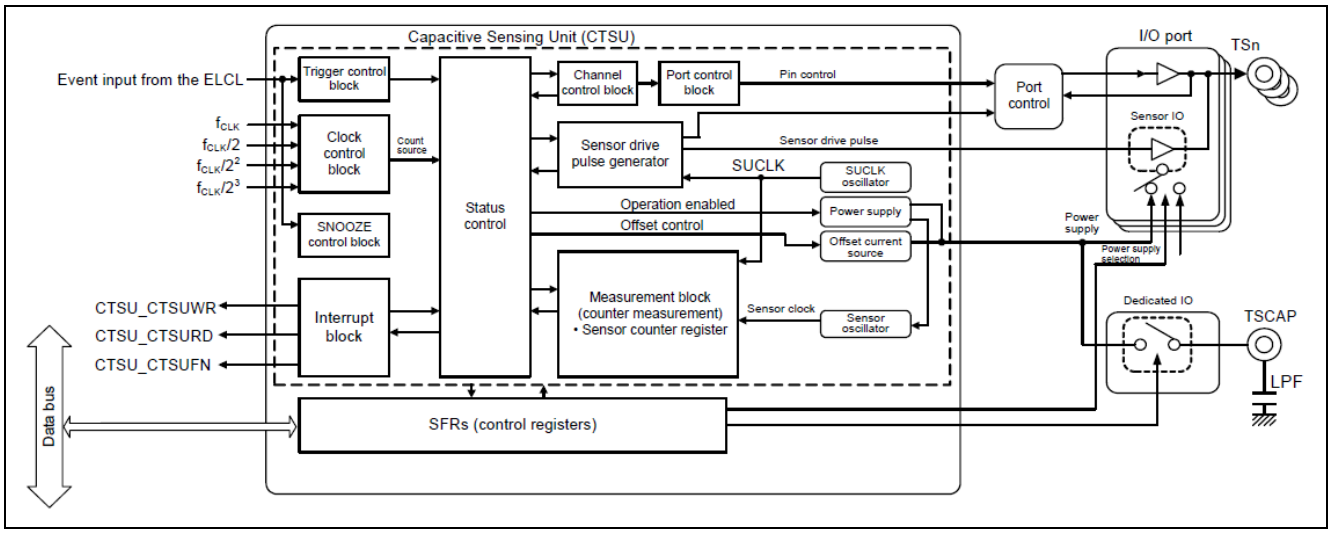

Figure 1-1 CTSU Block Diagram

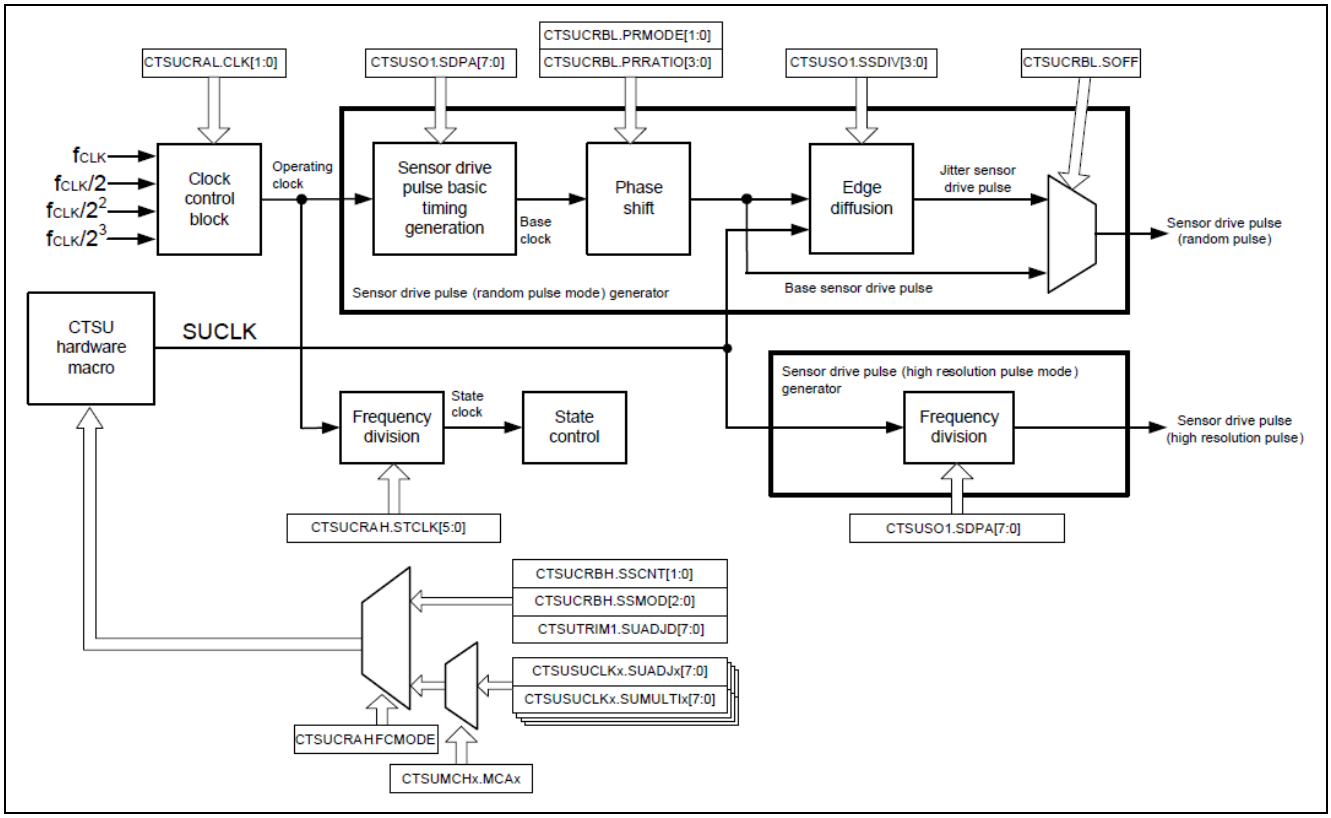

Figure 1-2 Sensor Drive Pulse Output Clock Configuration

Table 1-2 External Pins Used in CTSU

Pin name	Input/output	Function
TSm (m = 0 to 35)	Output	Electrostatic capacitance measurement pin, Mutual capacitance transmission pin, Active shield control pin, Current measurement pin
TSCAP	-	Secondary measurement power capacitor connection pin

2. Operation

2.1 Principles of measurement operation

Figure 2-1 shows the measurement circuit.

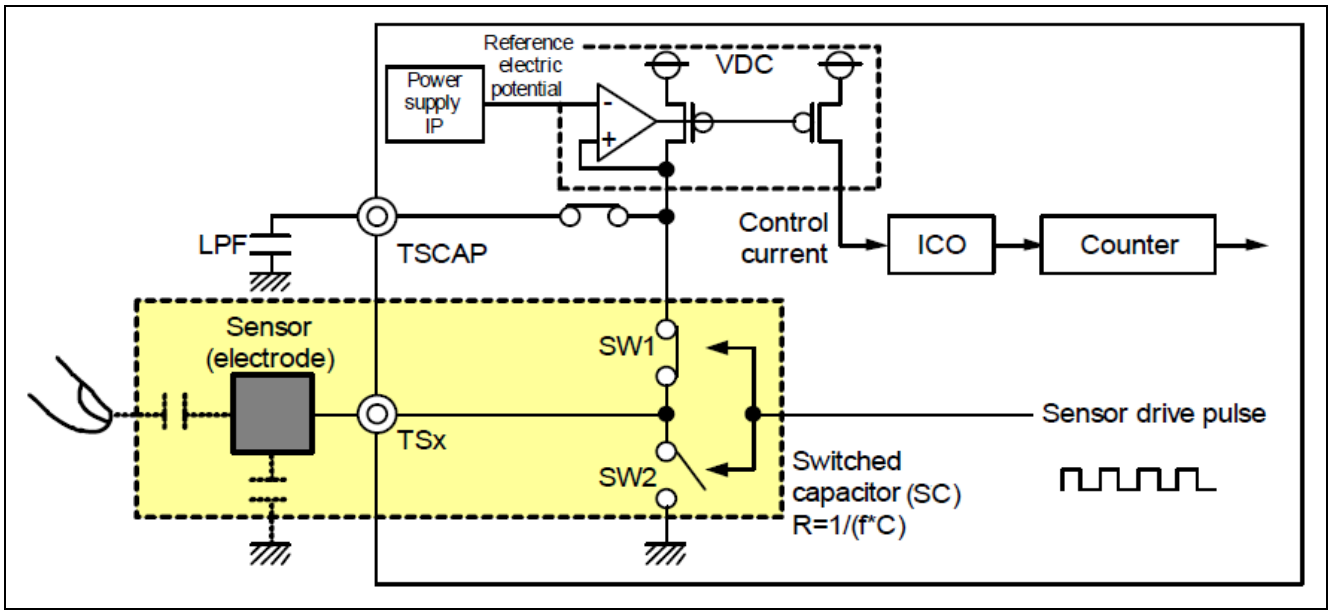

Figure 2-1 Measurement Circuit

Figure 2-2 to Figure 2-4 explain the electrostatic capacitance measurement operation principles of the CTSU current frequency conversion.

(1) The electrostatic capacitance of the electrode is charged by turning SW1 on and SW2 off (Figure 2-2).

(2) The charged capacitance is discharged by turning SW1 off and SW2 on (Figure 2-3).

Current flows through the switched capacitor filter by switching between (1) charging and (2) discharging at early timing. At this time, if a finger is in close proximity, the electrostatic capacitance changes, which varies the flowing current. A clock is generated by supplying the control current, which is proportional to the amount of current flowing through the switched capacitor filter, from the voltage down converter (VDC) circuit that generates TSCAP power supply to the ICO. The counter measures the clock frequency that varies depending on whether a finger is in close proximity. The software uses the read counter value to determine contact with a finger (Figure 2-3).

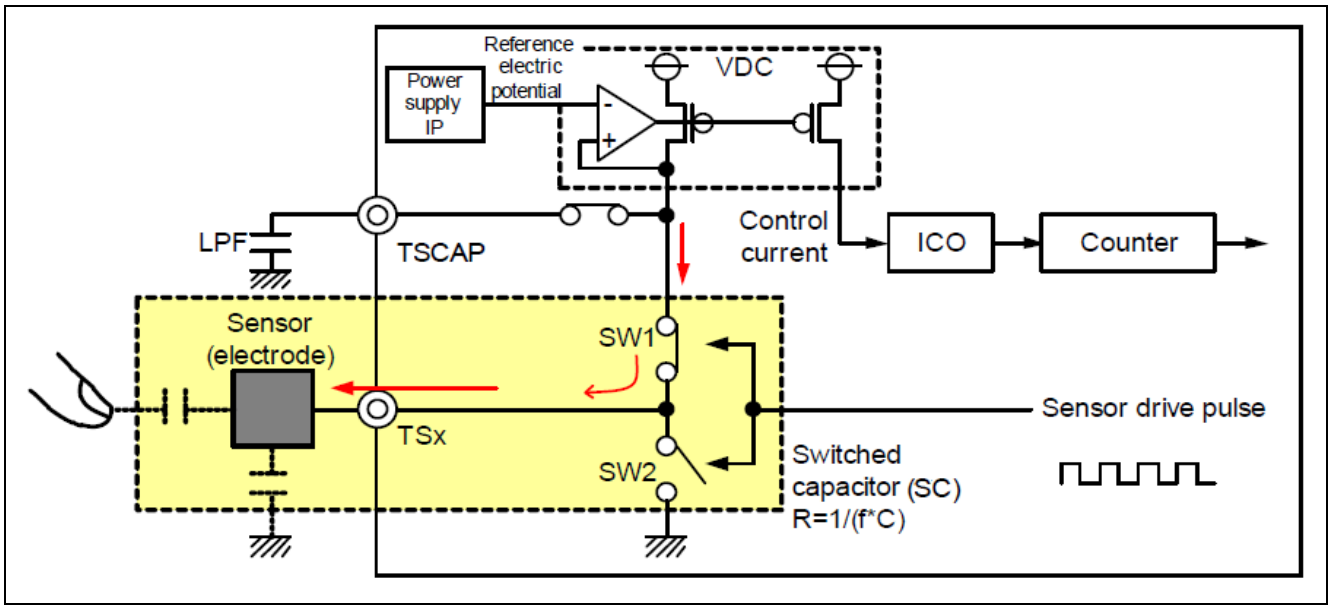

Figure 2-2 Charging Operation

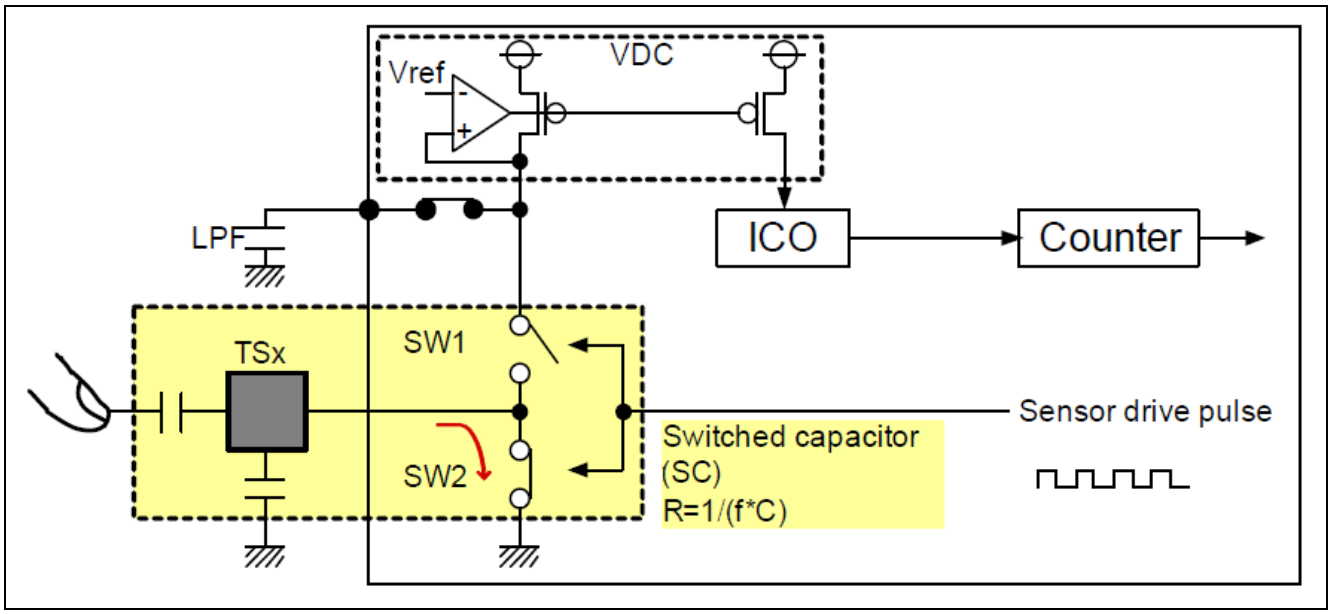

Figure 2-3 Discharging Operation

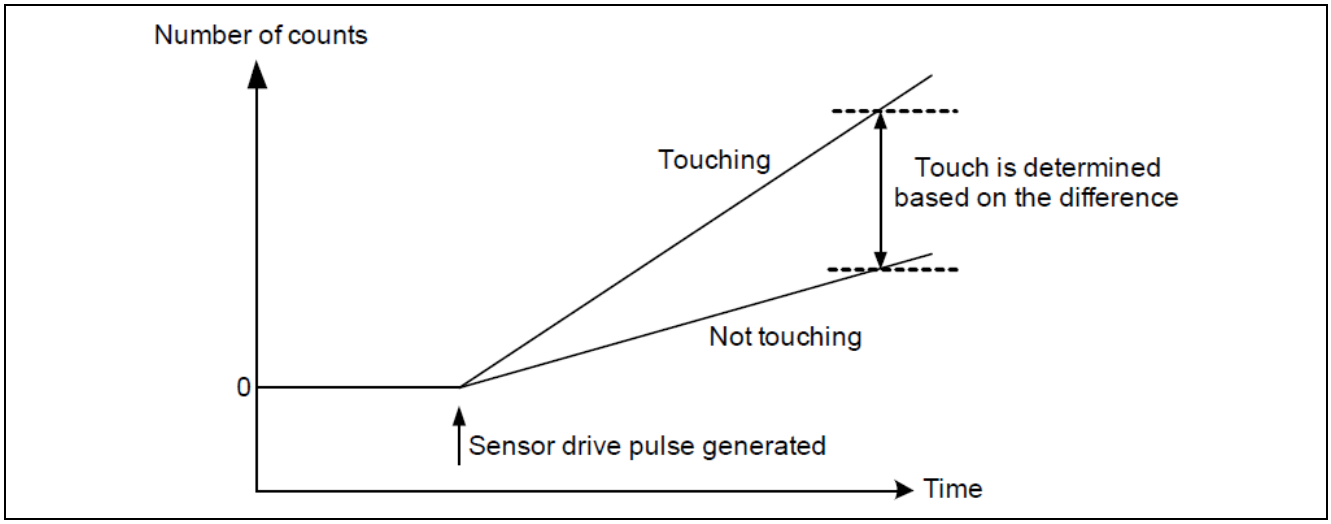

Figure 2-4 Change in Measured Value When a Finger is Touching or Not Touching

2.2 Initial settings flow

Figure 2-5 shows the flow for the CTSU initial settings.

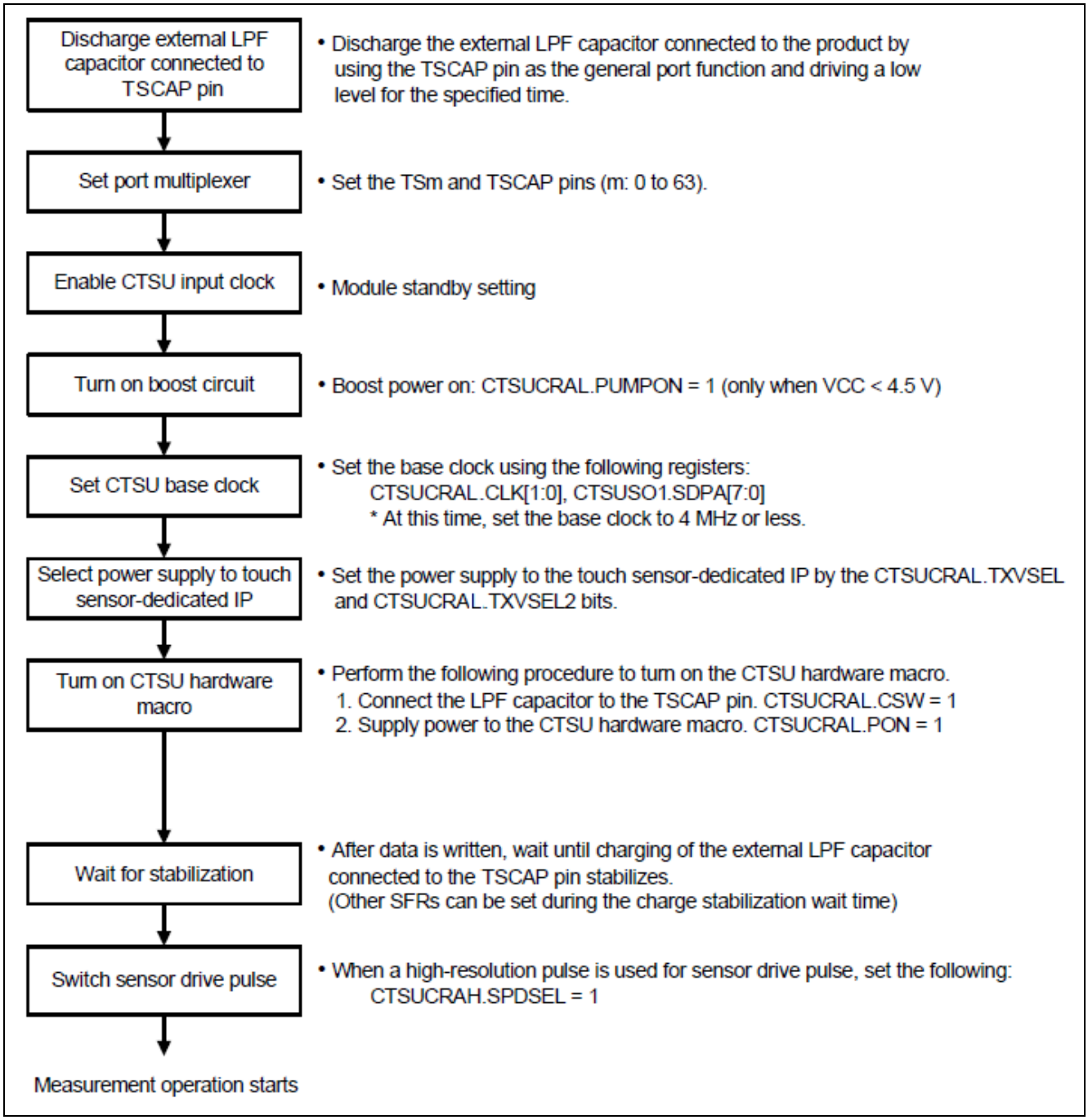

Figure 2-5 CTSU Initial Settings Flow

Figure 2-6 shows the flow for stopping CTSU operation and invoking the standby state.

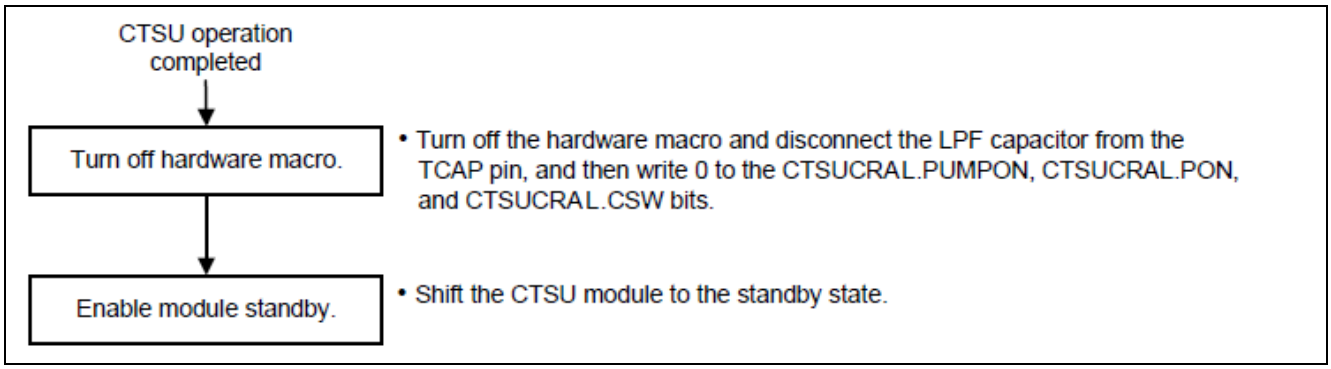

Figure 2-6 CTSU Stopping Flow

When restarting operation after it stops, follow the initial settings flow shown in Figure 2-5.

2.3 Status counter

The status counter indicates the current measurement status. The measurement status is shared by all three modes. Figure 2-7 shows the status operation transitions of the status counter.

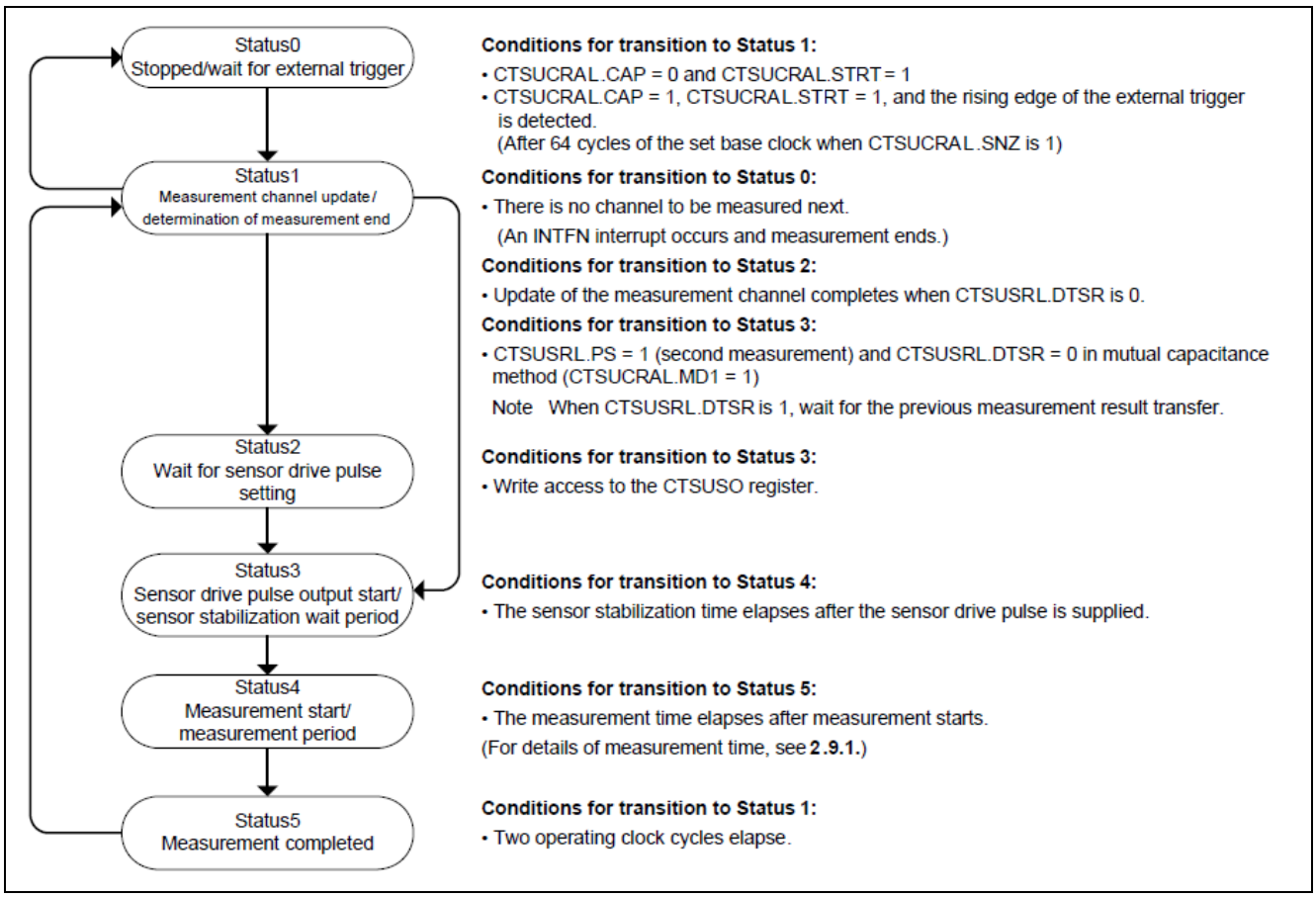

Figure 2-7 Status Operation Transitions

The status counter transitions to Status 0 after all of the specified measurement channels are measured.

The CTSUCRAL.STRT bit is cleared to 0 by hardware at a software trigger. When an external trigger is used, the CTSUCRAL.STRT bit remains 1 and the CTSU waits for the next trigger.

When operation is forced to stop (simultaneous writing 0 to the CTSUCRAL.STRT bit and writing 1 to the CTSUCRAL.INIT bit) during measurement or in the trigger waiting state, the status counter transitions to Status 0 and measurement stops.

If the channel to be measured is not set in the CTSUMCHL register, CTSUCHACn register (n = AL, AH, BL, BH for 64 or 36 channels, n = AL, AH for 12 or 24 channels), or CTSUCHTRCn register (n = AL, AH, BL, BH for 64 or 36 channels, n = AL, AH for 12 or 24 channels), the status counter transitions to Status 1, and then an INTFN_N interrupt is immediately generated and the status counter transitions to Status 0. The following shows situations where there is no channel to be measured.

- No measurement target channel is specified in the CTSUCHACn register.
- In single scan mode, the channel specified in the CTSUMCHL register is not a measurement target in the CTSUCHACn register.
- In the self-capacitance method, there is no receive channel to be measured on the combined settings of the CTSUCHACn and CTSUCHTRCn registers.
- In the mutual capacitance method, there is no transmit channel or receive channel to be measured on the combined settings of the CTSUCHACn and CTSUCHTRCn registers.

2.4 Measurement methods

The CTSU supports self-capacitance and mutual capacitance methods. Figure 2-8 illustrates the self-capacitance method and the mutual capacitance method.

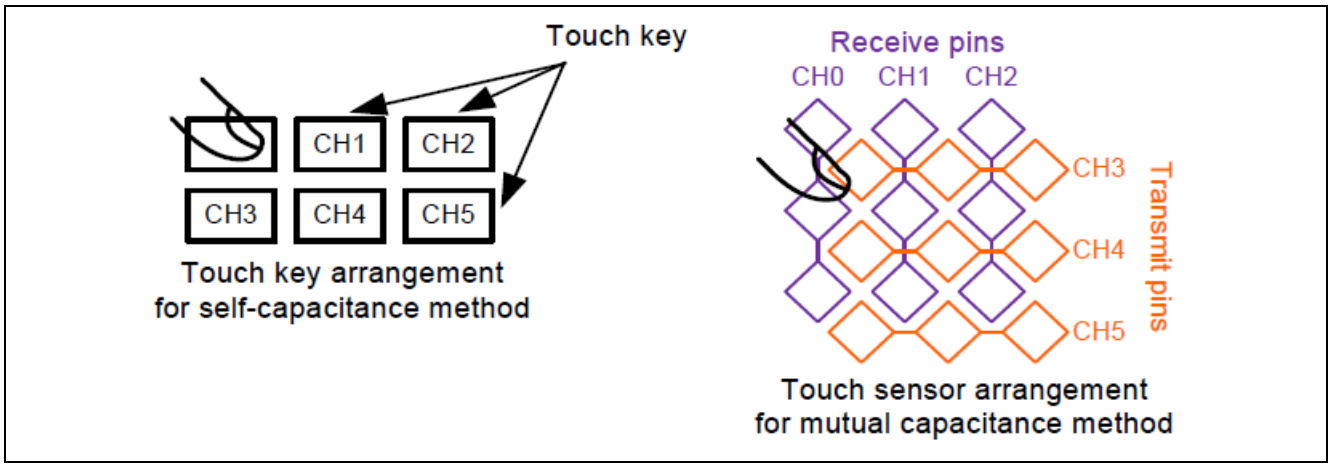

Figure 2-8 Overview of Self-capacitance Method and Mutual Capacitance Method

In the self-capacitance method, a single touch pin is allocated to a single touch key to measure individual electrostatic capacitance when a finger is in close proximity.

In the mutual capacitance method, the capacitance between two facing electrodes (transmit and receive pins) is measured.

2.4.1 Self-capacitance method operation

In the self-capacitance method, a single measurement pin is allocated to a single sensor to measure individual electrostatic capacitance. Scan mode (2.5) and sensor drive pulse (2.6) are selectable.

Figure 2-9 shows an operation example, and Figure 2-10 shows the timing chart.

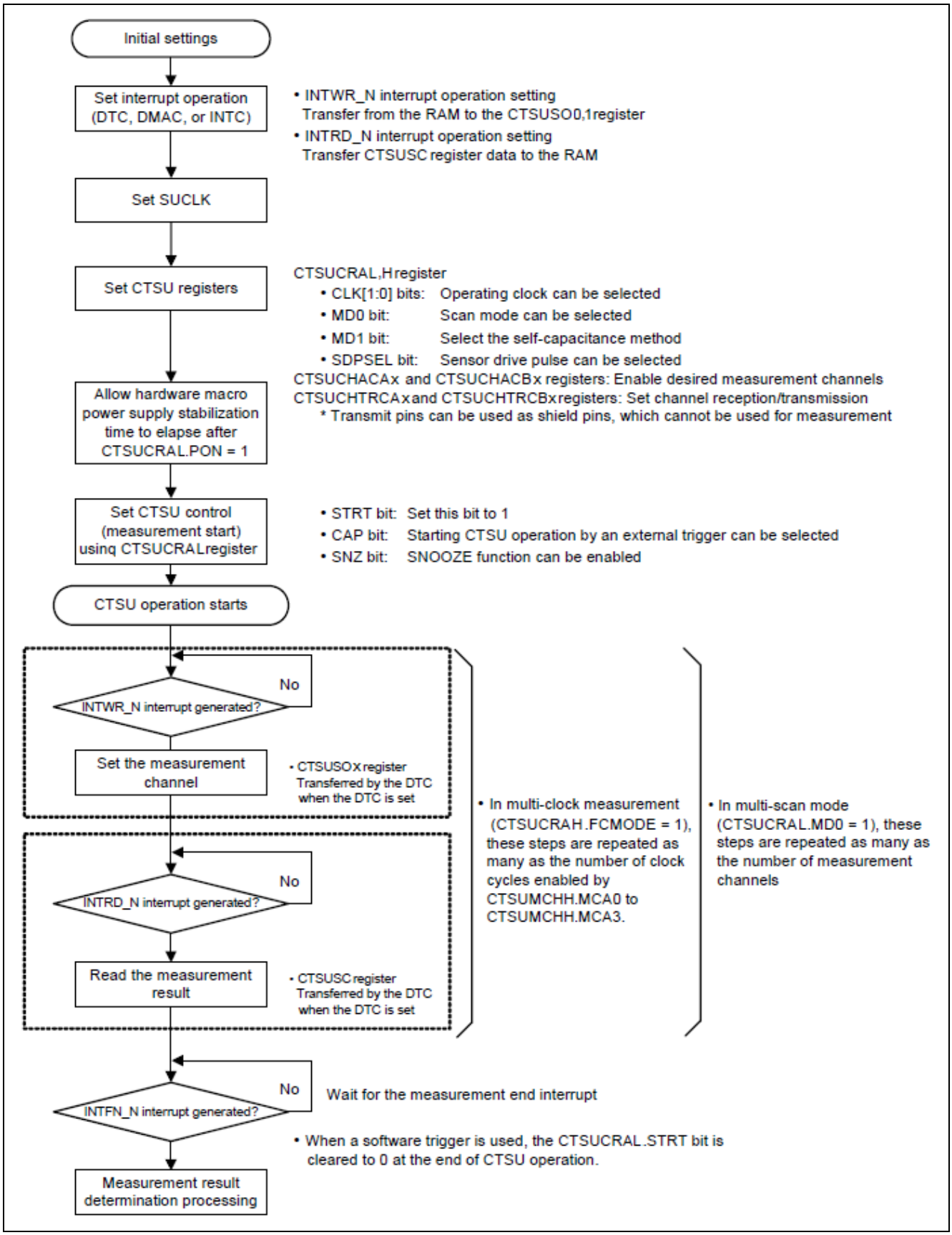

Figure 2-9 Software Flow and Operation Example for the Self-capacitance Method

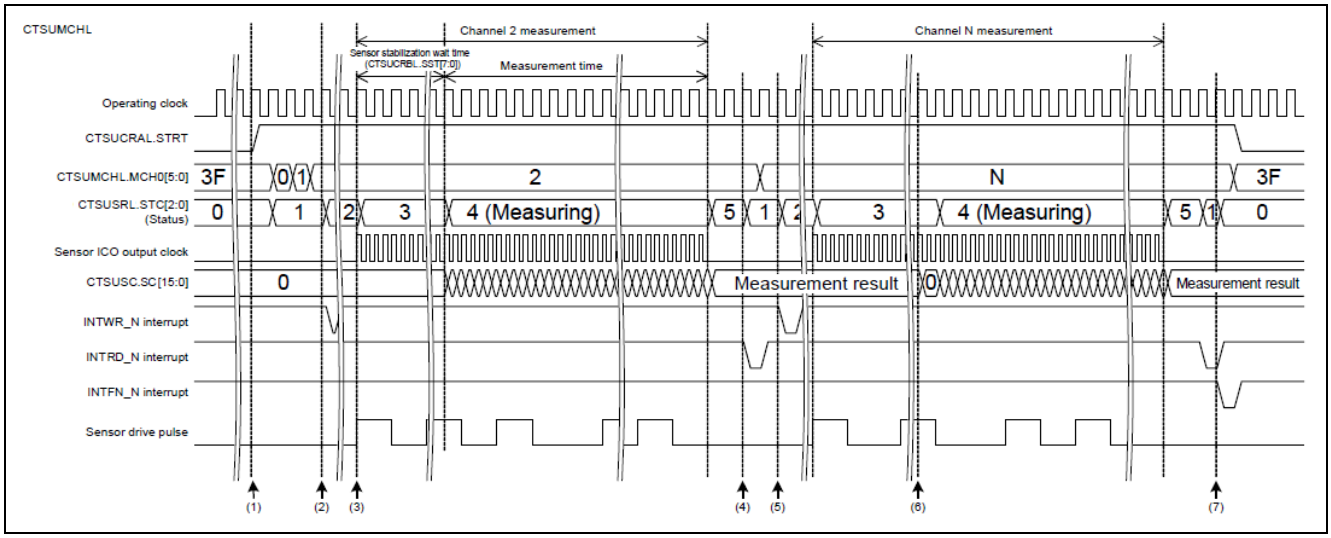

Figure 2-10 Timing Chart of the Self-capacitance Method (Software Trigger Selected as Measurement Start Condition)

The following describes the operation illustrated in Figure 2-10.

1. After various settings have been made, measurement starts when 1 is written to the CTSUCRAL.STRT bit.
2. The channel to be measured is determined in accordance with the set conditions, and then a request for setting the channel (INTWR_N interrupt) is output.
3. On completion of writing the measurement channel settings (CTSUSO0, CTSUSO1 register), the sensor drive pulse is output and the sensor ICO clock operates.
4. After the sensor stabilization wait time and the measurement period elapse and measurement ends, a measurement result read request (INTRD_N interrupt) is output.

   → In single scan mode, go to step 7.
5. After the channel to be measured is determined, a measurement channel setting request (INTWR_N interrupt) is output.
6. After the stabilization wait time elapses, the previous measurement result is cleared by reading it and measurement starts.
7. On completion of measurement for all channels, a measurement end interrupt (INTFN_N interrupt) is output to complete measurement (transition to Status 0).

Table 2-1 lists the measurement pin states in the self-capacitance method.

Table 2-1 Measurement Pin States in the Self-capacitance Method

Status	Receive channel measurement pins		Transmit channel measurement pins	ICO operation enable	Capacitive touch sensor-dedicated I/O operation
	Measured channel	Non-measured channel	Measured channel		
0	Low	Low/Hi-z	Low	Disabled	• All channels: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive
1	Low	Low/Hi-z	Low	Disabled	• All channels: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive
2	Low	Low/Hi-z	Low	Disabled	• All channels: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive After the CTSUSO0, CTSUSO1 register is written to, only the pins enter Status 3 (the capacitive touch sensor I/O pins of the measured channels start driving). After one cycle of the base clock, the CTSU enters Status 3.
3	Pulse	Low/Hi-z /pulse	Pulse Note	Enabled	• Measured receive channel: [Capacitive touch sensor I/O] drive [Normal I/O] Hi-z • Non-measured receive channel: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive When TXVSEL = 1 • Transmit channel: [Capacitive touch sensor I/O] drive [Normal I/O] Hi-z When TXVSEL = 0 • Transmit channel: Capacitive touch sensor I/O] Hi-z [Normal I/O] drive
4	Pulse	Low/Hi-z /pulse	Pulse Note	Enabled	Same as above
5	Low	Low/Hi-z	Low	Disabled	• All channels: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive The pins transition from Status 4 to this state after one cycle of the operating clock (all normal I/O pins are driven low).

Note Transmit pins in the self-capacitance method are not available for measurement. Use them for on-board shield.

2.4.2 Operation of the mutual capacitance method

In the mutual capacitance method, measurement is performed by outputting pulses to the target transmit channel to be measured so that a pulse edge is applied during the high-level period of the sensor drive pulse of the receive channel. A single measurement target is measured twice at rising and falling edges. The difference between the data of these two measurements is used to determine whether the electrode was touched, enabling higher touch sensitivity. Scan mode (2.5) and sensor drive pulse (2.6) are selectable.

Both transmission and reception are assigned to all channels that are set for measurement targets. Figure 2-11 shows the software flow an operation example, and Figure 2-12 shows the timing chart.

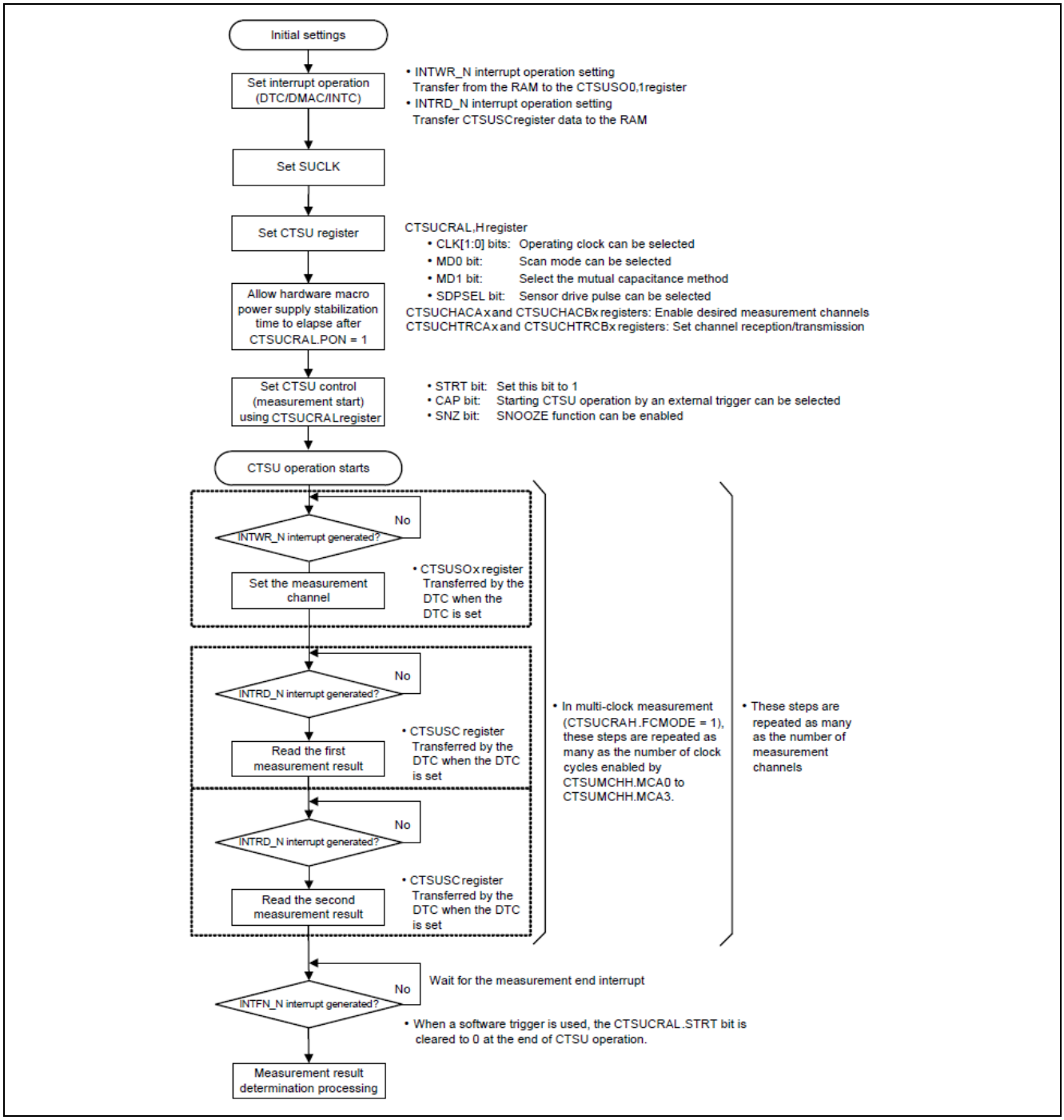

Figure 2-11 Software Flow and Operation Example of the Mutual Capacitance Method

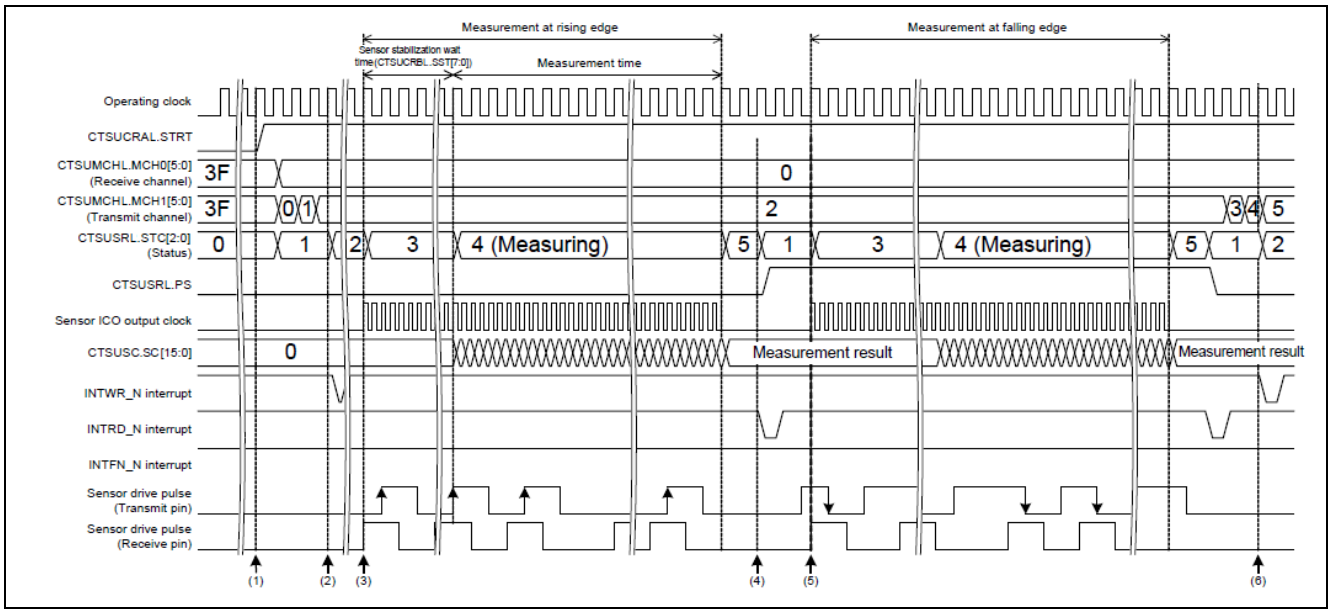

Figure 2-12 Timing Chart of the Mutual Capacitance Method (Software Trigger Selected as Measurement Start

The following describes the operation illustrated in Figure 2-12.

1. After various settings have been made, measurement starts when 1 is written to the CTSUCRAL.STRT h
2. The channel to be measured is determined in accordance with the set conditions, and then a request for setting the channel (INTWR_N interrupt) is output.
3. On completion of writing the measurement channel settings (CTSUSO0, CTSUSO1 register), the sensor drive pulse is output and the sensor ICO clock operates.

   At the same time, pulses are output to the transmit pin of the measurement channel so that a rising edge is applied during the high-level period of the sensor drive pulse (receive pin).
4. After the sensor stabilization wait time and the measurement period elapse and measurement ends, a measurement result read request (INTRD_N interrupt) is output.
5. The same channel is measured by outputting pulses so that a falling edge is applied during the high-level period of the sensor drive pulse (receive pin).
6. After the same channel is measured twice, the channel to be measured next is determined and measured in the same way.
7. On completion of measurement for all channels, a measurement end interrupt (INTFN_N interrupt) is output to complete measurement (transition to Status 0).

The mutual capacitance measurement status flag (PS bit) changes when the CTSU transitions from Status 5 to Status 1.

Table 2-2 lists the measurement pin states in the mutual capacitance method.

Table 2-2 Measurement Pin States in the Mutual Capacitance Method

Status	Receive channel measurement pins		Transmit channel measurement pins		ICO operation enable	Capacitive touch sensor-dedicated IO operation
	Measured channel	Non-measured channel	Measured channel	Non-measured channel		
0	Low	Low/Hi-z	Low	Low/Hi-z	Disabled	• All channels: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive
1	Low	Low/Hi-z	Low/high	Low/Hi-z	Disabled	• All channels: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive In the second measurement, only the pins enter Status 3 (the capacitive touch sensor I/O pins of the measured receive channels start driving and the measured transmit channels are driven high) after two cycles of the base clock, and then the CTSU enters Status 3 after one cycle of the base clock.
2	Low	Low/Hi-z	Low	Low/Hi-z	Disabled	• All channels: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive After the CTSUSO0, CTSUSO1 register is written to, only the pins enter Status 3 (the capacitive touch sensor I/O pins of the measured receive channels start driving). After one cycle of the base clock, the CTSU enters Status 3.
3	Pulse	Low/Hi-z	Pulse	Low/Hi-z	Enabled	• Measured receive channel: [Capacitive touch sensor I/O] drive [Normal I/O] Hi-z • Non-measured receive channel: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive When TXVSEL = 1 • Measured transmit channel: [Capacitive touch sensor I/O] drive [Normal I/O] Hi-z • Non-measured transmit channel: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive When TXVSEL = 0 • Measured transmit channel: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive • Non-measured transmit channel: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive
4	Pulse	Low/Hi-z	Pulse	Low/Hi-z	Enabled	Same as above
5	Low	Low/Hi-z	Low	Low/Hi-z	Disabled	• All channels: [Capacitive touch sensor I/O] Hi-z [Normal I/O] drive The pins transition from Status 4 to this state after one cycle of the operating clock (all normal I/O pins are driven low).

Figure 2-13 shows the transmit pulse output timing chart of the measurement channel.

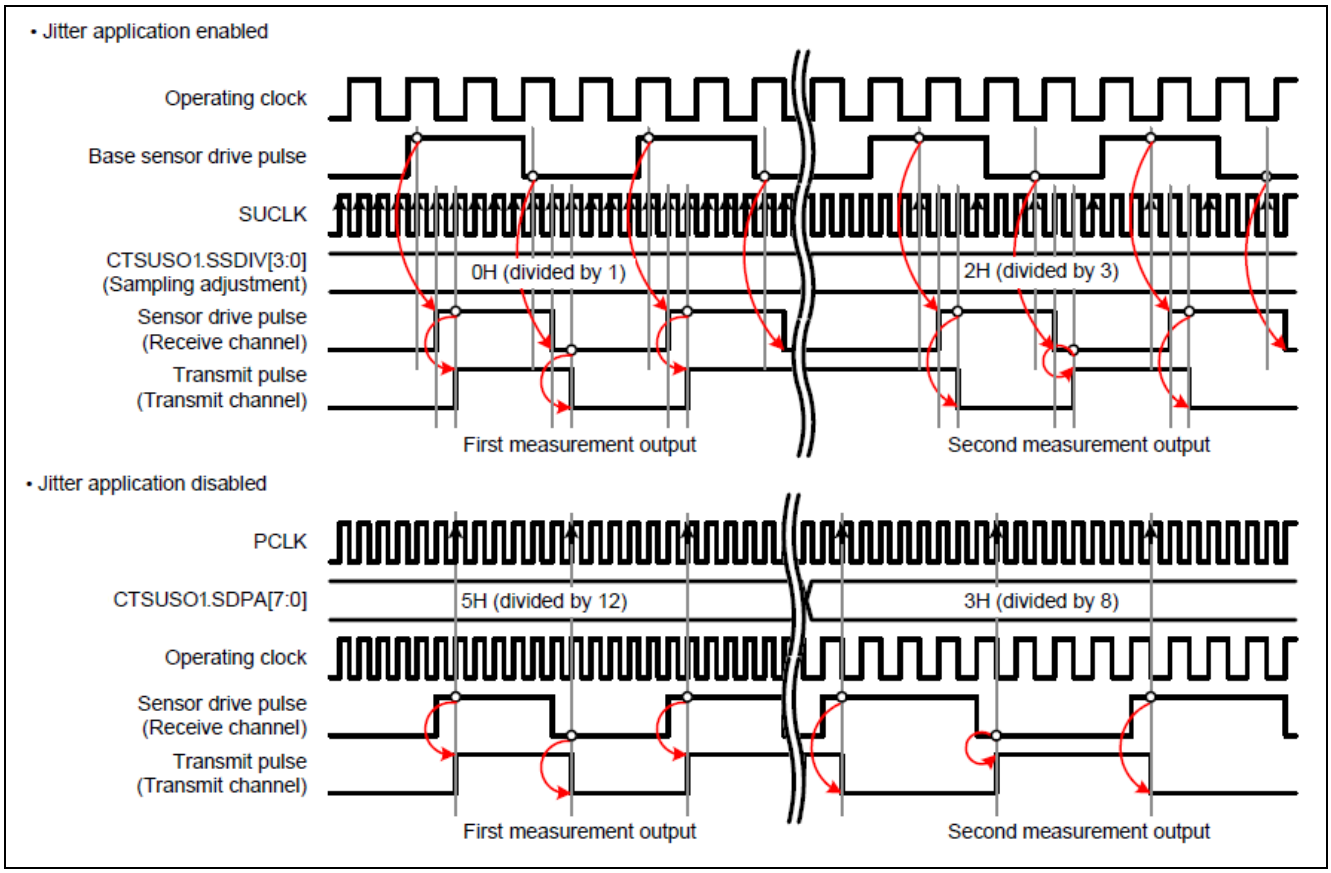

Figure 2-13 Transmit Pulse Timing Chart of the Mutual Capacitance Method

When jitter application is enabled (SOFF = 0), a transmit pulse is output with a delay of one SUCLK cycle from the sensor drive pulse.

When jitter application is disabled (SOFF = 1), a transmit pulse is output with a delay of one PCLK cycle from the sensor drive pulse.

2.5 Scan mode

Either of the following scan modes can be selected according to the CTSUCRAL.MD0 bit setting.

2.5.1 Single scan mode (CTSUCRAL.MD0 = 0)

In single scan mode, the electrostatic capacitance of a desired channel is measured.

2.5.2 Multi-scan mode (CTSUCRAL.MD0 = 1)

In multi-scan mode, the electrostatic capacitance of all channels set as measurement targets is sequentially measured in ascending order.

Figure 2-14 shows the measurement order in multi-scan mode.

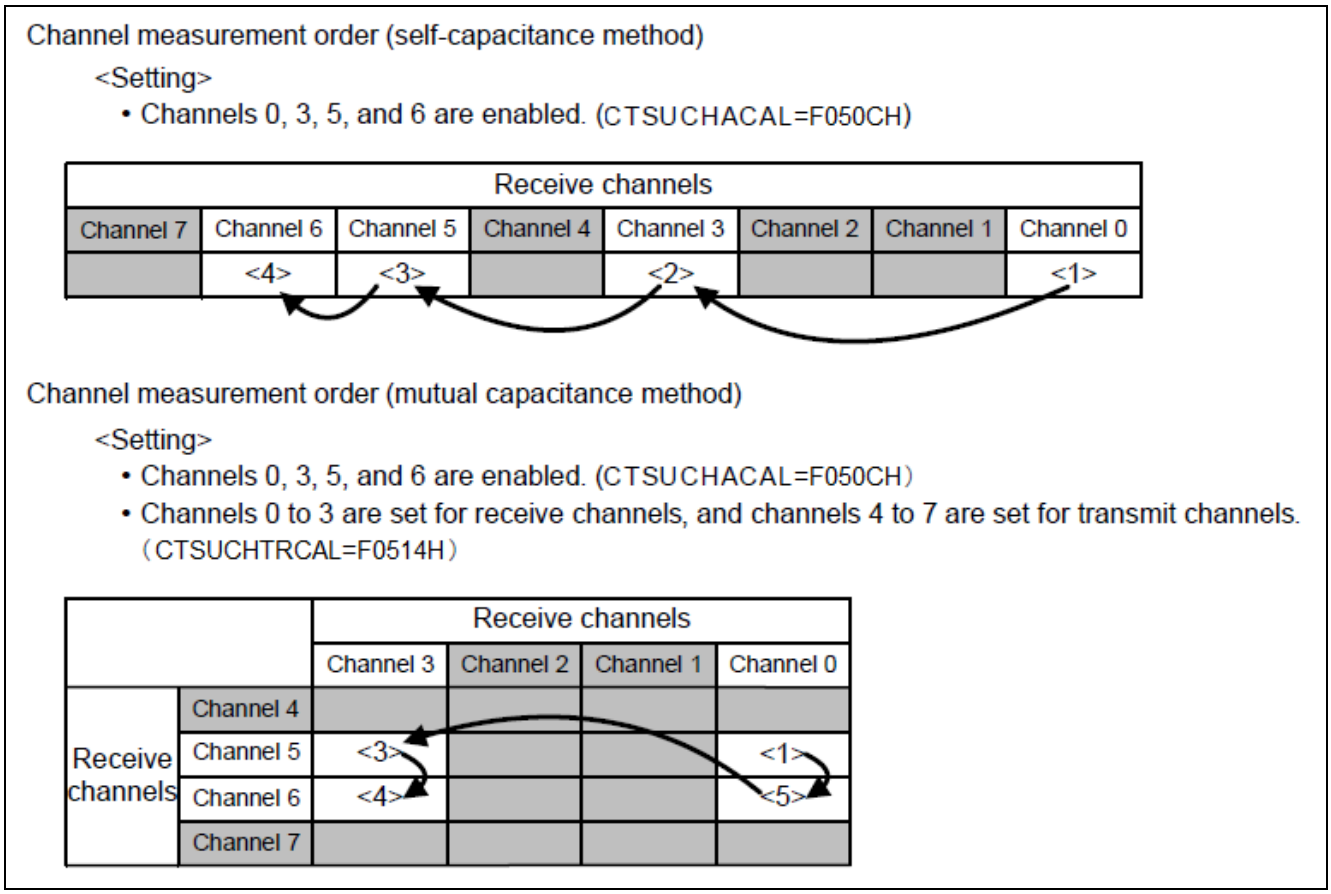

Figure 2-14 Measurement Order in Multi-scan Mode

2.6 Sensor drive pulse

The following sensor drive pulse is generated according to the CTSUCRAH.SDPSEL bit setting.

2.6.1 Random pulse mode (CTSUCRAH.SDPSEL = 0)

A sensor drive pulse for which noise prevention measures are taken using the following two functions is generated.

(1) Sensor drive pulse random phase shift function (180° phase shift)

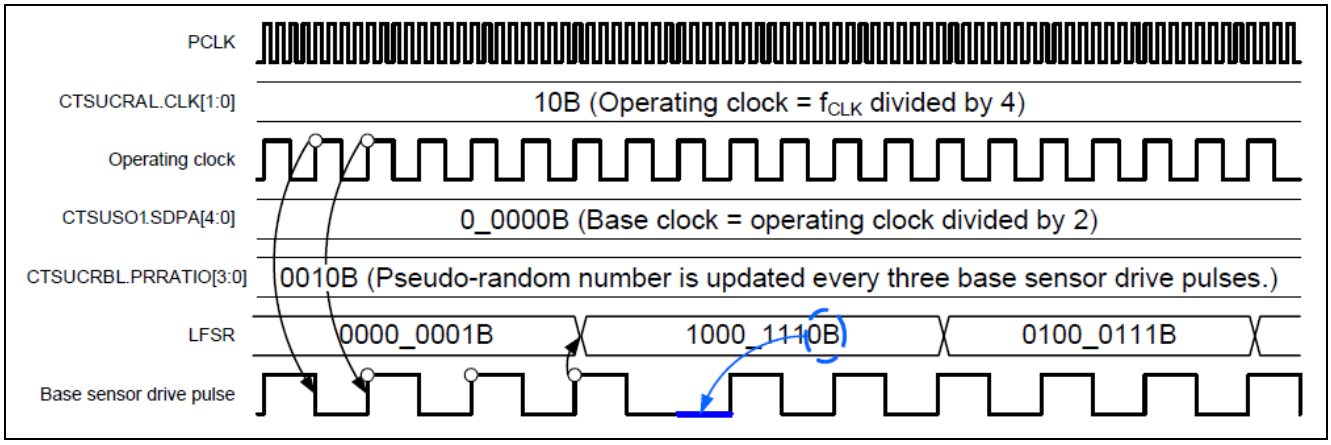

Figure 2-15 Random Phase Shift

The random phase shift function extends the low period of the base sensor drive pulse once when the bit 0 value in LFSR is 0B (Figure 2-15). The phase shift count in the pseudo-random number generation cycle is (maximum count - 1)/2 (Table 2-3).

Table 2-3 Phase Shift Count

CTSUCRBL.PRMODE[1:0]	00B (255 count)	01B (63 count)	10B (31 count)	11B (3 count)
Phase shift count per cycle	127	31	15	1

Note These values indicate phase shift count. One count is 1/2 cycle of the base sensor drive pulse. Phase shift count is independent of the CTSUCRBL.PRRATIO[3:0] value (Figure 2-15).

The following explains the measurement period in relation to the phase shift function.

The measurement period is set based on the period of two LSFR cycles (+180° phase shift in the first cycle and another +180° in the second cycle) as a basic unit so as to cancel the influence of noise synchronized with the base clock.

Measurement period = (period of two LSFR cycles) × (CTSUSO0.SNUM[5:0] + 1)

Table 2-4 lists primitive polynomials that implement LSFR.

The primitive polynomial types to be used are determined according to the pseudo-random number generation cycle selected by the CTSUCRBL.PRMODE[1:0] bits. Pseudo-random numbers are generated by using 16 types (255 cycles), six types (63 cycles), six types (31 cycles), or one type (3 cycles) of primitive polynomial. A polynomial (No.) is automatically selected according to the internal state of the hardware.

Table 2-4 Primitive Polynomials

No.	Pseudo-random number generation cycle (CTSUCRBL.PRMOD[1:0])			
	00B	01B	10B	11B
	255 cycles (8 bits)	63 cycles (6 bits)	31 cycles (5 bits)	3 cycles (2 bits) not random
0	$X^8 + X^4 + X^3 + X^2 + 1$	$X^6 + X + 1$	$X^5 + X^2 + 1$	$X^2 + X + 1$
1	$X^8 + X^5 + X^3 + X + 1$	$X^6 + X^4 + X^3 + X + 1$	$X^5 + X^3 + 1$	
2	$X^8 + X^5 + X^3 + X^2 + 1$	$X^6 + X^5 + 1$	$X^5 + X^3 + X^2 + X + 1$	
3	$X^8 + X^6 + X^3 + X^2 + 1$	$X^6 + X^5 + X^2 + X + 1$	$X^5 + X^4 + X^2 + X + 1$	
4	$X^8 + X^6 + X^4 + X^3 + X^2 + X + 1$	$X^6 + X^5 + X^3 + X^2 + 1$	$X^5 + X^4 + X^3 + X + 1$	
5	$X^8 + X^6 + X^5 + X + 1$	$X^6 + X^5 + X^4 + X + 1$	$X^5 + X^4 + X^3 + X^2 + 1$	
6	$X^8 + X^6 + X^5 + X^2 + 1$	$X^6 + X + 1$	$X^5 + X^2 + 1$	
7	$X^8 + X^6 + X^5 + X^3 + 1$	$X^6 + X^4 + X^3 + X + 1$	$X^5 + X^3 + 1$	
8	$X^8 + X^6 + X^5 + X^4 + 1$	$X^6 + X^5 + 1$	$X^5 + X^3 + X^2 + X + 1$	
9	$X^8 + X^7 + X^2 + X + 1$	$X^6 + X^5 + X^2 + X + 1$	$X^5 + X^4 + X^2 + X + 1$	
10	$X^8 + X^7 + X^3 + X^2 + 1$	$X^6 + X^5 + X^3 + X^2 + 1$	$X^5 + X^4 + X^3 + X + 1$	
11	$X^8 + X^7 + X^5 + X^3 + 1$	$X^6 + X^5 + X^4 + X + 1$	$X^5 + X^4 + X^3 + X^2 + 1$	
12	$X^8 + X^7 + X^6 + X + 1$	$X^6 + X + 1$	$X^5 + X^2 + 1$	
13	$X^8 + X^7 + X^6 + X^3 + X^2 + X + 1$	$X + X^4 + X^3 + X + 1$	$X^5 + X^3 + 1$	
14	$X^8 + X^7 + X^6 + X^5 + X^2 + X + 1$	$X^6 + X^5 + 1$	$X^5 + X^3 + X^2 + X + 1$	
15	$X^8 + X^7 + X^6 + X^5 + X^4 + X^2 + 1$	$X^6 + X^5 + X^2 + X + 1$	$X^5 + X^4 + X^2 + X + 1$	

Note The operation result is not 0 within the generation cycle of each pseudo-random number set by the CTSUCRBL.PRMODE[1:0] bits. When the CTSUCRBL.PRMODE[1:0] setting is modified, the operation result may become 0. In this case, it is reset to 01H and operation continues.

(2) Sensor drive pulse jitter application function

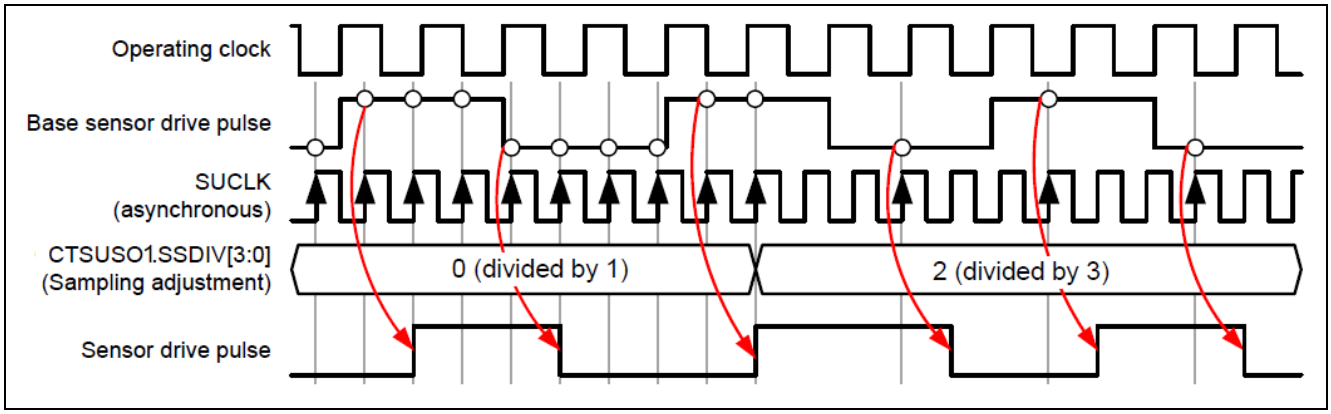

Figure 2-16 Jitter Application Function

To reduce synchronous noise of measurement pins, the jitter application function applies a jitter to the edges of the sensor drive pulse by sampling the base sensor drive pulse that toggles in synchronization with the operating clock using the asynchronous high-speed SUCLK. This function can be enabled or disabled by the CTSUCRBL.SOFF bit. To improve the noise immunity, the sampling cycle can be adjusted by the CTSUSO1.SSDIV[3:0] bits.

2.6.2 High resolution pulse mode (CTSUCRAH.SDPSEL = 1)

When the CTSUCRAH.SDPSEL bit is 1, the sensor drive pulse is generated by dividing SUCLK.

Set the frequency division ratio by the CTSUSO1.SDPA[7:0] bits. Noise immunity can be improved by adjusting the SUCLK cycle by software.

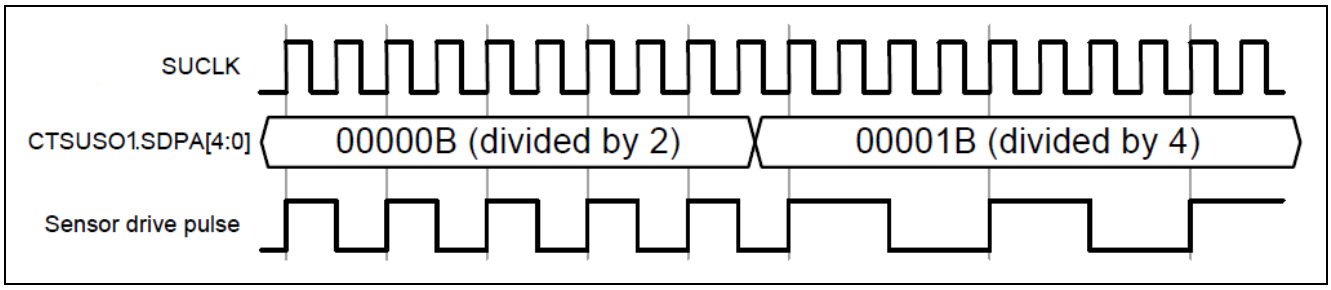

Figure 2-17 Sensor Drive Pulse (CTSUCRAH.SDPSEL = 1)

2.7 Switching power supply for transmit pins

TXVSEL bit and TXVSEL2 bit (Transmit pin power switching bits)

For the transmit TSm pins set by the CTSUCHTRCn (n = AL, AH, BL, BH) register, power supply of the capacitive touch sensor I/O is switched by the CTSUCRAL.TXVSEL and CTSUCRAL.TXVSEL2 bits. Table 2-5 lists the power states of TSm pins. Figure 2-18 illustrates state changes during measurement.

Pins used in the CTSU are set by the multifunction pin controller (MPC). Pins to be used for measurement are enabled or disabled by the CTSUCHACn (n = AL, AH, BL, BH) register setting.

Non-measured pins (whose same-phase pulse (shield) output is controlled by the CTSUCRAH.POSEL[1] bit) are allocated to the CTSU by the MPC, excluding pins whose channel setting is disabled. (The high-impedance output control by the CTSUCRAH.POSEL[0] bit includes channel-disabled pins.)

Whether a pin is used as a non-measured pin, a measured receive pin, or a measured transmit pin is determined in State 1. According to the State 1 result, power supply is switched to the power driver selected by TXVSEL at the transition from State 2 to State 3. Power supply returns to GPIO at the transition from State 4 to State 5.

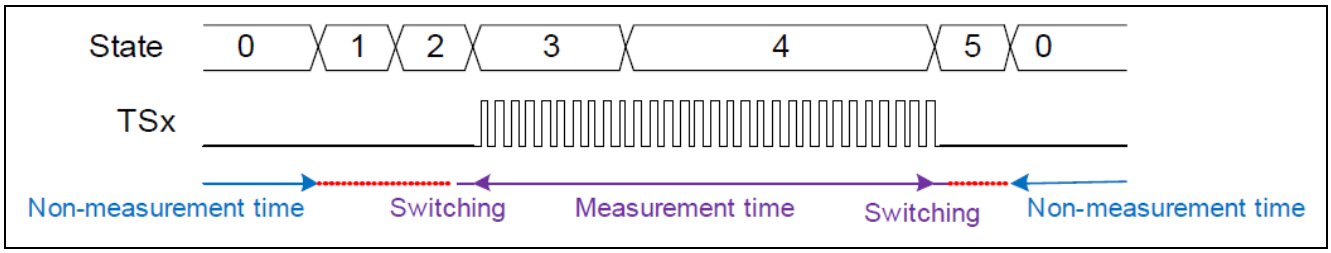

Figure 2-18 State Changes during Measurement

Table 2-5 Power States of TSm Pins

TXVSEL	TXVSEL2	Pins allocated to the CTSU by the MPC					
		Other than State 3 and State 4	Disabled Channels	Enabled Channels			
		CTSU setting TSx pins	Disabled TSx pins POSEL[1]: Disabled	Non-measured pins POSEL[1] = 0	Non-measured pins POSEL[1] = 1	Transmit pins	Receive pins
0	0	VDD (GPIO) Low output	VDD (GPIO) according to POSEL[0]	VDD (GPIO) according to POSEL[0]	VDD (GPIO) according to POSEL[0]	VDD (GPIO) Transmit pulse	TSCAP Measurement pulse
1	0	VDD (GPIO) Low output	VDD (GPIO) according to POSEL[0]	VDD (GPIO) according to POSEL[0]	VDD (REGC) according to POSEL[0]	VDD (REGC) Transmit pulse	TSCAP Measurement pulse
x	1	VDD (GPIO) Low output	VDD (GPIO) according to POSEL[0]	VDD (GPIO) according to POSEL[0]	VDD (dedicated) according to POSEL[0]	VDD (dedicated) Transmit pulse	TSCAP Measurement pulse

Figure 2-19 shows the peripheral circuits of I/O pins.

The I/O function for the capacitive touch sensor is assigned to the TSn pins in addition to the conventional GPIO function.

The circuit for the I/O pins (sensor I/O) for the capacitive touch sensor has a driver that can switch between the measurement power supply (VDDSENS (TSCAP)) and the core power supply (VDD (REGC)), a VDD (dedicated) driver wired in the chip to avoid common impedance with the GPIO power supply, and a switch for current measurement.

When the measurement power supply is selected (SEL = 0) for pins operated as a switched capacitor and used to measure electrostatic capacitance, ENO2 is asserted to input a drive pulse to TOUT.

Pins that output a transmit pulse of the mutual capacitance method are selectable from the following three drivers.

(1) GPIO driver: TXVSEL = 0 and TXVSEL2 = 0

ENO of GPIO is asserted to input a transmit drive pulse to DOUT.

Merit: The power-supply voltage (5 V) is available with high sensitivity and drive performance

Demerit: Subject to fluctuations in current consumption (including LED lighting) of GPIO

(2) VDD (REGC) driver: TXVSEL = 1 and TXVSEL2 = 0

SEL = 1 (VDD selected) and ENO2 is asserted in the sensor I/O to input a transmit drive pulse to TOUT.

Merit: Resistant to fluctuations in current consumption of GPIO

Demerit: The amplitude decreases, which lowers sensitivity and drive performance

(3) Dedicated VDD driver: TXVSEL = 0 and TXVSEL2 = 1

ENO3 of the sensor I/O is asserted to input the transmit drive pulse to TOUT.

Merit: Resistant to fluctuations in current consumption of GPIO. The power-supply voltage (5 V) is available with high sensitivity.

Demerit: Low drive performance (this driver is not provided in the IFCU)

To output a shield pulse, make the following setting.

(4) VDD (REGC) driver: TXVSEL = 1 and TXVSEL2 = 0

SEL = 1 (VDD select) and ENO2 is asserted in the sensor I/O to input a transmit drive pulse to TOUT.

If the transmit drive pulse is output with any other setting, shield effect cannot be obtained due to a different shield pulse amplitude.

When the measurement power supply is selected (SEL = 0) for pins used for measuring current without operating the switched capacitor in current measurement mode (DCMODE = 1), ENO2 is asserted. Set TOUT to 1 to output a high level. When DCBACK is set to 1, DCEN of the sensor I/O is asserted to connect the TSn pin voltage to the feedback, and DCEN of the I/O for the TSCAP pin is negated to disconnect the TSCAP voltage from the feedback.

Accurate current measurement is possible due to the feedback correction of the TSn pin voltage.

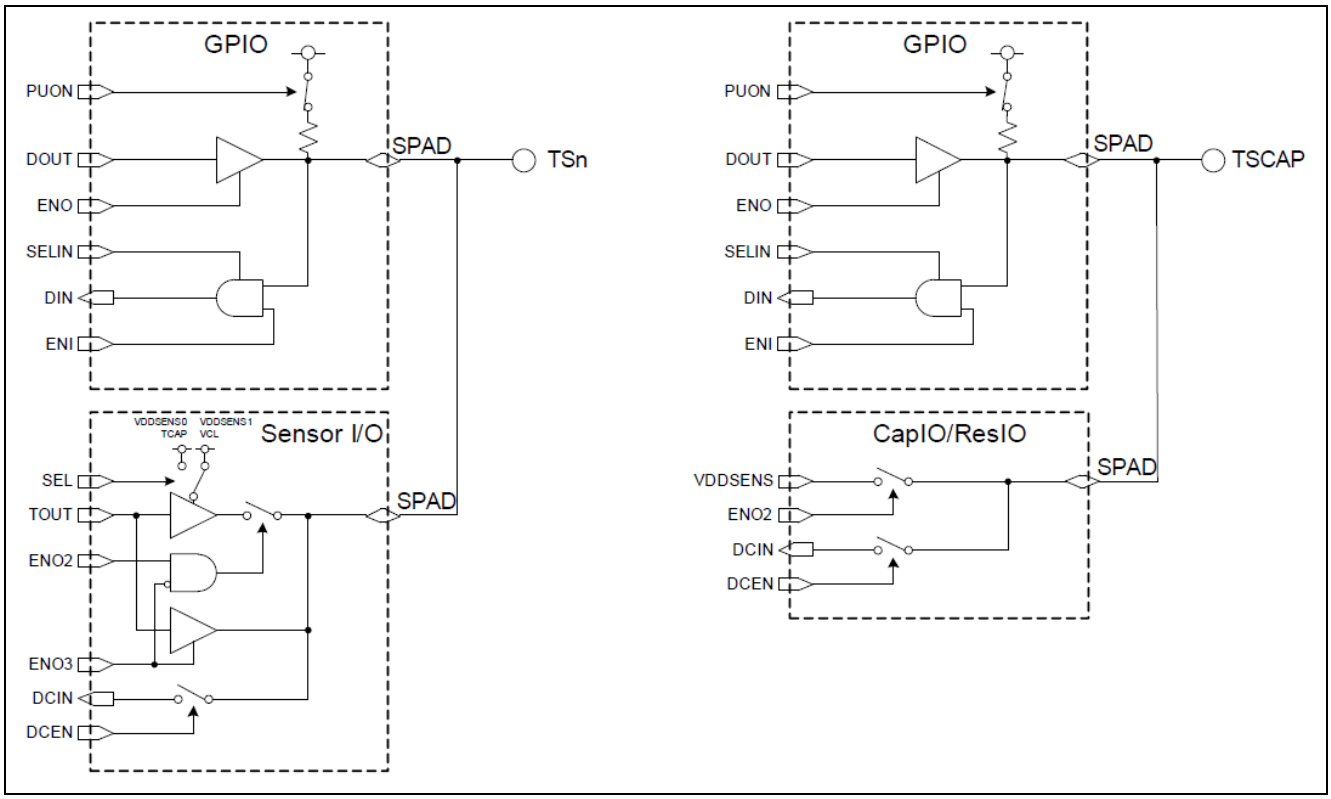

Figure 2-19 Peripheral Circuits of I/O Pins

2.8 Multi-clock measurement

Multiple clocks with different frequencies are used for measurements. Measurement results are compared by software and the results that may have been affected by noise can be excluded. This method is enabled only when high resolution pulse mode is selected (CTSUCRAH.SDPSEL = 1).

To perform multi-clock measurement, set CTSUCRAH.FCMODE to 1 and select clocks to be used for measurement by the CTSUMCHH.MCA0 to CTSUMCHH.MCA3 bits. Set the frequency using the CTSUSUCLK0 to CTSUSUCLK3 register corresponding to the selected clock.

Table 2-6 lists multi-clock setting registers.

The values of the frequency adjustment bits in the registers are adjusted (updated) by the clock recovery control based on the initial values specified in the registers.

Table 2-6 Multi-clock Setting Registers

	Valid bit	Frequency adjustment bit	Multiplication rate setting bit
Multi-clock 0	CTSUMCHH.MCA0	CTSUSUCLK0.SUADJ0[7:0]	CTSUSUCLK0.SUMULTI0[7:0]
Multi-clock 1	CTSUMCHH.MCA1	CTSUSUCLK1.SUADJ1[7:0]	CTSUSUCLK1.SUMULTI1[7:0]
Multi-clock 2	CTSUMCHH.MCA2	CTSUSUCLK2.SUADJ2[7:0]	CTSUSUCLK2.SUMULTI2[7:0]
Multi-clock 3	CTSUMCHH.MCA3	CTSUSUCLK3.SUADJ3[7:0]	CTSUSUCLK3.SUMULTI3[7:0]

Measurements are performed in ascending order of the clocks enabled by the CTSUMCHH.MCA0 to CTSUMCHH.MCA3 bits starting from MCA0 for each measurement channel. In multi-scan mode, after measurements with all enabled clocks are completed, the next channel is measured. Figure 2-20 shows the measurement order.

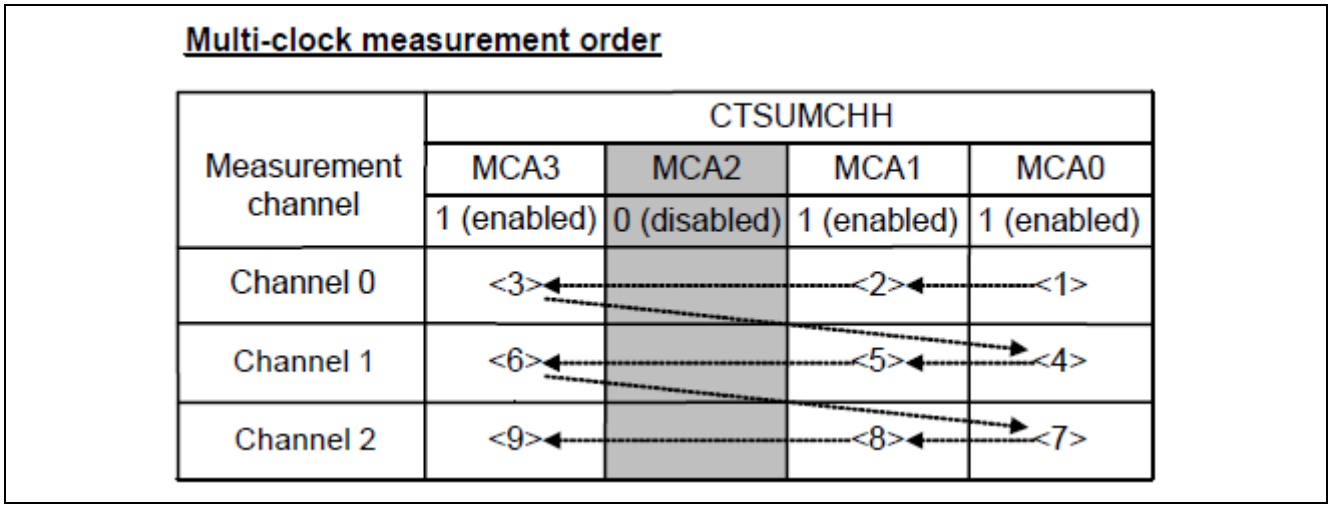

Figure 2-20 Multi-clock Measurement Order

2.9 Items common to different modes

2.9.1 Sensor stabilization wait time and measurement time

Figure 2-21 shows the entire timing of the sensor stabilization wait time and measurement time.

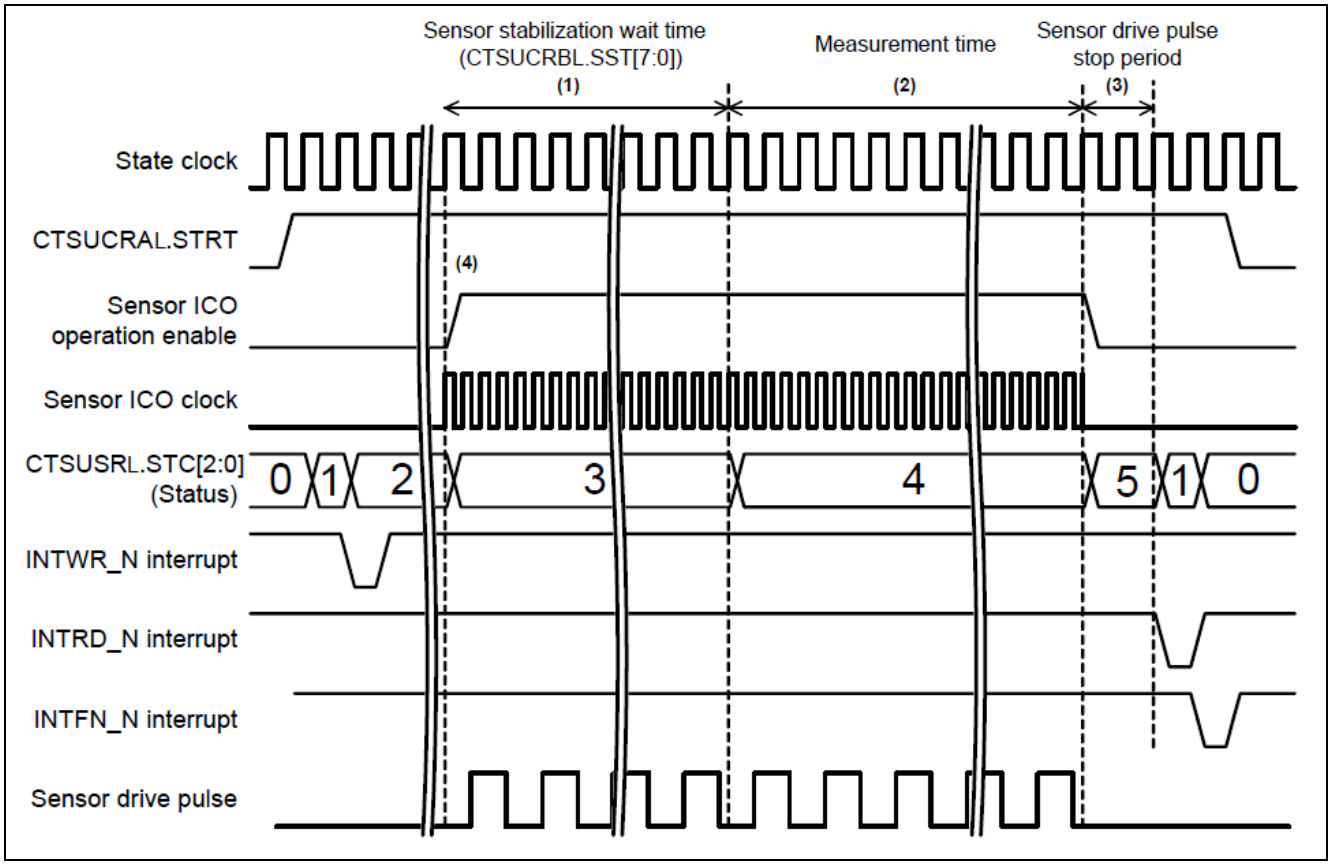

Figure 2-21 Sensor Stabilization Wait Time and Measurement Time

(1) Sensor stabilization wait time

In response to the INTWR_N interrupt request, output of the sensor drive pulse is started by a write access to the CTSUSO0, CTSUSO1 register. The CTSU waits for the stabilization time set by the CTSUCRBL.SST[7:0] bits.

(2) Measurement time

After the sensor stabilization wait time elapses, measurement starts. The measurement time is determined as follows by the sensor drive pulse.

- When CTSUCRAH.SDPSEL = 0

  The measurement time is determined by the base clock cycle, CTSUCRBL.PRMODE[1:0] bits, CTSUCRBL.PRRATIO[3:0] bits, and CTSUSO0.SNUM[5:0] bits.

- When CTSUCRAH.SDPSEL = 1

  The measurement time is determined by the STCLK cycle and the CTSUSO0.SNUM[7:0] bits.

  After the measurement time elapses, measurement of the channel is terminated.

(3) Sensor drive pulse stop time

After the measurement time elapses, the CTSU transitions to Status 1 after two operating clock cycles, and an INTRD_N interrupt occurs. Read the data from the CTSUSC register. At this time, the sensor

drive pulse output level is low. When measurement of all set channels is completed, CTSUCRAL.STRT is cleared to 0.

(4) Sensor ICO clock oscillation time

The sensor ICO clock oscillates while the CTSUSRL.STC[2:0] value is 011B or 100B.

<Measurement time when CTSUCRAH.SDPSEL = 0>
The measurement time is determined by the following five parameters specified by registers.

- The base clock cycle is determined by CTSUCRAL.CLK[1:0] and CTSUSO1.SDPA[7:0].
- The number of base clock cycles to update the linear feedback shift register (LFSR) is determined by CTSUCRBL.PRRATIO[3:0].
- The pseudo-random number generation cycle is determined by CTSUCRBL.PRMODE[1:0].
- A period of two pseudo-random number cycles is a basic unit. (The reason is described in 30.3.6.1.)
- The number of basic unit repetition times is set by CTSUSO0.SNUM[5:0].

Measurement time = basic unit × (CTSUSO0.SNUM[5:0] + 1)

Basic unit = (CTSUCRBL.PRRATIO[3:0] + 1) × 2 × number of states set by CTSUCRBL.PRMODE[1:0]
+ (number of states set by CTSUCRBL.PRMODE[1:0] - 1)/2

Table 2-7 lists the basic unit of the measurement cycle.

Table 2-7 Basic Unit of Measurement Cycle

PRRATIO[3:0]	CTSUCRBL.PRMODE[1:0]			
	00B (255 states)	01B (63 states)	10B (31 states)	11B (3 states)
0	637	157	77	7
1	1147	283	139	13
3	2167	535	263	25
7	4207	1039	511	49
15	8287	2047	1007	97

Note The values in the table are in cycles of the base clock.

2.9.2 Measurement start conditions and SNOOZE function

The CTSU has two measurement start conditions.

(1) Software trigger

When the CTSUCRAL.CAP bit is 0 (measurement operation started by a software trigger), software trigger is selected. When the CTSUCRAL.STRT bit is set to 1 (measurement operation start), measurement starts.

(2) External trigger

When the CTSUCRAL.CAP bit is 1 (measurement operation started by an external trigger), an event input from the logic and event link controller (ELCL) is selected as external trigger mode. For external trigger mode, set the ELCL and then start measurement by the CTSU. After the CTSUCRAL.STRT bit is set to 1 (measurement operation start), measurement starts at the falling edge of the external trigger.

If an external trigger is input during the measurement period, measurement does not start. The next external event becomes effective one cycle of the operating clock after an INTFN_N interrupt occurs.

When using the logic and event link controller, observe the following setting procedure.

1. Perform the CTSU initial setting flow.
2. When CTSUCRAL.STRT of the CTSU is 0 (stopped state), select the event source for the CTSU in the ELCL.
3. Set CTSUCRAL.CAP of the CTSU to 1, and then set CTSUCRAL.STRT to 1.
4. Start operation of the macro on the event output side.

(a) SNOOZE function

When an external trigger is selected, the SNOOZE function is enabled by setting the CTSUCRAL.SNZ bit to 1.

Figure 2-22 shows the timing chart of the SNOOZE function.

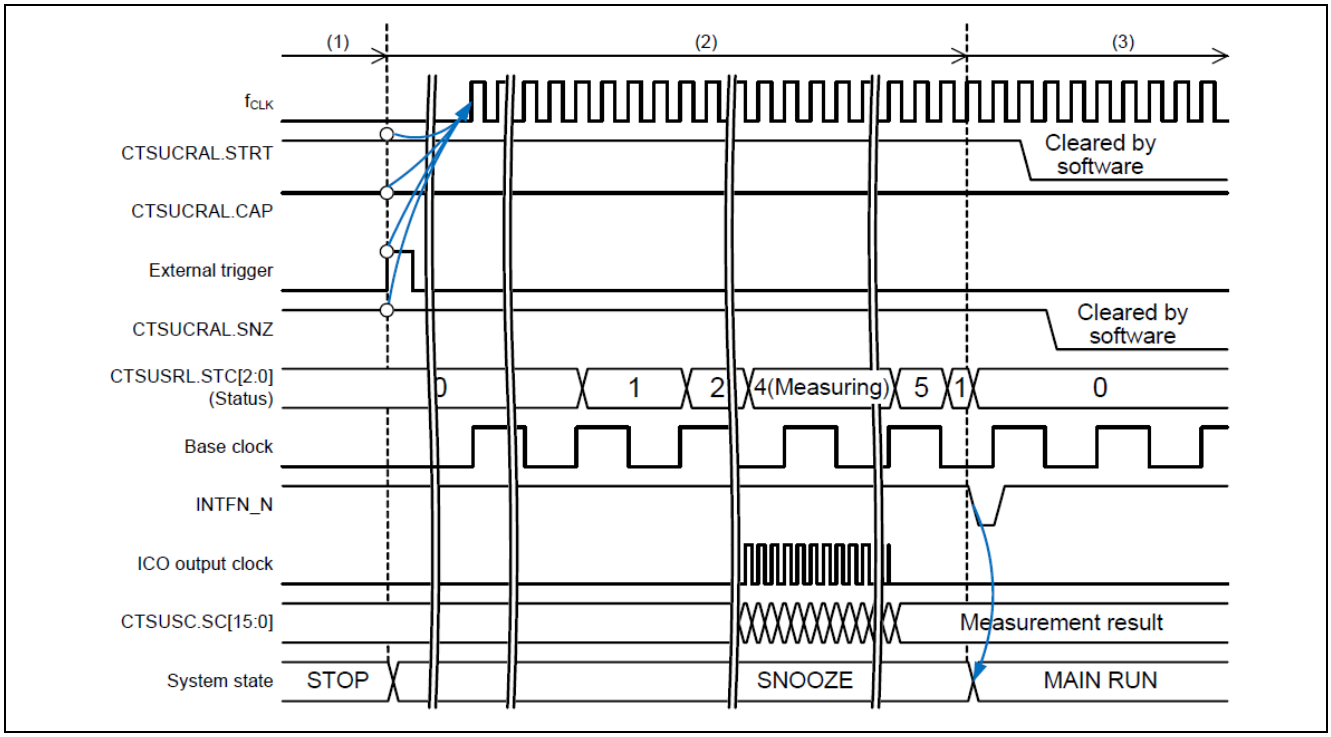

Figure 2-22 SNOOZE Function Timing Chart

(1) Clock supply by trigger input from the STOP state

After the CTSUCRAL.CAP bit and the CTSUCRAL.SNZ bit are set to 1, write 1 to the CTSUCRAL.STRT bit to shift the CPU to the STOP state. As soon as the CTSUCRAL.SNZ bit is set to 1, the CTSU transitions to the suspended state.

When a falling edge of the external trigger from the ELCL is detected in the STOP state, the CTSU sends a clock request and the system transitions to the SNOOZE state where PCLK is supplied.

(2) Normal measurement

After PCLK is supplied, the CTSU is released from the suspended state, the state counter transitions to Status 1 after 64 base clock cycles elapse, and measurement starts.

(3) CPU processing

After measurement is complete, the CPU returns to the RUN state by an INTFN_N interrupt to perform CPU processing.

To make measurement again, perform the following initialization procedure, and then transition to the STOP state.

a) Write 0 to the CTSUCRAL.STRT bit and write 1 to the CTSUCRAL.INIT bit simultaneously (forced stop).

b) Write 0 to the CTSUCRAL.SNZ bit.

Be forcibly stopping the CPU, read the measurement results.

(b) Intermittent operation without using the SNOOZE function

In systems where the ELCL cannot be used in the standby state or the SNOOZE function is not provided, normal measurement is performed using an external trigger. In this case, however, the CTSU hardware macro cannot transition to the standby state even while waiting for an external trigger for measurement. When the measurement interval is long, carry out the following procedure to reduce the power consumption.

- Configuration

  Connect an external trigger as a source for return from the standby state of the system.

- CTSU settings prior to the standby state

  When the CTSUCRAL.CAP bit is 0, CTSUCRAL.SNZ bit is 1, and CTSUCRAL.STRT bit is 0, shift the system to the standby state. In this state, the CTSU hardware macro transitions to the standby state.

- Starting measurement after return from the standby state

  After the return from the standby state, perform the following procedure to start measurement.

  1. Set the CTSUCRAL.SNZ bit to 0 to release the CTSU from the standby state.
  2. Wait for at least 64 base clock cycles.
  3. Start measurement using a software trigger.

2.9.3 Interrupts

The CTSU supports the following interrupts:

- Write request interrupt for setting registers for each channel (INTWR_N)
- Measurement data transfer request interrupt (INTRD_N)
- Measurement end interrupt (INTFN_N)

(1) Write request interrupt for setting registers for each channel (INTWR_N)

Store the settings for each measurement channel in the RAM, and set the DTC or INTC transfer associated with the INTWR_N interrupt in advance. The INTWR_N interrupt is output when the CTSU transitions from Status 1 to Status 2. Write the settings for the selected channel from the RAM to the CTSUSO0, CTSUSO1 register (Figure 2-23). Because write access to the CTSUSO0, CTSUSO1 register controls the transition to the next status, be sure to make a word (32 bits) access.

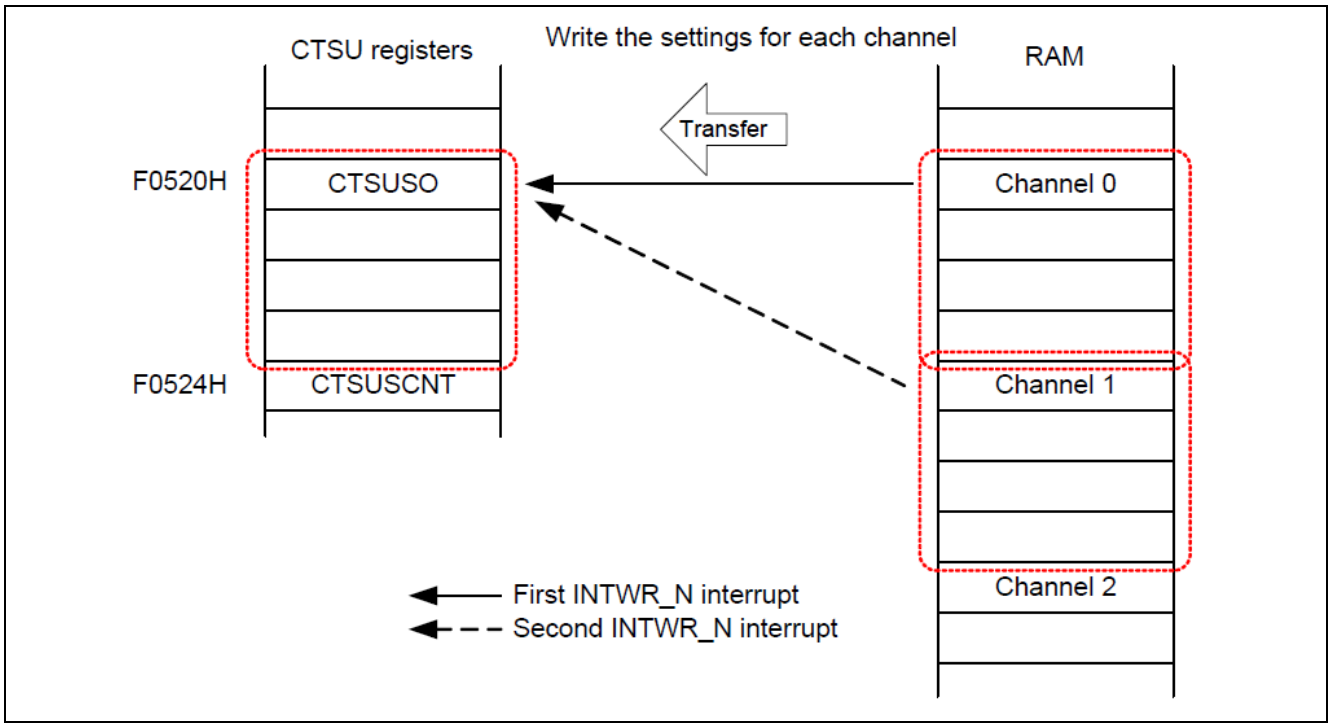

Figure 2-23 Example of DTC Transfer Operation Using the INTWR_N Interrupt

Make the following settings for operation when an interrupt occurs.

- Transfer destination address: CTSUSO0 register address
- Handling of transfer destination address: Single transfer of 4-byte data per interrupt (address fixed)
- Transfer source address: CTSUSO0 data storage address for the smallest number channel in the settings stored in the RAM
- Handling of transfer source address: Single transfer of 4-byte data per interrupt
- (The address of the first byte is continued from the previous interrupt handling.)
- Number of transfers per interrupt: Specify the number of measurements.

(2) Measurement data transfer request interrupt (INTRD_N)

Set the DTC or INTC transfer associated with the INTRD_N interrupt in advance. The INTRD_N interrupt is output when the CTSU transitions from Status 5 to Status 1 after measurement for one channel. Read the measurement result from the CTSUSC register (Figure 2-24).

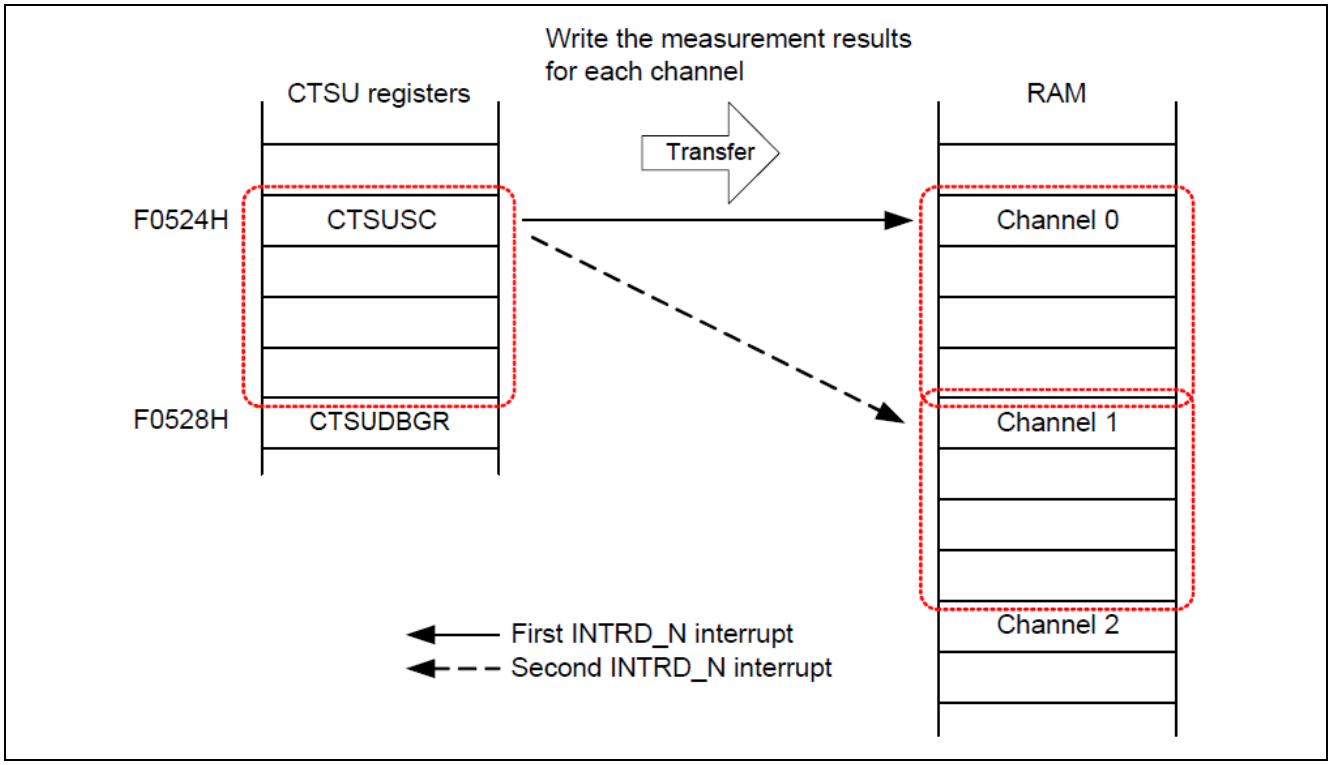

Figure 2-24 Example of DTC Transfer Operation Using the INTRD_N Interrupt

Make the following settings for operation when an interrupt occurs.

- Transfer source address: CTSUSC register address
- Handling of transfer source address: Single transfer of 4-byte data per interrupt (start address fixed)
- Transfer destination address: Measurement result data storage address for the smallest number channel in the settings stored in the RAM
- Handling of transfer destination address: Single transfer of 4-byte data per interrupt (The starting address is continued from the previous interrupt handling.)
- Number of transfers per interrupt: Specify the number of measurements.

(3) Measurement end interrupt (INTFN_N)

On completion of measurement for all channels, an interrupt occurs when the CTSU transitions from Status 1 to Status 0. The software checks the overflow flag (SOVR bit) and reads the measurement results for determination.

Interrupt requests are accepted or disabled in the interrupt control block.

3. Usage Notes

3.1 Measurement result data (CTSUSC register)

Read access during measurement is prohibited. If the measurement result data is accessed, an incorrect value may be read because of asynchronous operation.

3.2 Software trigger

When 10b (PCLKB/4) or 11B (PCLK/8) is selected in the CTSUCRAL.CLK[1:0] bits, to restart measurement by writing 1 to the CTSUCRAL.STRT bit after measurement is complete, wait for at least the number of cycles shown below after an interrupt occurs, and then write 1 to the CTSUCRAL.STRT bit.

When CTSUCRAL.CLK[1:0] = 10B: 3 cycles or more

When CTSUCRAL.CLK[1:0] = 11B: 7 cycles or more

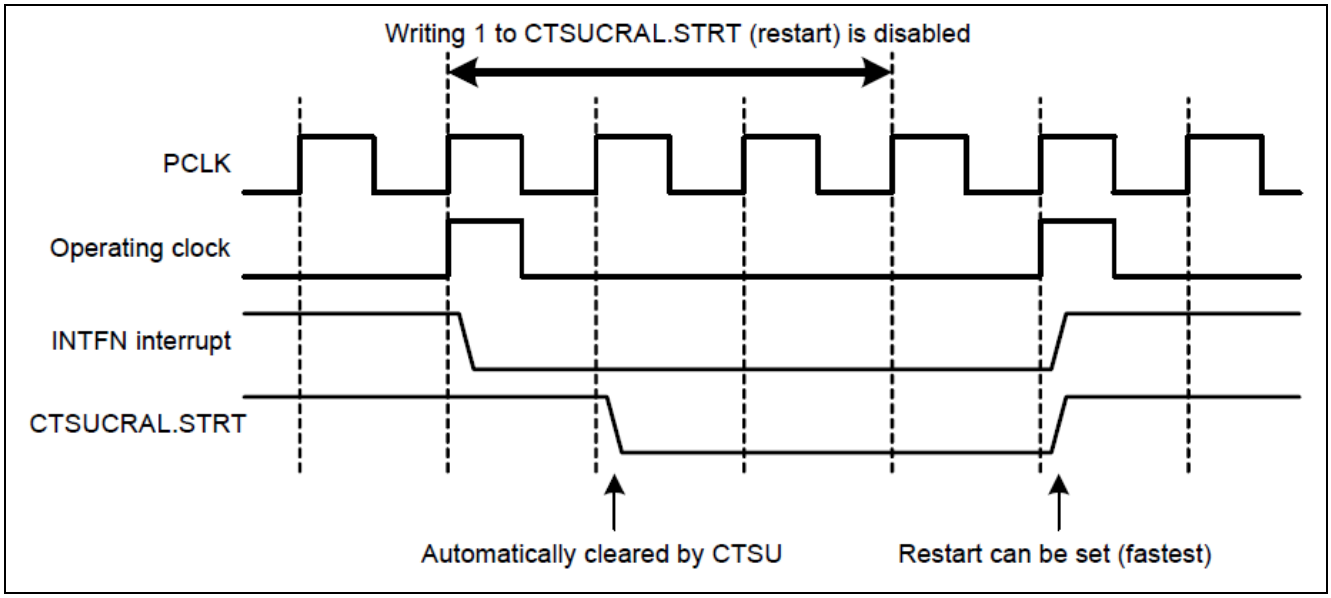

Figure 3-1 Notes on Restarting Measurement

3.3 External trigger

- If an external trigger is input during the measurement time, measurement does not start. The next external event is enabled one operating clock cycle after an INTFN_N interrupt occurs.
- To terminate external trigger mode, write 0 to the CTSUCRAL.STRT bit and 1 to the CTSUCRAL.INIT bit simultaneously (forced stop).

3.4 Notes on forced stop

To forcibly stop the current operation, be sure to write 0 to the CTSUCRAL.STRT bit and 1 to the CTSUCRAL.INIT bit simultaneously. After this setting, the operation stops and the internal control registers are initialized.

When the CTSUCRAL.INIT bit is used for initialization, the following registers are initialized in addition to the initialization of the internal measurement state.

- CTSUMCHL, CTSUMCHH register
- CTSUSRL register
- CTSUSC register

If operation is forced to stop, an interrupt request may be generated depending on the internal state. After a forced stop, also perform the processing for stopping and disabling the DTC or INTC.

If a DTC transfer stops in an installed system for some reason, also perform forced termination and initialization for the CTSU.

3.5 TSCAP pin

Before connecting the capacitor to the TSCAP pin by turning the switch on (CTSUCRAL.CSW = 1), output a low level by the I/O port control to fully discharge the capacitor.

3.6 Setting the sampling cycle when applying jitter

Set the CTSUCRAL.CLK[1:0] and CTSUSO1.SDPA[7:0] bits so that the sensor drive pulse sampling cycle when the jitter application function is enabled (CTSUCRBL.SOFF = 0) becomes less than 1/4 of the sensor drive pulse cycle.

3.7 Notes on measurement operation (CTSUCRAL.STRT bit = 1)

While measurement is in progress (CTSUCRAL.STRT bit = 1), do not stop the peripheral clock or change the port settings related to measurement pins (TSm pins and TSCAP pin) from an upper layer of the system.

If control against this constraint is performed, forcibly stop the CTSU (CTSUCRAL.STRT = 0 and CTSUCRAL.INIT = 1). After that, write 0 to the CTSUCRAL.PON and CTSUCRAL.CSW bits simultaneously and write 0 to the CTSUCRAL.SNZ bit to restart measurement from the initial setting flow shown in Figure 2-5.

3.8 Prohibiting transmission power switching (TXVSEL and TXVSEL2 bits) after initial settings

Do not change the CTSUCRAL.TXVSEL bit or CTSUCRAL.TXVSEL2 bit after the initial settings are completed.

If control against this constraint is performed, forcibly stop the CTSU (CTSUCRAL.STRT = 0 and CTSUCRAL.INIT = 1). After that, write 0 to the CTSUCRAL.PON and CTSUCRAL.CSW bits simultaneously and write 0 to the CTSUCRAL.SNZ bit to restart measurement from the initial settings flow shown in Figure 2-5.

3.9 Transmit pins in the self-capacitance method

Transmit pins in the self-capacitance method cannot be used for measurement. A pulse with the same phase as the measurement pulse is output from the transmit pins. Use the transmit pins for on-board shield. Do not select two or more transmit pins in the self-capacitance method.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2021.04.08	-	Initial version

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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