RH850/U2Bx

R/D Converter (RDC3AS)

Introduction

This application note describes the examples of operation using the R/D (resolver/digital) converter of delta-sigma analog-to-digital type (RDC3AS) of RH850/U2Bx.

Examples of tasks and applications described in this application note have been verified. However, before using this R/D converter, be sure to check operating environment.

Target Device

This application note applies to RH850/U2B series.

However, it does not apply to RDC3AL of U2B6.

Contents

1. Introduction

This application note describes how to use the R/D (resolver/digital) converter of delta-sigma analog-to-digital type (RDC3AS) of RH850/U2Bx.

1.1 Feature Used

The RH850/U2Bx hardware feature used in this application note is shown below.

- R/D (resolver/digital) converter of delta-sigma analog-to-digital type (RDC3AS)
- Delta Sigma A/D Converter (DSADC)
- Timer Pattern Buffer (TPBA)
- Peripheral Interconnect (PIC)
- Pin Functions (PORT)

2. R/D Converter Basics

2.1 Resolver and Resolver Digital Converter

2.1.1 The Usage of Resolver

A resolver is used where an angle sensor is required to be operated under the severe environment condition.

Major usage : Detecting angle for automobile use, aerospace, factory, and other severe environment.

A resolver is also used for control motors mounted on engine of HV and EV in the automobile field.

Figure 2.1 shows an example of the brushless DC motor control using a resolver and an R/D converter.

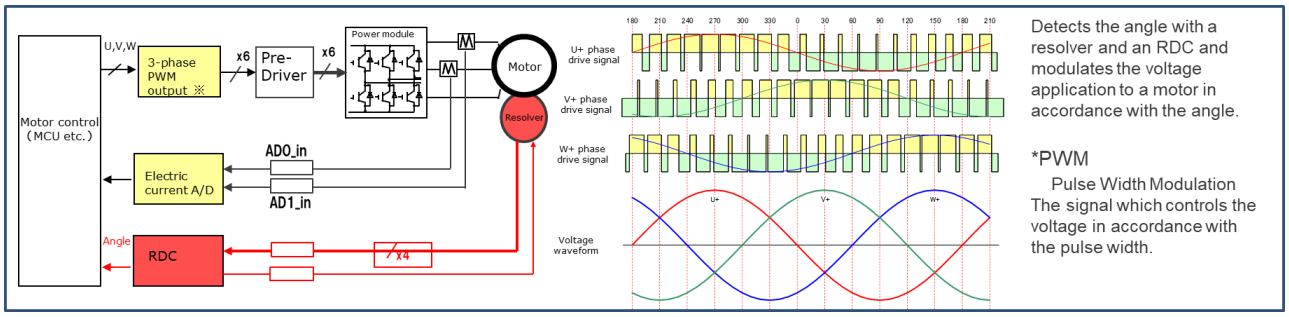


Figure 2.1 Brushless DC Motor Control

2.1.2 The Mechanism of Resolver

A resolver is a sensor used to detect the angle of the rotating shaft. The schematic diagram is shown in Figure 2.2. It is an analog device that has 2 excitation signal input pins (Ex+, Ex-) and 4 angle signal output pins (S1,S3,S2,S4). By inputting the AC signal into excitation signal input pins, signals including angle information can be obtained from angle signal output pins.

Signals output from angle signal output pins are converted to the digital angle (resolver angle : θ) with an R/D converter. The connection between S1-S3, S2-S4, and Ex+-Ex- are windings and thus short-circuited in terms of DC.

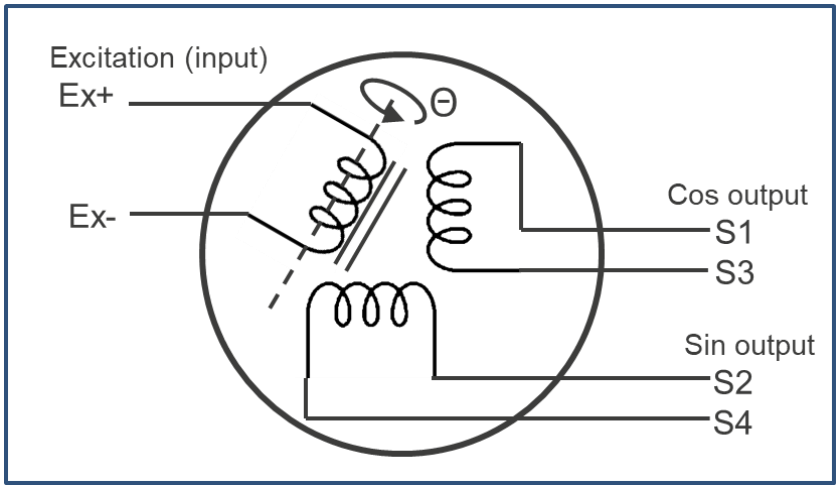


Figure 2.2 Mechanism of Resolver

A resolver operates as a variable coupling transformer which varies the amount of magnetic couplings between the primary winding (excitation) and the 2 secondary windings (Cos output, Sin output) according to the angle of the rotating shaft.

The excitation signal (input) : $f(\omega t)=(Ex+)-Ex(-)=E1 \cdot Sin(\omega t)$ Frequency (ω) ~10kHz

The Cos signal (output) : $S1-S3 = k \cdot Cos(\theta) \times f(\omega t)$

The Sin signal (output) : $S2-S4 = k \cdot Sin(\theta) \times f(\omega t)$ **Θ= The shaft angle**

2.1.3 Connecting Resolver and R/D Converter

The connection required for obtaining an angle from a resolver is shown in Figure 2.3.

A resolver receives the excitation signal which is output from either the reference signal generation circuit in an R/D converter or the sine wave generation circuit, and the R/D converter receives the output from the resolver. Generally, the differential amplifier receives outputs by considering noise immunity. Sometimes, the differential amplifier is incorporated in R/D converter. When an R/D converter does not have any reference signal generating functions, the reference signal is input to the R/D converter and the excitation buffer amplifier from the outside.

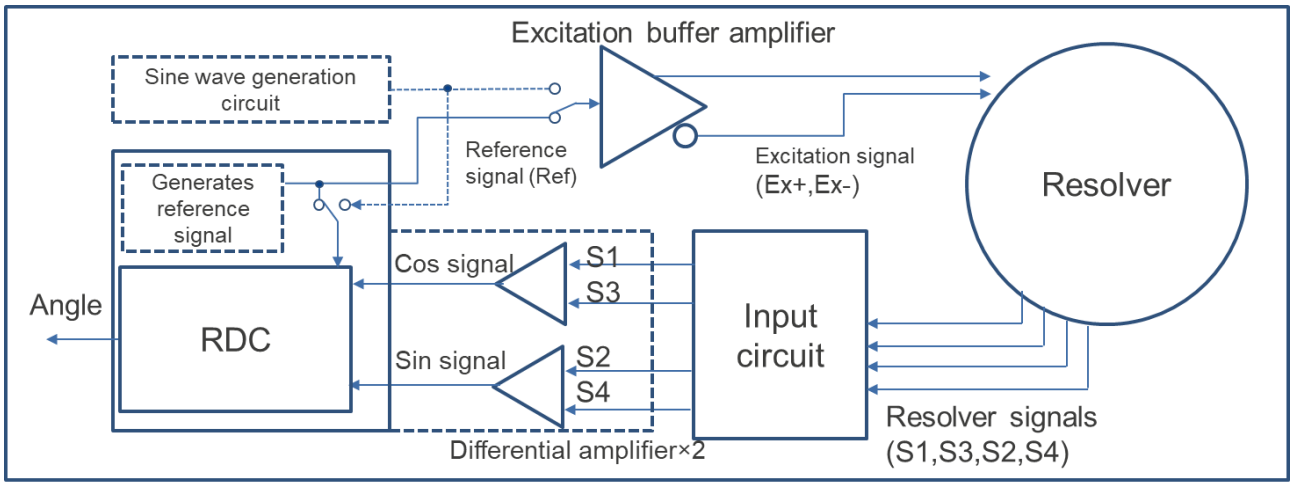


Figure 2.3 Connecting Resolver and R/D Converter

An example of the excitation signal input to a resolver and obtained resolver signals is shown in Figure 2.4.

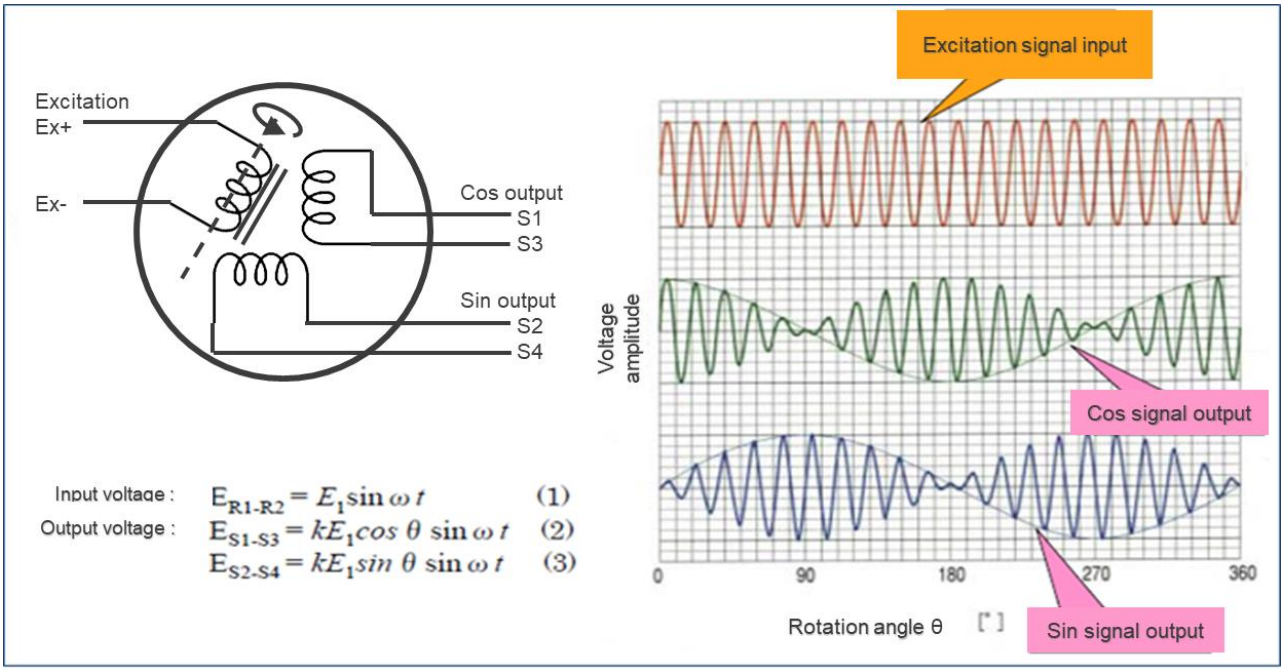


Figure 2.4 Output/Input Signal of Resolver

2.2 The Mechanism of R/D Converter

2.2.1 The Concept of R/D Converter

An R/D converter detects the resolver angle by using the resolver output signal (Cos signal and Sin signal), the reference signal, and the tracking loop which has an angle feedback. Figure 2.5 shows the schematic chart of R/D converter.

The difference between the resolver output signal and the preceding output angle is calculated as a deviation. The increase or decrease of the output angle is determined by the sign of the deviation.

When the output angle is correct (input angle θ = output angle Φ), the deviation ε becomes 0.

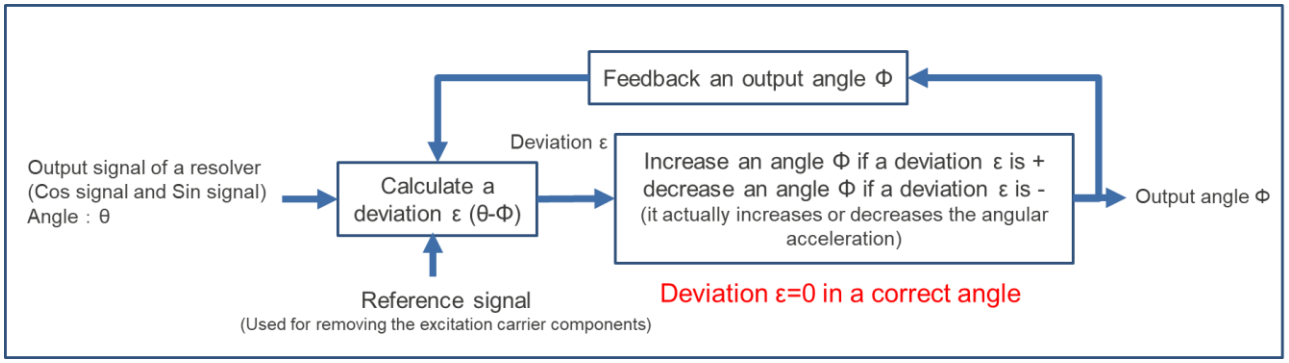


Figure 2.5 Concept of R/D Converter

2.2.2 The Actual Operation of R/D Converter

An R/D converter calculates digital angles from Cos signals and Sin signals and reference signals.

The feedback loop is designed as shown in Figure 2.6 to eliminate the difference between the angle of input signal(θ) and the internal holding angle (Φ). (Type II feedback loop)

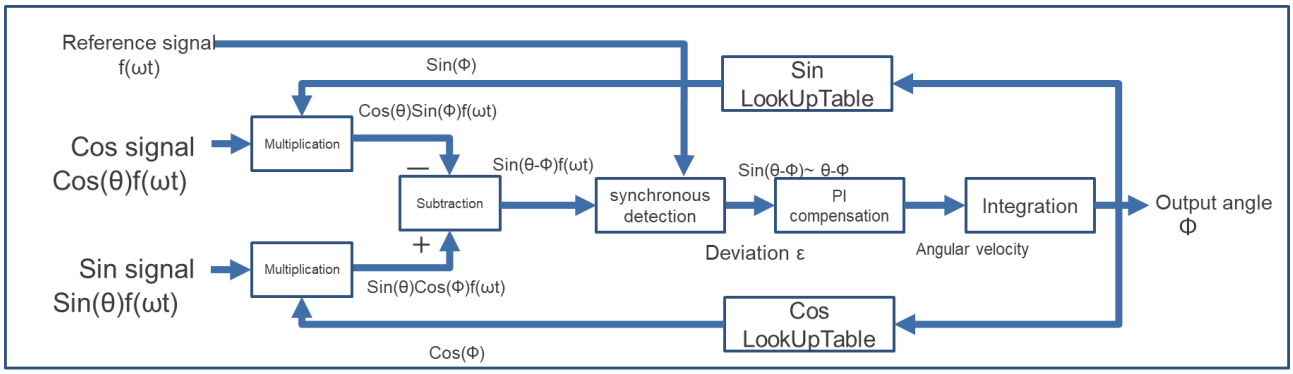


Figure 2.6 Feedback Loop of R/D Converter

An R/D converter calculates an angle using the principle below.

Multiplies Cos signal and Sin table in a Look Up Table $\cos(\theta) \cdot f(\omega t) \cdot \sin(\Phi)$ -(1)

Multiplies Sin signal and Cos table in a Look Up Table $\sin(\theta) \cdot f(\omega t) \cdot \cos(\Phi)$ -(2)

Calculates (2)-(1) $(\sin(\theta) \cdot f(\omega t) \cdot \cos(\Phi)) - (\cos(\theta) \cdot f(\omega t) \cdot \sin(\Phi))$

$= ((\sin(\theta) \cdot \cos(\Phi)) - (\cos(\theta) \cdot \sin(\Phi))) \cdot f(\omega t)$

Since $(\sin(\theta) \cdot \cos(\Phi)) - (\cos(\theta) \cdot \sin(\Phi)) = \sin(\theta - \Phi)$

$= \sin(\theta - \Phi) \cdot f(\omega t) \sim (\theta - \Phi) \cdot f(\omega t)$ -(3)

Eliminates f(ωt) with the synchronous detection by using the input f(ωt)

$(\theta - \Phi) \cdot f(\omega t) \rightarrow \theta - \Phi = \varepsilon$ -(4)

ε is the control deviation in this control loop. The negative feedback control provides feedback so that the control deviation becomes 0. When θ = Φ, the analog angle information from a resolver has been converted to the digital angle Φ.

Sets the response speed with the PI compensator in a loop.

2.2.3 Setting the R/D Converter Bandwidth

The bandwidth of the PI compensator needs to be set when an R/D converter is used. The bandwidth is expressed by the frequency. When a higher frequency is set, the response will be quicker but easily influenced by other factors such as noise. On the other hand, when a lower frequency is set, the response will be slower but has higher immunity toward noise and the R/D converter output becomes more stable. For the R/D converter mounted on the Renesas MCU, the default is 800Hz, but it can be changed.

Some R/D converters have a function to set the bandwidth automatically. When this function is used, the bandwidth is set low when the resolver is stable, and it is set high automatically when the quick response is required such as at acceleration. The R/D converters mounted on the Renesas MCU have an auto-adjusted function.

The bandwidth setting of an R/D converter has influence on response speed for acceleration and angle step but has no influence on the maximum speed of when a resolver is rotating stationary. For example, when the bandwidth is set low (around 200Hz), if a resolver is slowly accelerated, it can be tracked even the final speed is high (for example 1000Hz=60000rpm). Also, when a resolver is rotating stationary at high speed, the inside of the R/D converter remains stationary (ε is small) and the bandwidth is set low in auto-adjust.

Figure 2.7 shows the difference in output by the bandwidth of PI compensator setting.

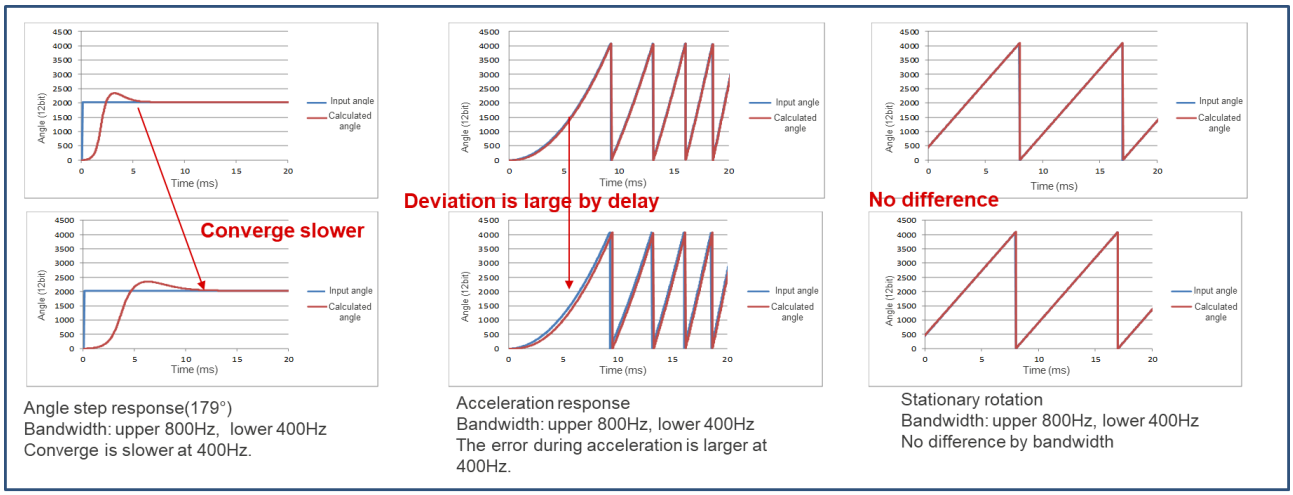


Figure 2.7 Output Change by Bandwidth Change of PI Compensator

2.3 Additional Information

2.3.1 The Handling of Angles in the Motor Control

In the brushless DC motor control, the input voltage into a motor is varied according to the shaft angle of the motor.
It should be noted that the mechanical shaft angle of a motor (mechanical angle), the output angle of a resolver (resolver angle) and the angle which determines the voltage applied to a motor (electrical angle) are not always equal depending on number of poles. The definition of terms in this document are as follows.

- Mechanical angle — The mechanical shaft angle of a motor
- Resolver angle — The angle output from an R/D converter
- Electrical angle — The angle which determines the voltage applied to a motor
- The number of resolver poles — The ratio of mechanical angle to resolver angle (mechanical angle : resolver angle=1 : the number of resolver poles)
- The number of motor pole pairs — The ratio of mechanical angle to electrical angle (mechanical angle : electrical angle=1 : the number of motor pole pairs)

Example : When the number of resolver poles is 2 and the number of motor pole pairs is 4:

> When the mechanical shaft rotates once, the resolver angle rotates twice and the voltage to the motor rotates 4 times. In this case, the controller device doubles the resolver angle (number of motor pole pairs/number of resolver poles) and calculates the applied voltage to the motor. The number of poles needs to be considered for the angular offset.

The reason for increasing the number of motor pole pairs in the brushless DC motor is because it enables the increase of the torque(rotation power of the motor). Since the number of poles of the VR resolver is more than 2, the mechanical angle, the electrical angle and the resolver angle are usually not equal. On the other hand, when the number of resolver poles and the number of motor pole pairs are same, the electrical angle and the resolver angle become equal.

Figure 2.8 shows an example of the angular relation when the number of resolver poles =2, the number of motor pole pairs=4.

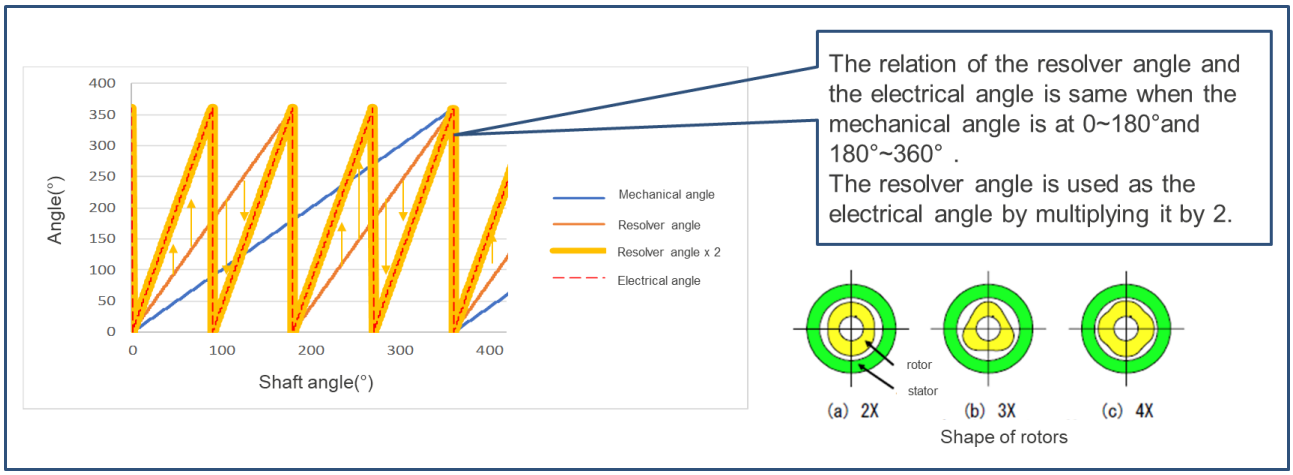


Figure 2.8 Relationship between Pole and Angle

When the number of resolver poles is large, the absolute value of the mechanical angle cannot be determined (mechanical angle X degree and X + 180degree cannot be distinguished).

For the motor control, the relative angle can be used for the rotation control as long as the number of motor pole pairs ≥ the number of resolver poles. For the VR resolver, the number of poles is always more than 2 because of its mechanism.

2.3.2 Occurrence of Errors/Occurrence Factors

When the input signal of an RDC is not ideal, error will occur in angle calculation. The main factor of errors are as follows.

- The amplitude of Sin signal and Cos signal is not aligned
- The offset is added to Sin signal or Cos signal.
- There is a large phase difference between Sin signal, Cos signal, and Ref signal.
- Sin signal and/or Cos signal are distorted.
- The resolver is attached inclined.

When error is caused by above factors, there are many cases where error has a cycle per rotation. Figure 2.9 shows the calculated angle when the amplitudes of Sin signal and Cos signal do not match. It can be seen that two error cycles are occurring in one rotation.

When an error is seen in the calculated angle, it is required to take measures such as investigating the cause and correcting it.

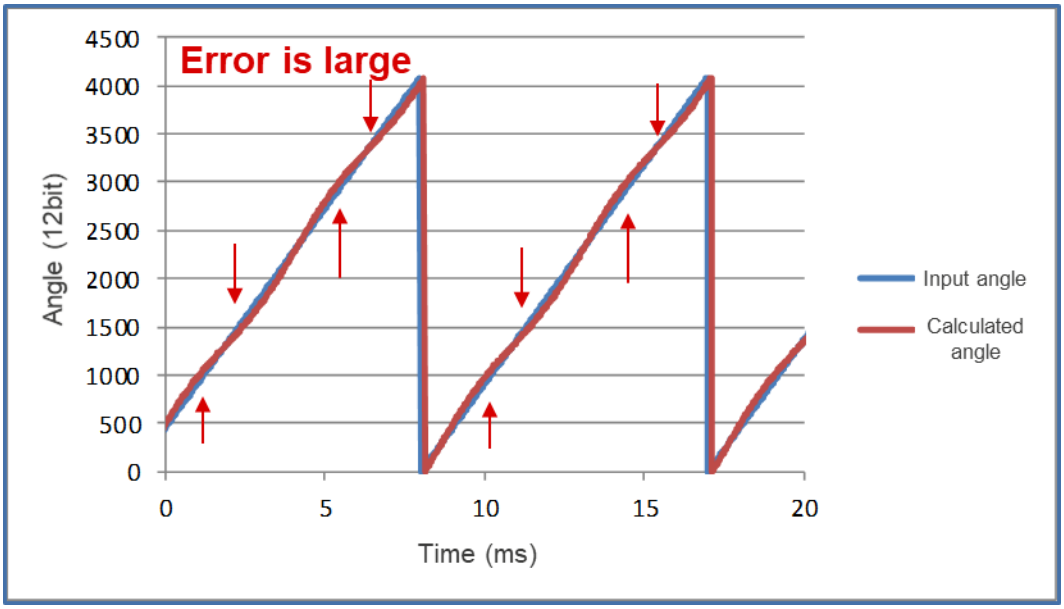


Figure 2.9 Calculated Angle When Amplitude Does Not Match

3. How to Use RDC3AS

3.1 Operating Specifications and Initial Setting

3.1.1 Operating Specifications

In this operation example, the VR resolver is used, and the angle is calculated from the output of the resolver.

The detail of operating specifications are as follows.

- Frequency of excitation signal is set to 10kHz *
- The excitation signal and reference pulse signal are generated by TPBA. And excitation phase signal is connected to RDC3AS via internal LSI connection . **
- Sensor Selection is VR resolver
- Maximum Angular Velocity Selection is set to 240000rpm , and resolution is 12bit
- PI Compensator Settings is set to Automatic adjustment

DSADC initial setting and wait process for excitation signal stability are performed first before proceeding to RDC3AS initialization. Angular data is collected in main function and stored to the RAM.

* In Section 2, the carrier signal generated in RDC is called reference signal, and the amplified signal to excite resolver generated by excitation buffer amplifier is called excitation signal. However, from this chapter onward, these two signals will be referred as excitation signal as according to the user's manual.

** To use DSADC or EXT_REF_IN for excitation signal input , see Section 3.4, Input Method for External Signal.

3.1.2 Detail of Sample System Configuration

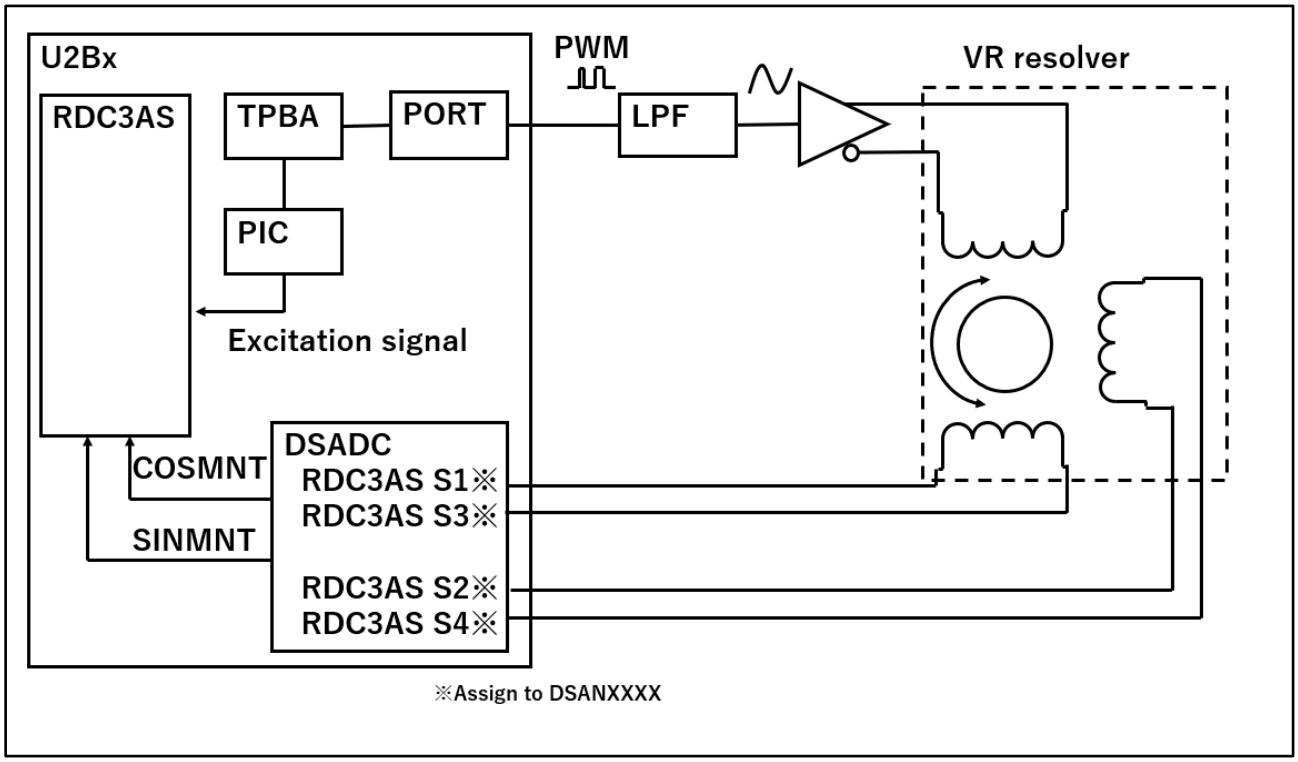


Figure 3.1 System configuration

Function of each element (IP)

- RDC3AS
  — Calculate angle information by using SINMNT,COSMNT from DSADC and excitation signal.
- DSADC
  — Receive differential signal from resolver and input to RDC3AS.
  — Transferring of ADC data to RDC3AS is performed automatically by hardware.
- TPBA
  — Generate PWM for excitation signal. The PWM signal is outputted via PORT.
  — TPBAnTINTPAT of TPBA is inputted to RDC3AS as excitation phase signal via PIC.
- PIC
  — Connect TPBAnTINTPAT of TPBA to RDC3AS as excitation phase signal.
- PORT
  — Output PWM signal generated by TPBA. The PWM will be smoothed by external LPF.

3.1.3 Explanation of Sample Software

3.1.3.1 Source File/Function List

Source files and functions used in this operation example are listed below.

Table 3-1 Source file/function list

Source file	Function	Function
main0.c	main0	Start the program and call other functions. After starting the RDC operation, store angular data to RAM in main loop.
rdc.c	rdc3as0_init	Initialization for RDC3AS0.
dsadc.c	dsadc_init	Global setting for DSADC. Call the SIN, COS pin setting function. Trigger the synchronization start for each channel.
dsadc.c	dsadc_cos_init	Setting for COS input of DSADC.
dsadc.c	dsadc_sin_init	Setting for SIN input of DSADC.
dsadc.c	dsadc_ref_init	Setting for REF input of DSADC.※ ※This function is used when inputting excitation signal from DSADC.
tpba.c	tpba0_init	Setting for TPBA0.
tpba.c	tpba0_enable	Start TPBA0.
pic.c	pic_init	Setting to connect TPBA0TINTPAT of TPBA0 to RDC3AS0.
port.c	port_init	Setting for terminal pins.

3.1.3.2 Detail of Functions

(1) main0

This is main function of the program.

After performing the following processing, an infinity loop is executed.

In the loop, angle values are obtained and stored to the RAM.

- Call the function for PORT initialization.
- Call the function for PIC initialization.
- Call the function for TPBA0 initialization and operation start.
- Call the function for DSADC initialization and wait for the excitation signal stability.
- Call the function for RDC3AS0 initialization.

(2) rdc3as0_init

After releasing the RDC3AS from Standby Mode, initialization for RDC3AS0 is performed.

Register settings used in this operation example are listed below.

After the initial register settings, Ki reset is used to reset the internal variable, enable error detection, and clear the error status.

Figure 3.2 shows the flow of register settings and RDC operation start.

Table 3-2 rdc3as0_init register settings

Register Name/Symbol	Set Value	Description
RDC3AS0.DSST	0x00000011	ΔΣADC group delay setting :10us (F2) ΔΣADC output update frequency setting :200kHz (F1b,F3b,F2,F4)
RDC3AS0.PI0	0x00020017	Control Variation Determination Clock Select: 200us Loop Gain Select : Automatic adjustment （BWCS=1 LPGS[2:0]=111）
RDC3AS0.PI1	0x00011B01	Maximum Angular Velocity Select :240000rpm Resolution (in bits)12bit（Default setting）
RDC3AS0.DIAG0	0x001A2933	Setting for error detection（Default setting）
RDC3AS0.DIAG1	0xB0000000	Setting for error detection（Default setting）
RDC3AS0.REF	0x0A110000 +phase correction value	Excitation Extraction Noise Filter :Not used Excitation Component Extraction Function: Used Sensor Selection VR resolver（SENS=1/EXIO=0） Input excitation phase signal selection : Use signal from timer in LSI.（REFINSL[1:0]=01） Excitation phase signal shape selection :Use period H pulse （EXRFPSL [1:0]=01） Excitation phase signal delay adjustment counter setting 26us（REFDLCT[15:0]=520 50ns/LSB changeable）
RDC3AS0.ENC0	0x00000120	Hysteresis Output Select : without going through the hysteresis circuit. Excitation Zero-Crossing Interrupt Output: Enable
RDC3AS0.ETEN	0x00050000	Counter Operation Enable A/D Conversion Start Trigger Enable

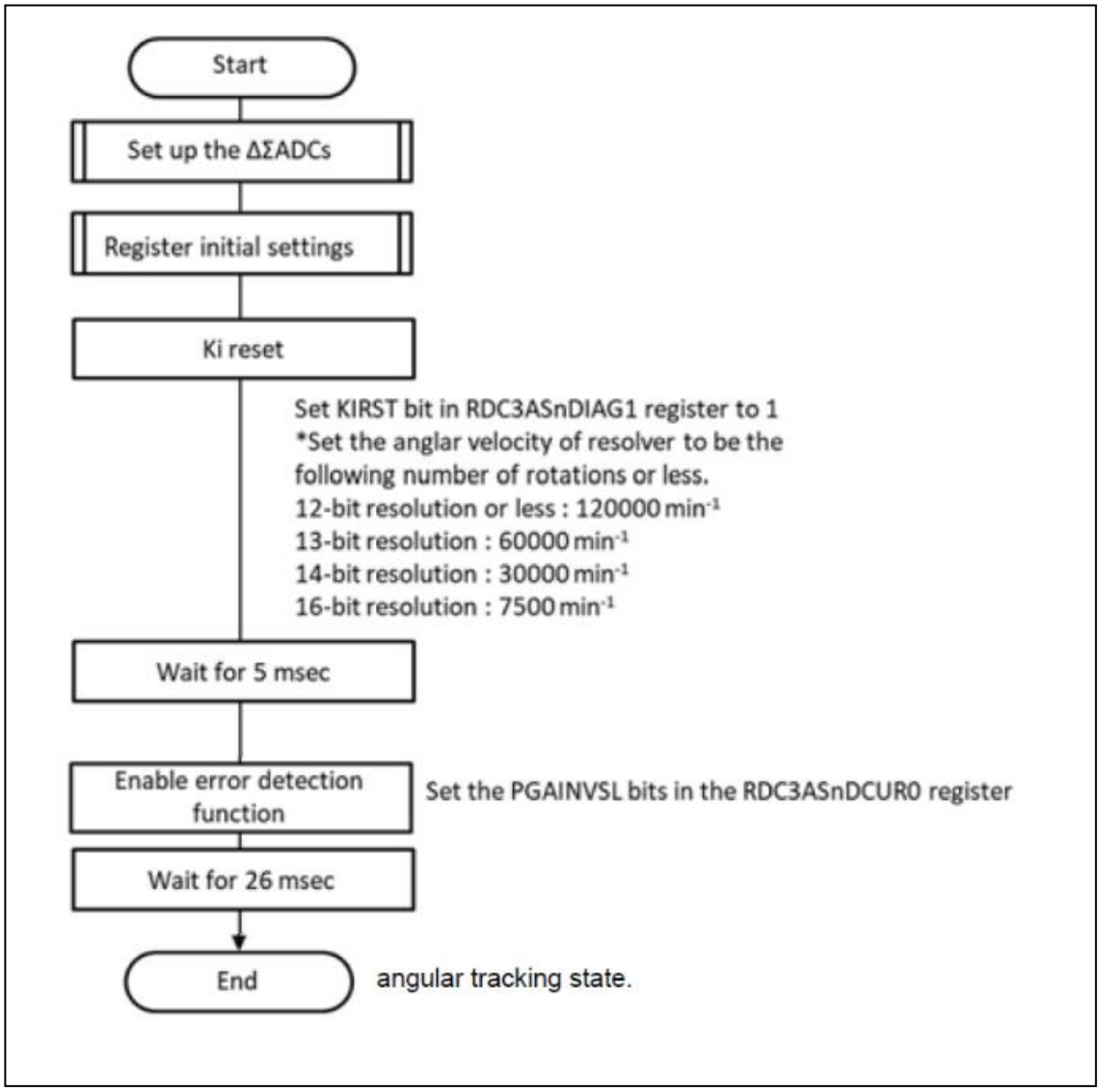


Figure 3-2 Flow of register settings and RDC operation start ※

※Note Set up for ΔΣADC is performed by calling the DSADC initialization function from main0. This flow has been modified for sample software. For details, see the user's manual.

(3) dsadc_init

After releasing the RDC3AS from Standby Mode, setting for DSADC0 common registers is performed.

And after setting the channel for SIN,COS(Ref), all channels will be started simultaneously.

Register settings used in this operation example are listed below.

Table 3-3 dsadc_init register settings

Register Name/Symbol	Set Value	Description
DSADC.ADGCR	0x00	Output as a signed value
DSADC.SYNSTCR	ADSTART=1	AD Synchronization Start : enable

(4) dsadc_cos_init

Setting for COS input of DSADC0 is performed.

Register settings used in this operation example are listed below.

The following terminals are assigned to the COS terminals of RDC3AS0.

RDC3AS0S1 DSAN150P: AN043

RDC3AS0S3 DSAN150N: AN041

Table 3-4 dsadc_cos_init register settings

Register Name/Symbol	Set Value	Description
DSADC15.VCR0	0x00200020;	Input Gain :X1 Number of input channel : 1 DFE :Not used Filter Type :F2 Differential input and use DSANn0P/DSANn0N
DSADC15.ADTCR	0x40	A/D Synchronization Start Enable
DSADC15.UCR	0x0000000	Use High Resolution Mode Data Format : Not masked End Virtual Channel Pointer :0
DSADC15.VCPTRR	0x00	A/D Conversion Ongoing Virtual Channel Number :0
DSADC15.SFTCR	0x00	DSADCnDIRj is not cleared by reading Interrupt disable

(5) dsadc_sin_init

Setting for SIN input of DSADC0 is performed.

Register settings used in this operation example are listed below.

The following terminals are assigned to the SIN terminals of RDC3AS0.

RDC3AS0S2 DSAN003P:AN012
RDC3AS0S4 DSAN003N:AN013

Table 3-5 dsadc_sin_init register settings

Register Name/Symbol	Set Value	Description
DSADC00.VCR0	0x00200026	Input Gain :X1 Number of input channel : 1 DFE :Not used Filter Type :F2 Differential input and use DSANn3P/DSANn3N
DSADC00.ADTCR	0x40	A/D Synchronization Start Enable
DSADC00.UCR	0x0000000	Use High Resolution Mode Data Format : Not masked End Virtual Channel Pointer :0
DSADC00.VCPTRR	0x00	A/D Conversion Ongoing Virtual Channel Number :0
DSADC00.SFTCR	0x00	DSADCnDIRj is not cleared by reading Interrupt disable

(6) dsadc_ref_init

Setting for REF input of DSADC0 is performed.

Register settings used in this operation example are listed below.

The following terminals are assigned to the REF terminals of RDC3AS0.

This function is not used when excitation signal input is selected from timer in LSI or external PIN is used.

RDC3AS0S2 DSAN130P:AN023
RDC3AS0S4 DSAN130N:AN030

Table 3-6 dsadc_ref_init register settings

Register Name/Symbol	Set Value	Description
DSADC13.VCR0	0x00200020	Input Gain :X1 Number of input channel : 1 DFE :Not used Filter Type :F2 Differential input and use DSANn0P/DSANn0N
DSADC13.ADTCR	0x40	A/D Synchronization Start Enable
DSADC13.UCR	0x0000000	Use High Resolution Mode Data Format : Not masked End Virtual Channel Pointer :0
DSADC13.VCPTRR	0x00	A/D Conversion Ongoing Virtual Channel Number :0
DSADC13.SFTCR	0x00	DSADCnDIRj is not cleared by reading Interrupt disable

(7) tpba0_init

After releasing TPBA0 from the Standby Mode , setting for TPBA0 is performed.

Register settings used in this operation example are listed below.

The PWM duty data is stored as 8-bit value in the array pattern_8bit. In tpba0_init, the 8 higher-order bits and 8 lower-order bits are combined and stored in TPBA0.BUFxx.

PWM period is set to 100us(frequency 10kHz) by setting TPBA0.CMP0 and TPBA0.CMP1.

Table 3-7 tpba0_init register settings

Register Name/Symbol	Set Value	Description
TPBA0.CTL	0x01	Use PCLK Data length 68bit Max buffer size 128
TPBA0.TOE	0x01	Output enables
TPBA0.TOL	0x00	Active High
TPBA0.CMP0	99	PWM period 1.25us （PCLK 80MHz）※
TPBA0.CMP1	79	Number of pattern ※

※Calculation of signal frequency

PCLK=80MHz TPBA0.CMP0=99 TPBA0.CMP1=79

(1/ PCLK)＊(TPBA0.CMP0+1)＊（TPBA0.CMP1+1）= 0.0125(us)＊100＊80=100(us) =10kHz

(8) tpba0_enable

Start the TPBA0.

Register settings used in this operation example are listed below.

Table 3-8 tpba0_enable register settings

Register Name/Symbol	Set Value	Description
TPBA0.TS	0x01	TABA0 Start timer

(9) pic_init

Setting for PIC is performed.

Register settings used in this operation example are listed below.

Table 3-9 pic_init register settings

Register Name/Symbol	Set Value	Description
PIC24.PIC2RDCEISEN0	0x00000001	Connect TPBA0TINTPAT of TPBA0 to DC3AS0.

(10) port_init

Setting for PORT is performed.

Set P34_0 to alternative mode 1 and output for TPBA0 output.

Register settings used in this operation example are listed below. ※

※ Setting can be made by using the PCR register too. In this case, protection removal is required.

Table 3-10 pic_init register settings

Register Name/Symbol	Set Value	Description
PORT0.PM34	0xFFFE	Set P34_0 to output.
PORT0.PFC34 PORT0.PFCE34 PORT0.PFCAE34 PORT0.PFCEAE34	0x0000 0x0000 0x0000 0x0000	Select alternative mode of P34_0 to 1.
PORT0.PMC34	0x0001	Set P34_0 to alternative mode

3.2 Phase Adjustment of Excitation Signal

When using VR resolver, the phase difference between excitation signal and carrier of received signal should be as minimum as possible.

Large phase difference may adversely affect RDC performance in terms of accuracy, tracking quality, etc.

User can adjust the phase difference between the carrier of the excitation signal and the resolver signal by following the procedure below.

After preparing the environment to operate RDC3AS and resolver, phase difference adjustment can be made by following the procedure below.

This adjustment should be performed with the suitable environment for actual operation to avoid the change of phase.

1. Activate event timer(ET) and A/D Conversion Start Trigger of RDC3AS.
   And input 1/4 of the excitation period value to RLD[15:0] of RDC3ASnETMCNT register.
   The excitation period value can be obtained from RDC3ASnETCAP register. Register settings are listed below.

Table 3-11 ET register setting for phase adjustment

Register Name/Symbol	Set Value	Description
RDC3AS0.ETEN	0x00050000	Enable event timer(ET) and A/D Conversion Start Trigger※
RDC3AS0.ETMCNT	0x0000XXXX	Set 1/4 of the excitation period value to RLD[15:0] For 10kHz , this value is 0x03E7.

※ This setting is same as in Table 3-2.

2. Set provisional value to REFDLCT[15:0] of RDC3ASn.REF register.
   And after operating RDC3AS, collect RDC3ASnETC value.

3. Adjust value of REFDLCT[15:0] of RDC3ASn.REF register to maximize the RDC3ASnETC value.
   The example of RDC3ASnETC value when the REFDLCT[15:0] value is changed is shown in the figure below.
   In this example, angle of resolver is 45 degree and frequency of excitation signal is 10kHz.

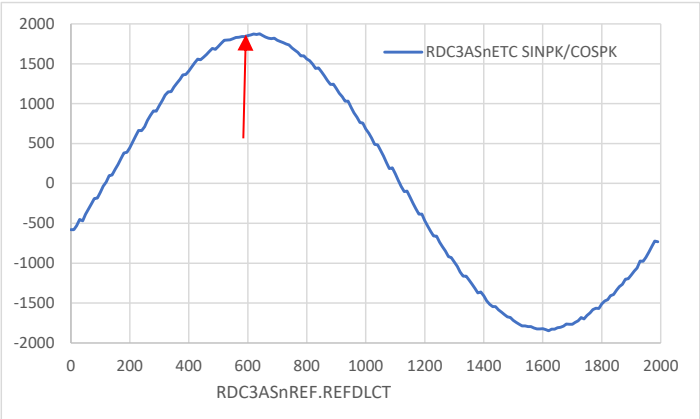


Figure 3-3 Example of phase adjustment
(RDC3ASnETC value with changing REFDLCT[15:0] value)

This example shows the reasonable value to set REFDLCT[15:0] is approximately at 600.

4. Correction for internal circuit
   With setting REFINSL=01 or 10,and REFETSL=0, the resolver signal has a delay(ΔT) of DSADC's sampling period (Fs) against exciter signal.

It needs to set the value with considering this delay for phase adjustment of excitation signal and/or setting for using ET timer.

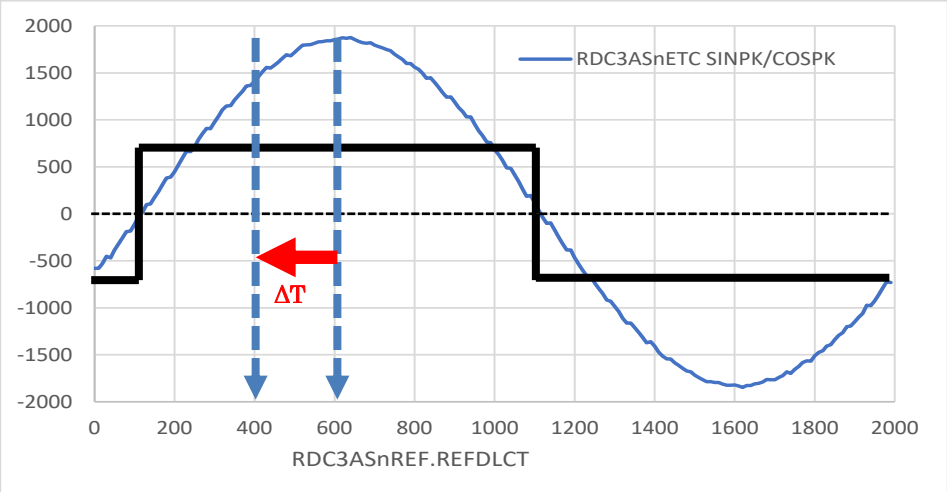


Figure 3-4 Example of phase adjustment

Delay(Δ T) settings are listed below.

Table 3-12 Delay(Δ T) value for internal circuit correction

DSADC Setting	Fs	Delay(Δ T)
F1a,F3a	100kHz	10us (200 LSB)※
F1b,F2,F3b,F4	200kHz	5us (100 LSB)※
F5	400kHz	2.5us (50 LSB)※

※LSB is the converted value to set to REFDLCT[15:0]. （1LSB=50ns）

For example, in the measurement results of Figure 3-4, if the DSADC setting is F1a, REFDLCT[15:0] is set to 400 (190H) at 600-200.

3.3 Supplementary Explanation of R/D Converter Usage

3.3.1 Control Variation Determination Clock

User's Manual states to set the control variation determination clock period to be longer than the excitation signal period. Please set longer control variation determination clock period to stabilize the operation when problems such as unable to track occur.

3.3.2 Input Signal Amplitude of Ki Reset

If Ki reset is performed when the SINMNT/COSMNT signal amplitude is smaller than as specified in User's Manual, the R/D converter will attempt to track the abnormal signal. Even if the SINMNT/COSMNT signal amplitude returns to normal afterwards, tracking cannot be performed or takes longer time to track.

DSADC has delay from signal input to output to RDC3AS due to internal filter.
Timing of Ki reset should be designed by considering this characteristic.

The signal amplifier of SINMNT,COSMNT can be checked with RDC3ASnETCregister.

3.3.3 Various Gain Values of Forced Gain Control

The 12-Level AGC is selected for the gain in the forced gain control, and the first Kv gain becomes the maximum value (x128). During the forced gain control, the Kv gain is automatically determined according to the AGC. Ki and Kp gains are fixed to the values exclusive for the forced gain control.

3.3.4 Correcting for Group Delay of DSADC

The correction for group delay of DSADC can be set by using DSDL[1:0] of RDC3ASnDSST register.

3.4 Input Method for External Signal

The method of inputting the excitation signal to the RDC3AS is not only done by using timer signal input via PIC method but can also be done by using DSADC method and using EXT_REF_IN input method. The outline of these methods is shown below.

3.4.1 Method of Using DSADC input

To use DSADC to input excitation signal, the DSADC channel for receiving the REF signal should be set the same as SIN and COS signals.

- After setting DSADC for REF input , set REFINSL[1:0] of RDC3ASnREF register to 00B.
- Set EXRFPSL [1:0] of RDC3ASnREF register to 00B.

In this method, PIC is not used.

To use this method, center level of REF input signal must be adjusted to 0.
If REF input signal has bias , the duty of the internal excitation signal may be biased, which can adversely affect the characteristics of RDC.

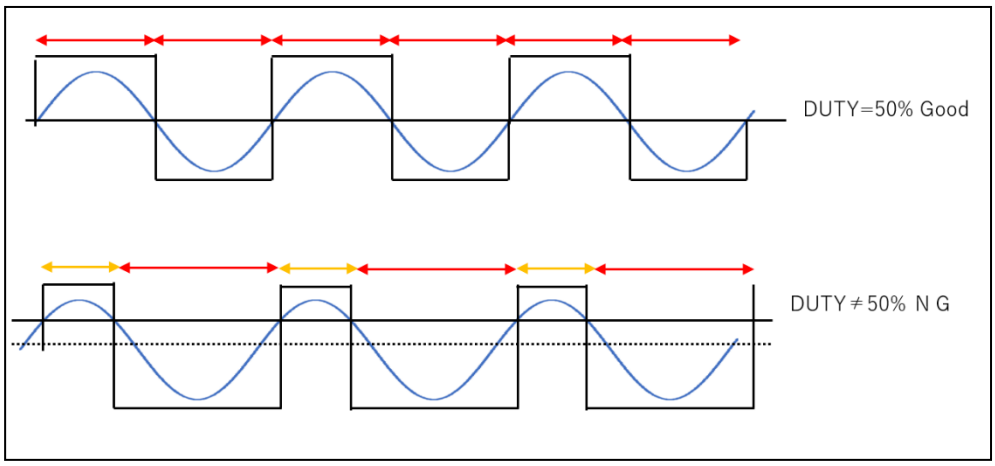


Figure 3.5 Duty bias of excitation signal

3.4.2 Method of Using EXT_REF_IN Input

To use EXT_REF_IN to input excitation signal , set RDC3ASnREF register and PORT.

- Set REFINSL[1:0] of RDC3ASnREF register to 10B.
- Set EXRFPSL [1:0] of RDC3ASnREF register to 00B.
- Set PORT for REFPLS_EXIN assign.

Example of alternative mode selection

- For RDC3AS0 :Set P34_1 to alternative mode 3 and input for RDC3AS0_REFPLS_EXIN.
- For RDC3AS1 :Set P00_4 to alternative mode 8 and input for RDC3AS1_REFPLS_EXIN.

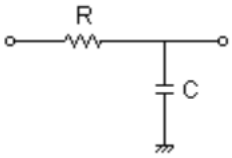
In this method, PIC is not used.

To use this method, the duty of REF input signal must be adjusted to 50%.
The bias in duty can adversely affect the characteristics of RDC.

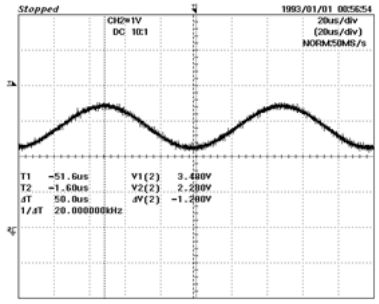
3.5 Smoothing for PWM generated with TPBA

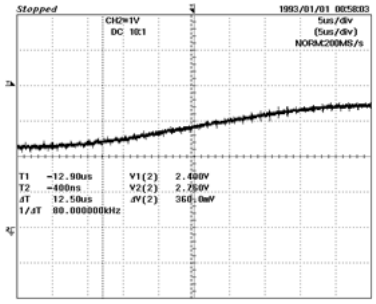
TPBA0 generates the exciter signal in sample software. The settings are shown in table 3-7.

In these setting , exciter signal is generated as PWM in 1.25us(800kHz) PWM period. And it needs to smooth with LPF to use for AC resolver. User needs to select optimum LPF with considering output level and ripple. The example of LPF setting with CR shown in Fig 3.6.



Example of CR LPF

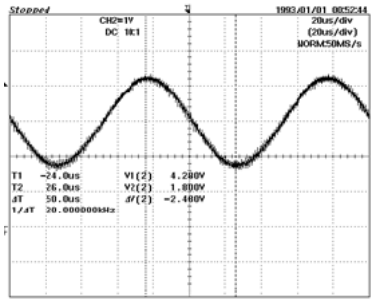


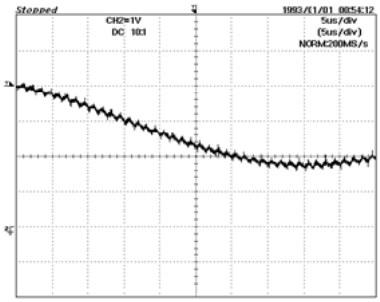


Setting1

C= 1000pF R=33kOHM
Fc is about 4800Hz

The level is 1.20Vpp.
This setting looks good.

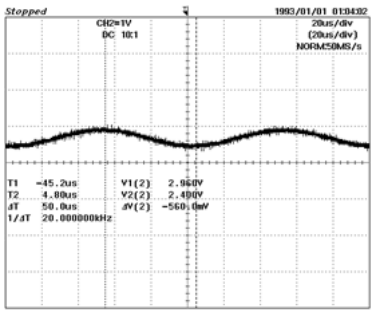


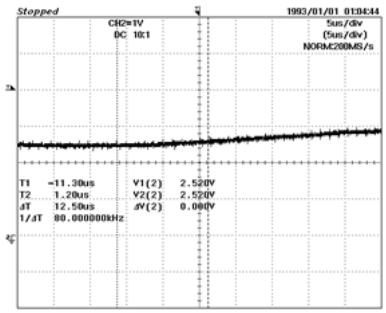


Setting2

C= 1000pF R=10kOHM
Fc is about 16000Hz

The level is 2.48Vpp.
Wave form looks be jagged by PWM yet.





Setting3

C= 1000pF R=100kOHM
Fc is about 1600Hz.

The level is 0.56Vpp.
Wave form looks good ,but level is small. Afraid bad S/N.

Figure 3.6 Duty bias of excitation signal

4. Error Detection

4.1 Overview of Error Detection Function

4.1.1 Configuration of R/D Converter

Figure 4.1 shows configuration of a resolver and the R/D converter. The RDC3AS has a function to detect errors of input signal from DSADC, excitation signal period, and tracking loop.

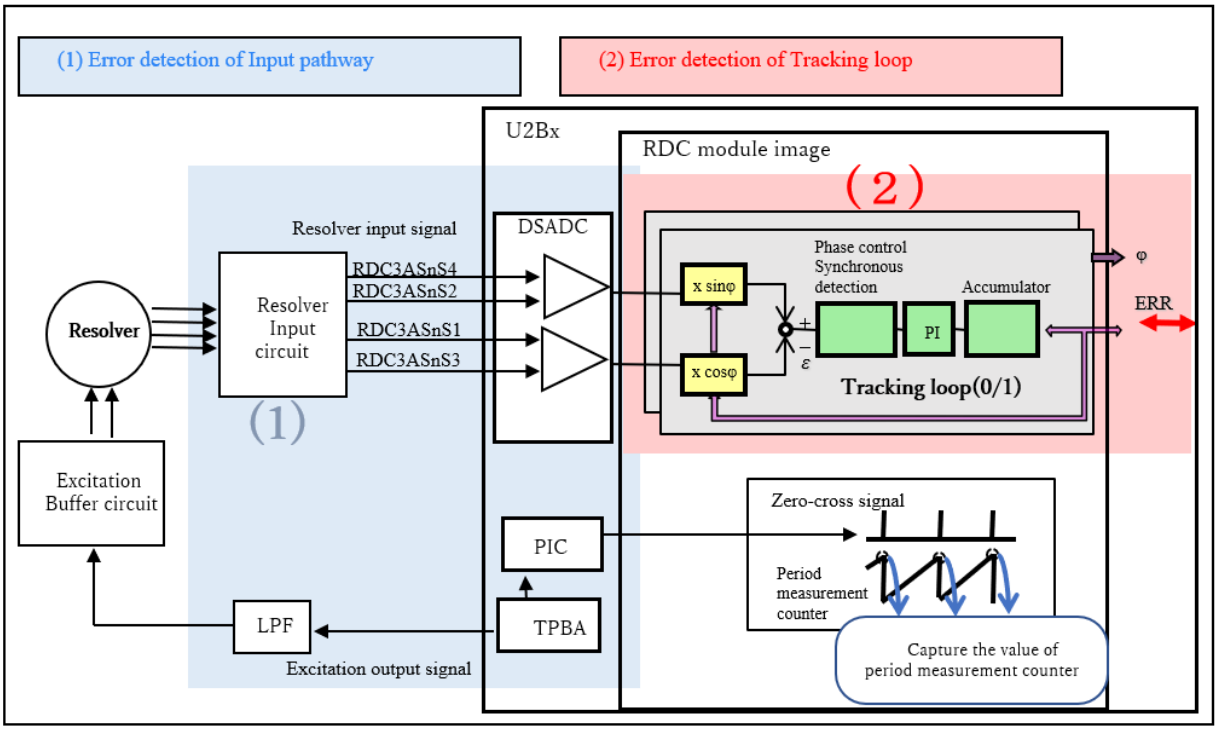


Figure 4.1 Simplified Diagram of R/D Converter

4.1.2 Error Detection in Input Paths

There are four kinds of error detections in input paths as shown in Figure 4.2.

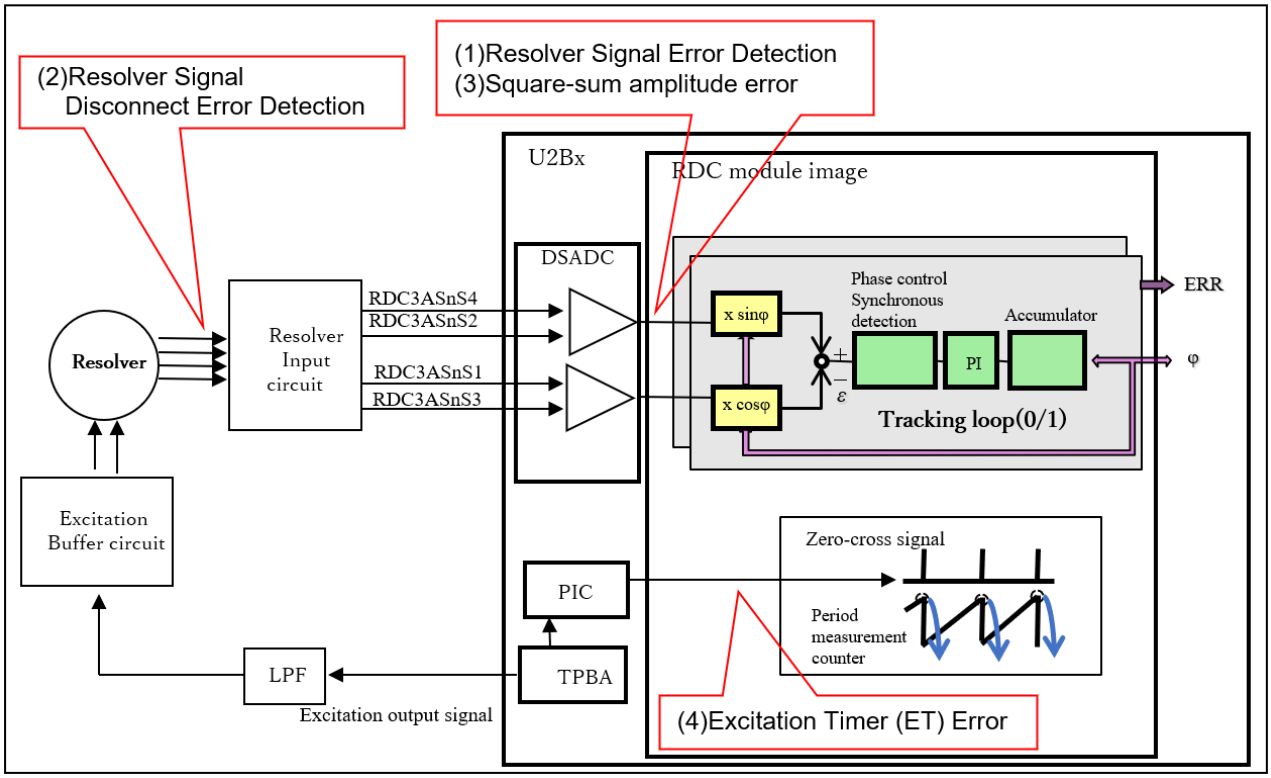


Figure 4.2 Error Detection in Input Paths

The overview of each error detection is as follows.

1. Resolver Signal Error Detection
   This function detects the amplitude reduction of the resolver signal caused by an error in the excitation signal. An error occurs when the resolver signal continues being within the threshold for a certain time.

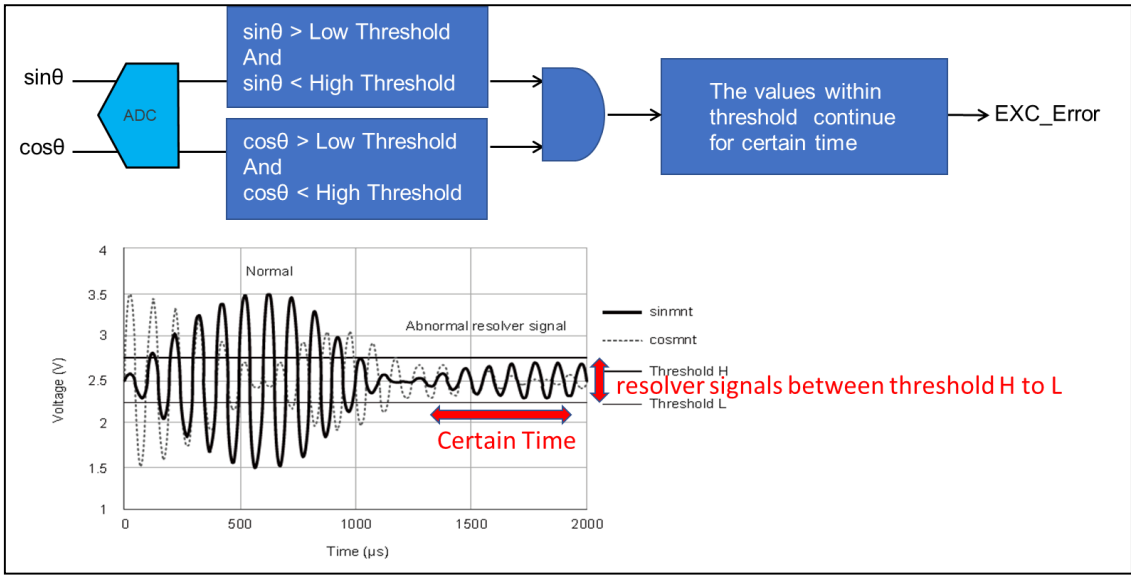


Figure 4.3 Overview of Resolver Signal Error Detection

2. Resolver Signal Disconnection Error Detection (cos, sin)
   This function detects disconnection of the resolver signal.
   For the VR resolver, error is detected when the common potential (the central potential of amplitude) of SINMNT and COSMNT continues to exceed the threshold value. For the DC resolver, error is detected when the potential of SINMNT and COSMNT exceeds the threshold value.

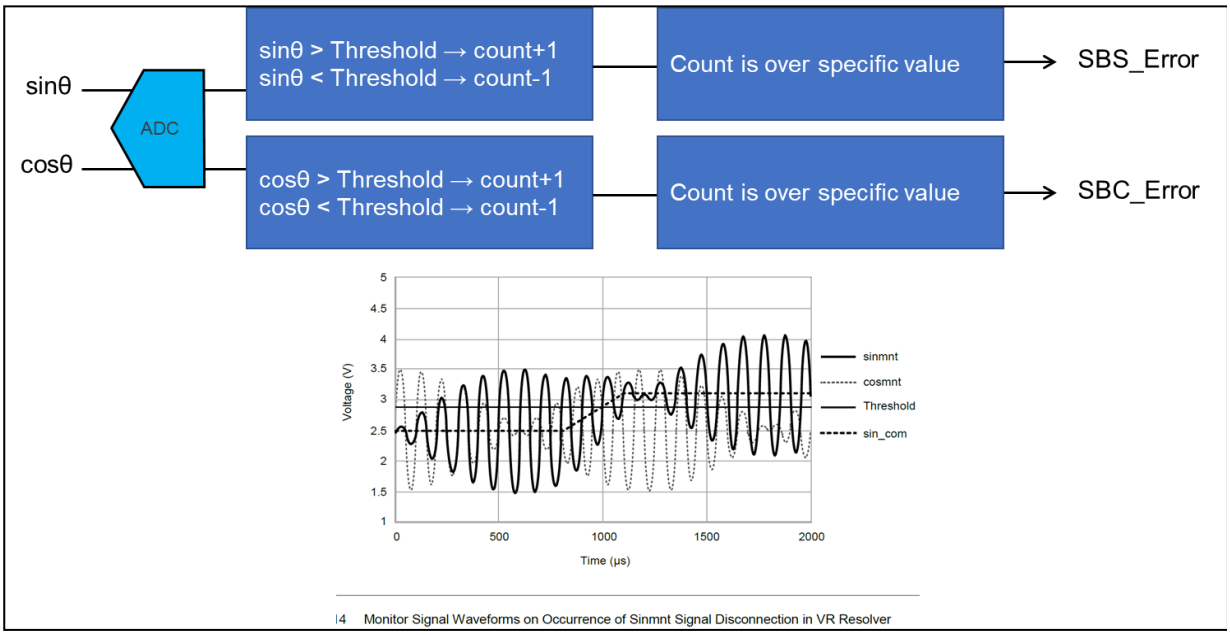


Figure 4.4 Overview of Resolver Signal Disconnection Error Detection (cos, sin)

3. Sum-of-Squares Amplitude Error Detection
   This function detects modulation, distortion, and noise in the amplitude of the resolver signal.

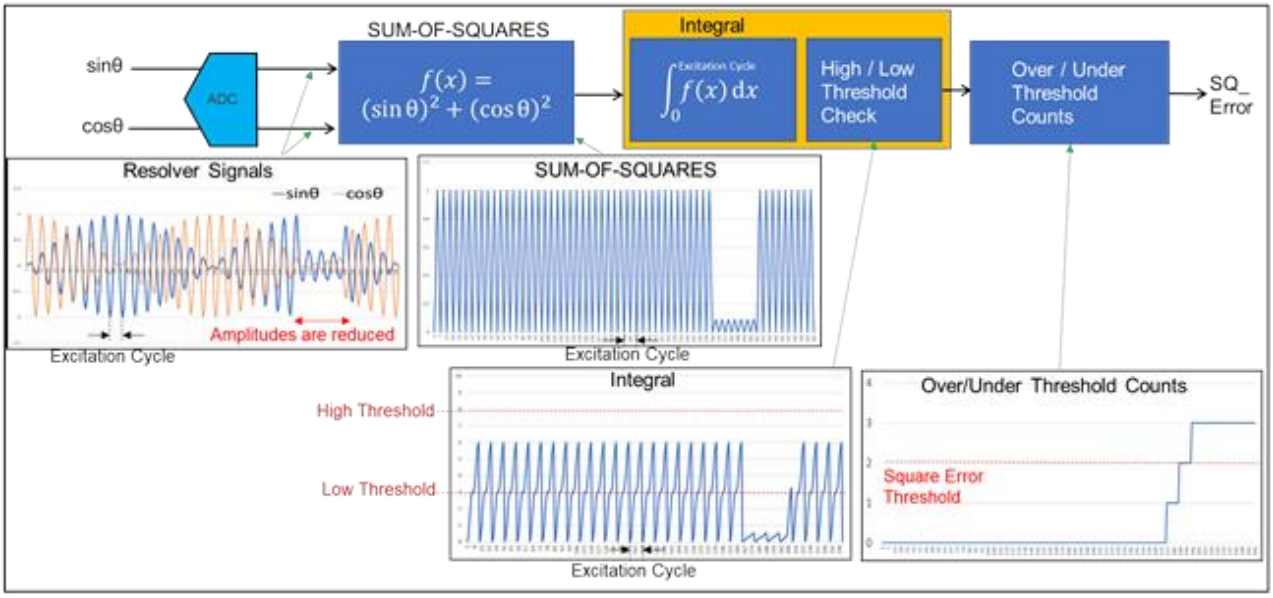


Figure 4.5 Overview of Sum-of Squares Amplitude Error Detection

4. Excitation Period Error Detection
   This function measures the period of the excitation signal. An error occurs when the period of the excitation signal is exceeding the expected value.
   The threshold is set to the CMP[15:0] of the RDC3ASnETCAP register.

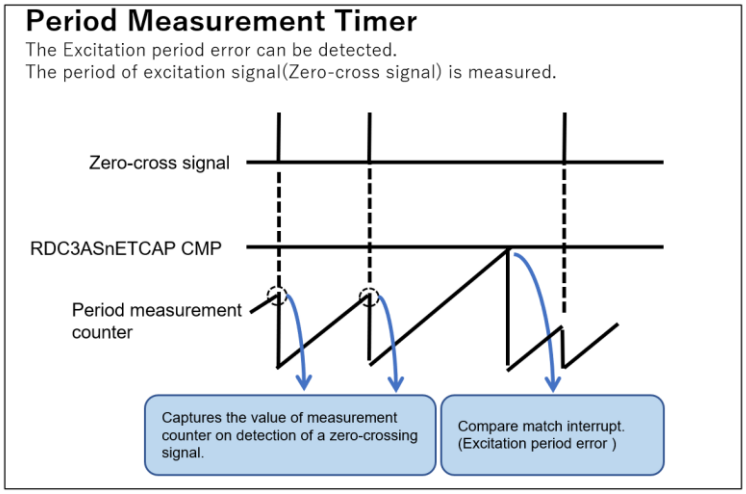


Figure 4.6 Overview of Excitation Period Error Detection

4.1.3 Error Detection in the Tracking Loop

There are two kinds of error detections in the tracking loop as shown in Figure 4.7.

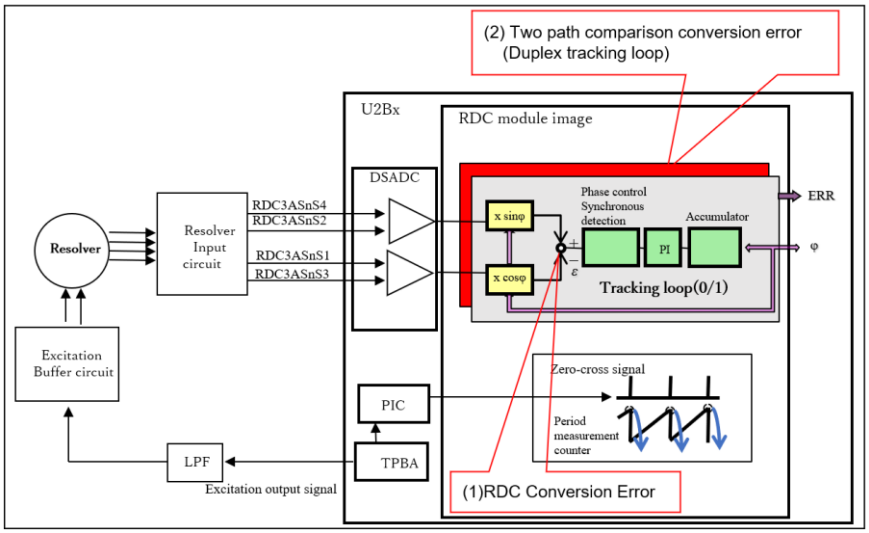


Figure 4.7 Error Detection in the Tracking Loop

The overview of each error detection is as follows.

1. R/D Conversion Error Detection
   This function monitors the control variation in the R/D conversion loop and detects calculation errors in the R/D conversion function.

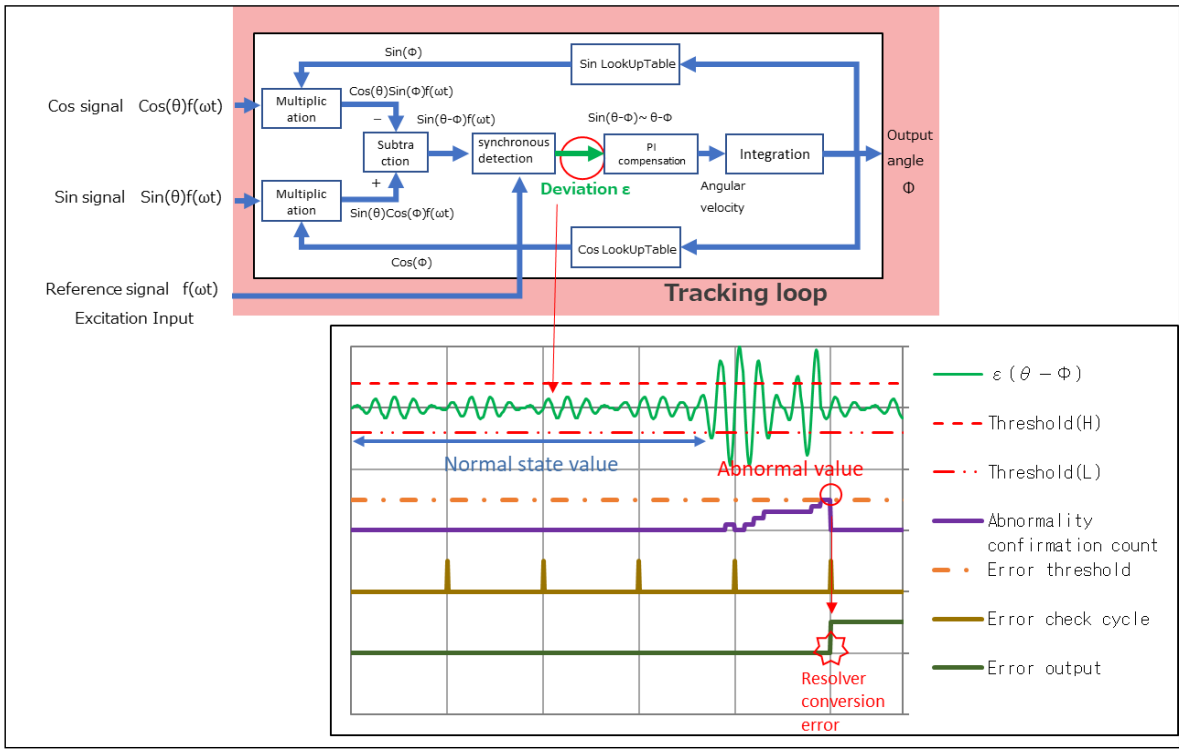


Figure 4.8 Overview of R/D Conversion Error

2. Two Paths Comparison Conversion Error Detection
   This function monitors the redundancy by comparing results of angle conversion in two paths. phi0 and phi1 in Figure 4.9 are always compared and monitored. An error occurs when results of phi0 and phi1 are different.

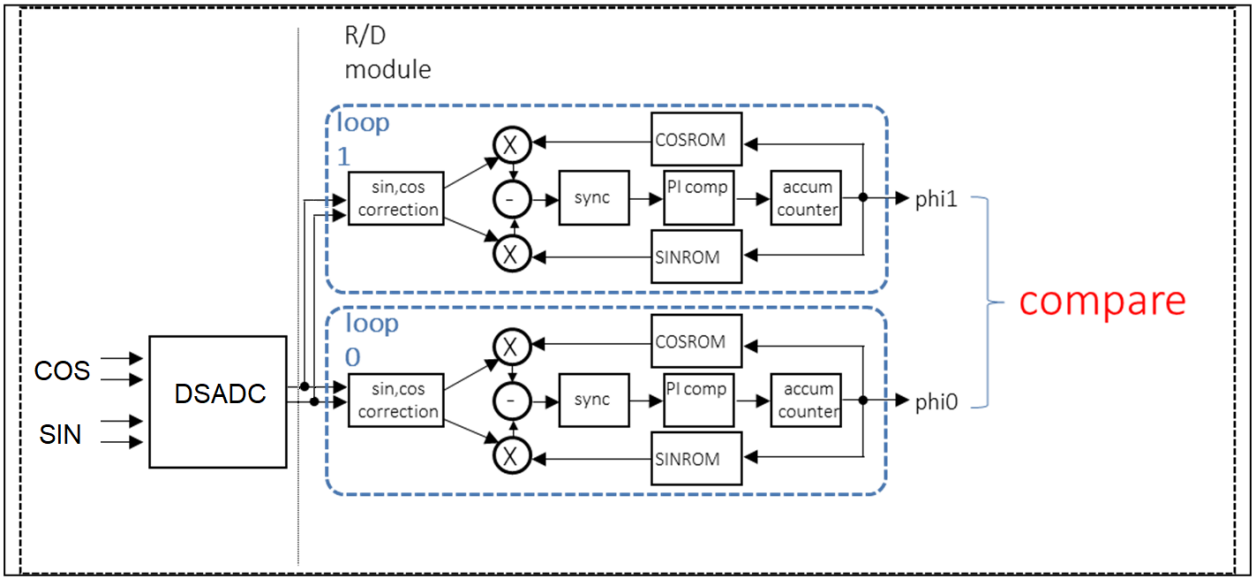


Figure 4.9 Overview of Two Paths Comparison Conversion Error Detection

4.2 Details of Error Detection Function

This section explains details of the error detection methods of the RDC3AS.

4.2.1 Resolver Signal Error Detection

This function detects the amplitude reduction of the resolver signal caused by an error in excitation signals input to the resolver. When a resolver signal error is detected, the RDC error interrupt request signal becomes high.

A resolver signal error is detected if the received signal by DSADC (SINMNT, COSMNT) fall below the threshold for approximately 300µs or longer. As for the DC resolver which does not have the excitation signal, a resolver signal error is detected if the monitor outputs fall below the threshold for approximately 300µs or longer.

The threshold can be set by " 2 × EXCETH[7:0) × 8 × (ADSVREFH -ADSVREFL)/4096 (Vpp)".

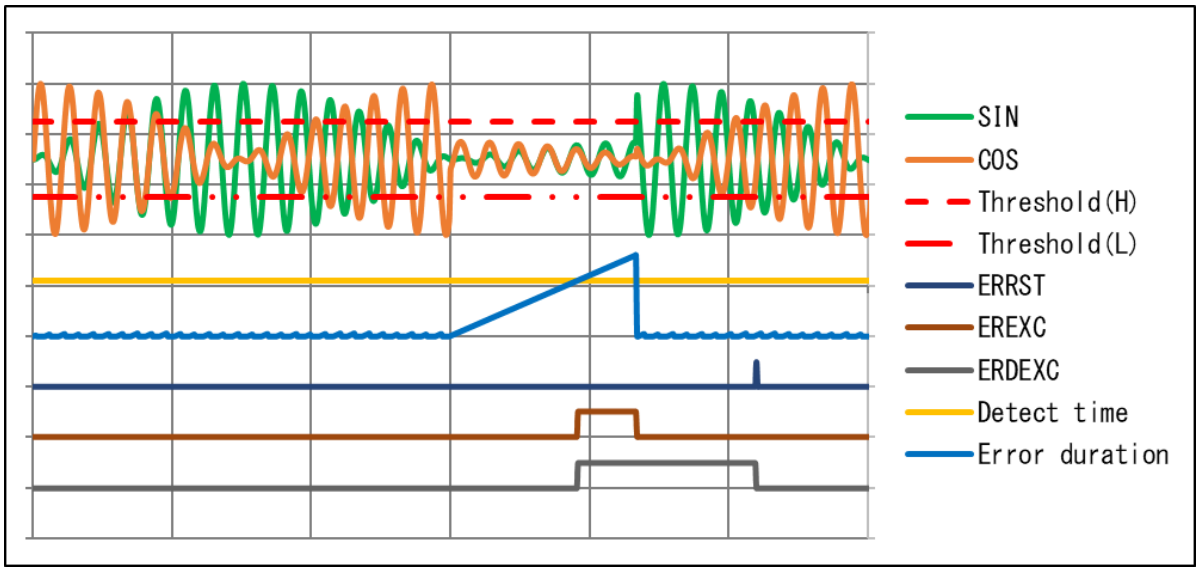


Figure 4.10 Resolver Signal Error Detection When VR Resolver is Used

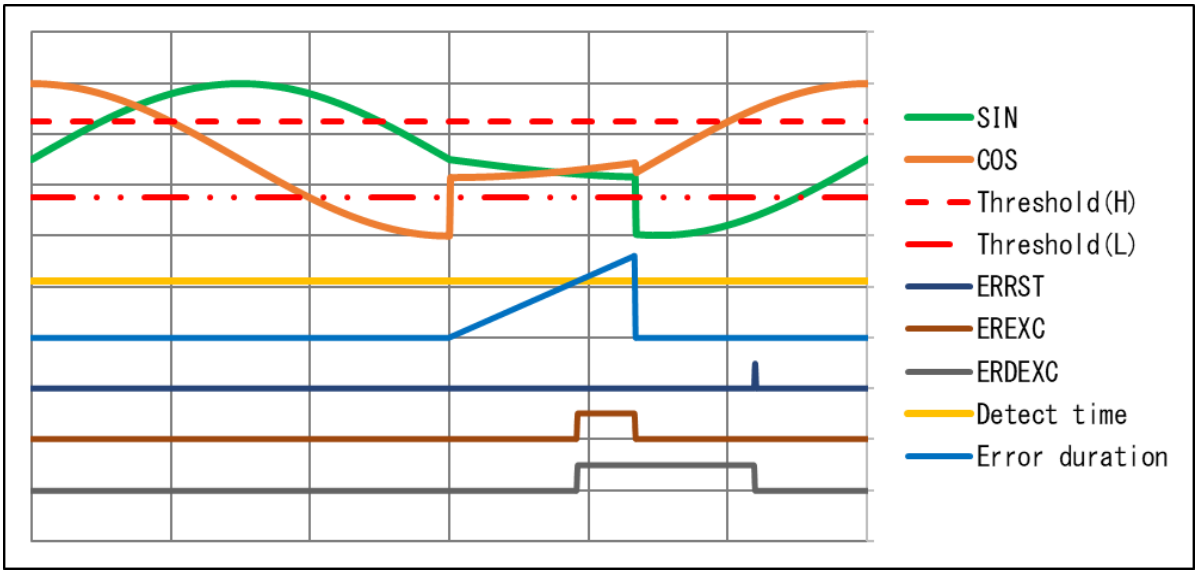


Figure 4.11 Resolver Signal Error Detection When DC Resolver is Used

4.2.1.1 Example of Register Settings

Table 4.1 shows the example of register settings of when the resolver signal error detection function is used.

Table 4.1 Example of Register Settings of When Resolver Signal Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 0/ RDC3ASnDIAG0	Resolver Signal Error Comparison Threshold/ EXCETH[7:0]	0x1A	Sets the threshold for use in detecting errors in the resolver signal. Set value in the left column is 0.102× (ADSVREFH - ADSVREFL) (Vpp).
Error detection register 1/ RDC3ASnDIAG1	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ASnDIAG2	Resolver Signal Error Select / EREXCS	0	Set the bits ERR, ERHD, EREXC, and ERDEXC to 1 on occurrence of a resolver signal error.

4.2.2 Resolver Signal Disconnection Error Detection

This function detects disconnection (including contact failure) of the resolver signals (S1 to S4). When a resolver signal disconnect error is detected, the RDC error interrupt request signal becomes high.

When operation with a VR resolver is selected (by setting the combination of values as SENS=1 and EXIO=0), this function monitors the common levels fluctuation of the received signal by DSADC (SINMNT, COSMNT) and determines any case of them exceeding the configured threshold to be a disconnection error. The threshold can be set by "SGBTH[7:0] × 8×(ADSVREFH - ADSVREFL)/4096 (V) ".

When operation with a DC resolver is selected (by setting the combination of values as SENS=0, EXIO=1), this function monitors whether the DC level of the monitored signals is exceeding the threshold or not. The threshold can be set by "SGBDTH[7:0] × 8 + 1024) × (ADSVREFH -ADSVREFL)/4096 (V)".

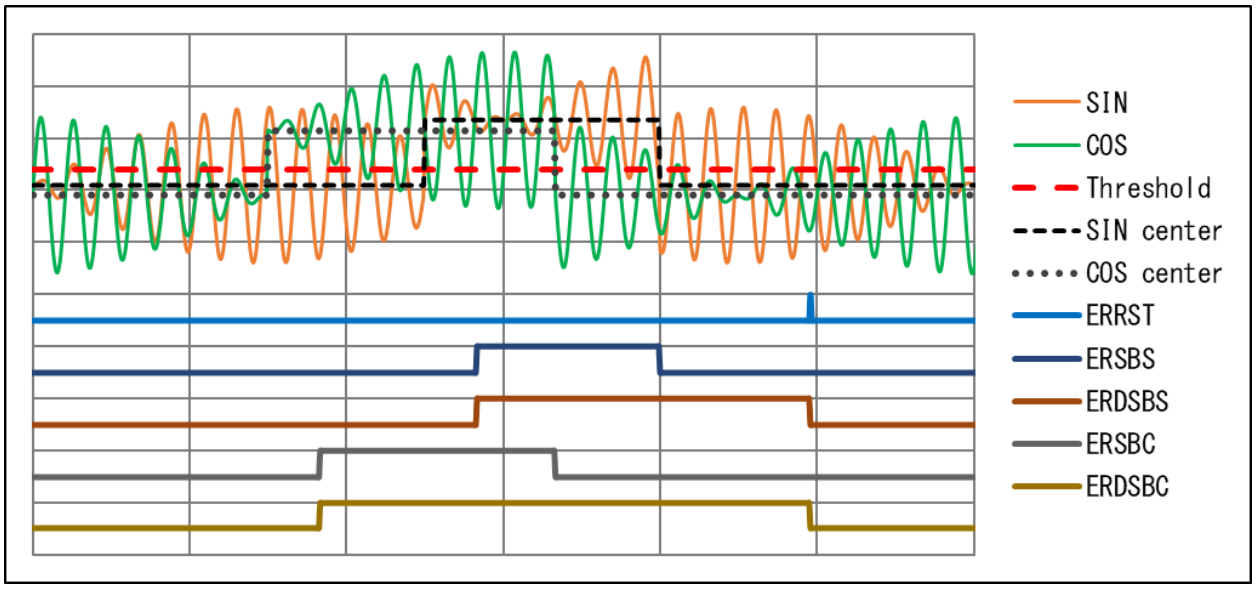


Figure 4.5 Resolver Signal Disconnection Error Detection When VR Resolver is Used

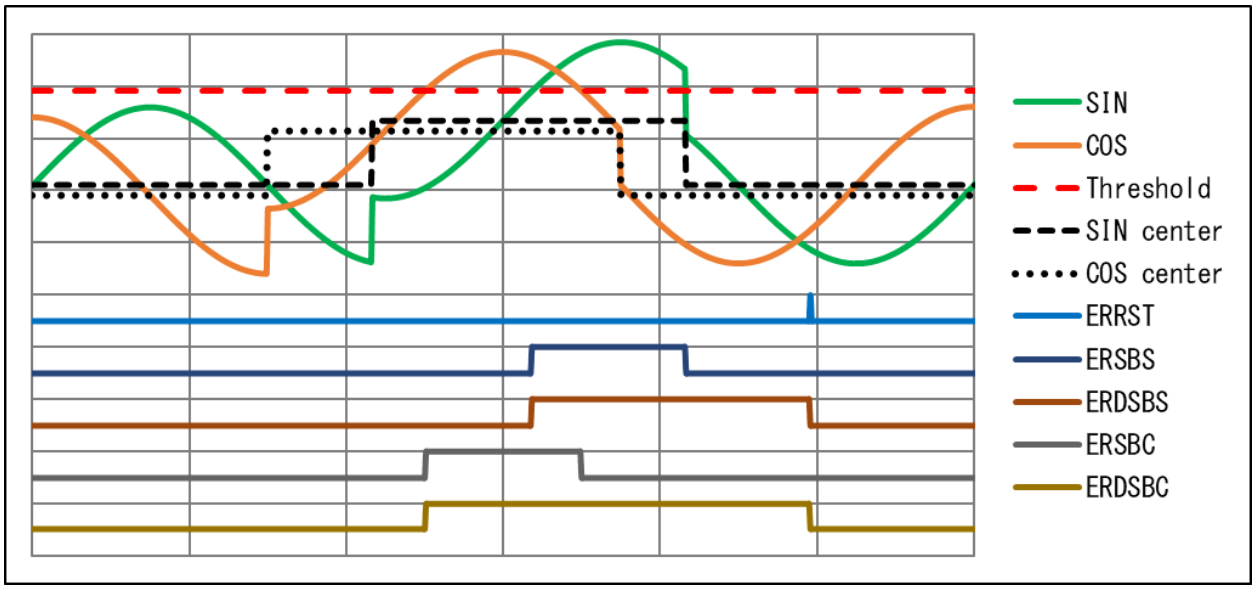


Figure 4.6 Resolver Signal Disconnection Error Detection When DC Resolver is Used

4.2.2.1 Example of Register Settings

Table 4.2 shows the example of register settings of when the resolver signal disconnection error detection function is used.

Table 4.2 Example of Register Settings of When Resolver Signal Disconnection Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 0/ RDC3ASnDIAG0	Disconnect Error Comparison Threshold (for VR Resolver) / SGBTH[7:0]	0x29	Sets the threshold for use in detecting disconnect errors when the VR resolver is used. Set value in the left column is0.08 × (ADSVREFH - ADSVREFL) (V).
	Disconnect Error Comparison Threshold Setting (for DC Resolver) / SGBDTH[7:0]	0x33	Sets the threshold for use in detecting disconnect errors when the DC resolver is used. Set value in the left column is 0.35 × (ADSVREFH - ADSVREFL) (V).
Error detection register 1/ RDC3ASnDIAG1	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ASnDIAG2	Disconnect Error (Cosine) Select / ERSBCS	0	Set the bits ERR, ERHD, ERSBC, and ERDSBC to 1 on occurrence of a disconnect error (cosine side)
	Disconnect Error (Sine) Select / ERSBSS	0	Set the bits ERR, ERHD, ERSBS, and ERDSBS to 1 on occurrence of a disconnect error (sine side)

4.2.3 R/D Conversion Error Detection

This function monitors the control variation in R/D conversion loop and detects operation errors in the R/D conversion function. When an R/D conversion error is detected, the RDC error interrupt request signal becomes high.

A control variation (ε) is recognized as excessive if the control variation rises above or falls below a configured threshold level. The threshold is a fixed value (see Section 66.5.3, Error Detect Characteristics in the user's manual for details). An R/D conversion error is detected if the control variation stays excessive for more than 50% of the error determination time set in the EDPS[1:0] bits in the RDC3ASnDIAG1 register.

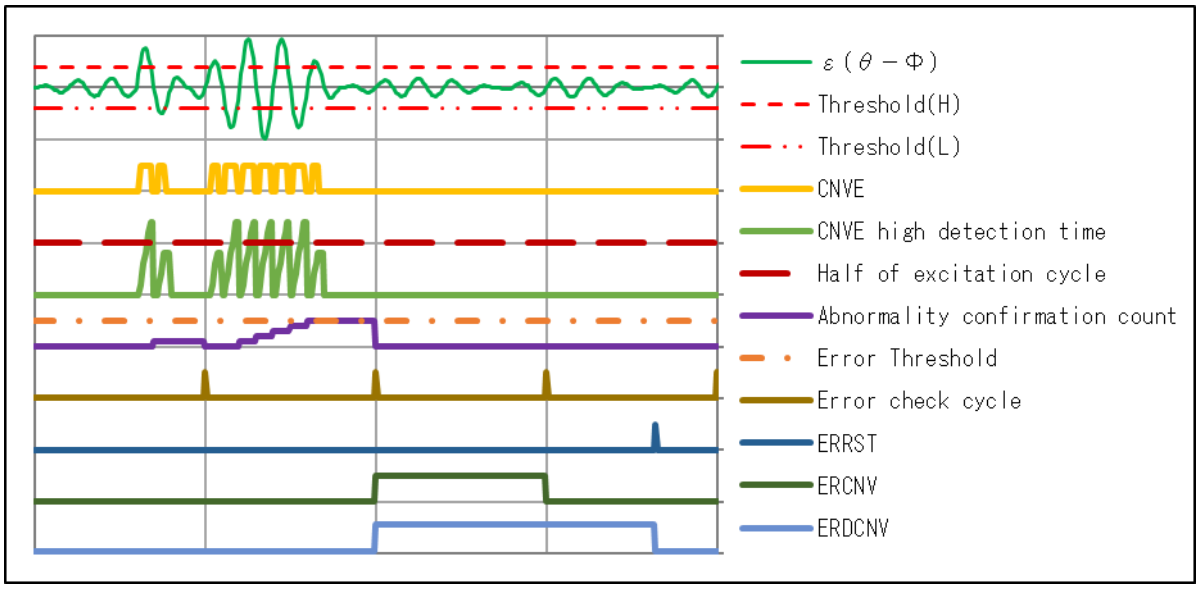


Figure 4.7 R/D Conversion Error Detection

"The internal control variation ε" is explained in Section 49.1.1.3 Operating Principle in the user's manual. When there is a difference between θ and Φ, the control variation becomes sine wave shape of the excitation period. To determine the gain of the PI compensator, the detected ε by synchronous detection is used.

When a resolver input angle (θ) and an R/D output angle (φ) are different, ε becomes a signal with an amplitude in the excitation period as sin(θ-φ) has a value (Figure 4.8). When a resolver input angle (θ) and an R/D output angle (φ) are matching, the value of ε will be nearing COM(2.5V) (Figure 4.9).

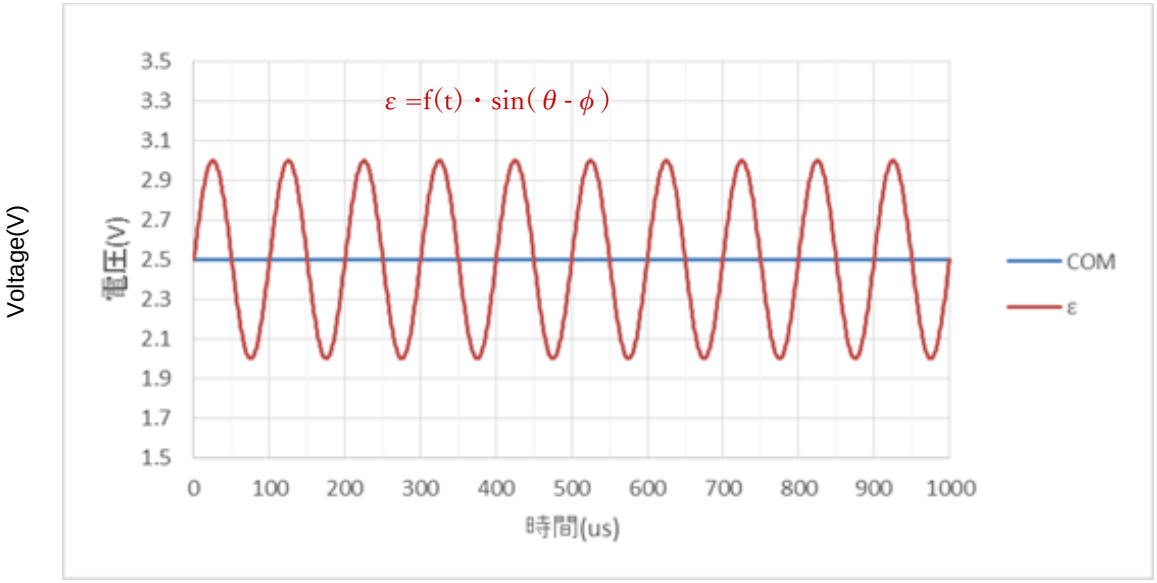


Figure 4.8 The Internal Control Variation When Angles are Different

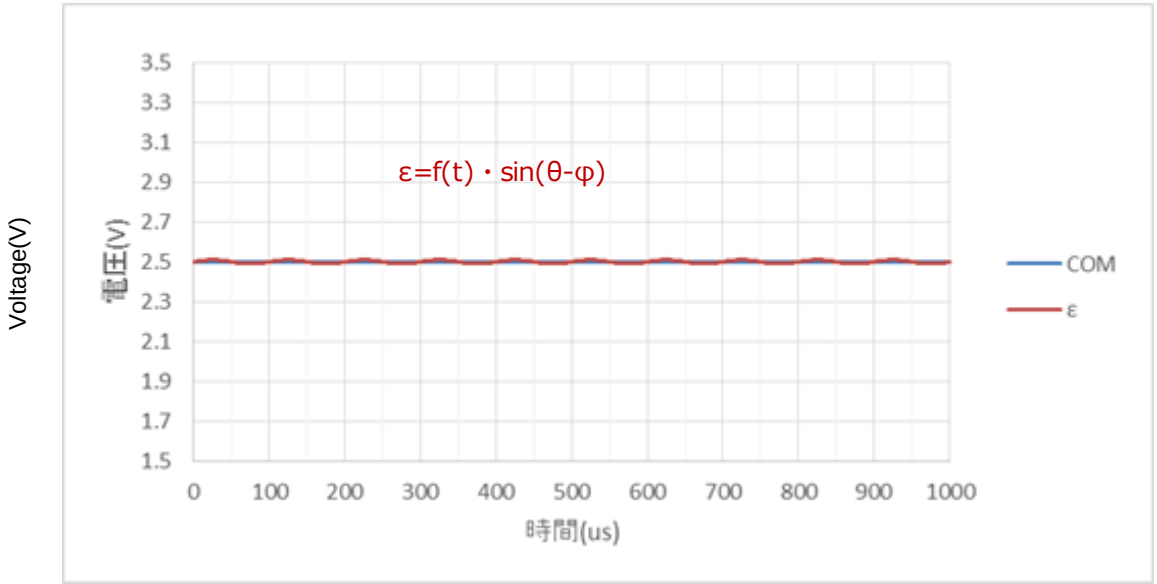


Figure 4.9 The Internal Control Variation When Angles are Matching

Since ε has an amplitude in the conversion error state in which a resolver input angle (θ) and a R/D output angle (φ) are different, set thresholds on the high side and the low side, and CNVE signal will be generated whenever the ε value is out of the ranges. When the CNVE is 1, the amplitude of ε is large.

The proportion of 1 and 0 of the CNVE signal can be determined at the counter circuit at every half period of excitation signal. When the proportion of 1 is exceeding 50% of the entire excitation half period, that excitation half period is determined as abnormal, and determined as normal when it is not exceeding. Determination of normal and abnormal of each excitation half period for the conversion error determination time (e.g., 7.3ms) which is selected by EDPS bit are aggregated. When abnormal half period is exceeding 50% of the entire half period, ERCNV bit and ERDCNV bit are set as an R/D conversion error.

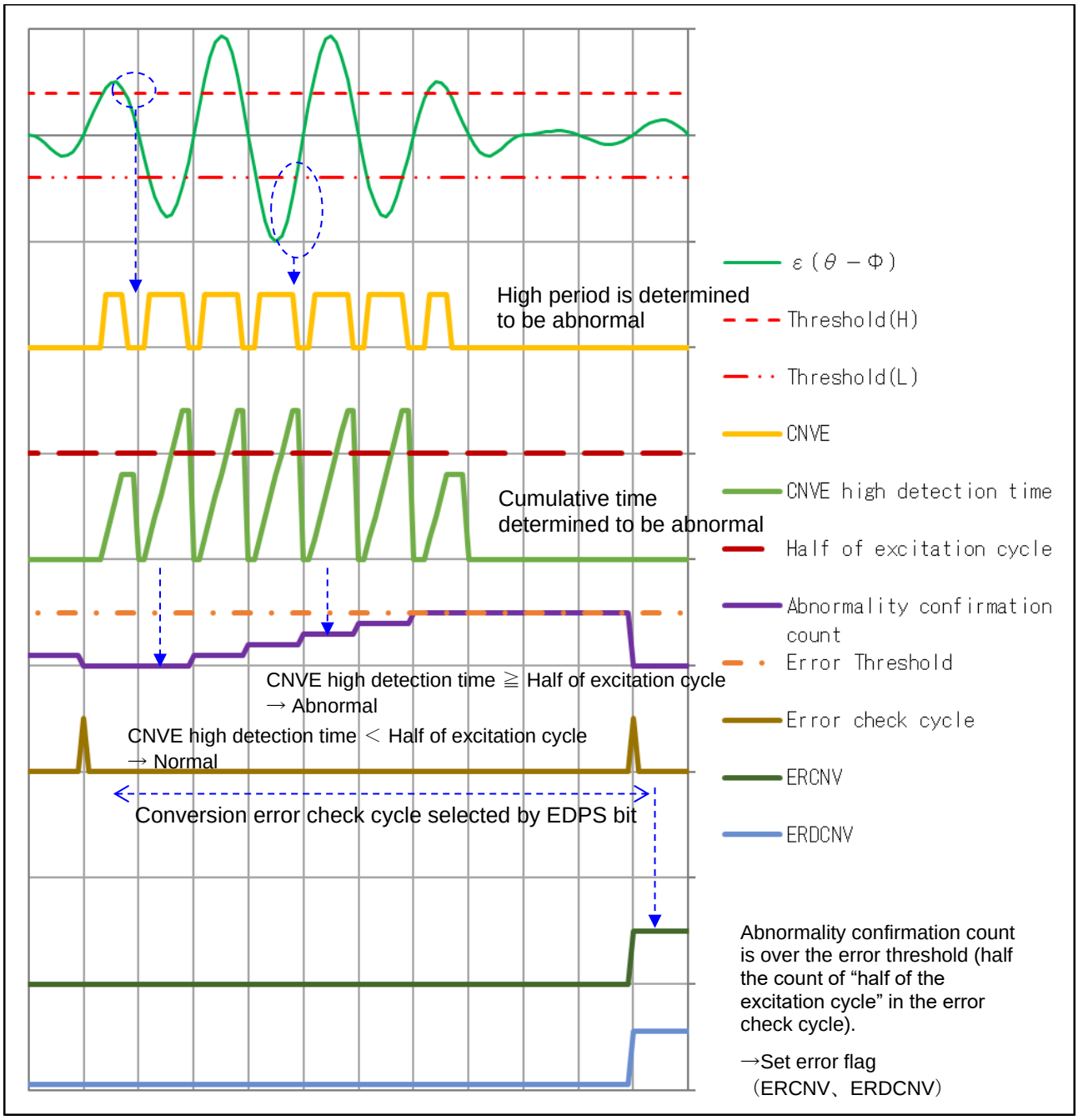


Figure 4.10 Principle of R/D Conversion Error Detection

4.2.3.1 Example of Register Settings

Table 4.3 shows the example of register settings of when the R/D conversion error detection function is used.

Table 4.3 Example of Register Settings of When R/D Conversion Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 1/ RDC3ASnDIAG1	Conversion Error Detection Circuit Select / CVEDS	0	The conversion error detection circuit which supports high-speed rotation of the RD conversion error detection signal.
	RD Conversion Error Determination Time Select / EDPS[1:0]	3	Selects the error determination time (for preventing sudden acceleration) for RD conversion Errors. 11b：7.37 msec
	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ASnDIAG2	Conversion Error Select / ERCNVS	0	Set the bits ERR, ERHD, ERCNV, and ERDCNV to 1 on occurrence of a conversion Error.

4.2.4 Two Paths Comparison Conversion Error Detection

This function compares the results of angle conversion from two loops and detects conversion errors and failures in the circuit.

This function compares the phi1 angles output and the phi2 angles output, and if the difference between two angles is larger than the threshold, this is judged to be a two paths comparison conversion error. The threshold value is set by the P2ANT[1:0] bits.

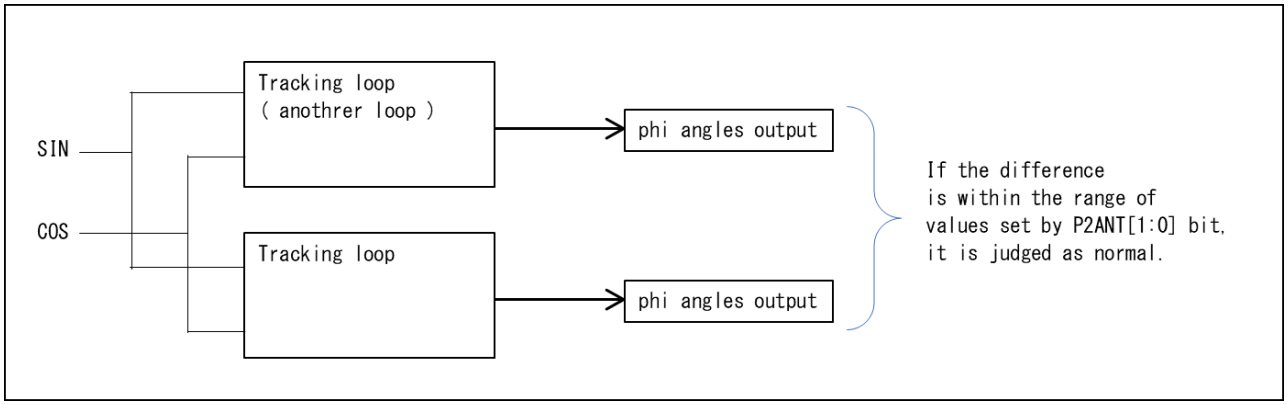


Figure 4.18 Two Paths Comparison Conversion Error Detection

4.2.4.1 Example of Register Settings

Table 4.4 shows the example of register settings of when the two paths comparison conversion error detection function is used.

Table 4.4 Example of Register Settings of When Two Paths Comparison Conversion Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 0/ RDC3ASnDIAG0	Two Paths Conversions Error Threshold / P2ANT [1:0]	0	Sets the threshold for use in detecting errors by comparing the results of conversion between phi1 and phi2 to ±8LSB.
Error detection register 1/ RDC3ASnDIAG1	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ASnDIAG2	Two Paths Conversion Error Select / ERP2S	0	Set the bits ERR, ERHD, ERP2, and ERDP2 to 1 on occurrence of a two paths conversion error

4.2.5 Sum-of-Squares Amplitude Error Detection

This function detects modulation, distortion, and noise in the amplitude of the sine and cosine signals input from the resolver.

The sum-of-squares of the received signal by DSADC (SINMNT, COSMNT) are taken and integrated within the excitation period.

Upper and lower threshold values are set for the value thus calculated and the number of times the calculated value rise above or fall below the thresholds is counted. If the number exceeds the threshold for the counted value, it is output as a sum-of-squares amplitude error. The procedure runs automatically, but user is required to set the upper and lower threshold for the integrated sum-of-squares values in the SQHTH and SQLTH bits and the threshold for the number of times the calculated value falls outside the range in the SQCTH bits. The counter values are cleared at the desired time by writing to the SQERST bit.

Figure 4. shows an example of waveforms where the amplitudes of the signals input to the resolver are reduced, the calculated value fell outside the threshold range five times, and a sum-of-squares amplitude error is generated.

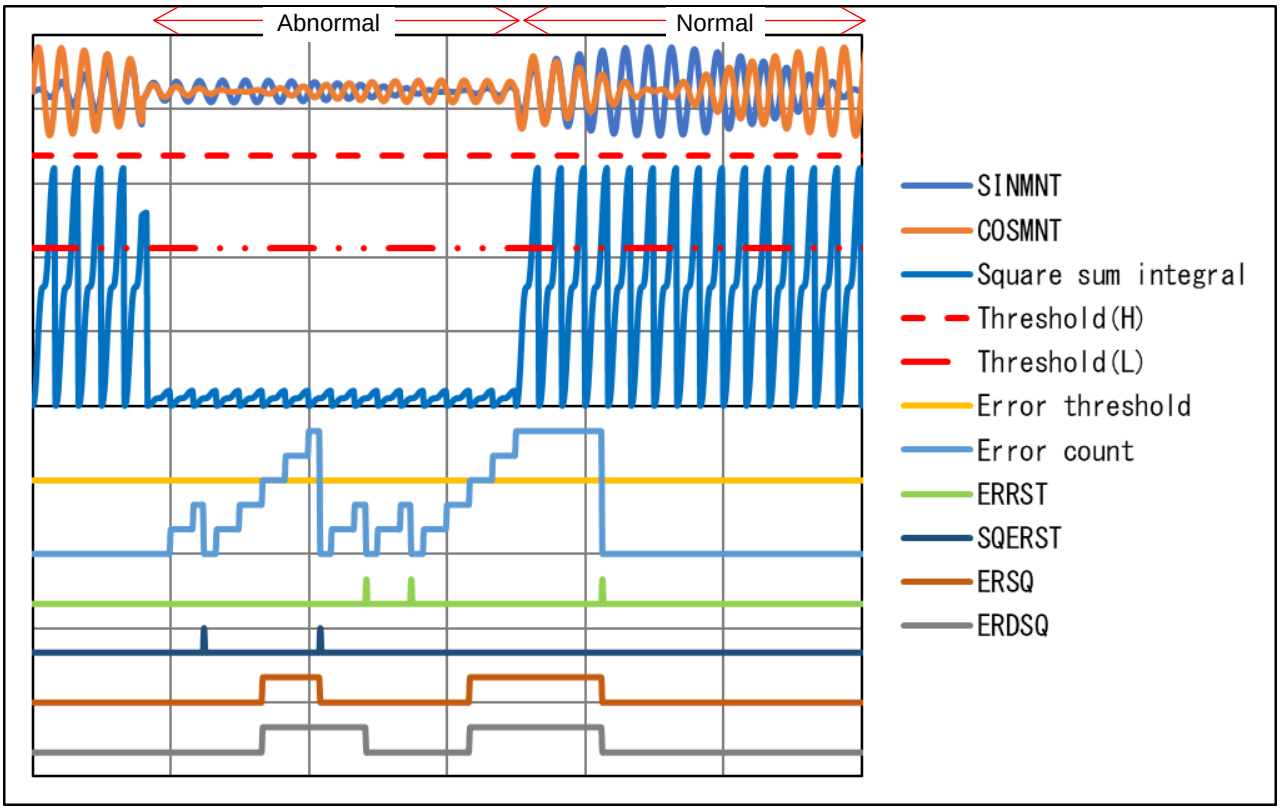


Figure 4.19 Sum-of-Squares Amplitude Error Detection

4.2.5.1 Example of Threshold Determination Method

The table below shows the value of the integrated sum-of-squares amplitude for the ideal waveform. They are different from actual values due to other influences such as noises. Set thresholds by considering these influences.
Calculate values which are not in the following tables by linear interpolation.

Table 49.101 Integrals of the Sums of Squares of SINMNT and COSMNT for One Cycle of Excitation

Excitation frequency (kHz)→	5 kHz	7.5 kHz	10 kHz	12.5 kHz	15 kHz	17.5 kHz	20 kHz
resolver signal amplitude ↓							
0.1 x ADSVREFH-ADSVREFL(Vpp)	243	162	120	95	77	66	56
0.2 x ADSVREFH-ADSVREFL(Vpp)	1023	678	502	395	322	271	231
0.3 x ADSVREFH-ADSVREFL(Vpp)	2279	1514	1118	883	714	607	521
0.4 x ADSVREFH-ADSVREFL(Vpp)	4075	2694	1995	1571	1271	1079	928
0.5 x ADSVREFH-ADSVREFL(Vpp)	6369	4228	3131	2462	1998	1689	1445
0.6 x ADSVREFH-ADSVREFL(Vpp)	9170	6078	4503	0	2873	2428	2083
0.7 x ADSVREFH-ADSVREFL(Vpp)	12499	8286	6111	4823	3914	3309	2849
0.8 x ADSVREFH-ADSVREFL(Vpp)	16352	10817	7994	6316	5117	4327	3715
0.9 x ADSVREFH-ADSVREFL(Vpp)	20667	13697	10121	7979	6469	5477	4697

∗ Table is a transcription of "Table 49.101" in the user's manual.

The example below is a case where the sum-of-squares amplitude error detection is executed under the following conditions.

- Resolver signal amplitude : 2.1Vpp
- Excitation frequency : 10kHz
- The number of conversions in the excitation frequency : SINMNT/COSMNT, 50 times each
- Acceptable error ranges from the ideal waveform : ±0.3Vp-p (1.8 to 2.4Vp-p)

From above conditions, the lower-limit value(1.8Vp-p) and the upper-limit value(2.4Vp-p) used for the sum-of-squares amplitude error detection are not described in above tables. Therefore, find values by linear interpolation between two points close to respective values. In the above example, the lower- and the upper-limit values become as follows.

- Lower-limit value :1644 Upper-limit value :2904

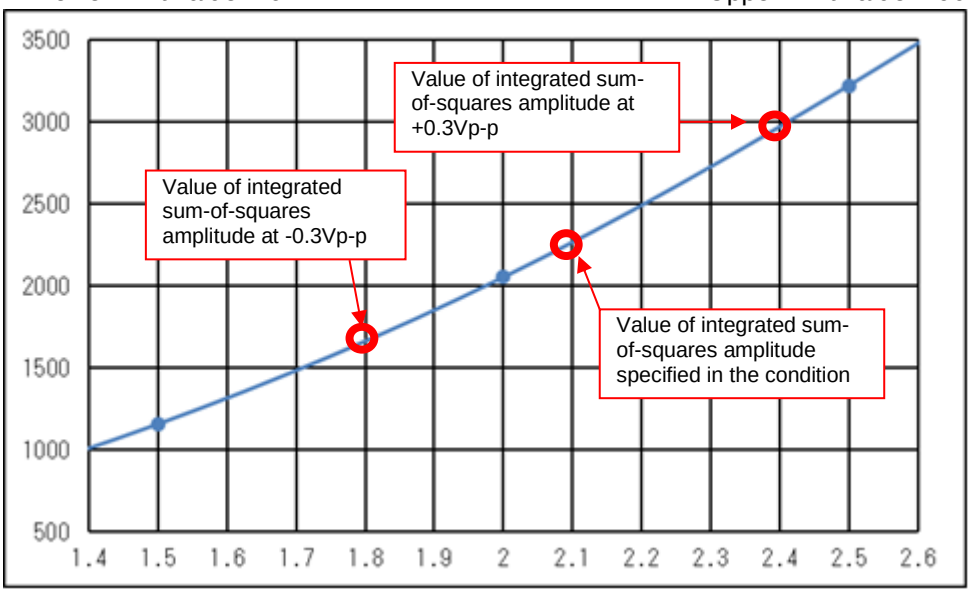


Figure 4.20 Image of Upper- and Lower-Limit Values Used in the Sum-of-Squares Amplitude Error Detection

4.2.5.2 Example of Register Settings

Table 4.5 shows the example of register settings of when the sum-of-squares amplitude error detection function is used.

Table 4.5 Example of Register Settings of When Sum-of-Squares Amplitude Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 1/ RDC3ASDIAG1	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Sum-of-Squares Amplitude Error Excitation Counter Reset / SQERST	1	Writing 1 to this bit resets the sum-of-squares amplitude error excitation counter to 0.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets "the error detection register 1" to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ASnDIAG2	Sum-of-Squares Amplitude Error Select / ERSQS	0	Set the bits ERR, ERHD, ERSQ, and ERDSQ to 1 on occurrence of a sum-of-squares amplitude error
Error detection register 3/ RDC3ASnDIAG3	Sum-of-Squares Amplitude Upper Threshold / SQHTH[15:0]	0x2000	Sets the upper threshold for values of the integrated sum-of-squares amplitude.
	Sum-of-Squares Amplitude Lower Threshold / SQLTH[15:0]	0x0200	Sets the lower threshold for the values of the integrated sum-of-squares amplitude.
Error detection register 4/ RDC3ASnDIAG4	Sum-of-Squares Amplitude Error Excitation Counts Threshold / SQCTH[2:0]	7	Selects the number of excitation periods in which abnormal amplitudes may be generated in the judgment of integrated sum-of-squares amplitude errors. The number of times set in these bits being exceeded is judged to represent an integrated sum-of-squares amplitude error.
Error detection register / RDC3ASnREF	Excitation Extraction Noise Filter /PLSNFS	1	Selects the noise filter for the excitation component extraction circuit. 1: The noise filter is used.

4.2.6 Excitation Period Error Detection

The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable between rise edge or fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in the RDC3ASnETCAP register. By reading the RDC3ASnETCAP register, the cycle of excitation signal can be obtained.

When the IREN bit in the RDC3ASnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request is generated if the value set in the RDC3ASnETCAP register matches the period measurement counter value. The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the RDC3ASnETCAP register. An excitation signal cycle error is detected upon the occurrence of an excitation timer interrupt request.

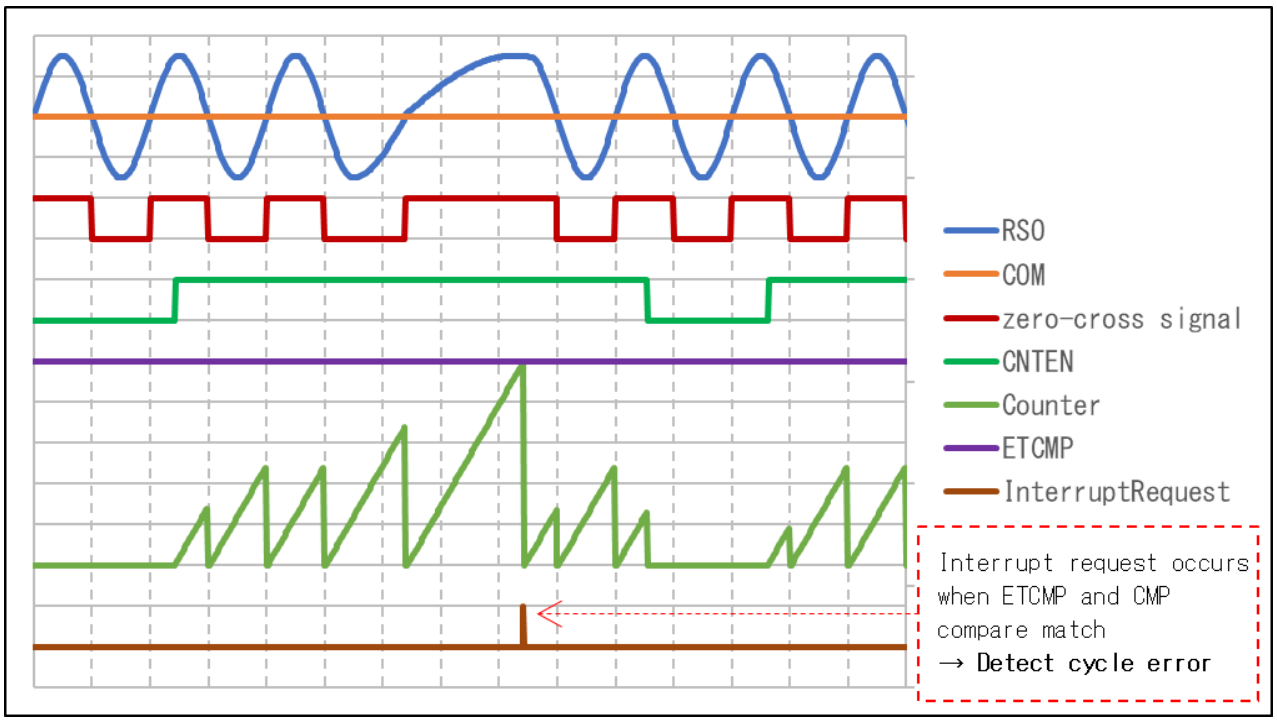


Figure 4.21 Excitation Period Error Detection

4.2.6.1 Example of Register Settings

Table 4.6 shows the example of register settings of when the period measurement timer of excitation signal is used as the excitation period error detection function.

Table 4.6 Example of Register Settings of When Excitation Period Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
ET Control Register / RDC3ASnETEN	Compare Match Function Enable / CMPEN	1	Enables and disables the compare match function. 1: Enables the compare match function.
	Interrupt Request Enable / IREN	1	Enables and disables interrupt requests. 1: Enables the output of interrupt.
	Counter Operation Enable / CNTEN	1	This is the count enable signal for the period measurement timer and the event timer. 1: The period measurement timer and the event timer are operated.
ET Capture Register / RDC3ASnETCAP	ET Compare / CMP[15:0]	0x1F40	Sets count value to generate a compare match. This example setting is the doubled value of the 10kHz excitation signal period (200µsec).

4.3 Notes on Error Detections

4.3.1 Notes on Resolver Signal Disconnection Error Detection

- For the resolver signal disconnection error detection, the level used to compare to the threshold in a VR resolver and a DC resolver are different. The common level of SINMNT/COSMNT is compared with the threshold when operating with a VR resolver, the level of SINMNT/COSMNT itself is compared with threshold when operating with a DC resolver. Thresholds for each resolver is set individually.

4.3.2 Notes on Sum-of-Squares Amplitude Error Detection

- The sum-of-squares amplitude error detection function is only available for resolvers that require the input of signals with excitation components, but not for DC resolvers, which do not require this.

- Setting the ERSQS bit to 0 enables the detection of sum-of-squares amplitude errors. After setting this bit to 0, clear the counted value by setting the SQERST bit to 1.

- In the sum-of-squares amplitude error detection, be sure to set the excitation extraction noise filter bit (PLSNFS) of the excitation setting register (RDC3ASnREF) to 1(The noise filter is used). This setting will prevent from extracting noise as the excitation period when the excitation signal has noise.

4.4 Flowchart of Entire Error Detection Register Settings

The flowchart below shows register settings of this operation example.

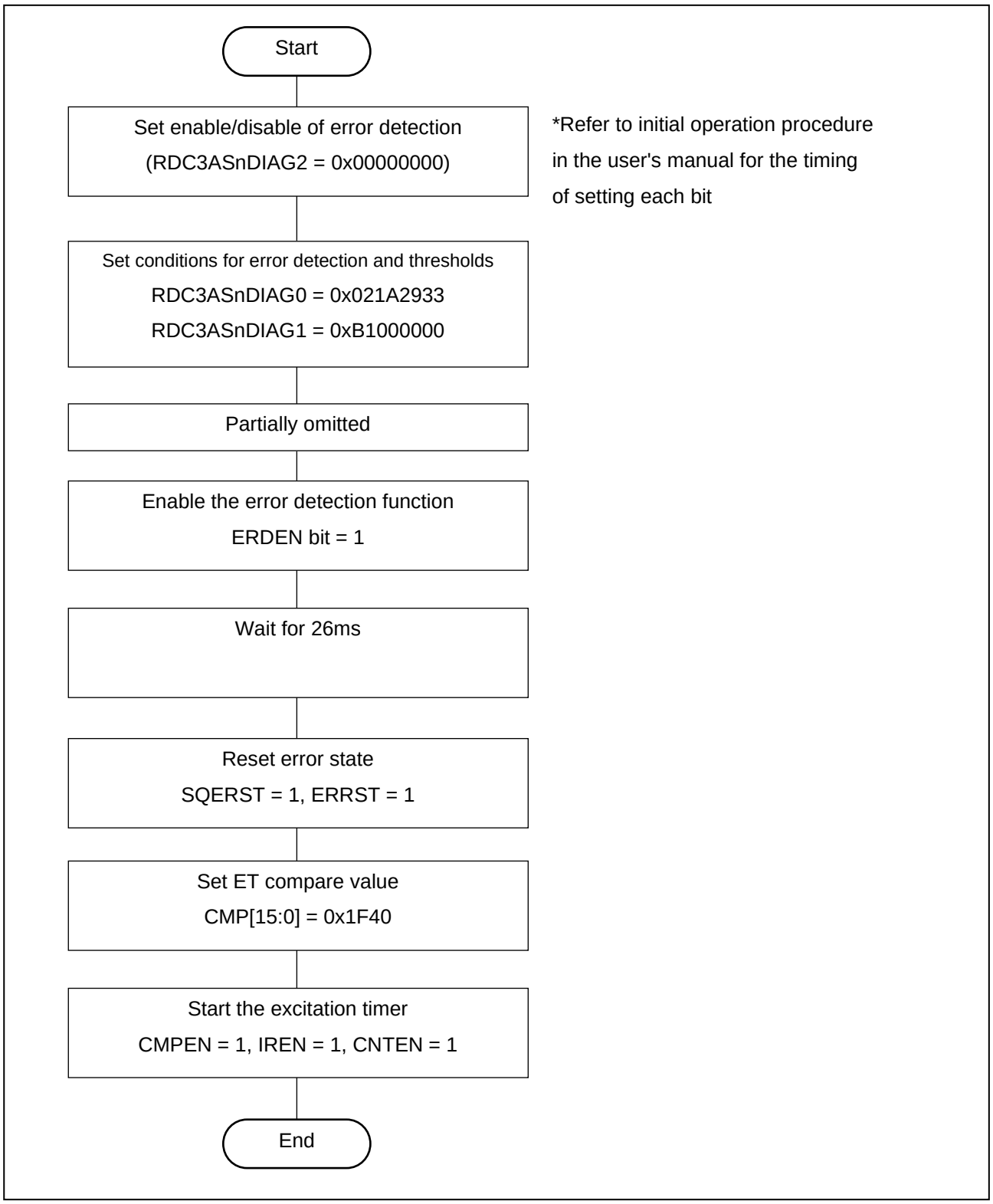


Figure 4.22 Flowchart of Register Settings

5. Self-Diagnosis

5.1 Built-in Self-Test Function (BIST)

RDC3AS has a built-in self-test (BIST) function to check the validity of specified operations.

By setting the BIST command in the RDC3ASnBIST1 register, this function generates the desired signal input that is simulated internally, and monitors the signal output in response.

The test items are shown below.

Table 5.1 BIST function

Items	Diagnosis
Angle Conversion BIST	Self-test of the R/D conversion function The following electrical angles can be set as a resolve signal input: ● Target angle 0° ● Target angle 45° ● Target angle 270°
Error Detection BIST	Self-test for the error detection function ● Resolver signal error detection BIST ● Resolver signal disconnect error detection BIST (sin / cos) ● R/D conversion error detection BIST ● Sum-of-Squares amplitude error detection BIST (high side / low side)

5.2 Details of BIST

5.2.1 Types of BIST

BIST is classified into two types depending on the length of execution time: short-period and long-period.

Long-period BIST can only be executed at power-on. Long-period BIST operates with an internally generated simulated signal for up to 10 ms BIST, so the angle output does not match the resolver input.

Short-period BIST can be performed during angle conversion and maintains angle conversion tracking during BIST execution. Short-period BIST can be performed even when the power is turned on, but long-period BIST should be performed first.

- Short-period BIST: resolver signal error detection BIST, resolver signal disconnect error detection BIST (sin/cos), sum-of-squares amplitude error detection BIST (high side/low side)
- Long-period BIST: angle conversion BIST, conversion error BIST

5.2.2 Execution of BIST

Perform the following settings to execute BIST.

(1) Enable the forced gain control function when executing a BIST. (Set the AGCD bit in the RDC3ALnPI1 register to 0.)

(2) To execute a short-period BIST, set the EINTEN bit to 0 to disable error interrupts.

(3) Set the phase correction bits in the sine and cosine angle correction register to 0° when executing the angle conversion BIST.

Sine phase correction bits SINPO[11:0] = 000H

Cosine phase correction bits COSPO[11:0] = 000H

(4) To execute conversion error BIST, set the EDPS bit to 10B.

(5) Clear the count value in the SQERST bit by setting 1 before running sum-of-squares amplitude detection BIST (high side/low side).

(6) When the BIST is completed,

set the BISTCL bit in the RDC3ALnBIST1 register to 1 to clear the BIST results.

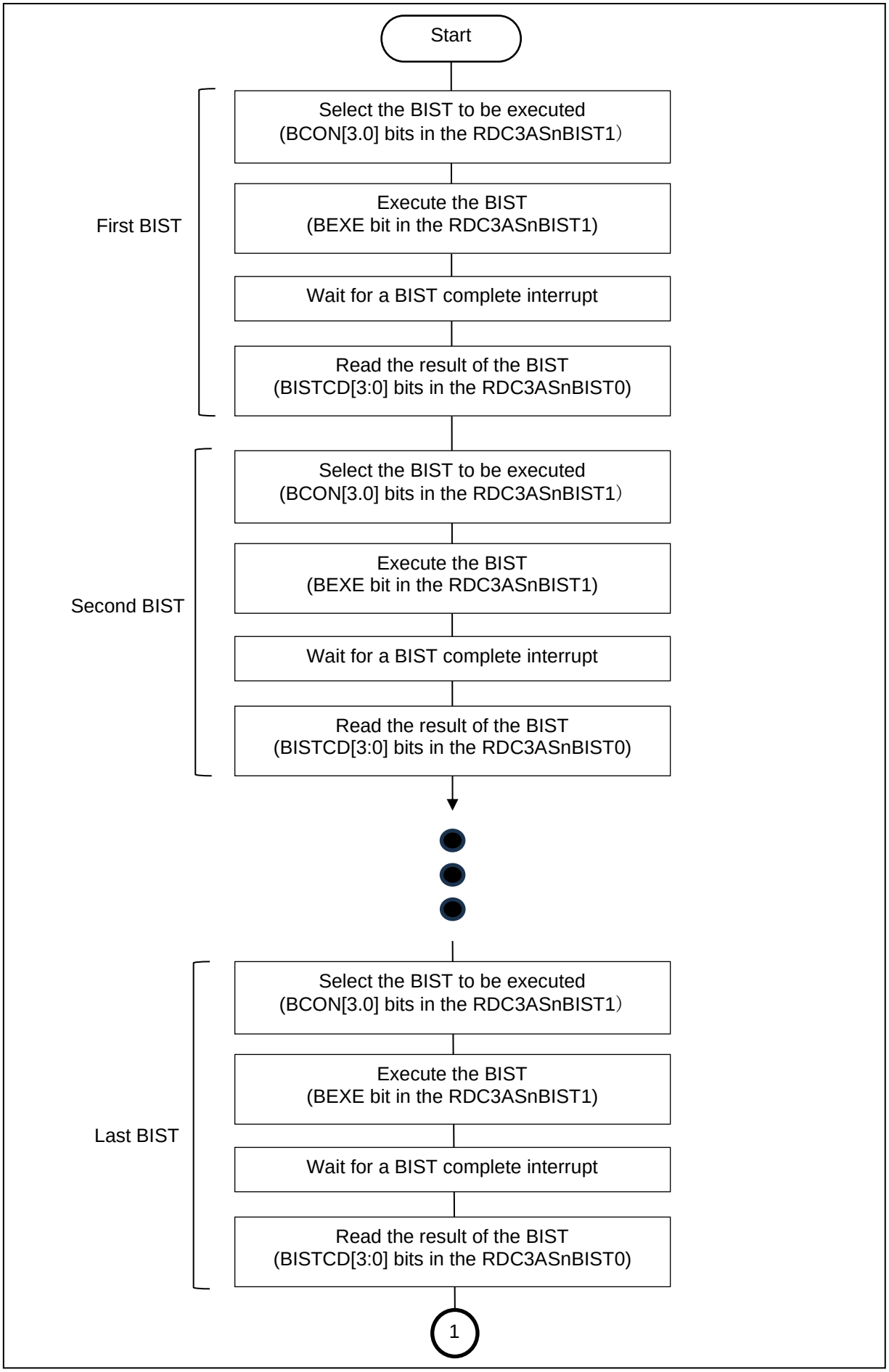
set the ERRST bit in the RDC3ALnDIAG1 register to 1 to reset the error signal.

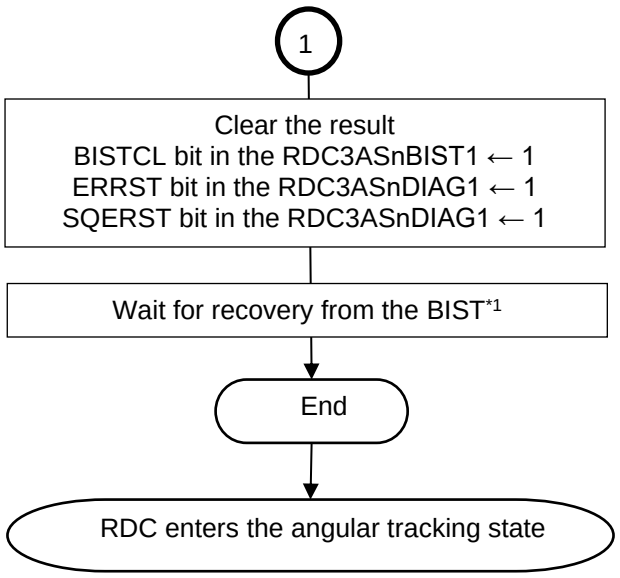
set the SQERST bit in the RDC3ALnDIAG1 register to 1 to reset the counter value of sum-of squares amplitude error.

Return the settings of the registers which were changed in steps (1), (2), (3), and (4) to their original values.

Table 5.2 BISTs for Each Setting of Values

BCON[3:0]	BIST to be Executed
0000	BEXE bit is disabled
0001	This setting is not allowed.
0010	Sum-of-squares amplitude error detection BIST (low side)
0011	Sum-of-squares amplitude error detection BIST (high side)
0100	This setting is not allowed.
0101	Angle conversion BIST (0°)
0110	Angle conversion BIST (45°)
0111	Angle conversion BIST (270°)
1000	This setting is not allowed.
1001	Error detection BIST: resolver signal error detection BIST
1010	Error detection BIST: resolver signal disconnection detection BIST (cosine side)
1011	Error detection BIST: Resolver signal disconnection detection BIST (sine side)
1100	Error detection BIST: conversion error BIST
1101	This setting is not allowed.
1110	This setting is not allowed.
1111	This setting is not allowed.

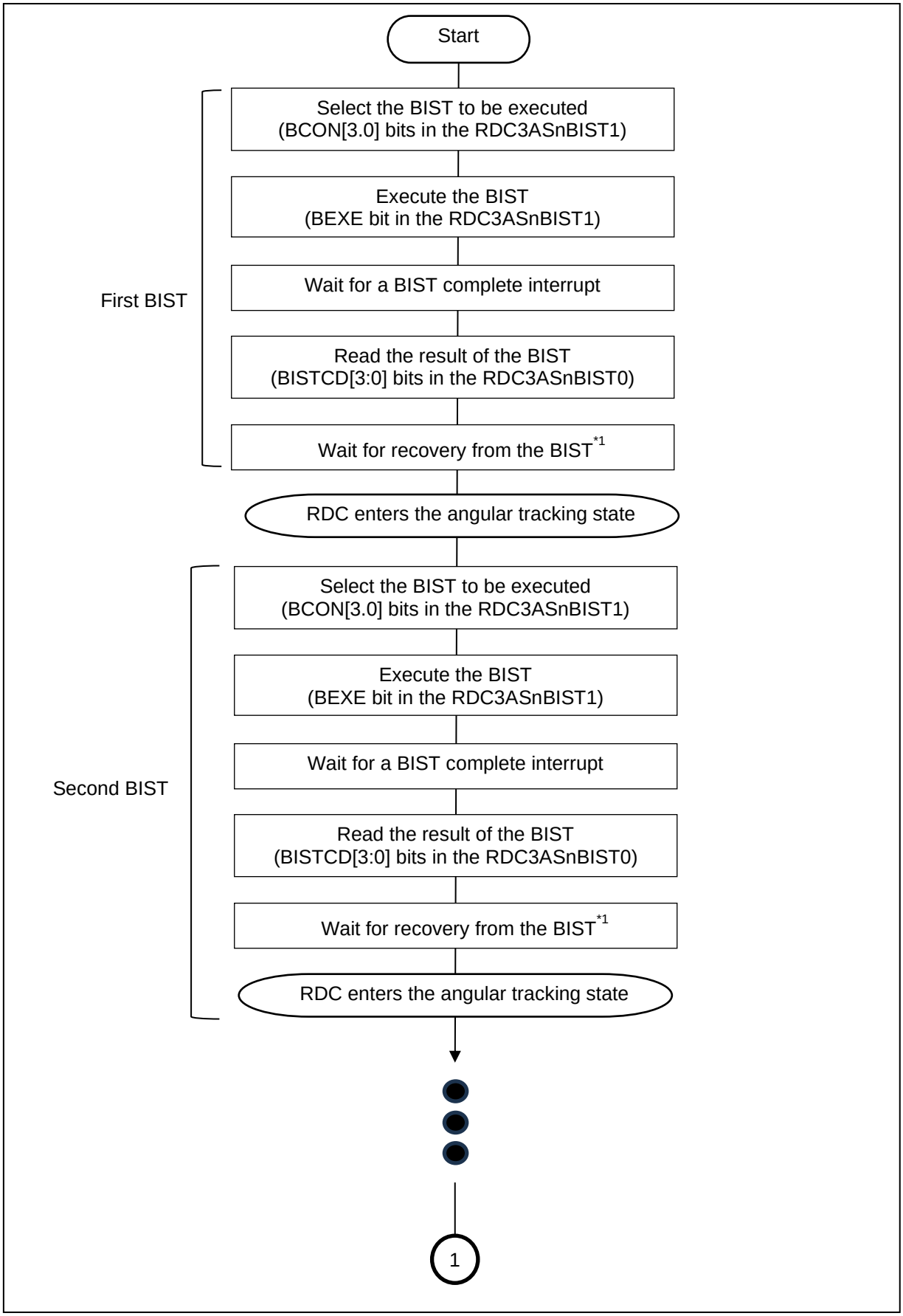

Start
First BIST
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ASnBIST1)
Execute the BIST
(BEXE bit in the RDC3ASnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ASnBIST0)
Second BIST
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ASnBIST1)
Execute the BIST
(BEXE bit in the RDC3ASnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ASnBIST0)
Last BIST
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ASnBIST1)
Execute the BIST
(BEXE bit in the RDC3ASnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ASnBIST0)
1

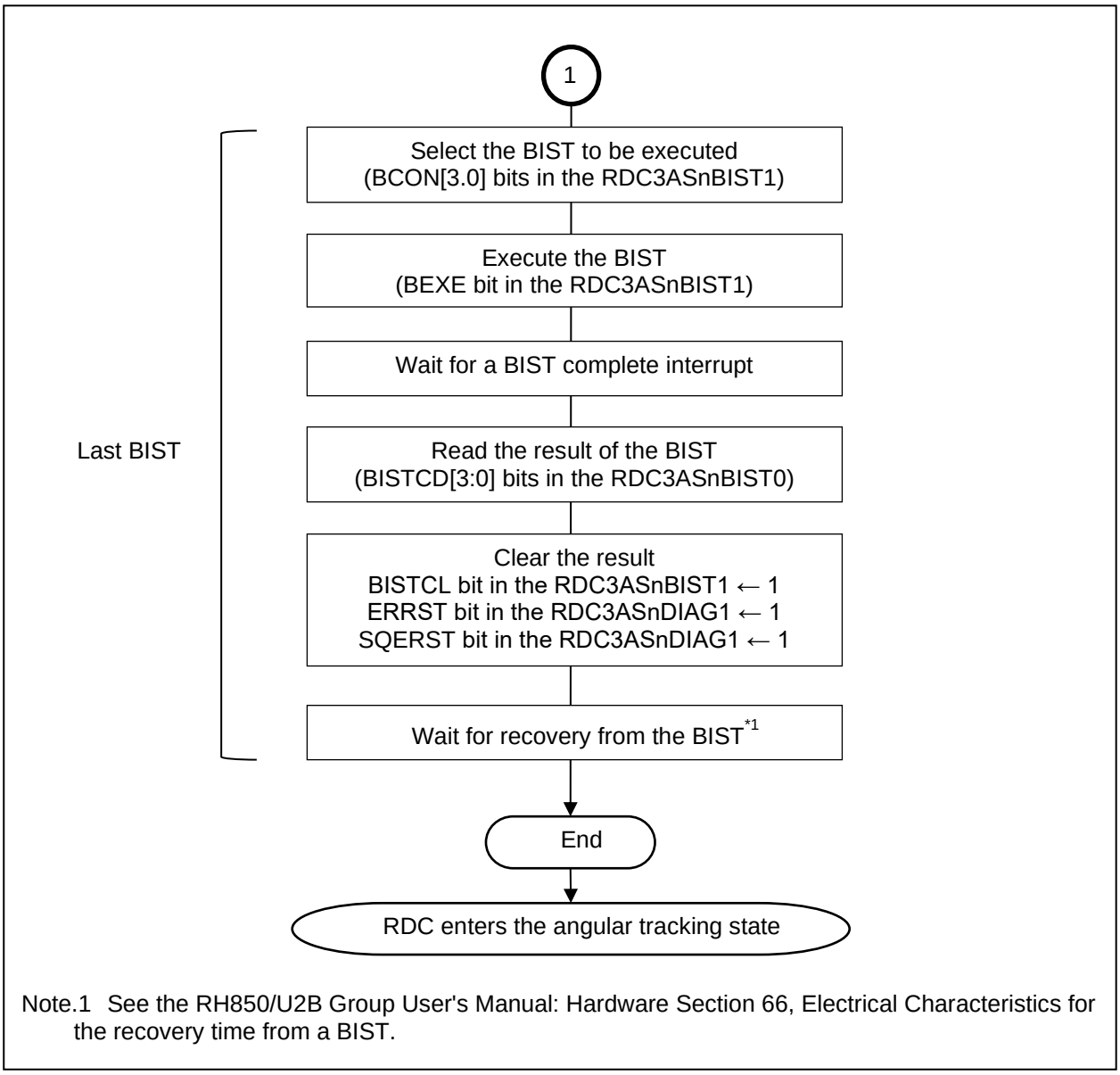


Note.1 See the RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics for the recovery time from a BIST.

Perform all long-period BISTs you want to perform first, and then perform short-period BISTs.

Figure 5.1 Sequence of Executing BISTs after Starting Up the Power


Start
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ASnBIST1)
Execute the BIST
(BEXE bit in the RDC3ASnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ASnBIST0)
Wait for recovery from the BIST*1
First BIST
RDC enters the angular tracking state
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ASnBIST1)
Execute the BIST
(BEXE bit in the RDC3ASnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ASnBIST0)
Wait for recovery from the BIST*1
Second BIST
RDC enters the angular tracking state
1



Note.1 See the RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics for the recovery time from a BIST.

Figure 5.2 Sequence of Executing BISTs during Angle Conversion (Short-period BIST)

5.3 Notes of BIST

- Depending on the BIST, a RDC error interrupt is generated due to the erroneous internal state. If the occurrence of this error disturbs the operation, disable RDC error interrupt by the EINTEN bit.

6. Excitation signal output using GTM

In addition to TPBA, the interrupt signal from GTM (GTM_PSM_IRQ signal) can also be selected as the reference signal for RDC3AS. This section explains how to do this.

This section describes only the changes from "3.How to Use RDC3AS ".

6.1 Operating Specifications and Initial Setting

6.1.1 Operating Specifications

Please refer to "3.1.1 Operating Specifications."

6.1.2 Detail of Sample System Configuration

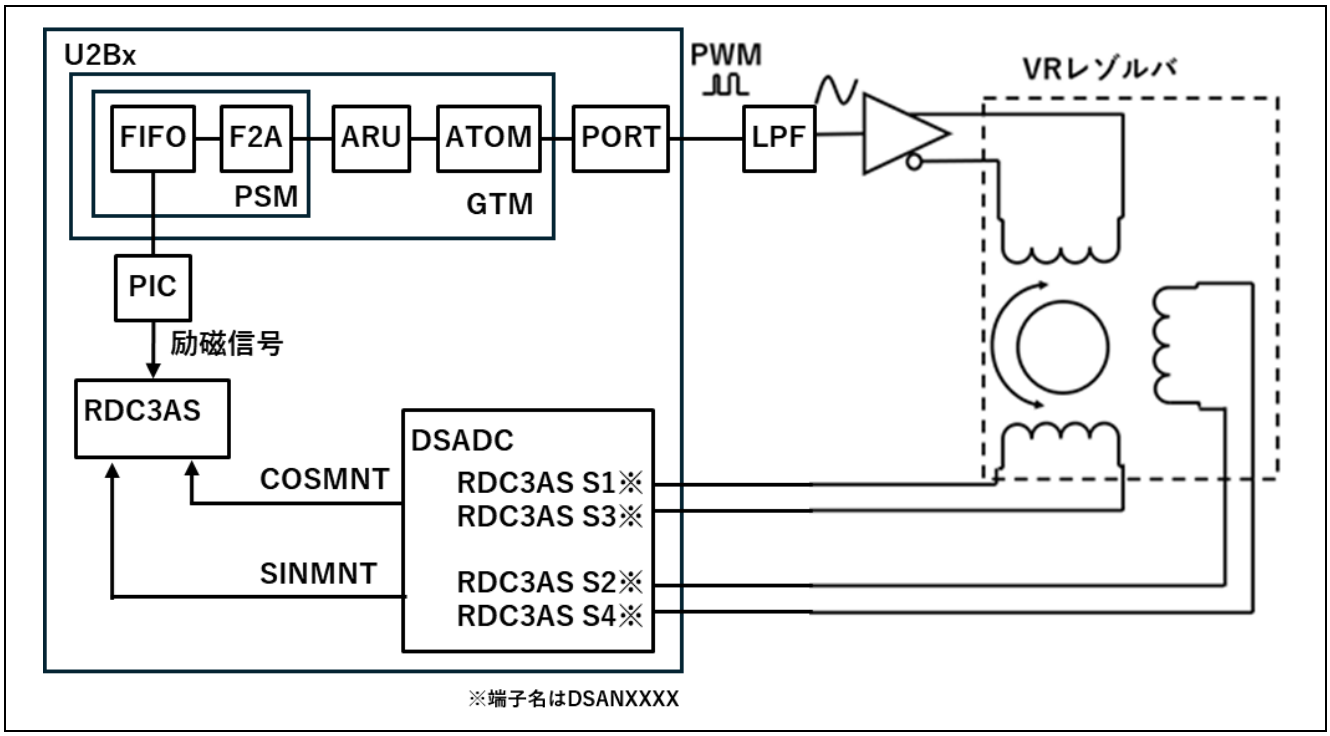


Figure 6.1 System configuration

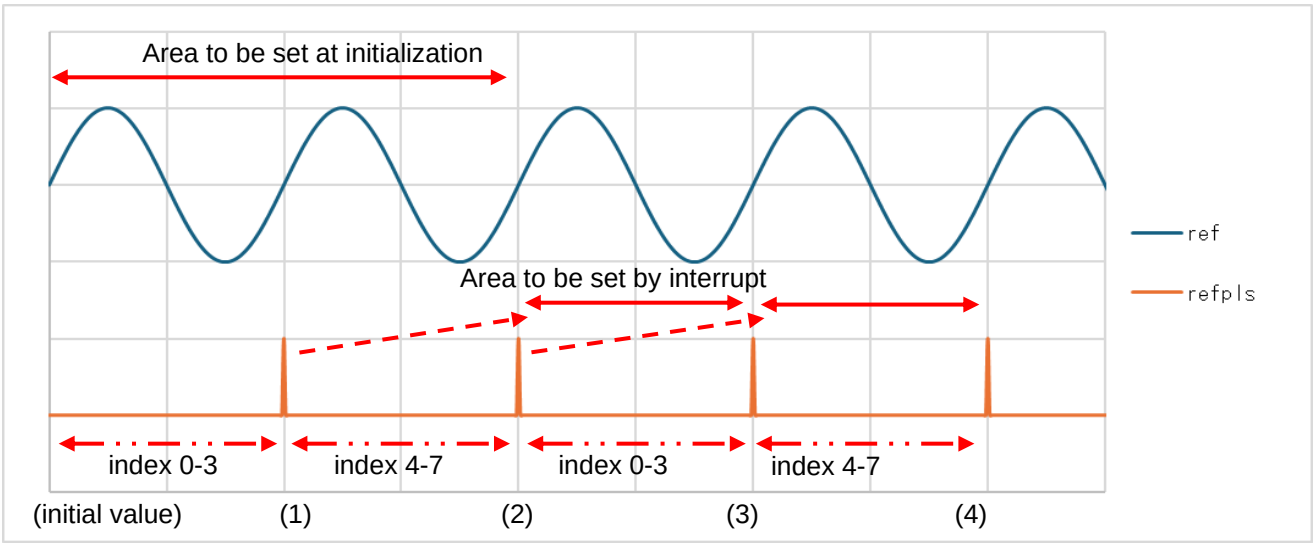
Function of each element (IP)

- RDC3AS, DSADC, PORT
  - Please refer to "3.1.2 Detail of Sample System Configuration".
- GTM
  - The duty value stored in the FIFO is transferred to ATOM via F2A and ARU. ATOM outputs the PWM signal based on the transferred duty value.
  - FIFO outputs an interrupt signal (GTM_PSM_IRQ signal) depending on the number of stored Duty values.
- PIC
  - Connect GTM_PSM_IRQ of GTM to RDC3AS as excitation phase signal.
- PORT
  - Output PWM signal generated by ATOM. The PWM signal will be smoothed by external LPF.

GTM-FIFO Operation

In this operation example, the output setting value is set for two cycles at initialization. Since the GTM_PSM_IRQ signal needs to be output every cycle, a watermark (hereinafter WM) is set at the end of each cycle. The interrupt is processed when the number of FIFO buffers falls below WM. The interrupt process stores the output setting value used in the FIFO buffer.

The interrupt mode is level mode. In other modes, the GTM_PSM_IRQ signal may be output continuously while the interrupt condition is satisfied.



No		initial value	(1)		(2)		(3)		(4)	
			Before interrupt	After interrupt	Before interrupt	After interrupt	Before interrupt	After interrupt	Before interrupt	After interrupt
Buffer index	0	Data0-0	(emptiness)	Data1-0	Data1-0	Data1-0	(emptiness)	Data3-0	Data3-0	Data3-0
	1	Data0-1	(emptiness)	Data1-1	Data1-1	Data1-1	(emptiness)	Data3-1	Data3-1	Data3-1
	2	Data0-2	(emptiness)	Data1-2	Data1-2	Data1-2	(emptiness)	Data3-2	Data3-2	Data3-2
	3	Data0-3	(emptiness)	Data1-3	Data1-3	Data1-3	(emptiness)	Data3-3	Data3-3	Data3-3
	4	Data0-4	Data0-4	Data0-4	(emptiness)	Data2-0	Data2-0	Data2-0	(emptiness)	Data4-0
	5	Data0-5	Data0-5	Data0-5	(emptiness)	Data2-1	Data2-1	Data2-1	(emptiness)	Data4-1
	6	Data0-6	Data0-6	Data0-6	(emptiness)	Data2-2	Data2-2	Data2-2	(emptiness)	Data4-2
	7	Data0-6	Data0-6	Data0-6	(emptiness)	Data2-3	Data2-3	Data2-3	(emptiness)	Data4-3

6.1.3 Explanation of Sample Software

6.1.3.1 Source File/Function List

Source files and functions used in this operation example are listed below.

Table 6.1 Source file/function list

Source file	Function name	Function
main0.c	main0	Start the program and call other functions. After starting the RDC operation, store angular data to RAM in main loop
gtm_ref.c	gtm_ref_main	Initialize the excitation signal by GTM.
	gtm_ref_reset	Resets the status of the GTM resources to be used.
	gtm_ref_psm_init	The output value of the Ref signal is set by PSM initialization.
	gtm_ref_atom_init	Configure the output settings of the Ref signal by ATOM.
	gtm_ref_atom_enable	Start ATOM operation.
	int_gtm_ref_fifo_set	Update the output value of the Ref signal by interrupt.
rdc.c	rdc3as0_init	Please refer to "3.1.3 Explanation of Sample Software".
dsadc.c	dsadc_init	Please refer to "3.1.3 Explanation of Sample Software".
	dsadc_cos_init	Please refer to "3.1.3 Explanation of Sample Software".
	dsadc_sin_init	Please refer to "3.1.3 Explanation of Sample Software".
	dsadc_ref_init	Please refer to "3.1.3 Explanation of Sample Software".
pic.c	pic_init	Setting to connect GTM_PSM_IRQ of GTM to RDC3AS0
port.c	port_init	Setting for terminal pins.

6.1.3.2 Detail of Functions

(1) main0

This is main function of the program.

After performing the following processing, an infinity loop is executed.

In the loop, angle values are obtained and stored to the RAM.

- Call the function for PORT initialization.
- Call the function for PIC initialization.
- Call the function for GTM initialization and operation start.
- Call the function for DSADC initialization and wait for the excitation signal stability.
- Call the function for RDC3AS0 initialization.

(2) gtm_ref_main

Initialize the excitation signal by GTM.

- Set the number of ARU routes to 125 (0-124).
- Call the function for gtm_ref_reset.
- Call the function for gtm_ref_psm_init.
- Call the function for gtm_ref_atom_init

Table 6.2 gtm_ref_main register settings

Register Name/Symbol	Set Value	Description
GTM0.GTM_CTRL	& 0xFFFFFFFE	RF_PROT = 0
GTM0.ARU_CADDR_END	124	Set the number of ARU routes to 125 (0-124).

(3) gtm_ref_reset

Initialize the excitation signal by GTM.

- Allow GTM_PSM_IRQ output
- Enable CMU
- Stop ATOM operation
- Disable ATOM interrupts
- Clear ATOM interrupt flag

Table 6.3 gtm_ref_reset register settings

Register Name/Symbol	Set Value	Description
GTM0_1.IRQ_SEL100	0x00000000	Disable output of ATOM interrupt signals outside GTM
GTM0_1.IRQ_SEL800	0x000000FF	Allow output of GTM_PSM_IRQ interrupt signals outside GTM
GTM0.GTM_CLS_CLK_CFG	0x000000AA	Set the frequency to 1/2 of the GTM supply clock
GTM0.CMU_CLK_EN	0x000000AA	Allow CMU operation
GTM0.CMU_GCLK_NUM	0x00000001	CMU clock division (numerator)
GTM0.CMU_GCLK_DEN	0x00000001	CMU clock division (denominator)
GTM0.ATOM0_AGC_OUTEN_CTRL	0x00000400	Disable CH5 output
GTM0.ATOM0_AGC_OUTEN_STAT	0x00000400	Clear CH5 output status
GTM0.ATOM0_AGC_ENDIS_CTRL	0x00000400	Disable CH5 operation
GTM0.ATOM0_AGC_ENDIS_STAT	0x00000400	clear CH5 operation status
GTM0.ATOM0_CH5_IRQ_EN	0x00000000	Disable CH5 interrupt
GTM0.ATOM0_CH5_IRQ_NOTIFY	0x00000003	Clear CH5 interrupt status

(4) gtm_ref_psm_init

The output value of the Ref signal is set by PSM initialization.

- FIFO settings (start address, end address, WM settings)
- F2A settings (FIFO to ARU)
- Store FIFO setting value via AFD (store setting value in sin_tbl_ref array)
- Clear FIFO interrupt status
- Enable F2A

Table 6.4 gtm_ref_psm_init register settings

Register Name/Symbol	Set Value	Description
GTM0.FIFO0_CH0_START_ADDR	0x00000000	FIFO start address
GTM0.FIFO0_CH0_END_ADDR	0x000000FF	FIFO end address
GTM0.FIFO0_CH0_LOWER_WM	0x00000080	WM that generates an interrupt when it falls below
GTM0.FIFO0_CH0_UPPER_WM	0x000000AA	WM that generates an interrupt when it exceeds
GTM0.FIFO0_CH0_FILL_LEVEL	0x00000040	WM overflow detection setting
GTM0.FIFO0_CH0_IRQ_MODE	0x00000000	Level mode setting
GTM0.FIFO0_CH0_IRQ_EN	0x00000004	Only Lower_WM interrupt is enabled
GTM0.FIFO0_CH0_CTRL	0x00000001	Normal mode
GTM0.F2A0_ENABLE	0x00000002	F2A enable
GTM0.F2A0_CH0_ARU_RD_FIFO	0x000001FE	Set the ARU routing address to ARU_EMPTY_ADDR.
GTM0.F2A0_CH0_STR_CFG	0x00060000	Set transfer direction from FIFO to ARU
GTM0.AFD0_CH0_BUF_ACC	output value	Output value to be transferred to ATOM (sin_tbl_ref)
GTM0.FIFO0_CH0_IRQ_NOTIFY	0x0000000F	Clear FIFO interrupt status

The contents of the sin_tbl_ref array are as follows:

Table 6.5 sin_tbl_ref setting value

index	value	index	value	index	value	index	value
0	0.00000000	16	1.00000000	32	0.00000000	48	-1.00000000
1	0.09801714	17	0.99518473	33	-0.09801714	49	-0.99518473
2	0.19509032	18	0.98078528	34	-0.19509032	50	-0.98078528
3	0.29028468	19	0.95694034	35	-0.29028468	51	-0.95694034
4	0.38268343	20	0.92387953	36	-0.38268343	52	-0.92387953
5	0.47139674	21	0.88192126	37	-0.47139674	53	-0.88192126
6	0.55557023	22	0.83146961	38	-0.55557023	54	-0.83146961
7	0.63439328	23	0.77301045	39	-0.63439328	55	-0.77301045
8	0.70710678	24	0.70710678	40	-0.70710678	56	-0.70710678
9	0.77301045	25	0.63439328	41	-0.77301045	57	-0.63439328
10	0.83146961	26	0.55557023	42	-0.83146961	58	-0.55557023
11	0.88192126	27	0.47139674	43	-0.88192126	59	-0.47139674
12	0.92387953	28	0.38268343	44	-0.92387953	60	-0.38268343
13	0.95694034	29	0.29028468	45	-0.95694034	61	-0.29028468
14	0.98078528	30	0.19509032	46	-0.98078528	62	-0.19509032
15	0.99518473	31	0.09801714	47	-0.99518473	63	-0.09801714

(5) gtm_ref_atom_init

Configure the output settings of the Ref signal by ATOM.

- AGC settings
- ATOM CH5 settings
- Initial compare value settings

Table 6.6 gtm_ref_atom_init register settings

Register Name/Symbol	Set Value	Description
GTM0.ATOM0_AGC_OUTEN_CTRL	0x00000800	Enable CH5 output
GTM0.ATOM0_AGC_OUTEN_STAT	0x00000800	Set CH5 output status
GTM0.ATOM0_AGC_FUPD_CTRL	0x00000400	Disable force update
GTM0.ATOM0_AGC_INT_TRIG	0x00000400	Disable interrupt triggers
GTM0.ATOM0_CH5_CTRL	0x0000080A	SOMP mode, Using ARU
GTM0.ATOM0_CH5_RDADDR	0x01FE0001	Configure ARU transfer from F2A0
GTM0.ATOM0_CH5_CN0	0x00000000	Counter initial value
GTM0.ATOM0_CH5_CM0	0x00000002	Cycle initial value
GTM0.ATOM0_CH5_CM1	0x00000000	Duty initial value
GTM0.ATOM0_CH5_SR0	0x00000002	Reload cycle initial value
GTM0.ATOM0_CH5_SR1	0x00060000	Reload duty initial value
GTM0.ATOM0_CH5_IRQ_EN	0x00000000	Disable interrupt
GTM0.ATOM0_AGC_GLB_CTRL	0x08000000	Enable reload

(6) gtm_ref_atom_enable

Start ATOM operation.

Table 6.7 gtm_ref_atom_enable register settings

Register Name/Symbol	Set Value	Description
GTM0.ATOM0_AGC_ENDIS_CTRL	0x00000800	Enable CH5 operation
GTM0.ATOM0_AGC_ENDIS_STAT	0x00000800	Enable CH5 operation status

(7) int_gtm_ref_fifo_set

Interrupt processing. The output value of the Ref signal is updated by the interrupt.

- Store FIFO setting value via AFD (store setting value in sin_tbl_ref array)
- Clear FIFO interrupt status

Table 6.8 int_gtm_ref_fifo_set register settings

Register Name/Symbol	Set Value	Description
GTM0.AFD0_CH0_BUF_ACC	output value	Output value to be transferred to ATOM (sin_tbl_ref)
GTM0.FIFO0_CH0_IRQ_NOTIFY	0x0000000F	Clear FIFO interrupt status

(8) pic_init

Setting to connect GTM_PSM_IRQ of GTM to RDC3AS0

Table 6.9 pic_init register settings

Register Name/Symbol	Set Value	Description
PIC24.PIC2RDCEISEN0	0x00000003	Input GTM_PSM_IRQ to RDC3AS0

(9) port_init

Setting for terminal pins.

Table 6.10 port_init register settings

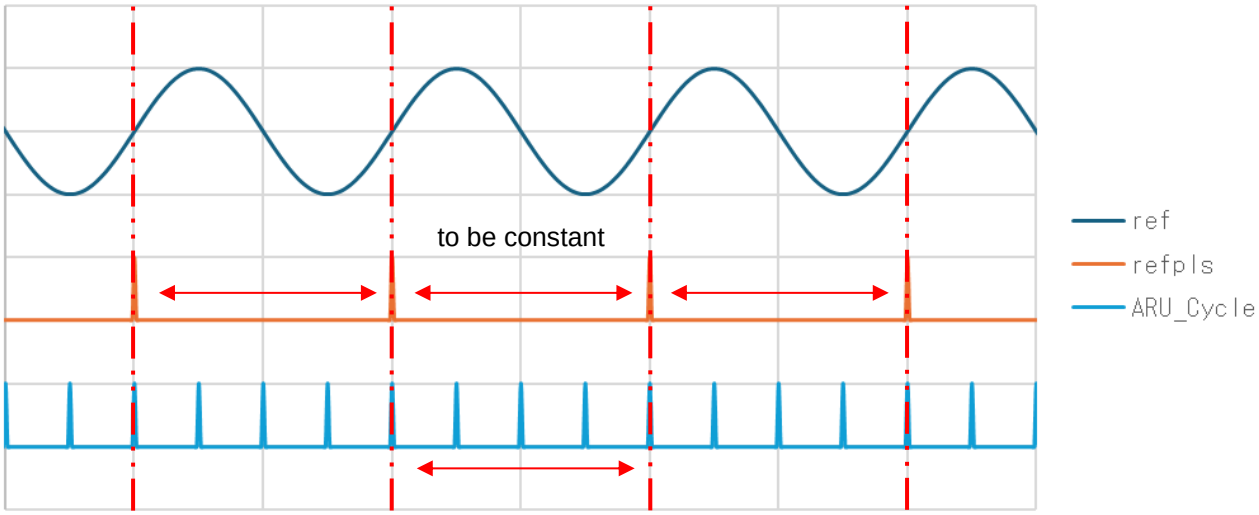
Register Name/Symbol	Set Value	Description
PORT0.PCR00_5	0x0000006D	Configure to ATOM0_5

6.2 Notes on excitation signals using GTM

When using GTM as an excitation signal, the following points should be noted:

- When using GTM_PSM_IRQ as a reference signal for RDC3AS, the excitation signal period must be integral multiple of the ARU round trip time.
- The GTM_PSM_IRQ signal generation period must be constant.

Otherwise, the generation timing of the GTM_PSM_IRQ signal is unstable. RDC3AS conversion may become uncontrollable.



Adjust ARU_Cycle and refpls to be integer multiples.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.03.31	-	First edition
2.00	2023.06.13	21 25	Correction for internal circuit added Smoothing for PWM generated with TPBA added
3.00	2023.09.29	48-	Add “5. Self-Diagnosis”
4.00	2024.07.11	54	Add “6. Excitation signal output using GTM”

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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