Summary

This application note explains the procedure example when performing CAN gateway mode in the RH850/U2A series of automotive single-chip microcontrollers from Renesas Electronics (hereafter referred to as U2A).

These documents and programs are intended to understand the RH850/U2A built-in function, and are not intended for mass production design.

Aim of this document and software is to provide supplemental information for the function on RH850/U2A. It is not intended to implement in the design for mass production.

There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2A-EVA Group

Target Integrated Development Environment

CS+ (from Renesas Electronics)

Version: V8.07.00

Device file: DR7F702300.DVF

:DR7F702301.DVF

:DR7F702302.DVF

Reference Document


For function details and electrical characteristics, please refer to “User’s Manual: Hardware”.

This application note is based on the following manual.

- RH850/U2A-EVA User’s Manual (Rev.1.20): R01UH0864EJ0120

The register name in this text omits “RSCFDnCFD”.
Contents

1. Gateway Function .................................................................................................................................................. 3

2. Gateway Operation ................................................................................................................................................. 4
   2.1 Gateway in Transmit/Receive FIFO Buffer ..................................................................................................... 5
      2.1.1 Gateway Procedure in Transmit/Receive FIFO Buffer ............................................................................ 5
      2.1.2 Transmission Abort Function .................................................................................................................. 7
      2.1.3 Interval Transmission Function .............................................................................................................. 8
      2.1.4 Transmit/Receive FIFO Buffer Interrupt Processing (Gateway Mode) ...................................................... 10
      2.2 Gateway Function by Transmit Queue ........................................................................................................... 13
      2.2.1 Gateway Procedure in Transmit Queue ................................................................................................... 13
      2.2.2 Transmission Abort Function ................................................................................................................ 15
      2.2.3 Transmit Queue Interrupt Processing (Gateway Mode) ............................................................................ 16

3. CAN-CAN FD Gateway (Only in CAN FD Mode) ................................................................................................. 18

4. CAN-related Interrupt Processing ....................................................................................................................... 19

5. Notes on Processing Flow .................................................................................................................................... 19
   5.1 Functions ........................................................................................................................................................ 19
   5.2 Setting for Each Channel, FIFO, and Buffer ................................................................................................. 19
   5.3 Infinite Loop ............................................................................................................................................... 19

6. Appendix .......................................................................................................................................................... 20
   6.1 Software Explanation ................................................................................................................................. 20
1. Gateway Function

The functions available when performing the CAN gateway are listed below. Refer to the next chapters for each processing details.

2.1 Gateway in Transmit/Receive FIFO Buffer
2.2 Gateway Function by Transmit Queue
2. Gateway Operation

Setting the transmit/receive FIFO buffer or transmit queue to gateway mode allows receive messages to be transmitted from any channel without CPU intervention.

Figure 2-1 shows the operation example in the gateway mode (transmit/receive FIFO buffer).
2.1 Gateway in Transmit/Receive FIFO Buffer

When a transmit/receive FIFO buffer with CFM[1:0] bits in the CFCCk register set to "10" (gateway mode) is selected with the GAFLP1j register, messages that passed through the filter processing of the receive rule are stored in the specified transmit/receive FIFO buffer and are automatically transmitted from the buffer.

In the transmit/receive FIFO buffer, messages are sent in order from the first stored message. The priority determination is performed only for the next message to be sent in the transmit/receive FIFO buffer.

In gateway mode, read and write operations are not available for the transmit/receive FIFO buffer, but the messages transmitted from the transmit/receive FIFO buffer in the gateway mode can be checked by using the mirror function.

In gateway mode, the user can choose whether to capture or discard the latest received frame while the transmit/receive FIFO is full.

Refer to "CAN Configuration Application Note", for the configuration settings for using the transmit/receive FIFO buffer in gateway mode.

2.1.1 Gateway Procedure in Transmit/Receive FIFO Buffer

In gateway mode, the messages are transmitted and received automatically within the RS-CANFD module, thus the transmission/reception processing is not required by the program.

Figure 2-2 and Figure 2-3 show the procedure for enabling and disabling the use of transmit/receive FIFO buffers.

![Gateway Procedure Diagram]

Note 1. In transmit mode or gateway mode, rewrite the transmit/receive FIFO buffer usage enable settings in channel communication mode or channel standby mode.

Note 2. Enable the transmit/receive FIFO buffer usage after performing the configuration setting for using the transmit/receive FIFO buffer.

Figure 2-2 Procedure for Enabling Transmit/Receive FIFO Buffer Usage
Note 1. In transmit mode or gateway mode, rewrite the transmit/receive FIFO buffer usage disable settings in channel communication mode or channel standby mode.

Note 2. When the transmit/receive FIFO buffer is disabled, the transmit/receive FIFO buffer empty status is flagged at the following timings.
   - The transmit/receive FIFO buffer becomes empty immediately when the message in it is not being transmitted or is not to be transmitted next.
   - The transmit/receive FIFO buffer becomes empty after transmission completion, CAN bus error detection, or arbitration lost when the message in it is being transmitted or to be transmitted next.

Note 3. Even if the transmit/receive FIFO buffer usage is disabled with the transmit/receive FIFO interrupt request present (CFSTSk.CFTXIF = 1 or CFSTSk.CFRXIF = 1), the transmit/receive FIFO interrupt request is not automatically canceled (CFSTSk.CFTXIF = 0 or CFSTSk.CFRXIF = 0). When canceling the transmit/receive FIFO interrupt request, set it by the program.

Figure 2-3 Procedure for Disabling Transmit/Receive FIFO Buffer Usage
2.1.2 Transmission Abort Function

By disabling the transmit/receive FIFO buffer usage setting (CFCCk.CFE = 0), all messages in the transmit/receive FIFO buffer are lost, and the transmit/receive FIFO buffer empty status flag in the transmit/receive FIFO buffer status register is set to "1" (CFSTSk.CFEMP = 1). The transmit/receive FIFO buffer empty status flag becomes "1" at the timing below. Messages are not stored in the transmit/receive FIFO buffer while the transmit/receive FIFO buffer usage is disabled.

- The transmit/receive FIFO buffer becomes empty immediately when the message in it is not being transmitted or is not to be transmitted next.
- The transmit/receive FIFO buffer becomes empty after transmission completion, CAN bus error detection, or arbitration lost when the message in it is being transmitted or to be transmitted next.

The interrupt is not generated by the transmission abort completion of the transmit/receive FIFO buffer. However, aborting during transmission may cause a CANm transmit/receive FIFO transmission completion interrupt due to completion of transmission. Refer to "CAN Transmission Procedure Application Note" for the details.

Refer to “Figure 2-3 Procedure for Disabling Transmit/Receive FIFO Buffer Usage” for the transmission abort procedure of the transmit/receive FIFO buffer.
2.1.3 Interval Transmission Function

When using the transmit/receive FIFO buffer set to the transmit mode or the gateway mode and continuously transmitting messages from the same transmit/receive FIFO buffer, the interval time between the message transmissions can be set.

After the transmit/receive FIFO buffer is enabled (CFCCk.CFE = 1) and the first message is successfully sent from the transmit/receive FIFO buffer, the interval timer starts counting (after the 7th bits of the CAN protocol EOF). After that, when the interval time elapses, the next message is sent and the interval timer is reset. The timing at which the interval timer stops is shown below.

• When disabled the transmit/receive FIFO buffer usage (CFCCk.CFE = 0)
• When transitioned to the channel reset mode

Table 2-1 shows the count source of the interval timer and the calculation formula of the interval time, Figure 2-4 shows the block diagram of the interval timer, and Figure 2-5 shows the operation example of the interval timer.

<table>
<thead>
<tr>
<th>CFCCk CFITR</th>
<th>CFITSS</th>
<th>Count Source</th>
<th>Interval Time Formula*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Clock obtained by dividing pclk/2 by the value of ITRCP[15:0] bits in the GCFG register</td>
<td>1/f_PBA × 2 × M × N</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Clock obtained by dividing pclk/2 by 10 times the value of ITRCP[15:0] bits in the GCFG register</td>
<td>1/f_PBA × 2 × M × 10 × N</td>
</tr>
<tr>
<td>-</td>
<td>1</td>
<td>Nominal CANm bit time clock</td>
<td>1/f_CANBIT × N</td>
</tr>
</tbody>
</table>

Note) M: Clock source division value of the interval timer for FIFO (Set value of GCFG.ITRCP [15:0])
N: Message transmission interval (Set value of CFCCk.CFITT [7:0])
f_PBA: pclk frequency
f_CANBIT: Frequency of nominal CANm bit time clock
Figure 2-4 Block Diagram of Interval Timer

Figure 2-5 Operation Example of Interval Transmission (Gateway Mode)

Note 1. Since the prescaler is not initialized when the transmission is completed, the first interval time will have an error of up to 1 count of the interval timer.

Note 2. When the transmit/receive FIFO buffer is determined to be the next transmission in the priority determination, the transmission starts. From the time the transmission request is issued until the transmission starts, the transmission usually starts with a delay of 3 clocks or less of the CANm bit time. A longer delay may occur due to multiple internal processes such as receive filter processing, message routing, and transmission priority determination.
2.1.4 Transmit/Receive FIFO Buffer Interrupt Processing (Gateway Mode)

(a) Transmit/Receive FIFO Buffer Reception Interrupt Processing

If the transmit/receive FIFO reception interrupt is enabled, the transmit/receive FIFO reception interrupt is generated when the condition selected by the CFIM bit of the CFCCk register is satisfied.\(^1\)

The transmit/receive FIFO reception interrupt can be enabled or disabled for each transmit/receive FIFO buffer by the CFRXIE bit of the CFCCk register.

The condition for generating a transmit/receive FIFO reception interrupt is selectable for each transmit/receive FIFO buffer by the CFIM bit and CFIGCV bit of the CFCCk register.

Table 2-2 summaries the transmit/receive FIFO reception interrupt source in the gateway mode.

<table>
<thead>
<tr>
<th>CFCCk</th>
<th>CFIGCV</th>
<th>Generation Condition of FIFO Reception Interrupt Request</th>
<th>How to clear the interrupt request</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-</td>
<td>Every one message is received</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>000*</td>
<td>When the message is stored up to 1/8 in the FIFO buffer</td>
<td>Write &quot;0&quot; to the CFRXIF bit of the CFSTSk register</td>
</tr>
<tr>
<td></td>
<td>001</td>
<td>When the message is stored up to 2/8 in the FIFO buffer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>010*</td>
<td>When the message is stored up to 3/8 in the FIFO buffer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>011</td>
<td>When the message is stored up to 4/8 in the FIFO buffer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>100*</td>
<td>When the message is stored up to 5/8 in the FIFO buffer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>101</td>
<td>When the message is stored up to 6/8 in the FIFO buffer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>110*</td>
<td>When the message is stored up to 7/8 in the FIFO buffer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>111</td>
<td>When the FIFO buffer is full</td>
<td></td>
</tr>
</tbody>
</table>

* Setting is prohibited when the number of buffers in the transmit/receive FIFO buffer is set to 4 messages (CFCCk.CFDC[2:0] = 001).

(b) Transmit/Receive FIFO Buffer Full Interrupt

If the transmit/receive FIFO buffer full interrupt is enabled, the transmit/receive FIFO buffer full interrupt is generated when the transmit/receive FIFO buffer becomes full.\(^2\)

The transmit/receive FIFO buffer full interrupt can be enabled or disabled for each transmit/receive FIFO buffer by the CFFIE bit in the CFCCEx register.

The transmit/receive FIFO buffer full interrupt is expected to be used in the following cases.
1. Interrupt request at the number of stages set by the CFIGCV bit in the transmit/receive FIFO buffer
2. Interrupt request with the transmit/receive FIFO buffer full status

These interrupt requests make facilitate data management in the transmit/receive FIFO.

---

\(^1\) Even if the transmit/receive FIFO buffer usage is disabled while the transmit/receive FIFO interrupt request is generated, the transmit/receive FIFO interrupt request is not automatically canceled. When canceling the receive/transmit FIFO interrupt request, set it by the program.
(c) Transmit/Receive FIFO One-frame Reception Completion Interrupt

If enabled the transmit/receive FIFO one-frame reception interrupt, the transmit/receive FIFO one-frame reception interrupt is generated when the transmit/receive FIFO buffer receives one frame.\(^1\)

Transmit/receive FIFO one-frame reception interrupt can be enabled or disabled for each transmit/receive FIFO buffer by the CFOFRXIE bit in the CFCCEk register.

(d) Transmit/Receive FIFO Transmission Interrupt Processing

If the transmit/receive FIFO transmission interrupt is enabled, the transmit/receive FIFO transmission interrupt is generated when the condition selected by the CFIM bit of the CFCCk register is satisfied.\(^1\)

Transmit/receive FIFO transmission interrupt can be enabled or disabled for each transmit/receive FIFO buffer by the CFTXIE bit in the CFCCk register.

The condition for generating a transmit/receive FIFO transmission interrupt can be selected for each transmit/receive FIFO buffer by the CFIM bit of the CFCCk register.

Table 2-3 summarizes the transmit/receive FIFO transmission interrupt source in the gateway mode.

<table>
<thead>
<tr>
<th>CFIM</th>
<th>FIFO Transmission Interrupt Request Generation Condition</th>
<th>Interrupt Request Clear Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Each 1 message transmission completion</td>
<td>Write “0” to CFTXI bit in CFSTSk register</td>
</tr>
<tr>
<td>0</td>
<td>Buffer becomes empty due to the completion of message transmission.</td>
<td></td>
</tr>
</tbody>
</table>

(e) Transmit/Receive FIFO One-frame Transmission Interrupt Processing

If enabled the transmit/receive FIFO one-frame transmission interrupt, the transmit/receive FIFO one-frame transmission interrupt is generated when the transmit/receive FIFO buffer transmits one frame.\(^1\)

The transmit/receive FIFO one-frame transmission interrupt can be enabled or disabled for each transmit/receive FIFO buffer by the CFOFTXIE bit in the CFCCEk register

\(^1\) Even if the transmit/receive FIFO buffer usage is disabled while the transmit/receive FIFO interrupt request is generated, the transmit/receive FIFO interrupt request is not automatically canceled. When canceling the receive/transmit FIFO interrupt request, set it by the program.
(i) Global Error Interrupt Processing

When the FIFO message lost interrupt is enabled, the global error interrupt is occurred when a message lost in the transmit/receive FIFO buffer is detected. The FIFO message lost interrupt can be enabled or disabled commonly for the entire module using MEIE bit in the GCTR register.

Table 2-4 summaries the global error interrupt source.

<table>
<thead>
<tr>
<th>Global Error Interrupt Request Generation Condition</th>
<th>Interrupt Request Clear Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>When the message lost of the transmit/receive FIFO buffer is detected.</td>
<td>Write “0” to CFMLT bit in CFSTSk register</td>
</tr>
</tbody>
</table>

*1 For the global error interrupt, multiple interrupt sources can be selected.

- Transmit history buffer overflow:
  - THLES bit in GERFL register (THLELT bit in the THLSTSm register for all channels)
- DLC error: DEIE bit in GCTR register
- CAN-FD message payload overwrite: CMPOFIE bit in GCTR register
- Transmit queue message overwrite: QOWEIE bit in GCTR register
- Transmit queue message lost: QMEIE bit in GCTR register
- GW FIFO message overwrite: MOWEIE bit in GCTR register
- FIFO message lost: MEIE bit in GCTR register
2.2 Gateway Function by Transmit Queue

When a transmit queue with TXQGWE bit in the TXQCC0 to 2m register set to 1B (transmit queue gateway mode) is selected with the GAFLP1j register, messages that passed through the filter processing of the receive rule are stored in the specified transmit queue and are automatically transmitted from the buffer.

In the transmit queue, messages with the highest priority by ID are transmitted first. In gateway mode, set the transmit queue depth to the number of IDs used in the transmit queue + 3.

In the gateway mode, when the transmit queue is accessed while it is full, the transmit queue message lost flag (TXQMLT bit in TXQSTS0 to 2m register) is set and the message is discarded.

Also, refer to “CAN Configuration Application Note” for the configuration setting to use the transmit queue.

2.2.1 Gateway Procedure in Transmit Queue

In the gateway mode, the messages are transmitted and received automatically within the RS-CANFD module, thus the transmission/reception processing is not required by the program.

Figure 2-6 and Figure 2-7 show the procedure for enabling and disabling the use of transmit queues.

Note 1. In transmit mode or gateway mode, rewrite the transmit queue usage enable setting in channel communication mode or channel standby mode.

Note 2. Enable the transmit queue usage after performing the configuration setting for using the transmit queue.

![Diagram of Procedure for Enabling Transmit Queue Usage]

Figure 2-6 Procedure for Enabling Transmit Queue Usage
Note 1. In transmit mode or gateway mode, rewrite the transmit queue usage disable settings in channel communication mode or channel standby mode.

Note 2. When the transmit queue is disabled, the transmit queue empty status is flagged at the following timings.
   • The transmit queue becomes empty immediately when the message in it is not being transmitted or is not to be transmitted next.
   • The queue becomes empty after transmission completion, CAN bus error detection, or arbitration lost when the message in it is being transmitted or to be transmitted next.

Note 3. Even if the transmit queue usage is disabled with the transmit queue interrupt request present (TXQSTS0 to 3m.TXQTXIF = 1 or TXQST0 to 3m.TXQOFTXIF = 1), the transmit queue interrupt request is not automatically canceled (TXQSTS0 to 3m.TXQTXIF = 0 or TXQSTS0 to 3m. TXQOFTXIF = 0). When canceling the transmit queue interrupt request, set it by the program.

Figure 2-7 Procedure for Disabling Transmit Queue Usage
2.2.2 Transmission Abort Function

By disabling the transmit queue usage setting (TXQCC0 to 3m.TXQE = 0), all messages in the transmit queue are lost, and the transmit queue empty status flag in the transmit queue status register is set to "1" (TXQSTS0~3m.TXQEMP = 1). The transmit queue empty status flag becomes "1" at the timing below. Messages are not stored in the transmit queue while the transmit queue usage is disabled.

• The transmit queue becomes empty immediately when the message in it is not being transmitted or is not to be transmitted next.
• The transmit queue becomes empty after transmission completion, CAN bus error detection, or arbitration lost when the message in it is being transmitted or to be transmitted next.

Refer to “Figure 2-7 Procedure for Disabling Transmit Queue Usage” for the transmission abort procedure of the transmit queue.
2.2.3 Transmit Queue Interrupt Processing (Gateway Mode)

(a) Transmit Queue One-Frame Routing Interrupt Processing

When selecting the transmit queue to the routing destination in GW mode, if the transmit queue one-frame routing interrupt is enabled, the transmit queue one-frame routing interrupt is generated when the transmit queue receives one frame.\(^1\)

The transmit queue one-frame routing interrupt can be enabled or disabled for each transmit queue by the TXQOFRXIE bit in the TXQCC0 to 2m register.

(b) Transmit Queue Channel Transmission Interrupt Processing

If the transmit queue interrupt is enabled (by the TXQTXIE bit in the TXQCC register), the transmit queue interrupt is generated when the condition selected by the TXQIM bit in the TXQCC register is satisfied.\(^1\)

Transmit queue transmission interrupt can be enabled or disabled for each transmit queue by the TXQTXIE bit in the TXQCC0 to 3m register.

“Table 2-5 Transmit Queue Transmission Interrupt Source” summarizes the transmit queue transmission interrupt source in the gateway mode.

<table>
<thead>
<tr>
<th>TXQIM</th>
<th>Transmit Queue Request Generation Condition</th>
<th>Interrupt Request Clear Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Each 1 message transmission completion</td>
<td>Write “0” to TXQTXIF bit in TXQSTS0 to 3m register</td>
</tr>
<tr>
<td>0</td>
<td>Transmit queue becomes empty due to the completion of message transmission</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) Even if the transmit queue usage is disabled while the interrupt request is generated, the interrupt request is not automatically canceled. When canceling the interrupt request, set it by the program.
(c) Transmit Queue One-Frame Transmission

If enabled the transmit queue one-frame transmission interrupt, the transmit queue one-frame transmission interrupt is generated when the transmit queue transmits one frame.\(^1\)

Transmit queue one-frame transmission interrupt can be enabled or disabled for each transmit queue by the CFOFTXIE bit in the TXQCC0 to 2m register.

(d) Transmit Queue Full Interrupt Request

If the transmit queue full interrupt is enabled, the transmit queue full interrupt is generated when TXQ of the routing destination becomes full.\(^1\)

The transmit queue full interrupt can be enabled or disabled for each transmit queue by the TXQFIE bit in the TXQCC0 to 2m register.

(e) Global Error Interrupt Processing

When the transmit queue message lost interrupt is enabled, the global error interrupt is generated when a message lost in the transmit queue is detected. The transmit queue message lost interrupt can be enabled or disabled commonly for the entire module using QMEIE bit in the GCTR register.

Table 2-6 summaries the global error interrupt source.

<table>
<thead>
<tr>
<th>Global Error Interrupt Request Generation Condition</th>
<th>Interrupt Request Clear Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>When the message lost of the transmit queue is detected.</td>
<td>Write “0” to TXQMLT bit in TXQSTS0 to 2m register(^1)</td>
</tr>
</tbody>
</table>

\(^1\) For the global error interrupt, multiple interrupt sources can be selected.

- Transmit history overflow:
  - THLES bit in GERFL register (THLELT bit in the THLSTSm register for all channels)
  - DLC error: DEIE bit in GCTR register
  - CAN-FD message payload overwrite: CMPOFIE bit in GCTR register
  - Transmit queue message overwrite: QOWEIE bit in GCTR register
  - Transmit queue message lost: QMEIE bit in GCTR register
  - GW FIFO message overwrite: MOWEIE bit in GCTR register
  - FIFO Message Lost: MEIE bit in GCTR register

\(^1\) Even if the transmit queue usage is disabled while the interrupt request is generated, the interrupt request is not automatically canceled. When canceling the interrupt request, set it by the program.
3. CAN-CAN FD Gateway (Only in CAN FD Mode)

When using the gateway function in CAN FD mode, the frame to be transmitted can be replaced with the classical CAN frame or the CAN FD frame.

Setting the GWEN bit in the CmFDCFG register to “1” enables the CAN-CAN FD gateway, and the GWFDF and GWBRS bits in the CmFDCFG register allow selection of the FDF and BRS bits in the transmit frame. If the DLC value of the received CAN frame is “1001B” or more and the GWFDF bit is set to “1” (CAN FD frame), the DLC is replaced with “1000B”.

Do not route the following frames when the CAN-CAN FD gateway is enabled.

- CAN FD frame with payload length greater than 8 bytes
- Remote frame

Also, when the CAN-CAN FD gateway is enabled, transmit only the following frames from the corresponding channel according to the GWFDF settings.

- GWFDF = 0: Transmit the reception frame as the classical CAN frame
- GWFDF = 1: Transmit the reception frame as the CAN FD frame
4. CAN-related Interrupt Processing

Refer to “CAN Configuration Application Note” for the CAN-related interrupt.

5. Notes on Processing Flow

5.1 Functions

In this application note, there are cases where even a single line of processing is described as a function, but this is only to clarify the processing for each function. When actually creating a program, it is not always necessary to make it a function. This is just to clarify the processing for each function.

5.2 Setting for Each Channel, FIFO, and Buffer

In this application note, even if processing is required for each channel, FIFO, or buffer, only one processing is described. When actually creating a program, perform multiple processes as necessary.

5.3 Infinite Loop

In order to simplify the explanation, some parts of the processing flow are shown as an infinite loop. When actually creating the program, please make sure that each loop has a time limit and that it exits when the loop overtimes. Figure 5-1 shows an example of processing with the loop time limit.

![Flowchart showing processing example with loop time limit](image-url)

Figure 5-1 Processing Example when Waiting for Loop Time Limit
6. Appendix

6.1 Software Explanation

Module Explanation

The following shows a list of modules for the sample program of CAN-FD mode 64-byte message transmission.

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main_pm0</td>
<td>Perform each setting and application start.</td>
</tr>
<tr>
<td>PORT setting processing</td>
<td>PORT_Init</td>
<td>Perform PORT initial setting.</td>
</tr>
<tr>
<td>Transmit/Receive FIFO reception completion interrupt setting processing</td>
<td>R_CAN_TxRxFI FO_IRQ_init</td>
<td>Perform transmit/receive FIFO reception completion</td>
</tr>
<tr>
<td>CAN initial setting processing</td>
<td>R_CAN_Init</td>
<td>Perform CAN initial setting.</td>
</tr>
<tr>
<td>Global operation mode setting</td>
<td>R_CAN_GlobalStart</td>
<td>Transfer global mode to global operation mode, and enable receive FIFO and transmit/receive FIFO usage.</td>
</tr>
<tr>
<td>CAN start processing</td>
<td>R_CAN_ChStart</td>
<td>Perform CAN0 activation.</td>
</tr>
<tr>
<td>CAN start processing</td>
<td>R_CAN_ChStart</td>
<td>Perform CAN1 activation.</td>
</tr>
</tbody>
</table>

Register Setting

The following shows a list of the register setting of each function for the sample program of CAN-FD mode 64-byte message transmission.

In this program, if the CAN FD message (64-byte data message with ID:0x222 (Standard ID)) is received by CAN0, it is set to be transmitted from CAN1.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Setting Value</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFDGCFG</td>
<td>0x0000100E</td>
<td>・Unused interval timer prescaler ・Set channel 0bit time clock to time stamp clock source selection. ・Set bit time clock to time stamp source selection. ・No time stamp source division. ・Reject the message in message payload overflow. ・Set internal clock (clkc [80MHz]) to CAN clock source selection. ・Mirror mode disables ・DLC exchanges enables ・DLC check enables ・Set ID priority to transmit priority selection</td>
</tr>
<tr>
<td>CFDCmNCFG (m=0, 1)</td>
<td>0x061C0C03</td>
<td>Set 1 Mbps to communication speed ・NBRP :3(4BRP) ・NTSEG1:14(15TQ) ・NTSEG2:3(4TQ) ・NSJW :3(4TQ)</td>
</tr>
<tr>
<td>CFDCmNCFG (m=2~7)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDCmDCFG (m=0, 1)</td>
<td>0x03030E00</td>
<td>Set 4 Mbps to communication speed ・DBRP :0(1BRP) ・DTSEG1:14(15TQ) ・DTSEG2:3(4TQ) ・DSJW :3(4TQ)</td>
</tr>
<tr>
<td>CFDCmDCFG (m=2~7)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDCmFDCFG (m=0~7)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>Register Name</td>
<td>Setting Value</td>
<td>Function</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>---------------</td>
<td>--------------------------------------------------------------------------</td>
</tr>
<tr>
<td>CFDGAFLCFGv (v=0)</td>
<td>0x00010001</td>
<td>CAN0 number of rules: 1</td>
</tr>
<tr>
<td>CFDGAFLCFGv (v=1~3)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDGAFLDCTR</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDGAFLIDj (j=1)</td>
<td>0x00000222</td>
<td>IDE selection: 0 (Standard ID)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RTR selection: 0 (Data frame)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Receive rule target message selection: 0 (When a message transmitted from another CAN node is received)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID setting value: 0x222 (01000100010b)</td>
</tr>
<tr>
<td>CFDGAFLIDj (j=2)</td>
<td>0x20000222</td>
<td>IDE selection: 0 (Standard ID)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RTR selection: 0 (Data frame)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Receive rule target message selection: 1 (When the own transmitted message is received)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID setting value: 0x222 (01000100010b)</td>
</tr>
<tr>
<td>CFDGAFLIDj (j=3~16)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDGAFLMj (j=1, 2)</td>
<td>0xC00007FF</td>
<td>IDE mask: 1 (Enable)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RTR mask: 1 (Enable)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID mask: 0x7FF</td>
</tr>
<tr>
<td>CFDGAFLMj (j=3~16)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDGAFLP0j (j=1, 2)</td>
<td>0x0012000F</td>
<td>Global acceptance filter list pointer: 0x0012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Receive buffer enable: 0 (Receive buffer unused)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Global acceptance filter list routing destination 0 to 2 setting: Specify transmit/receive FIFO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reception rule DLC setting: 0xF (1111b)</td>
</tr>
<tr>
<td>CFDGAFLP0j (j=3~16)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDGAFLP1j (j=1)</td>
<td>0x00000800</td>
<td>Enable channel 1 TX queue 0 as reception destination</td>
</tr>
<tr>
<td>CFDGAFLP1j (j=2)</td>
<td>0x00001000</td>
<td>Enable channel 1 TX queue 1 as reception destination</td>
</tr>
<tr>
<td>CFDGAFLP1j (j=3~16)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDRMNMB</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
<tr>
<td>CFDRFCCx (x=0~7)</td>
<td>0x00000000</td>
<td>Not set</td>
</tr>
</tbody>
</table>
### Table 6-4 CANFD Register Setting (3/3)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Setting Value</th>
<th>Function</th>
</tr>
</thead>
</table>
| CFDCFCCk (k=3) | 0x00400271 | - Set "0" to message transmission interval  
- Set 32 messages to communication FIFO buffer stage setting  
- Set buffer 0 to transmit buffer link setting  
- Set 1/8 message storing to communication FIFO reception interrupt request generation timing selection  
- Set "Interrupt generated when the FIFO counter reaches the CFIGCV value for receive / Interrupt generated when the FIFO has transmitted the last message for transmit” to communication FIFO interrupt source selection.  
- Set reference clock period x1 to communication FIFO interval timer resolution  
- Set reference clock to communication FIFO interval timer clock source selection  
- Set CAN-CAN GW FIFO to communication FIFO mode  
- Set 64 bytes to communication FIFO payload data size  
- Set disable to communication FIFO TX interrupt  
- Set disable to communication FIFO RX interrupt  
- Set enable to communication FIFO |
| CFDCFCCk (k=4) | 0x00400073 | - Set "0" to message transmission interval  
- Set 32 messages to communication FIFO buffer stage setting  
- Set buffer 0 to transmit buffer link setting  
- Set 1/8 message storing to communication FIFO reception interrupt request generation timing selection  
- Set "Interrupt generated when the FIFO counter reaches the CFIGCV value for receive / Interrupt generated when the FIFO has transmitted the last message for transmit” to communication FIFO interrupt source selection.  
- Set reference clock period x1 to communication FIFO interval timer resolution  
- Set reference clock to communication FIFO interval timer clock source selection  
- RX FIFO mode to communication FIFO mode  
- Set 64 bytes to communication FIFO payload data size  
- Set disable to communication FIFO TX interrupt  
- Set disable to communication FIFO RX interrupt  
- Set enable to communication FIFO |
| CFDCFCCk (k=0~2,5~23) | 0x00000000 | Not set |
| CFDTMIECy (y=0~15) | 0x00000000 | Not set |
| CFDTXQCm (m=0~3) | 0x00000000 | Not set |
| CFDGCTR | 0x00000000 | - No time stamp prescaler counter reset  
- Disable GW FIFO message overwrite interrupt  
- Disable TXQ message lost interrupt  
- Disable TXQ message overwrite interrupt  
- Disable payload overflow interrupt  
- Disable transmit history buffer overflow interrupt  
- Disable FIFO message lost interrupt  
- Disable DLC error interrupt  
- Disable Global sleep request  
- Global mode control keeps current value |
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.11</td>
<td>2023.01.23</td>
<td>-</td>
<td>Released English version of R01AN4895J0111.</td>
</tr>
</tbody>
</table>
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system evaluation test for the given product.
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.

5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.

6. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“VULNERABILITY ISSUES”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.

8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that all conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

10. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products. (Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries. (Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

Contact information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2023 Renesas Electronics Corporation. All rights reserved.