RH850/U2A-EVA Group
Example of capacitor placement

Introduction
This document describes the example of capacitor placement of RH850/U2A-EVA Group.
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design of your product or system. Renesas Electronics assumes no responsibility for any losses incurred by
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Target Device
● RH850/U2A-EVA Group
   ➢ RH850/U2A16
   ➢ RH850/U2A8
   ➢ RH850/U2A6
Contents

1. Decoupling capacitors ........................................................................................................... 3
   1.1 Capacitor placement and number of capacitors ................................................................. 3
   1.2 Types of capacitors ............................................................................................................. 3
   1.3 3-terminal capacitor ........................................................................................................... 3

2. Example of capacitor placement ............................................................................................. 4
   2.1 Example capacitor connection for BGA516 package (U2A16) ........................................... 4
   2.2 Example capacitor connection for BGA373 package (U2A16/U2A8) ................................ 5
   2.3 Example capacitor connection for BGA292 package (U2A16/U2A8) ............................... 6
   2.4 Example capacitor connection for BGA292 package (U2A6) ........................................... 7
   2.5 Example capacitor connection for BGA156 package (U2A6) ........................................... 8
   2.6 Example capacitor connection for HLQFP176 package (U2A6) ........................................ 9
   2.7 Example capacitor connection for HLQFP144 package (U2A6) ........................................ 10

3. PCB layout guidelines - Top layer / Bottom layer ................................................................. 11
   3.1 Example capacitor placement for BGA516 package (U2A16) .......................................... 11
   3.2 Example capacitor placement for BGA373 package (U2A16/U2A8) ................................. 13
   3.3 Example capacitor placement for BGA292 package (U2A16/U2A8) ................................. 15
   3.4 Example capacitor placement for BGA292 package (U2A6) ............................................ 17
   3.5 Example capacitor placement for BGA156 package (U2A6) ............................................ 19
   3.6 Example capacitor placement for HLQFP176 package (U2A6) ......................................... 21
   3.7 Example capacitor placement for HLQFP144 package (U2A6) ......................................... 23

4. Revision History ..................................................................................................................... 25
1. Decoupling capacitors

1.1 Capacitor placement and number of capacitors

- Please refer Chapter.2 “Example of capacitor placement” and Chapter.3 “PCB layout guidelines -Top layer / Bottom layer”.
- Capacitors has been kept as close as feasible to the related supply pin.

1.2 Types of capacitors

- 0.1uF, 0.22uF, 10uF or higher
  *1: This is expected value. Please follow the Power IC specification.
- 10uF 3-terminal ceramic capacitor (Very low ESR/ESL is required)

1.3 3-terminal capacitor

3-terminal capacitor is recommended for reduction of radiation noise.
2. Example of capacitor placement

2.1 Example capacitor connection for BGA516 package (U2A16)

It is recommended that the capacitor for AnVREF is closer to related pin than the capacitor for AnVCC.

Legend
- capacitor (If not specified;
  - expected value is 0.1uF.
  - please connect GND terminal of capacitors to a nearby VSS ball)
- capacitor (Expected value is 10uF or higher.
  Please follow the Power IC specification.)
- 3-terminal capacitor

Example in gray square shows the connection for VDD external power supply. Please refer the SVR guideline, if SVR used.

10uF feed-through capacitor as filter (Recommended)
2.2 Example capacitor connection for BGA373 package (U2A16/U2A8)

### Legend
- **3-terminal capacitor**
  - If not specified; expected value is 0.1\(\mu\)F.
  - Please connect GND terminal of capacitors to a nearby VSS ball.
- **Capacitor**
  - Expected value is 10\(\mu\)F or higher.
  - Please follow the Power IC specification.

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**U2A16/U2A8**

- **A0VCC** (AD4, AD5, AE5)
- **A0VREFH** (AE4)
- **A0VSS** (AC4, AD3, AE2, AE3)
- **A1VCC** (AB1, AB2, AC2)
- **A1VREFH** (AC1)
- **A1VSS** (AC3, AD1, AD2, AE1)
- **A2VCC** (AD22, AD23, AE22)
- **A2VREFH** (AE23)
- **A2VSS** (AC22, AC23, AD24, AD25, AE24, AE25)
- **GETH0PVCC** (J23)
- **GETH0RVCC** (K22)
- **GETH0BVCC** (K23)
- **GETH0VCL** (J22)
- **VSS**

**System**

- **SYSVCC** (H22)
- **AWOVCL** (T15)
- **AWOVCL** (A22)
- **VCC** (D7)
- **VCC** (K4)
- **VCC** (T4)
- **VDD** (N4)
- **VDD** (V22)
- **VSS**
- **SVRDRVCC** (B17, C17)
- **SVRDRVSS** (A16, B16)
- **SVRAVCC** (B18, C18)
- **SVRAVSS** (A19, B19)

**Digital IO**

- **E0VCC** (D18)
- **E0VCC** (T22)
- **E0VCC** (AB12)
- **VSS**
- **E1VCC** (D9, D10)
- **E1VCC** (M4)
- **VSS**
- **E2VCC** (AB14)
- **VSS**
- **LVDVCC** (D16)
- **VSS**

**Gigabit Ethernet (3.3V)**

- **0.22\(\mu\)F feed-through capacitor as decoupling (Recommended)**

**SYSVCl (T15)**

- **Open**
- **0.22\(\mu\)F feed-through capacitor as filter (Recommended)**

**Example in gray square**

- Shows the connection for VDD external power supply.
- Please refer to the SVR guideline, if SVR used.

**SVRAVCC**

- **Core voltage**
- **10\(\mu\)F feed-through capacitor as filter (Recommended)**

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It is recommended that the capacitor for AnVREF is closer to related pin than the capacitor for AnVCC.
2.3 Example capacitor connection for BGA292 package (U2A16/U2A8)

![Diagram of capacitor connection for BGA292 package (U2A16/U2A8)]

Legend:
- capacitor (If not specified; expected value is 0.1uF, please connect GND terminal of capacitors to a nearby VSS ball)
- capacitor (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor

Example in gray square shows the connection for VDD external power supply. Please refer to the SVR guideline, if SVR is used.
It is recommended that the capacitor for AnVREFH is closer to related pin than the capacitor for AnVCC.
2.5 Example capacitor connection for BGA156 package (U2A6)

It is recommended that the capacitor for AnVREFH is as close as possible to related pin.

Example in gray square shows the connection for VDD external power supply. Please refer the SVR guideline, if SVR used.
2.6 Example capacitor connection for HLQFP176 package (U2A6)

It is recommended that the capacitor for \( \text{AnVREFH} \) is as close as possible to related pin.

Example in gray square shows the connection for VDD external power supply. Please refer the SVR guideline, if SVR used.

10uF feed-through capacitor as filter (Recommended)
2.7 Example capacitor connection for HLQFP144 package (U2A6)

It is recommended that the capacitor for AnVREFH is as close as possible to related pin.

Legend
- capacitor (If not specified; - expected value is 0.1uF. - please connect GND terminal of capacitors to a nearby VSS ball)
- capacitor (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor

Example in gray square shows the connection for VDD external power supply. Please refer the SVR guideline, if SVR used.
3. PCB layout guidelines -Top layer / Bottom layer-

3.1 Example capacitor placement for BGA516 package (U2A16)

Legend
- capacitor (analog, Digital IO)
  (The capacitance is 0.1uF if not specified.)
- capacitor (system)
  (Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (Core voltage)
  (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor (analog, Digital IO)
- 3-terminal capacitor (Core voltage)

Please refer to the SVR guideline, if SVR used.
Example of capacitor placement

Please refer the SVR guideline, if SVR used.

Bottom Layer
3.2 Example capacitor placement for BGA373 package (U2A16/U2A8)

Legend
- capacitor (analog, Digital ID) 
  (The capacitance is 0.1uF if not specified.)
- capacitor (system) 
  (The capacitance is 0.1uF if not specified.)
- capacitor (Core voltage) 
  (The capacitance is 0.1uF if not specified.)
- capacitor (analog, Digital ID) 
  (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor (analog, Digital ID) 
- 3-terminal capacitor (Core voltage)

Please refer to the SVR guideline, if SVR used.
Bottom Layer
3.3 Example capacitor placement for BGA292 package (U2A16/U2A8)

Legend
- capacitor (analog, Digital IO)
  (The capacitance is 0.1uF if not specified.)
- capacitor (system)
  (The capacitance is 0.1uF if not specified.)
- capacitor (Core voltage)
  (The capacitance is 0.1uF if not specified.)
- capacitor (analog, Digital IO)
  (Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (system)
  (Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (Core voltage)
  (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor (analog, Digital IO)

Top Layer

Please refer to the SVR guideline, if SVR used.
Example of capacitor placement

Please refer the SVR guideline, if SVR used.

Bottom Layer
### 3.4 Example capacitor placement for BGA292 package (U2A6)

<table>
<thead>
<tr>
<th>Legend</th>
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<tbody>
<tr>
<td>capacitor (analog, Digital IO) (The capacitance is 0.1μF if not specified.)</td>
</tr>
<tr>
<td>capacitor (system) (Expected value is 10μF or higher. Please follow the Power IC specification.)</td>
</tr>
<tr>
<td>capacitor (Core voltage) (Expected value is 10μF or higher. Please follow the Power IC specification.)</td>
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<tr>
<td>capacitor (Core voltage) (The capacitance is 0.1μF if not specified.)</td>
</tr>
<tr>
<td>3-terminal capacitor (analog, Digital IO)</td>
</tr>
<tr>
<td>3-terminal capacitor (Core voltage)</td>
</tr>
</tbody>
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#### Top Layer

Please refer the SVR guideline, if SVR used.

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| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| A | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| C | P10_8 | P10_9 | P10_10 | P10_11 | P10_12 | P10_13 | P10_14 | P10_15 | P10_16 | P10_17 | P10_18 | P10_19 | P10_20 | P10_21 | P10_22 | P10_23 | P10_24 | P10_25 | P10_26 |
| D | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| E | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC |
| F | P10_2 | P10_3 | P10_4 | P10_5 | P10_6 | P10_7 | P10_8 | P10_9 | P10_10 | P10_11 | P10_12 | P10_13 | P10_14 | P10_15 | P10_16 | P10_17 | P10_18 | P10_19 | P10_20 | P10_21 |
| G | P10_2 | P10_3 | P10_4 | P10_5 | P10_6 | P10_7 | P10_8 | P10_9 | P10_10 | P10_11 | P10_12 | P10_13 | P10_14 | P10_15 | P10_16 | P10_17 | P10_18 | P10_19 | P10_20 | P10_21 |
| K | P10_2 | P10_3 | P10_4 | P10_5 | P10_6 | P10_7 | P10_8 | P10_9 | P10_10 | P10_11 | P10_12 | P10_13 | P10_14 | P10_15 | P10_16 | P10_17 | P10_18 | P10_19 | P10_20 | P10_21 |

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**Please refer the SVR guideline, if SVR used.**
Example of capacitor placement

Please refer the SVR guideline, if SVR used.

Bottom Layer
3.5 Example capacitor placement for BGA156 package (U2A6)

Legend
- capacitor (analog, Digital IO) (The capacitance is 0.1uF if not specified.)
- capacitor (system) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- capacitor (Core voltage) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor (analog, Digital IO)
- 3-terminal capacitor (Core voltage)

Please refer the SVR guideline, if SVR used.

Top Layer
Example of capacitor placement

Please refer the SVR guideline, if SVR used.

Bottom Layer
3.6 Example capacitor placement for HLQFP176 package (U2A6)

Legend
- 3-terminal capacitor (analog, Digital IO)
- Capacitor (system) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- Capacitor (Core voltage) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor (Core voltage) (Expected value is 10uF or higher. Please follow the Power IC specification.)
- Capacitor (analogue, Digital IO) (The capacitance is 0.1uF if not specified.)
- Capacitor (analogue, Digital IO) (The capacitance is 0.1uF if not specified.)
- Capacitor (analogue, Digital IO) (Expected value is 10uF or higher. Please follow the Power IC specification.)

Please refer the SVR guideline, if SVR used.

Exposed PAD (VSS)

Top Layer
Example of capacitor placement

Please refer the SVR guideline, if SVR used.

Exposed PAD (VSS)

Bottom Layer
3.7 Example capacitor placement for HLQFP144 package (U2A6)

Legend
- Capacitor (analog, Digital IO) (The capacitance is 0.1uF if not specified.)
- Capacitor (system) (The capacitance is 0.1uF if not specified.)
- Capacitor (Core voltage) (The capacitance is 0.1uF if not specified.)
- 3-terminal capacitor (analog, Digital IO) (Expected value is 10uF or higher. Please follow the Power IC specification.)

Exposed PAD (VSS)

Top Layer

Please refer the SVR guideline, if SVR used.

Analog 5V

Exposed PAD (VSS)
Exposed PAD (VSS)

Bottom Layer
4. Revision History

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<th>Summary</th>
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<td>Sep.30.20</td>
<td>all</td>
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<td>Add U2A8</td>
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<td>1.10</td>
<td>Jun.30.22</td>
<td>all</td>
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<td>Add U2A6</td>
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**General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products**

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. **Precaution against Electrostatic Discharge (ESD)**
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. **Processing at power-on**
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. **Input of signal during power-off state**
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. **Handling of unused pins**
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. **Clock signals**
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. **Voltage application waveform at input pin**
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_L$ (Max.) and $V_L$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_L$ (Max.) and $V_L$ (Min.).

7. **Prohibition of access to reserved addresses**
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. **Differences between products**
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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