

RH850/U2A-EVA Group

CAN Transmission Procedure

Summary

This application notes explain the procedure example for performing the CAN transmission of automotive single-chip microcontroller RH850/U2A series for automobile (hereinafter called U2A).

Aim of this document and software is to provide supplemental information for the function on RH850/U2A. It is not intended to implement in the design for mass production.

There is no guarantee to update in this document and software to reflect the latest manual, errata, technical update and development environment. You are fully responsible for the incorporation or any other use of the information of this document in the design of your product or system, and please refer to latest manual, errata, technical update and development environment.

Target Device

- RH850/U2A-EVA Group

Target Integrated Development Environment

CS+(from RENESAS Electronics)

Version	:V8.07.00
Device File	:DR7F702300.DVF
	:DR7F702301.DVF
	:DR7F702302.DVF

Reference Document

RH850/U2A-EVA User's Manual: Hardware

For function details and electrical characteristics, please refer to "User's Manual: Hardware".

This application note is based on the following manual.

- RH850/U2A-EVA User's Manual (Rev.1.30): R01UH0864EJ0130

The register name "RSCFDnCFD" is omitted in this text.

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1. Transmission Functions

The available functions when performing the CAN message transmission are shown below. For the details on each process, refer to the following chapters.

2. Transmission

3. Transmission using Transmit/Receive FIFO Buffers

4. Transmission using Transmission Queue

5. Transmit History Buffer Function

2. Normal Transmission

This function is transmission of the data frame or the remote frame using the transmit buffer.

There are 64 transmit buffers per channel, and it can be used as the transmit buffer, the link for the transmit/receive FIFO buffer (transmit mode, gateway mode), or the transmission queue.

When using the buffers as the link for transmit/receive FIFO buffer (transmit mode, gateway mode) or the transmission queue, set "H'00" to the corresponding TMCp register and "0" (interrupt disable) to the TMIEp bit in the TMIEy register. In this case, the corresponding flags in the corresponding TMSTSp register, TMTRSTSy register, TMTARSTSy register, TMTTCSTSy register, and TMTARSTSy register are not changed.

The functions of the transmit buffer are shown below. For the configuration settings for using the transmit buffer, refer to "CAN Configuration Application Note".

- Message transmission
- Transmission abort
- One-shot transmission (Retransmit disable function)

2.1 Message Transmit Function

This function is the transmission of the data frame or the remote frame. The message can be sent to set the transmit request to the transmit buffer (the TMTR bit in TMCp is "1".)

The transmission result can be confirmed by the corresponding TMTRF [1:0] flag in the TMSTSp register.

If the transmission is successful, no transmission abort request (the TMTRF [1:0] flag is "B'10"), or transmission abort required (the TMTRF [1:0] flag is "B'11"). (About the transmission is completed (the TMTRF [1:0] flag is "B'11"), refer to "2.2 Transmission Abort Function".)

For each transmit buffer, interrupt enable/disable when transmission is completed can be set by the TMIEp bit in the TMIECy register

Figure 2-1 shows the transmit buffer operation.

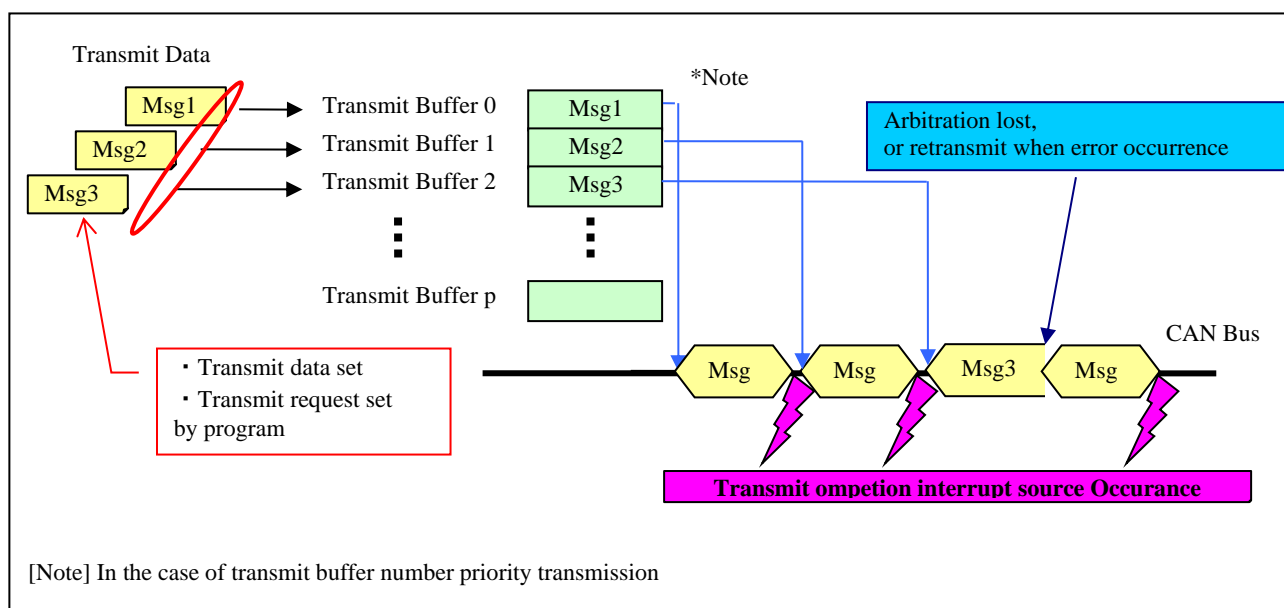


Figure 2-1 Transmit Buffer Operation (Transmit from Channel 0)

2.1.1 Message Transmit Procedure from Transmit Buffers

Figure 2-2 shows the message transmit procedure from transmit buffer.

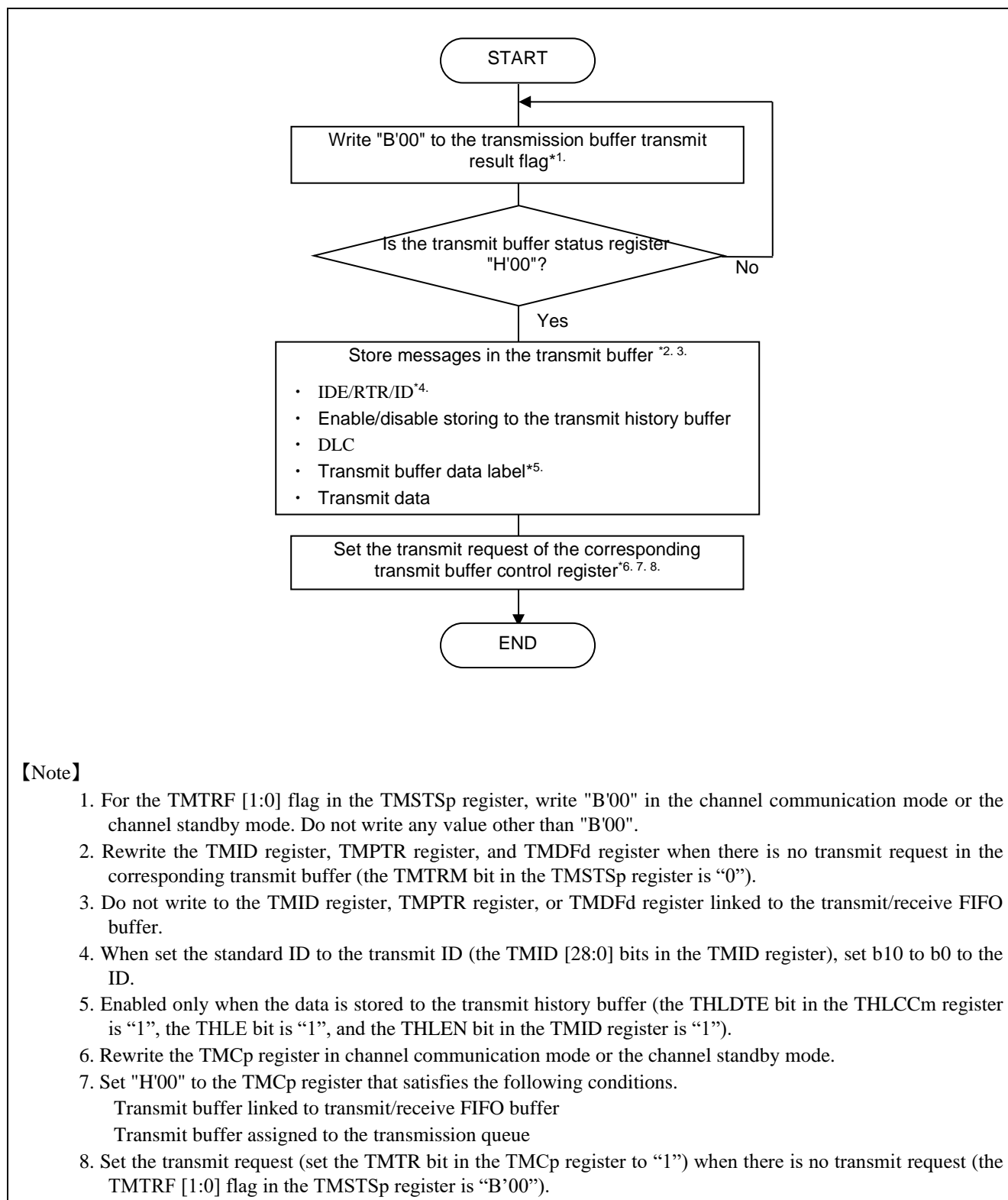


Figure 2-2 Message Transmit Procedure from Transmit Buffer

2.2 Transmission Abort Function

If two or more nodes start transmitting at the same time, the node with the lower CAN ID priority will be an arbitration lost (the message will be aborted in one-shot transmissions, and the message will be retained (retransmitted) in normal transmissions). A message will not be successfully sent unless it is sent without an arbitration lost or while the CAN bus in idling.

In such cases, the transmission abort function discards the message being retransmitted. The transmission abort function is effective when you want to set the time limit for sending a message, or when you want to send an urgent high-priority message.

Figure 2-3 shows the example of the transmission abort function.

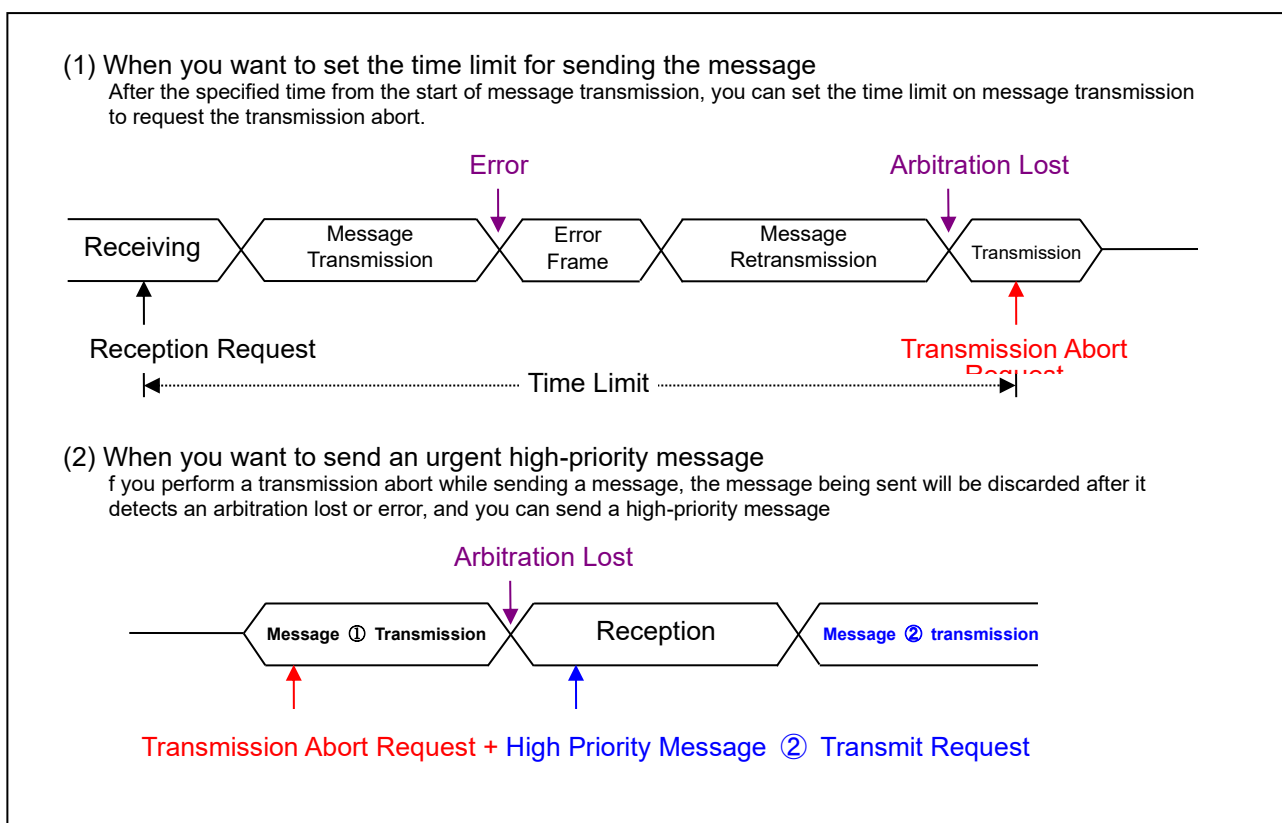


Figure 2-3 Example of Transmission Abort Function

When the transmission abort request is issued (the TMTRM bit in the TMSTSp register is “1”) and a transmit abort request is issued to the transmit buffer (the TMTAR bit of the TMCp register is “1”) the transmit request is cancelled.

After the transmission abort request is issued, the actual aborted timing is shown below.

Transmitting message or the message decided as the next transmitted message by the transmission priority decision

- When the arbitration lost is occurred
- When the error is occurred

Message other than the above.

- When the transmission abort request is issued

When the transmission abort is completed, the TMTRF [1:0] flag in the TMSTSp register becomes “B’01” and the transmit request is canceled (the TMTRM bit becomes “0”).

After issuing the transmission abort request to the transmitting message or the message determined as the next transmitted message by the transmission priority determination, if the transmission is completed successfully without the arbitration lost or error, the transmission is completed: There is the abort request (TMTRF [1:0] flag is “B’11”).

Figure 2-4 shows the operation during the transmission abort.

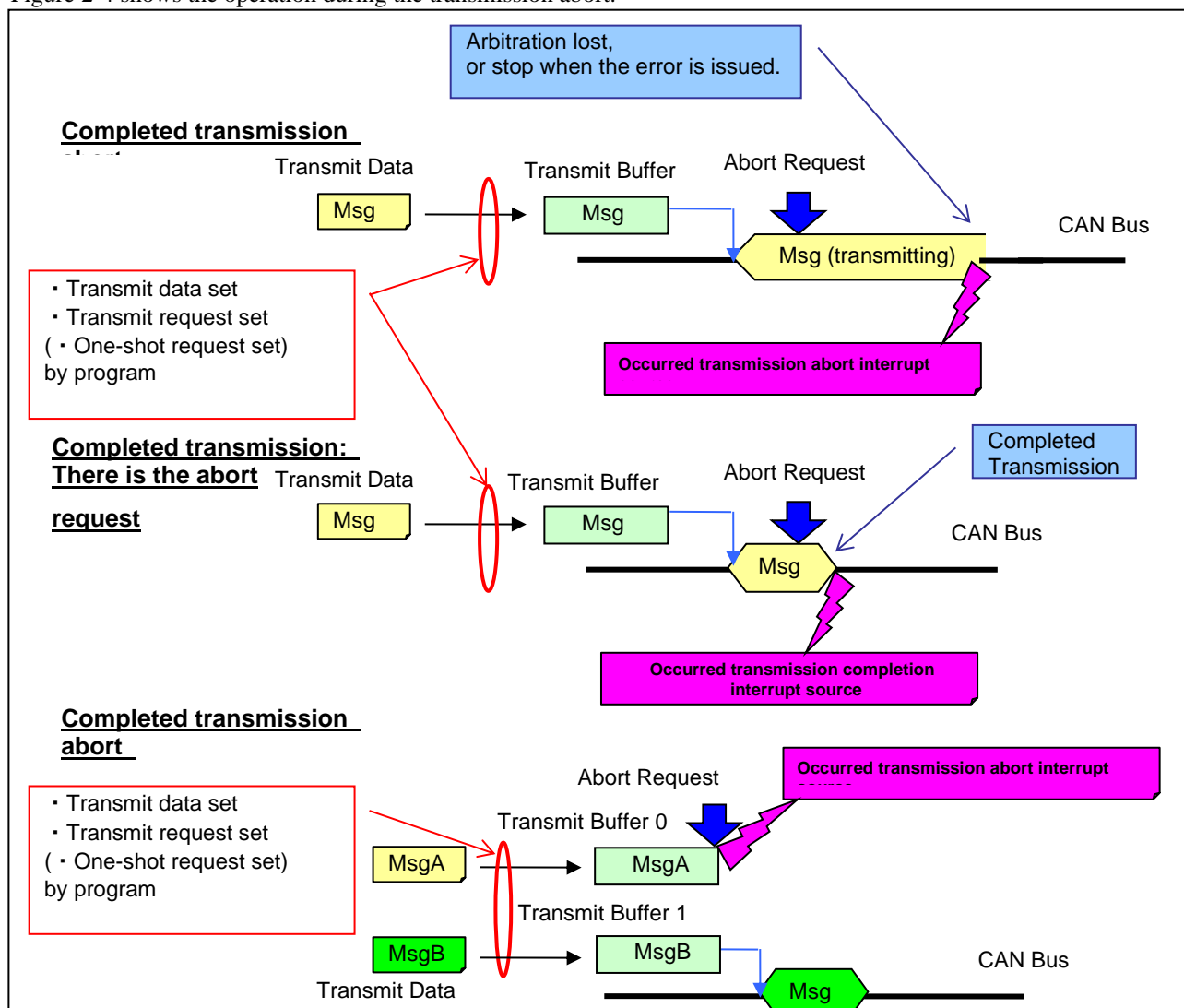
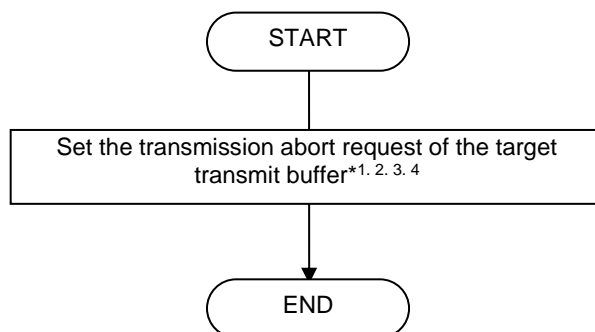


Figure 2-4 Operation during Transmission Abort

2.2.1 Transmission Abort Procedure

Figure 2-5 shows the transmission abort procedure.



【Note】

1. Rewrite the TMCp register by channel communication mode or channel standby mode.
2. Set "H'00" to the transmit TMCp register that satisfies the following conditions.
 - Transmit buffer linked to the transmit/receive FIFO buffer
 - Transmit buffer assigned to the transmission queue
3. When there is the transmit request in the transmit buffer (the TMTR bit in the TMCp register is "1"), the transmission abort request can be issued (the TMTAR bit in the TMCp register is "1").
4. Depending on the timing, the transmission result becomes "transmission completed: there is the transmission abort (the TMTRF[1:0] flag in the TMSTSp register is "B'11")". Therefore, if the transmission result is to be determined, please check not only "the transmission is complete (TMTRF [1:0] flag is "B'01")" but also "the transmission is completed: there is the transmission abort". Please refer to "2.4.3 Processing procedure after transmission completion and transmission abort completion" about the procedure for confirming transmission completion and transmission abort completion.

Figure 2-5 Transmission Abort Procedure

2.3 One-shot Transmit Function

If enable the one-shot (the TMOM bit in the TMCp register is “1”) when issuing the message transmit request, transmission is performed only once. Retransmission is not performed when the arbitration lost or the error is issued.

The one-shot transmission result can be confirmed by the TMTRF [1: 0] flag in the TMSTSp register. If the one-shot transmission is successful, the transmit buffer transmit result status is “transmission completed: no transmission abort request (TMTRF [1: 0] flag is “B'10”)” or “transmission completed: there is a transmission abort request (TMTRF [1: 0] flag will be “B'11””. If the arbitration lost or the error occurs, the abort is completed (TMTRF [1: 0] flag is “B'01”). (Refer to "2.2 Transmission Abort Function" for “transmission completion: there is a transmission abort request (TMTRF [1: 0] flag is "B'1")”). Figure 2-6 shows the operation of one-shot transmission.

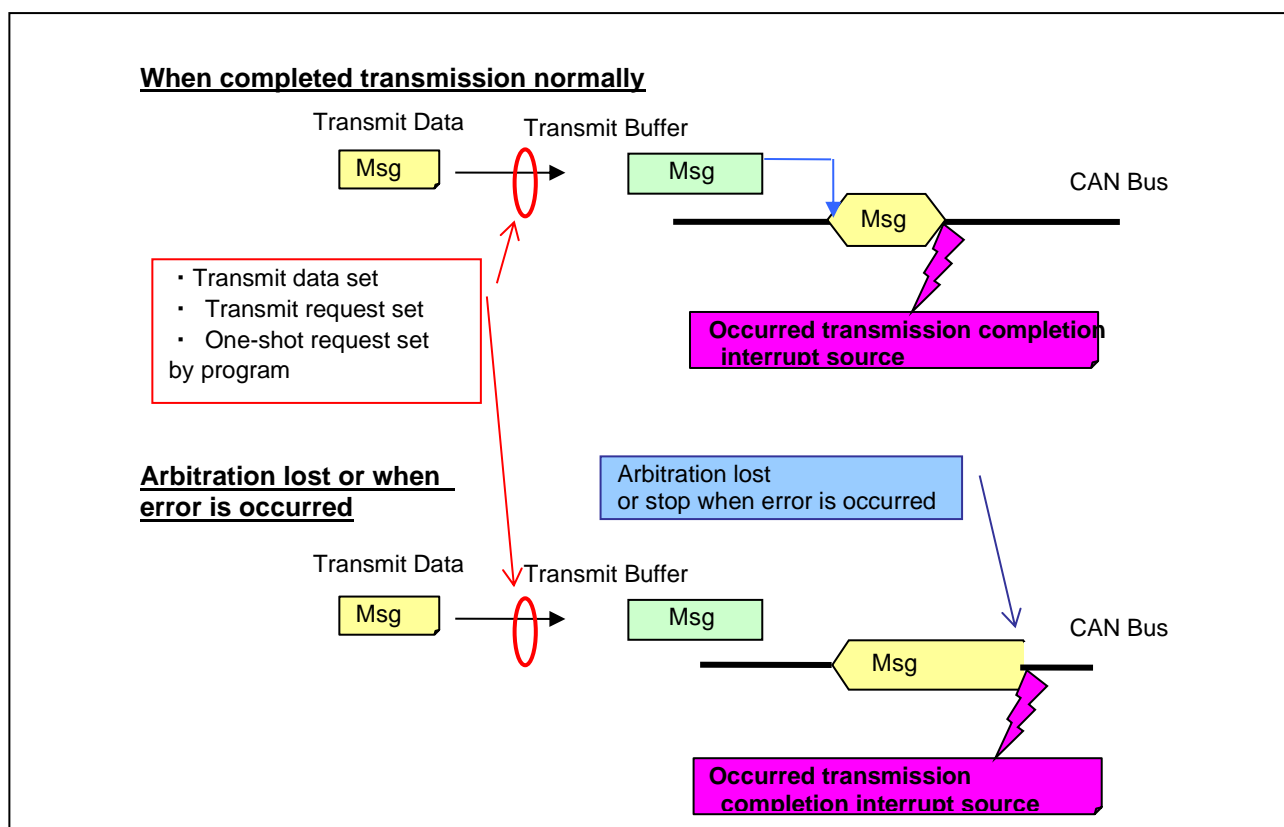
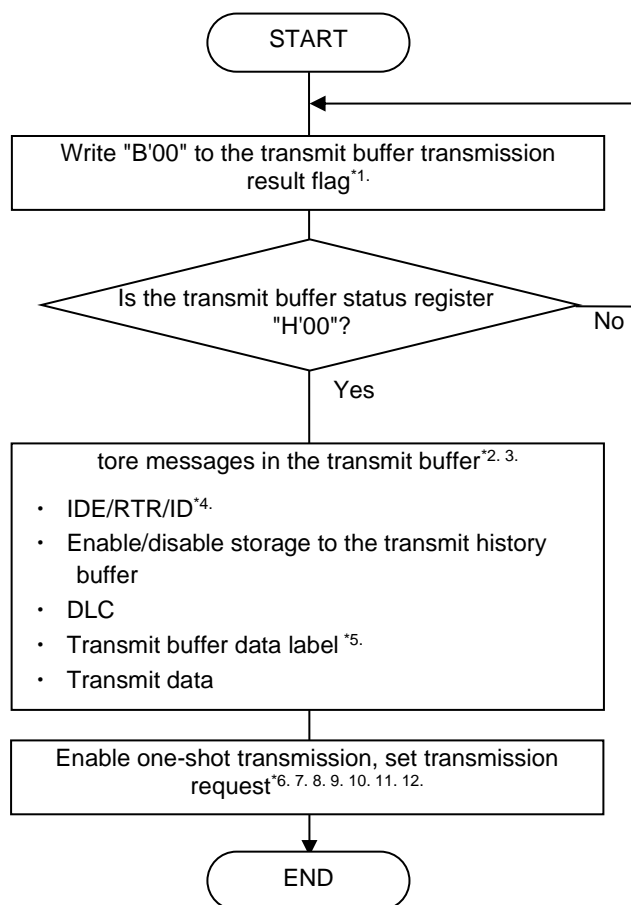


Figure 2-6 Operation during One-shot Transmission

2.3.1 One-shot Transmission Procedure

Figure 2-7 shows the one-shot transmission procedure.



【Note】

1. For the TMTRF [1:0] flag in the TMSTSp register, write "B'00" in the channel communication mode or the channel standby mode. Do not write any value other than "B'00".
2. Rewrite the TMID register, TMPTR register, and TMDFd register when there is no transmit request in the corresponding transmit buffer (the TMTRM bit in the TMSTSp register is "0").
3. Do not write to the TMID register, TMPTR register, or TMDFd register linked to the transmit/receive FIFO buffer.
4. When set the standard ID to the transmit ID (the TMID [28:0] bits in the TMID register), set b10 to b0 to the ID.
5. Enabled only when the data is stored to the transmit history buffer (the THLDTE bit in the THLCCm register is "1", the THLE bit is "1", and the THLEN bit in the TMID register is "1").
6. Rewrite the TMCp register in channel communication mode or the channel standby mode.
7. Set "H'00" to the TMCp register that satisfies the following conditions.
 - Transmit buffer linked to transmit/receive FIFO buffer
 - Transmit buffer assigned to the transmission queue
8. Set the transmit request (set the TMTR bit in the TMCp register to "1") when there is no transmit request (the TMTRF [1:0] flag in the TMSTSp register is "B'00").
9. Even if the transmission fails, the retransmission specified in the CAN protocol is not performed.
10. Enable one-shot transmission (the TMOM bit in the TMCp register is "1") when there is no transmission request in the transmit buffer (the TMTRM bit in the TMSTSp register is "0").
11. When enable the one-shot transmission, set at the same time as the transmit request (set "1" to the TMTR bit and the TMOM bit at the same time).

12. Depending on the timing, the transmission result becomes “transmission completed: there is the transmission abort (the TMTRF[1:0] flag in the TMSTSp register is "B'11")”. Therefore, if the transmission result is to be determined, please check not only “the transmission is complete (TMTRF [1:0] flag is "B'01")” but also “the transmission is completed: there is the transmission abort”. Please refer to "2.4.3 Processing procedure after transmission completion and transmission abort completion" about the procedure for confirming transmission completion and transmission abort completion.

Figure 2-7 One-shot Transmit Procedure

2.4 Transmit Buffer Interrupt Processing

2.4.1 Transmit Complete Interrupt Processing

If the transmit complete interrupt is enabled, the CANm transmission interrupt is occurred when the transmission is completed. Whether to enable or disable the transmission completion interrupt can be set for each transmit buffer by the TMIEp bit in the TMIECy register

The transmission completion interrupt is CANm transmission interrupt source. Determine the source within the interrupt as necessary when using the multiple interrupt sources.

For the interrupt source of CANm transmission, refer to "CAN Configuration Application Note"

2.4.2 Transmission Abort Complete Interrupt Processing

If the transmission abort complete interrupt is enabled, the CANm transmission interrupt is occurred when the transmission abort is completed. Whether to enable or disable the transmission abort completion interrupt can be set for each channel by the TAIE bit in the CmCTR register. However, if the "transmission is completed: there is an abort request (TMTRF [1:0] flag is "B'11")", the transmission abort completion interrupt is not occurred and the transmission completion interrupt is generated.

The transmission abort interrupt is CANm transmission interrupt source. Determine the source within the interrupt as necessary when using the multiple interrupt sources.

For the Interrupt source of CANm transmission refer to "CAN Configuration Application Note".

2.4.3 Processing Procedure after Transmission Completion and Transmission Abort Completion

Figure 2-8, Figure 2-9, and Figure 2-10 show the processing procedure after the transmission is completed and the transmission abort is completed.

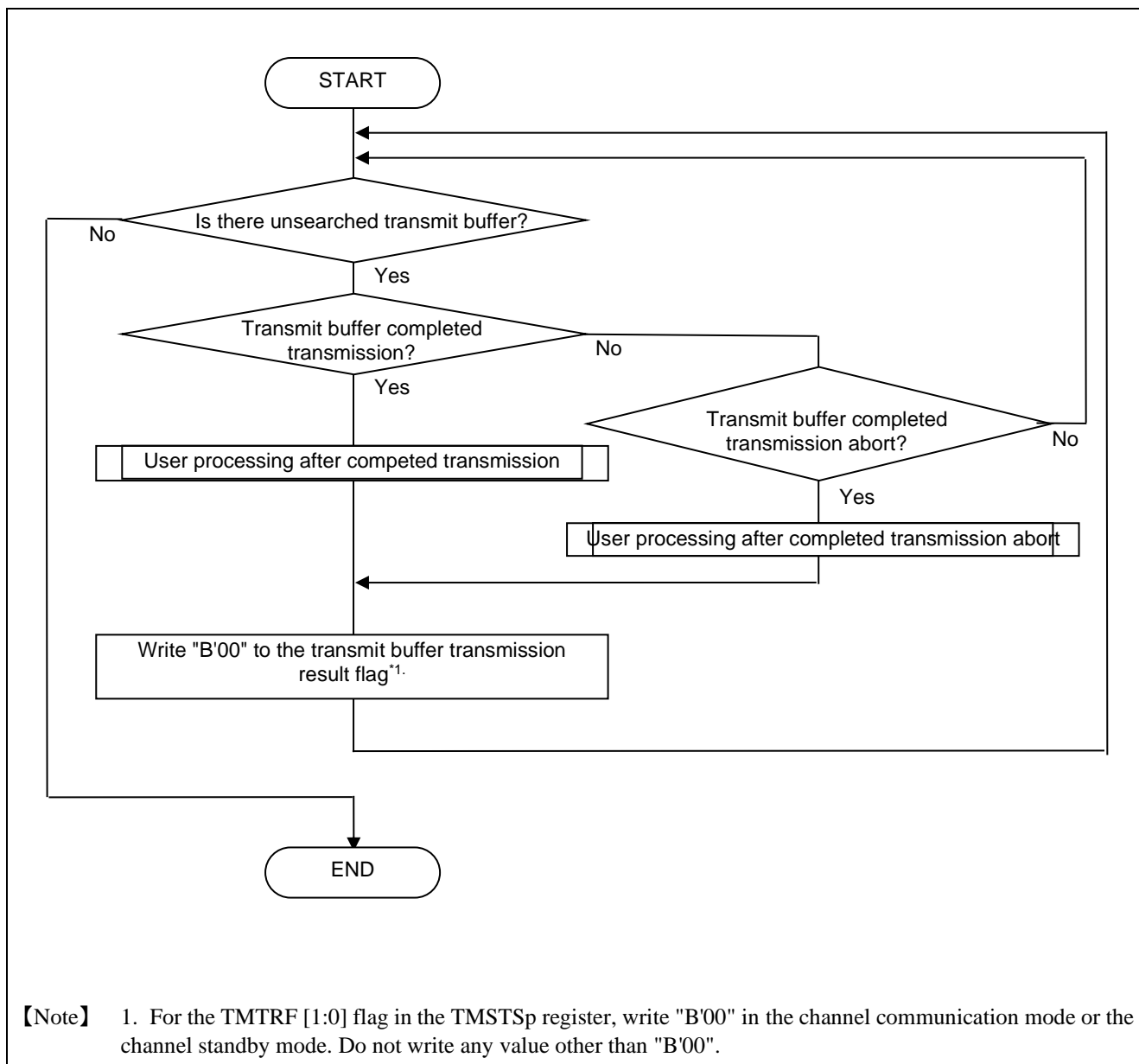
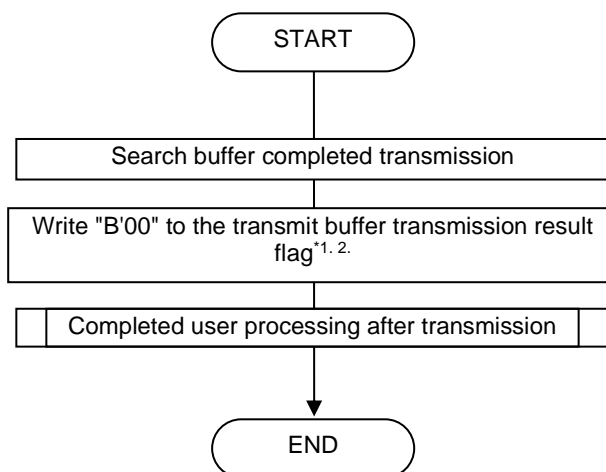


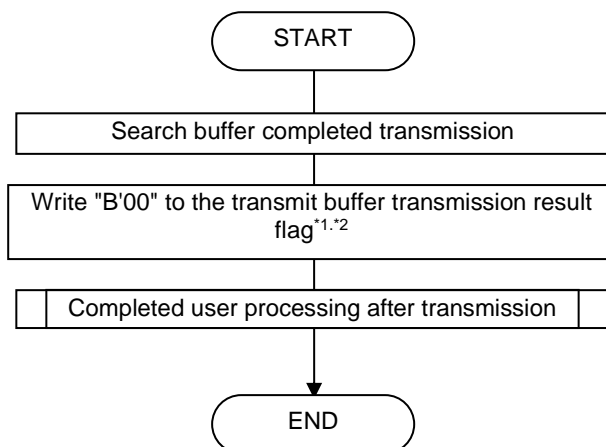
Figure 2-8 Processing Procedure after Completed Transmission and Completed Transmission Abort (unused interrupt)



【Note】

1. For the TMTRF [1:0] flag in the TMSTSp register, write "B'00" in the channel communication mode or the channel standby mode. Do not write any value other than "B'00".
2. Refer to “CAN Configuration Application Note” for the interrupt source flag processing procedure when using the interrupt.

Figure 2-9 Processing Procedure after Completed Transmission (using interrupt)



【Note】

1. For the TMTRF [1:0] flag in the TMSTSp register, write "B'00" in the channel communication mode or the channel standby mode. Do not write any value other than "B'00".
2. Refer to “CAN Configuration Application Note” for the interrupt source flag processing procedure when using the interrupt.

Figure 2-10 Processing Procedure after Completed Transmission Abort (using interrupt)

3. Transmission using Transmit/Receive FIFO Buffers

This function is transmission of the data frame or the remote frame by the transmit/receive FIFO buffers.

The transmit/receive FIFO buffers are three buffers per channel and can store up to 128 messages. It will be sent in order from the first stored message.

The transmit/receive FIFO buffer can be used in either receive mode, transmit mode, or gateway mode (only transmit mode is described in this chapter).

Refer to “CAN Reception Procedure Application Note” for the reception mode.

Refer to “CAN Gateway Mode Procedure Application Note” for the gateway mode.

The transmit/receive FIFO buffer is linked to the transmit buffer (selected by the CFTML [4:0] bit in the CFCCk register). When the transmit/receive FIFO buffer is used (the CFE bit in the CFCCk register is set to “1”), the priority determination of transmission is performed, and the priority determination is performed only for the next message to be sent in the transmit/receive FIFO buffer.

The transmit function of the transmit/receive FIFO buffer is shown below. Refer to "CAN Configuration Application Note" for using the transmit/receive FIFO buffer.

- Message transmit function
- Transmission abort function
- Interval transmit function

3.1.1 Message Transmit Function

The function is transmission of the data frame or the remote frame. The message stored in the transmit/receive FIFO buffers are transmitted in the order in which they were stored.

Figure 3-1 shows the transmit mode operation of the transmit/receive FIFO buffer.

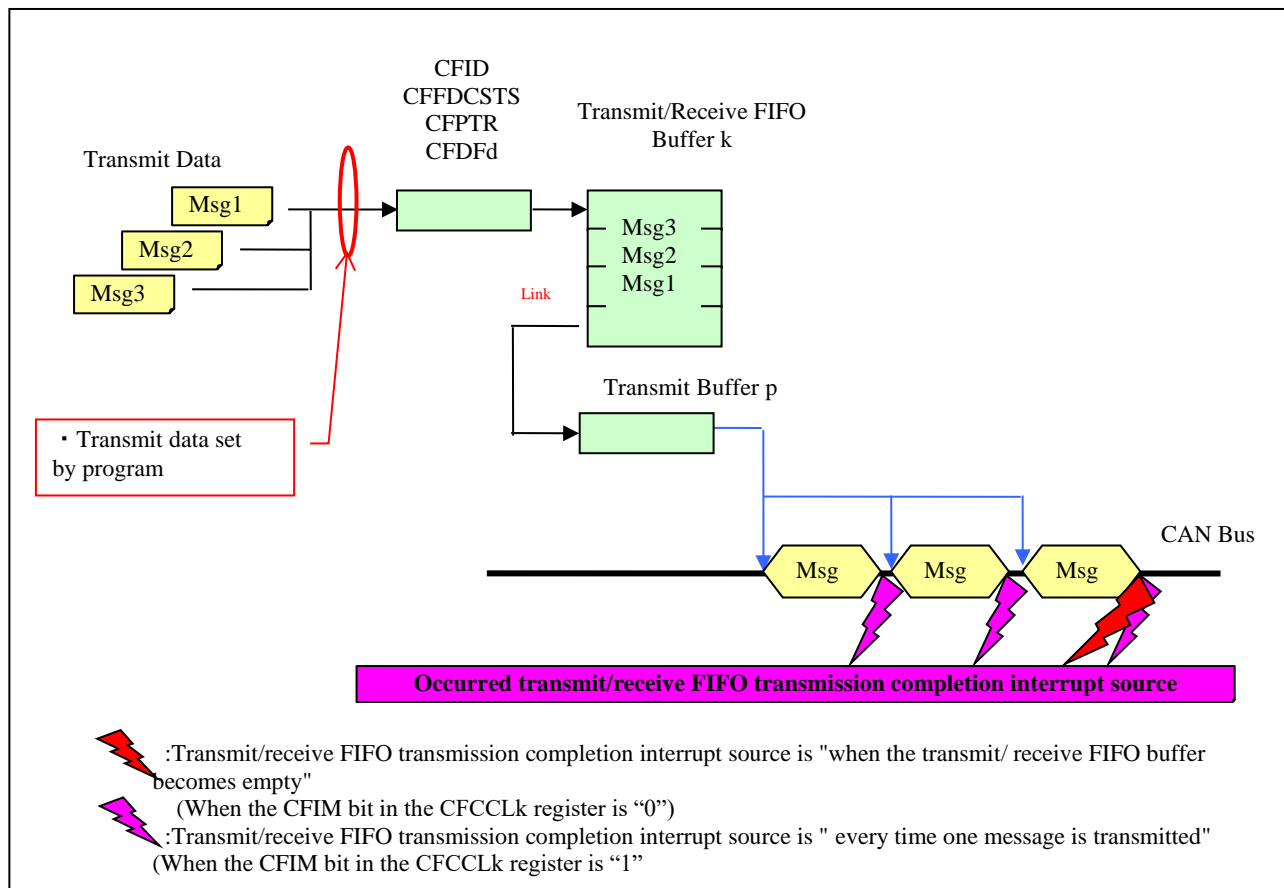
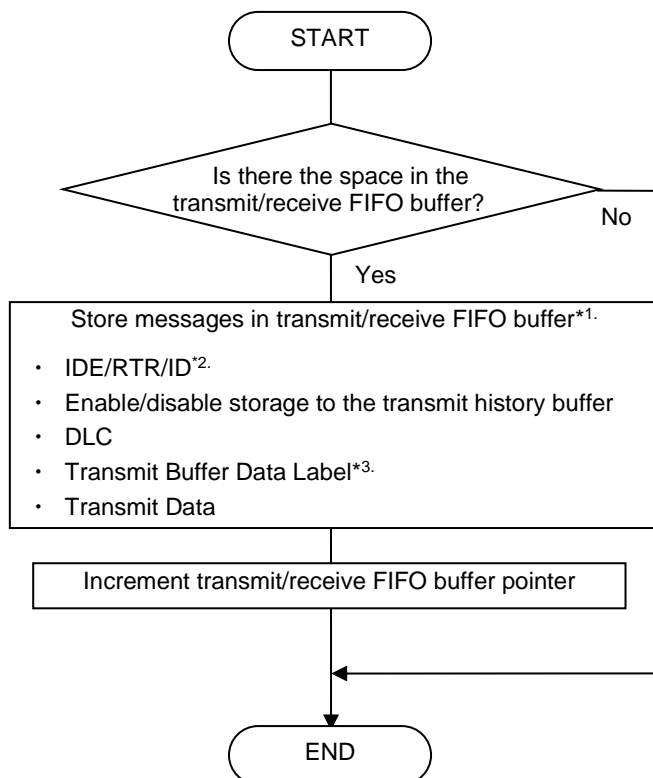


Figure 3-1 Transmit/Receive FIFO Buffer (Transmit mode) Operation

3.1.2 Message Transmission Procedure from Transmit/receive FIFO

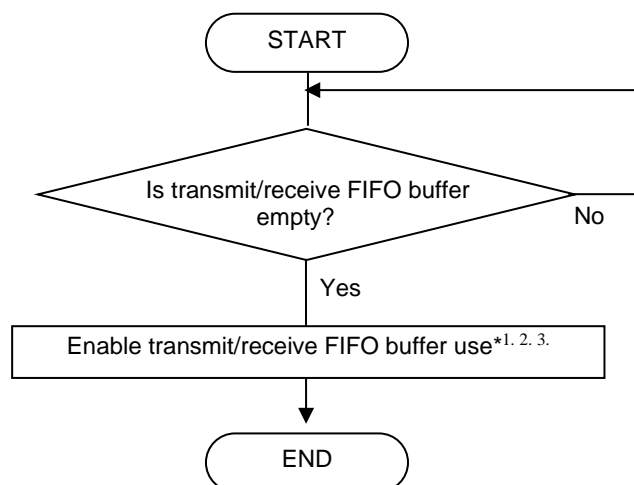
Figure 3-2 shows the procedure of sending the message from the transmit/receive FIFO buffer. Figure 3-3 and Figure 3-4 show the procedure for enabling/prohibiting the transmit/receive FIFO buffer.



【Note】

1. Only when the transmit/receive FIFO buffer is in transmit mode (the CFM [1:0] bit in the CFCCk register is "B'01"), the CFID register, CFPTR register, and CFDFd register can be written.
2. When setting the standard ID to the transmission ID (the CFID [15:0] bit in the CFIDL register) in the transmit mode, set the ID in b10 to b0. Set "0" to b28 to b11.
3. Enabled only when the data is stored to the transmit history buffer (the THLE bit in the THLCCm register is "1", the THLE bit is "1", and the THLEN bit in the CFID register is "1") and in the transmit mode.
4. Increment the transmit/receive FIFO buffer pointer if the following conditions are satisfied (write "H'FF" in the CFPC bit in the CFPCTRk register).
 - In transmit mode
 - When using transmit/receive FIFO (the CFE bit in the CFCCk register is "1")
 - After writing the transmit message to the transmit/receive FIFO buffer
 - The transmit/receive FIFO is not full (the CFFLL flag in the CFSTSk register is "0")

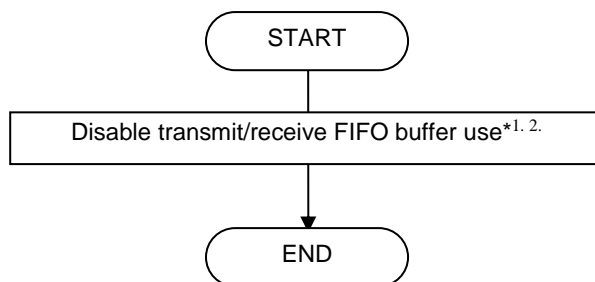
Figure 3-2 Message Transmission Procedure from Transmit/Receive FIFO Buffer



【Note】

1. When using the transmit mode, if the transmit/receive FIFO buffer is disabled, the transmit/receive FIFO buffer will be empty after transmission completion, CAN bus error detection, or arbitration lost if the message is being transmitted or is determined to be the next transmission.
2. When using the transmit mode, rewrite the transmit/receive FIFO buffer enable/disable (the CFE bit in the CFCCk register) in channel communication mode or channel standby mode.
3. Enable the transmit/receive FIFO buffer use (CFE bit is "1") after performing the configuration setting for using the transmit/receive FIFO buffer.

Figure 3-3 Procedure for Enabling Using Transmit/Receive FIFO Buffer



【Note】

1. Rewrite to enable/disable the transmit/receive FIFO buffer (the RFE bit in the RFCCx register) in the channel communication mode or the channel halt mode during the transmit mode using.
2. Even if the transmit/receive FIFO buffer use is disabled (the CFE bit is "0") while the interrupt request is occurred (the CFTXIF flag in the CFSTSk register is "1"), the CFTXIF flag is not automatically set to "0". Set "0" to the interrupt request flag by the program.

Figure 3-4 Procedure for disabling Using Transmit/Receive FIFO Buffer

3.2 Transmission Abort Function

The messages in the transmit/receive FIFO buffer can be aborted by disabling the transmit/receive FIFO buffer. The all messages in the transmit/receive FIFO buffer are aborted by the transmit/receive FIFO buffer aborting, not just the messages being sent (the transmit/receive FIFO buffer becomes empty (the CFEMP flag in the CFSTSk register is "1")). You can check the transmit/receive FIFO buffer aborting completion by checking that the transmit/receive FIFO buffer is empty

The interrupt is not occurred by the transmission abort completion of the transmit/receive FIFO. However, if aborted during transmission, the transmit/receive FIFO transmission completion interrupt may be occurred. Refer to " Figure 3-4 Procedure for disabling Using Transmit/Receive FIFO Buffer" for the transmission abort procedure of the transmit/receive FIFO buffer.

3.3 Interval Transmission Function

When using a transmit/receive FIFO buffer set to transmission mode or gateway mode, the interval time between messages can be set for consecutive messages transmitted from the same transmit/receive FIFO buffer.

When messages are transmitted continuously from the same transmit/receive FIFO buffer in transmission mode or gateway mode, the interval time between message transmissions can be set.

When the transmit/receive FIFO buffer is enabled (the CFE bit in the CFCCk register is “1”), the interval timer starts counting after the first message is successfully transmitted from the transmit/receive FIFO buffer ((After the 7th bit in EOF in the CAN protocol). After that, when the interval time has elapsed, the next message will be transmitted and the interval timer will be reset.

The timing at which the interval timer stops is shown below.

- When disable the transmit/receive FIFO buffer use (the CFE bit is “0”).
- When transfer to the channel reset mode.

Table 3-1 shows the count source of the interval timer and the calculation formula of the interval timer, Figure 3-5 shows the block diagram of the interval timer, and Figure 3-6 shows the operation example of the interval timer.

Table 3-1 Interval Timer Counter Source and Interval Time Calculation Formula

CFCC		Counter Source	Interval Time Calculation Formula
CFITR	CFITSS		
0	0	The Clock that divides the pclk/2 by the value of ITRCP [15.0] bits of GCFG register	$1/f_{PBA} \times 2 \times M \times N$
1	0	The Clock that divides the pclk/2 by the multiplied value of ITRCP [15.0] bits of GCFG register by 10.	$1/f_{PBA} \times 2 \times M \times 10 \times N$
-	1	CANm normal bit time clock	$1/f_{CANBIT} \times N$

【Note】

M: Divided value of the clock source of the interval timer for FIFO (set value of the GCFG.ITRCP [15: 0])

N: Message transmission interval (set value of the CFCCk.CFITT [7: 0])

f_{PBA} : pclk frequency

f_{CANBIT} : Normal CANm bit time clock frequency

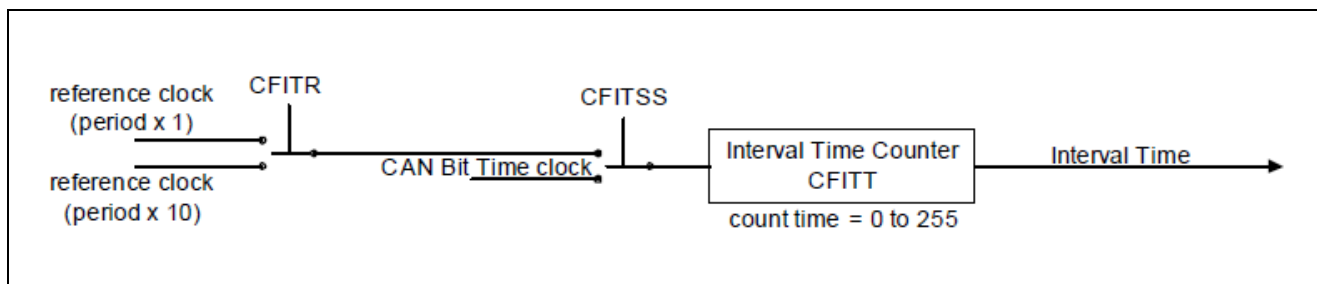


Figure 3-5 Block Diagram of Interval Timer

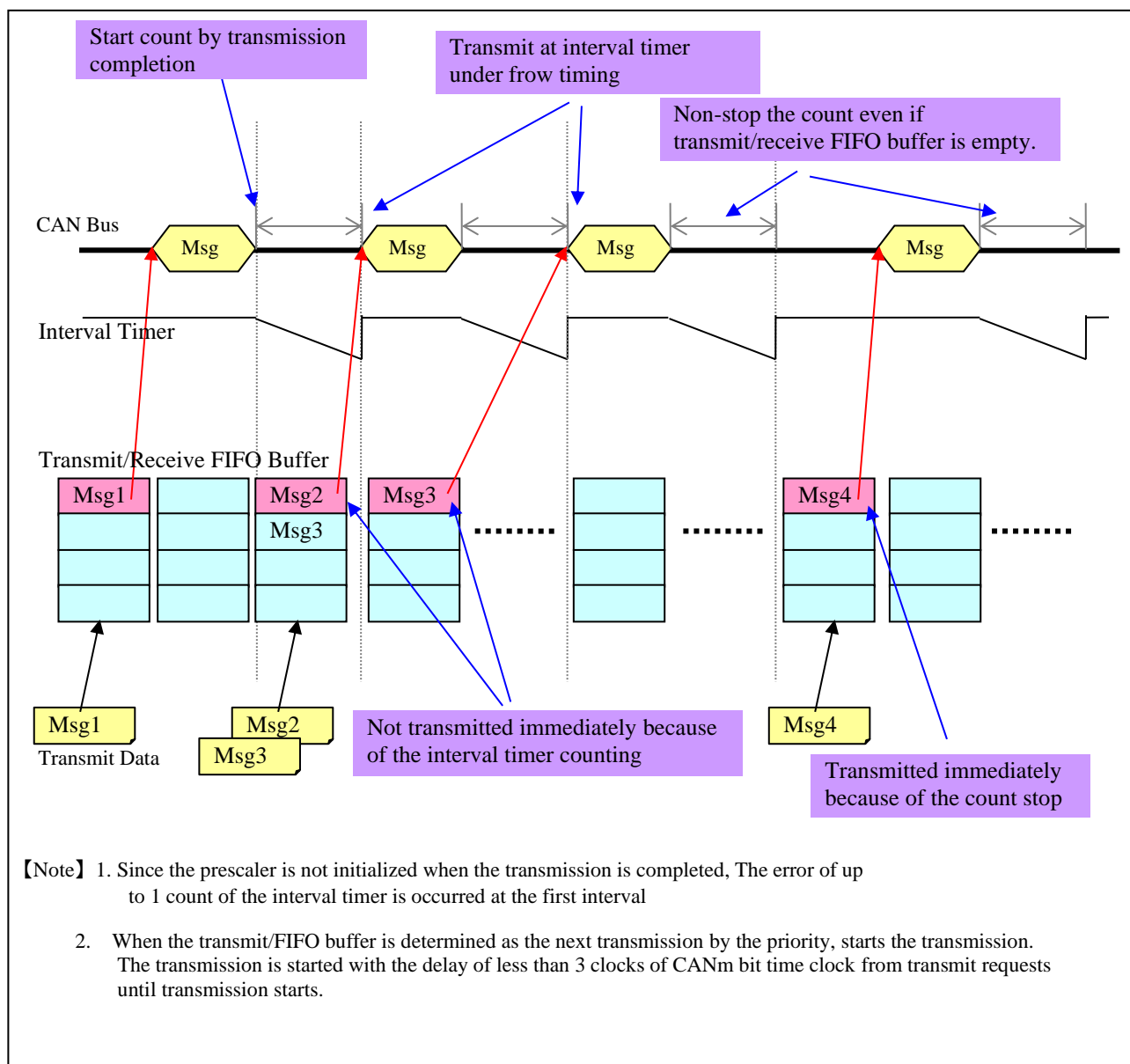


Figure 3-6 Interval Transmission Operation Example (Transmit Mode)

3.4 Interrupt Processing of Transmit/Receive FIFO Buffer (Transmit Mode)

3.4.1 Transmit/Receive FIFO Transmission Interrupt Processing

If enabling the transmit/receive FIFO transmission completion interrupt, the CANm transmit-related interrupt is generated by the condition selected by the CFIM bit in the CFCCk register setting. The enable/disable of the transmission queue one-frame interrupt is settable per transmit/receive FIFO buffer by the CFTXIE bit in the CFCCk register.

Further, the transmit/receive FIFO transmission completion interrupt becomes the CANm transmission interrupt source. Discriminate the source within the interrupt as necessary if you use the multiply interrupt sources.

Refer to “CAN Configuration Application Note” for the CANm transmission interrupt generation source.

Even if the use of the transmit/receive FIFO buffer is disabled (the CFE bit is “0”) while the interrupt request is being generated (the CFTXIF flag in the CFSTSk register is “1”), the CFTXIF flag is not automatically set to “0”. Set “0” to the interrupt request flag with the program

The transmit/receive FIFO transmission completion interrupt sources in the transmit mode are shown below.

- Transmit/receive FIFO transmission completion interrupt request is generated when the buffer becomes empty due to the message transmission completion.

- Transmit/receive FIFO transmission completion interrupt request is generated when each one message transmission is completed

3.4.2 Transmit/Receive FIFO One-frame Transmission Interrupt

If the transmit/receive FIFO one-frame transmission interrupt is enabled, the interrupt is generated when the one-frame transmission is completed. The enable/disable of the transmission completion interrupt is settable for each transmit/receive FIFO buffer by the CFOFTXIE register in the CFCCEk register.

Further, the transmit/receive FIFO one-frame transmission completion interrupt becomes the CANm transmission interrupt source. Discriminate the source within the interrupt as necessary if you use the multiply interrupt sources.

Refer to “CAN Configuration Application Note” for the CANm transmission interrupt generation source.

Even if the use of the transmit/receive FIFO buffer is disabled (the CFE bit is “0”) while the interrupt request is being generated (the CFOFTXIF flag in the CFSTSk register is “1”), the CFTXIF flag is not automatically set to “0”. Set “0” to the interrupt request flag by the program.

4. Transmission using Transmission Queue

This function is transmission of the data frame or the remote frame by using the transmission queue.

There are 4 transmission queues for each channel. Up to 32 buffers can be allocated to U2A-EVA, U2A16, and U2A8 for each transmission queue. Up to 16 buffers can be allocated to U2A6 for each transmission queue.

The transmission queue functions are shown below. For the configuration settings for using the transmission queue, Refer to "CAN Configuration Application Note" for the configuration settings to use the transmission queue

- Message Transmit Function
- Transmission Abort Function

4.1 Message Transmit Function

This function is the transmission using the data frame or the remote frame.

If the transmission queue is used, selects ID priority for the message priority.

All message in the transmission queue are targetted as the trasmit priotiry determination and trasnmitted in order to ID priority regardless of thr stored order. If the two messages that have same IDs are stored the trasnmitt queue, the order that these messages are transmitted may be different from the order stored in the transmission queue.

Figure 4-1 shows the operation of transmission queue.

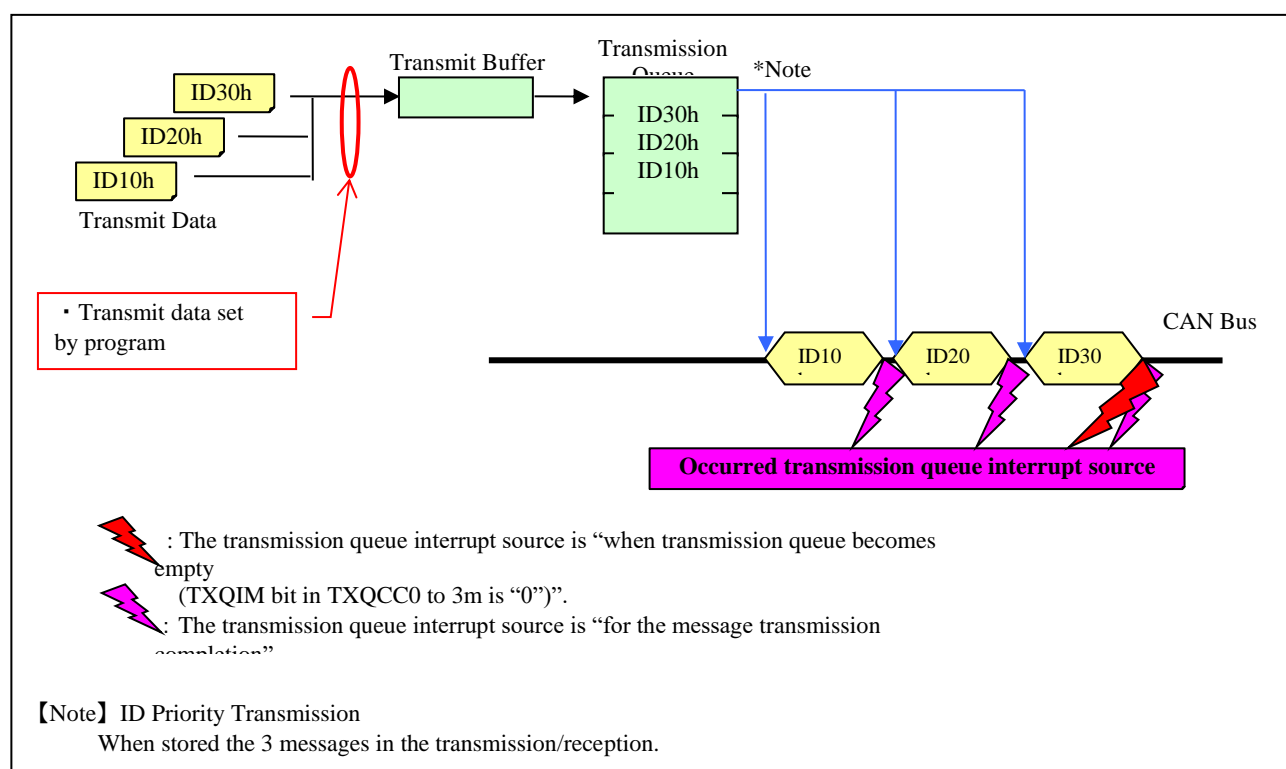
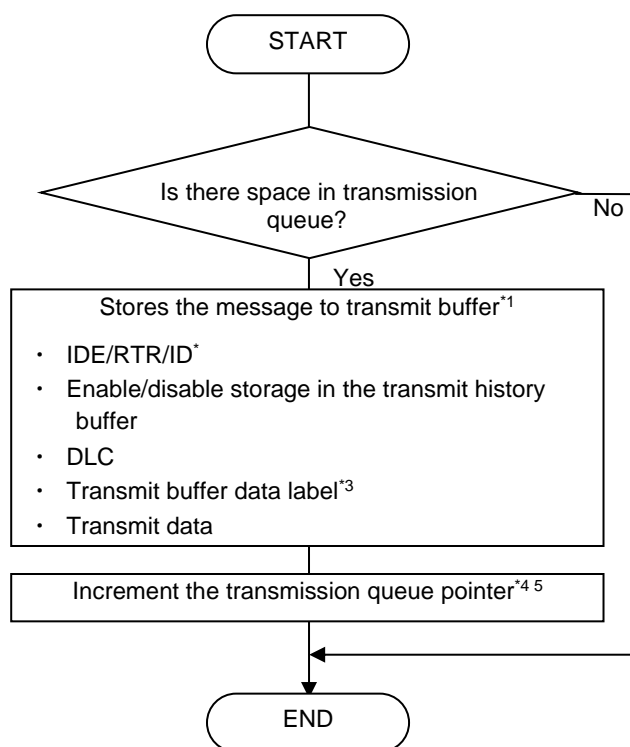


Figure 4-1 Transmission Queue Operation

4.1.1 Message Transmission Procedure from Transmission Queue

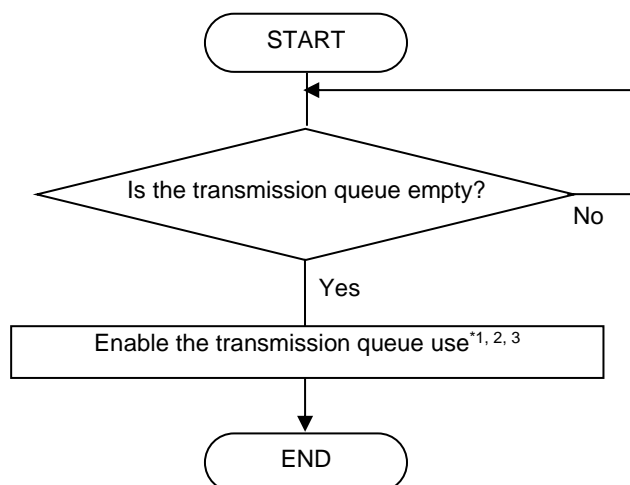
Figure 4-1 shows the message transmission procedure from the transmission queue.



【Note】

1. If allocated to the transmission queue, write to the transmit buffer only.
2. When set the standard ID to the transmit ID (the TMID [28:0] bits in the TMID register), set the ID to b10 to b0. Set "0" b28 to b11.
3. It is enabled only when stored to the transmit history buffer (the THLE bit in the THLCCm register is "1" and the THLEN bit in the TMID register is "1").
4. After writing the transmit message to the transmission queue, increment the transmission queue pointer (write "H'FF" in the TXQPC [7:0] bit in the TXQPCTRM register).
5. Increment the transmission queue pointer when the transmission queue is used (the TXQE bit in the TXQCC0 to 3m register is "1") and the transmission queue is not full (the TXQFLL flag in the TXQSTS0 to 3m register is "0").

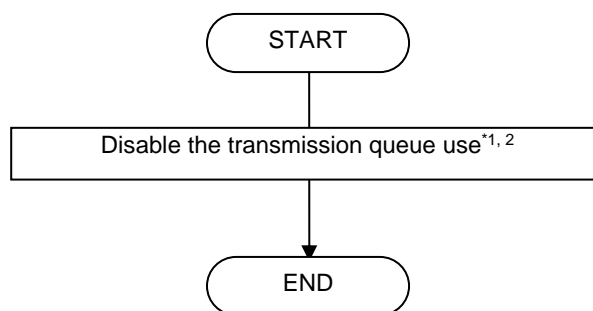
Figure 4-2 Message Transmission Procedure from Transmission Queue



【Note】

1. When disables the transmission queue, and if it is not transmitting the transmission queue message and decided the next transmission, the transmission queue will be empty. If the transmission queue message is already transmitting or decided the next transmission, it will be empty after the transmission completion, CAN Bus error, and arbitration lost.
2. Rewrite the transmission queue enable/disable (the TXQE bit in the TXQCC0 to 3m register) by the channel communication mode or channel halt mode.
3. Set the number of buffers to be allocated to the transmission queue (set "B'0010" or higher to the TXQDC [4:0] bits in the TXQCC0), and then enable the transmission queue (set "1" to the TXQE bit).

Figure 4-3 Use Enable Procedure of Transmission Queue



【Note】

1. Rewrite the transmission queue enable/disable (the TXQE bit in the TXQCC0 to 3m register) by the channel communication mode or channel halt mode.
2. Even if the use of the transmit/receive FIFO buffer is disabled (the TXQE bit is "0") while the interrupt request is generated (the TXQIF flag in the TXQSTS0 to 3m register is "1"), the TXQIF flag is not automatically set to "0". Set the interrupt request flag to "0" with the program.

Figure 4-4 Use Disable Procedure of Transmission Queue

4.2 Transmit Abort Function

By disabling the transmission queue the message in the transmission queue can be aborted. The abort by the transmission queue aborts all messages in the transmission queue, not just the transmitting messages (the transmission queue will be empty (the TXQ31EMP to TXQ31EMP flag in the TXQSTS0 to 3m register will be "1")). The abort completion of the transmission queue can be performed to check the transmission queue emptiness.

The interrupt is not generated when the transmission abort of the transmission queue is completed. However, if aborting during transmission, the transmission queue completion interrupt may occurred due to transmission completion. Refer to "Figure 2-3 Example of Transmission Abort Function" for the details.

4.3 Transmission Queue Interrupt Processing

4.3.1 Transmission Queue Interrupt Processing

If the transmission queue interrupt is enabled, the CANm transmit-related interrupt is generated when the condition selected by the TXQIM bit setting in the TXQCC0 to 3m register is satisfied. The transmission queue interrupt can be enabled or disabled for each transmission queue by the TXQIE bit in the TXQCC0 to 3m register

Further, the transmission queue interrupt becomes the CANm transmission interrupt source. Discriminate the source within the interrupt as necessary if you use the multiply interrupt sources. The generation source of the CANm transmit-related interrupt can be check by the GTINTSTSs register. Refer to "CAN Configuration Application Note" for the CANm transmission interrupt generation source.

Even if the use of the transmit/receive FIFO buffer is disabled (the CFE bit is "0") while the interrupt request is being generated (the CFTXIF flag in the CFSTSk register is "1"), the CFTXIF flag is not automatically set to "0". Set "0" to the interrupt request flag with the program.

The transmit/receive FIFO transmission completion interrupt sources in the transmit mode are shown below

- The transmission queue interrupt request is generated when the transmission queue becomes empty due to the message transmission completion
- The transmission queue interrupt request is generated when each one message transmission is completed

4.3.2 Transmission Queue One-frame Transmission Interrupt Processing

The enable/disable of the transmission queue one-frame interrupt is settable per transmit/receive FIFO buffer by the TXQOFTXIE bit in the TXQCCC0 to 3m register. If enabling the transmission queue interrupt, the CANm transmit-related interrupt is generated per frame transmission.

Further, the transmission queue one-frame transmission interrupt becomes the CANm transmission interrupt source. Discriminate the source within the interrupt as necessary if you use the multiply interrupt sources. The generation source of the CANm transmit-related interrupt can be check by the GTINTSTSs register.

Refer to "CAN Configuration Application Note" for the CANm transmission interrupt generation source

Even if the use of the transmit/receive FIFO buffer is disabled (the CFE bit is "0") while the interrupt request is being generated (the TXQOFTXIF flag in the TXQSTS0 to 3m register is "1"), the TXQSTS0 to 3m flag is not automatically set to "0". Set "0" to the interrupt request flag by the program.

5. Transmit History Buffer Function

The message information completed the transmission can be stored to the transmit history buffer. Each channel has one transmit history buffer, and the transmit history buffer can store 64 transmit history data.

5.1 Transmit History Data Storage Function

It is settable to store whether the type of the buffer of the message transmit source and the transmit history data for each message. The buffer type of the message transmit source is settable in the configuration. Refer to “CAN configuration Application Note” for the configuration setting to use the transmit history buffer.

Whether storing the transmit history data setting and the rebel data setting is settable in the transmission of each message.

Refer to “Figure 2-2 Message Transmit Procedure from Transmit Buffer”, “Figure 3-2 Message Transmission Procedure from Transmit/Receive FIFO Buffer”, and “Figure 4-2 Message Transmission Procedure from Transmission Queue” for the setting procedure in the transmission.

After succeeded the transmission, the following information is stored to the transmit history buffer as the transmit history data.

Buffer Type: The type of buffer transmitted the stored message

(Transmit buffer, Transmit/Receive FIFO buffer, or Transmitted buffer by the gateway)

Buffer Number: The transmit buffer of the transmit source or the number of the transmit/receive FIFO buffer (Refer to Table 5-1)

Label Data: Label information of transmit message. Settable the label information in the transmit message.

Time Stamp: The time stamp value of the transmit message

Table 5-1 Buffer Number of Transmit History Data

Buffer Type Buffer Number	B'001	B'010	B'100
	Transmit Buffer	Transmit/Receive FIFO Buffer	Transmission Queue
B'0000000	Transmit buffer 0	Transmit buffer number linked with transmit/receive FIFO buffer by the CFTML [4:0] bits of the CFCCk register	Transmit buffer number allocated with transmission queue performed the transmission
B'0000001	Transmit buffer 1		
B'0000010	Transmit buffer 2		
B'0000011	Transmit buffer 3		
B'0000100	Transmit buffer 4		
B'0000101	Transmit buffer 5		
B'0000110	Transmit buffer 6		
B'0000111	Transmit buffer 7		
B'0001000	Transmit buffer 8		
B'0001001	Transmit buffer 9		
B'0001010	Transmit buffer 10		
B'0001011	Transmit buffer 11		
B'0001100	Transmit buffer 12		
B'0001101	Transmit buffer 13		
B'0001110	Transmit buffer 14		
B'0001111	Transmit buffer 15		
⋮	⋮		
B' 1011111	Transmit buffer 95		

Figure 5-1 shows the transmit history buffer operation.

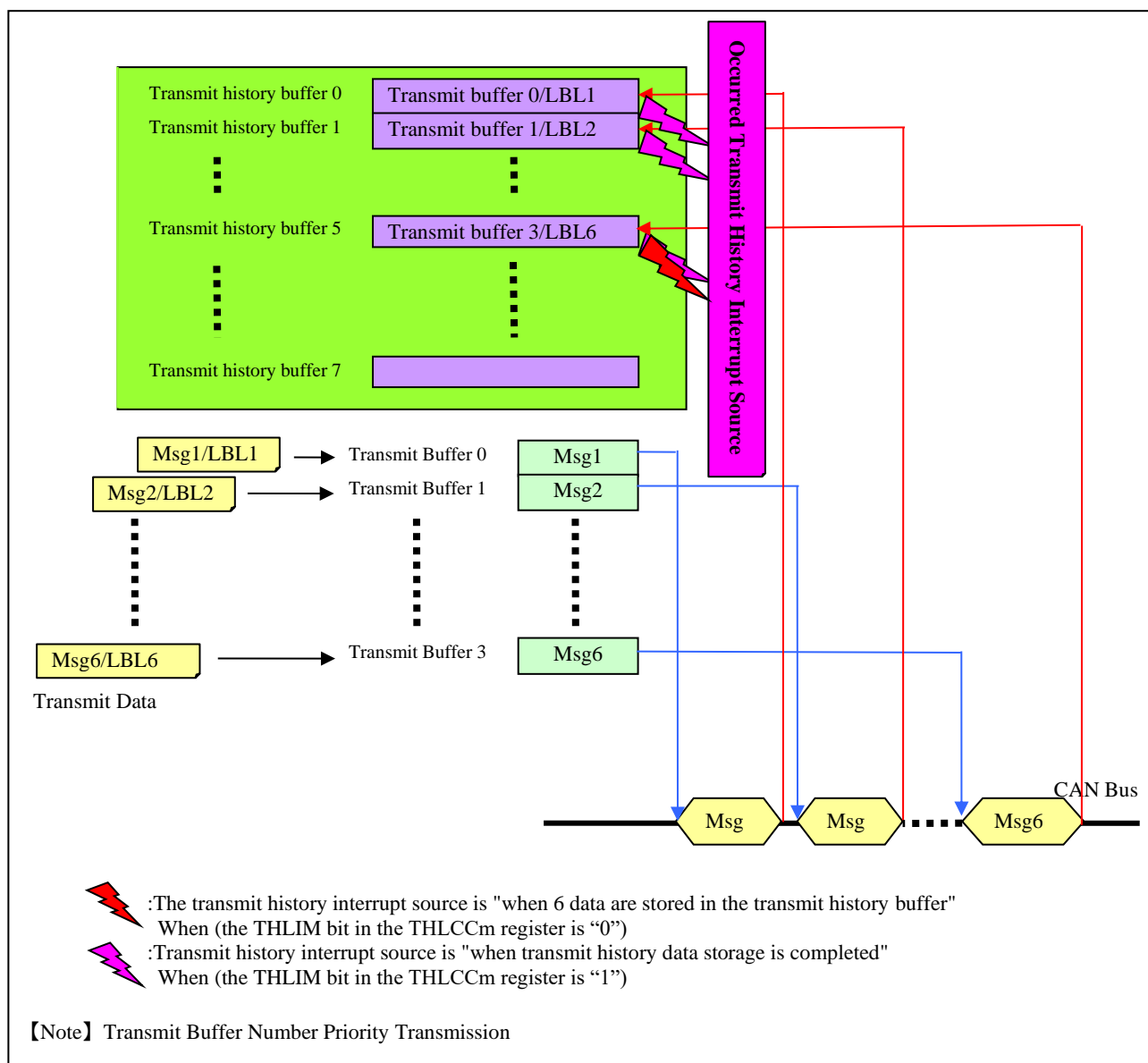
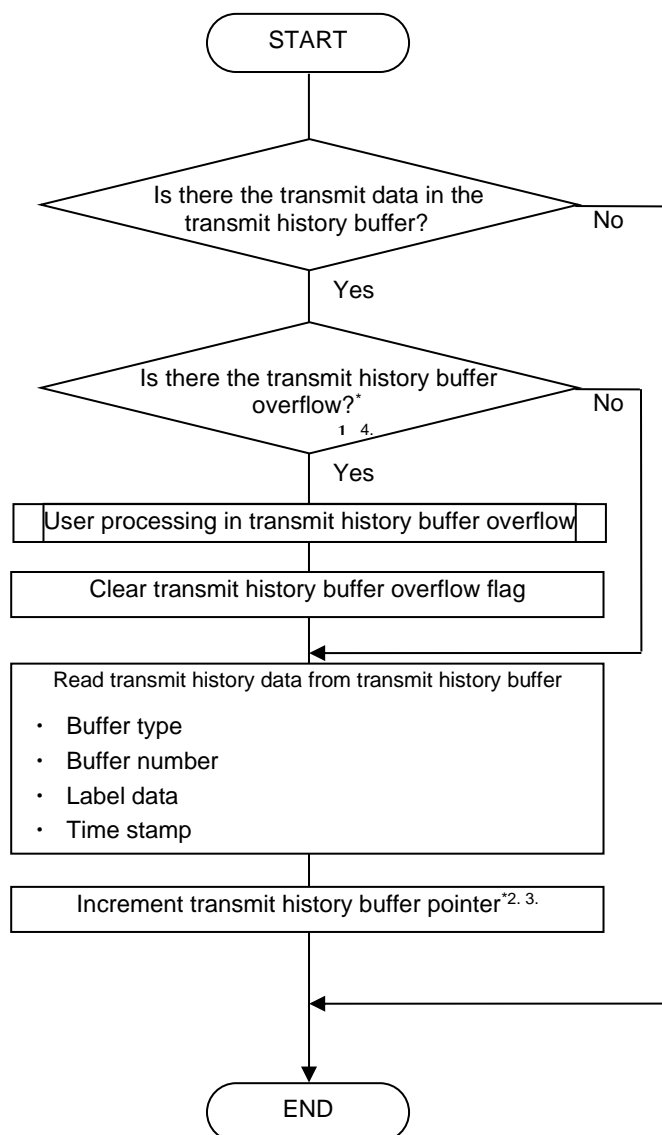


Figure 5-1 Transmit History Buffer Operation

5.1.1 Transmit History Buffer Read Procedure

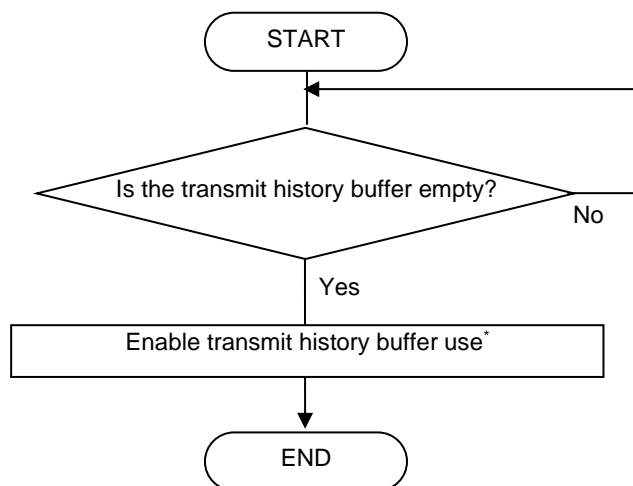
Figure 5-2 shows the read procedure for the transmit history data from the transmit history buffer. Figure 5-3 and Figure 5-4 shows the enable and disable procedure of the transmit history buffer.



【Note】

1. Write “0” to the THLELT bit in the THLSTSm register to by the program.
2. After reading the transmit history buffer (the THLACCM register), increment the transmit history buffer pointer (the THLPC [7:0] bit in the THLPCTRM register is “H'FF”).
3. Increment the transmit history buffer pointer when the transmit history buffer is used (the THLE bit in the THLCCM register is “1”) and the transmit history buffer is not empty (the THLEMP bit in the THLSTSm register is “0”).
4. If the transmit history buffer overflow interrupt is enabled, execute within the global error interrupt processing.

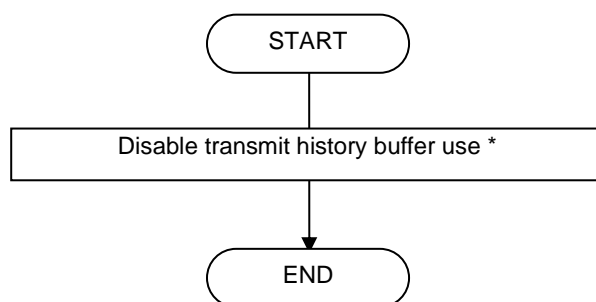
Figure 5-2 Transmit History Buffer Read Procedure



【Note】

1. Rewrite the enable/disable of the transmit history buffer (the THLE bit in the THLCCm register) in the channel communication mode or the channel standby mode.

Figure 5-3 Transmit History Buffer Use Enable Procedure



【Note】

1. Rewrite the enable/disable of the transmit history buffer (the THLE bit in the THLCCm register) in the channel communication mode or the channel standby mode.
2. Even if the transmit history buffer use is disabled (the THLE bit is "0") while the interrupt request is occurred (the THLIF flag in the THLSTSm register is "1"), the interrupt request flag (THLIF flag) is not automatically set to "0". Set "0" to the interrupt request flag by the program.

Figure 5-4 Transmit History Buffer Use Disable Procedure

5.2 Transmit History Buffer Interrupt Processing

5.2.1 Transmit History Interrupt Processing

If the transmit history interrupt is enabled, the CANm transmit-related interrupt is generated when the condition selected by the THLIM bit setting in the THLCCm register is satisfied.

Further, the transmission queue interrupt becomes the CANm transmission interrupt source. Discriminate the source within the interrupt as necessary if you use the multiply interrupt sources.

Refer to “CAN Configuration Application Note” for the CANm transmission interrupt generation source.

Even if the use of the transmit/receive FIFO buffer is disabled (the THLE bit is “0”) while the interrupt request is being generated (the THLIF flag in the THLSTSm register is “1”), the THLIF flag is not automatically set to “0”. Set “0” to the interrupt request flag with the program

The enable/disable of the transmit history interrupt is settable per transmit/receive history buffer by the THLIE bit in the THLCCm register.

Also, the stage of the transmit history buffer generated the transmit history interrupt request is settable by the THLIM bit in the THLCCm register per the transmit history buffer.

The transmit history interrupt sources are shows below.

- When the transmit history buffer is stored to 3/4 of the number of the transmission history buffer stages, the transit history interrupt request is generated
- The transmit history interrupt request is generated when each one transmit history data storing is completed.

5.2.2 Global Error Interrupt Processing

the global error interrupt is generated when the overflow if the transmit history buffer is detected to enable the transmit history buffer overflow interrupt. The transmit history buffer overflow interrupt enable/disable is settable in common to entire modules by THLEIE bit in the GCTR register.

6. CAN-related Interrupt Source

Refere to “CAN Configuration Application Note” for the CAN-related interrupt.

7. Transmit Data Patting (Only CAN FD Mode)

When the payload length shown by the DLC value of the set transmit message exceeds the payload storage area size, the excess payload is patted by “CCh”.

- Set transmit/receive FIFO to transmission of gateway mode:

When the payload length set to CFPLS [2:0] bits in the CFCCk register exceeds the payload storage area size

- In CAN-FD mode

When DLC value of the classical frame is 8 or more

8. Cautions of Processing Flow

Refere to “CAN Configuration Application Note” for the precautins of processing flow.

9. Appendix

9.1 Request to Transmit Buffer

The occurred interrupt source is different by the issued request to buffer and the condition that stops the transmission.

Table 9-1 shows the request to the transmit buffer and the generated interrupt condition generated.

Table 9-1 Request to Transmit Buffer and Generated Interrupt Source

TMCp Register			Generation Event	Transmission Result (TMTRF[1:0] flag in TMSTSp regsiter)	Generation Interrupt Source
Transmission request (TMTR)	Transmission abort request (TMTAR)	One-shot transmit request (TMOM)			
“1”	“0”	“0”	Transmission completion	“B’10” Completed transmission: No abort request	Transmission completion interrupt
			Occurred arbitration lost or error	“B’00” In transmitting	None
“1”	“1”	“0”	Transmission completion	“B’11” Completed transmission: Abort request	Transmission abort interrupt
			Occurred arbitration lost or error	“B’01” Completed transmission abort	Transmission abort interrupt
“1”	“0”	“1”	Transmission completion	“B’10” Transmit completed: No abort request	Transmission completion interrupt
			Occurred arbitration lost or error	“B’01” Completed transmission abort	Transmission abort interrupt
“1”	“1”	“1”	Transmission completion	“B’11” Completed transmission: Abort request	Transmission completion interrupt
			Occurred arbitration lost or error	“B’01” Competed transmission abort	Transmission abort interrupt
“0”	“x”	“x”	Impossible Setting		

Revision History

Rev.	Data	Description	
		Page	Summary
1.10	2022.01.20	-	Released English version of r01an4893jj0110

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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