RH850/F1x Series

Hardware Design Guide

R01AN1410EJ0420
Rev. 4.20
January 26, 2016

Introduction

This application note is intended to provide RH850/F1x series specific information and recommendations on the device usage. It should be used in conjunction with the corresponding RH850/F1x series user manuals and data sheets.

Target Device

RH850/F1L Group

- RH850/F1L (176 pin)
- RH850/F1L (144 pin)
- RH850/F1L (100 pin)
- RH850/F1L (80 pin)
- RH850/F1L (64 pin)
- RH850/F1L (48 pin)

RH850/F1M Group

- RH850/F1M (233 pin)
- RH850/F1M (176 pin)
- RH850/F1M (144 pin)

RH850/F1H Group

- RH850/F1H (272 pin)
- RH850/F1H (233 pin)
- RH850/F1H (176 pin)

Table of Contents

Table of Figures

1. Reference Documents

This chapter contains information about the device reference documentation.

1.1 User Manual

The user manual provides information about the functional behaviour of the device.

RH850/F1L User's Manual:	R01UH0390EJxxxx
RH850/F1M User's Manual:	R01UH0518EJxxxx
RH850/F1H User's Manual:	R01UH0445EJxxxx

1.2 Data Sheet

The data sheet provides information about the electrical behaviour of the device.

RH850/F1L (176 pin) Data Sheet:	R01DS0170EJxxxx
RH850/F1L (144 pin) Data Sheet:	R01DS0210EJxxxx
RH850/F1L (100 pin) Data Sheet:	R01DS0211EJxxxx
RH850/F1L (80 pin) Data Sheet:	R01DS0212EJxxxx
RH850/F1L (64 pin) Data Sheet:	R01DS0213EJxxxx
RH850/F1L (48 pin) Data Sheet:	R01DS0214EJxxxx
RH850/F1M Data Sheet :	R01DS0250EJxxxx
RH850/F1H Data Sheet:	R01DS0234EJxxxx

1.3 Operating Precaution

The operating precaution provides information about user's manual and data sheet differences and actual device implementations.

RH850/F1L (176 pin) Operating Precaution:	R01TU0046EDxxxx
RH850/F1L (144 pin) Operating Precaution:	R01TU0051EDxxxx
RH850/F1L (100 pin) Operating Precaution:	R01TU0052EDxxxx
RH850/F1L (80 pin) Operating Precaution:	R01TU0053EDxxxx
RH850/F1L (64 pin) Operating Precaution:	R01TU0063EDxxxx
RH850/F1L (48 pin) Operating Precaution:	R01TU0064EDxxxx
RH850/F1M (233 pin) Operating Precaution:	R01TUxxxxEDxxxx
RH850/F1M (176 pin) Operating Precaution:	R01TU0077EDxxxx
RH850/F1M (144 pin) Operating Precaution:	R01TUxxxxEDxxxx
RH850/F1H (272 pin) Operating Precaution	R01TU0068EDxxxx
RH850/F1H (233 pin) Operating Precaution	R01TU0076EDxxxx
RH850/F1H (176 pin) Operating Precaution	R01TU0065EDxxxx

2. Power Supply

2.1 Power Supply Overview of RH850/F1L Group

2.1.1 Power Supply Pin Overview of RH850/F1L Group

The devices of the RH850/F1L group have the following power supply pins.

Device	Power Supply Pins
RH850/F1L-176pin	REGVCC EVCC, EVSS BVCC, BVSS AnVREF, AnVSS (n = 0, 1)
RH850/F1L-144pin	REGVCC EVCC, EVSS BVCC, BVSS AnVREF, AnVSS (n = 0, 1)
RH850/F1L-100pin	REGVCC EVCC, EVSS A0VREF, A0VSS
RH850/F1L-80pin	REGVCC EVCC, EVSS A0VREF, A0VSS
RH850/F1L-64pin	REGVCC EVCC, EVSS A0VREF, A0VSS
RH850/F1L-48pin	REGVCC EVCC, EVSS A0VREF, A0VSS

The pins AWOVCL, AWOVSS and ISOVCL, ISOVSS are available on all devices to connect external capacitors.

2.1.2 Power Supply Pin Configuration of RH850/F1L Group

Depending on the device, the following power supply pin configuration applies:

The EVCC supply pins are internally connected.

The BVCC supply pins are internally connected.

2.1.3 Power Supply Pin Architecture of RH850/F1L Group

The RH850/F1L group supports different power supply architectures. The power supply architecture depends on the chosen RH850/F1L group device, application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1L group:

- REGVCC = EVCC = VPOC to 5.5V
- BVCC = VPOC to REGVCC
- A0VREF = 3.0V to 5.5V
- A1VREF = 3.0V to 5.5V
- AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

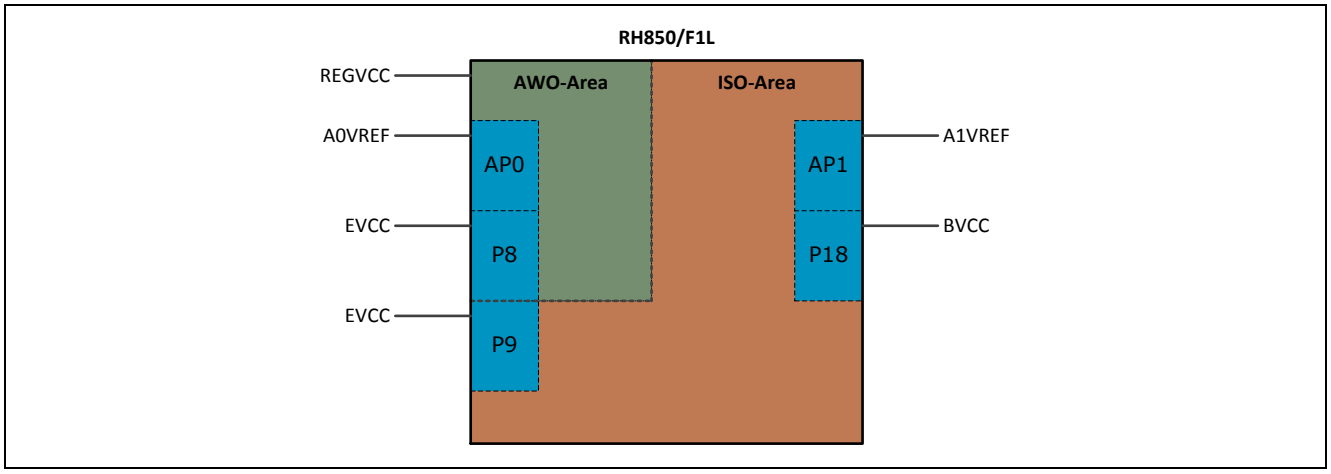


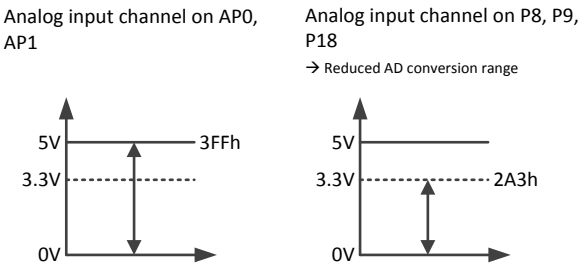
Figure 1 RH850/F1L Power supply architecture

Case 1 – Single Supply 5V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Case 2 – Single Supply 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Case 3 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V
Limitation	Analog port function limitation applies to P18
→	Operation permitted

Case 4 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	Common condition REGVCC = EVCC not met
→	Operation not permitted

Case 5 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9 and P18
→	Operation permitted

Case 6 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with digital function only P9 – Port usable with digital function only AP1 – Port usable with analog or digital function P18 – Port usable with digital function only
Limitation	No limitation applies to P8, P9 and P18 when these ports are used as digital port only.
→	Operation permitted

Case 7 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V
Limitation	Analog port function limitation applies to P8, P9 and P18.
→	Operation permitted

2.1.4 Power Supply Timing of RH850/F1L Group

The RH850/F1L group has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms.

For details on the electrical characteristics, please refer to the corresponding device data sheet.

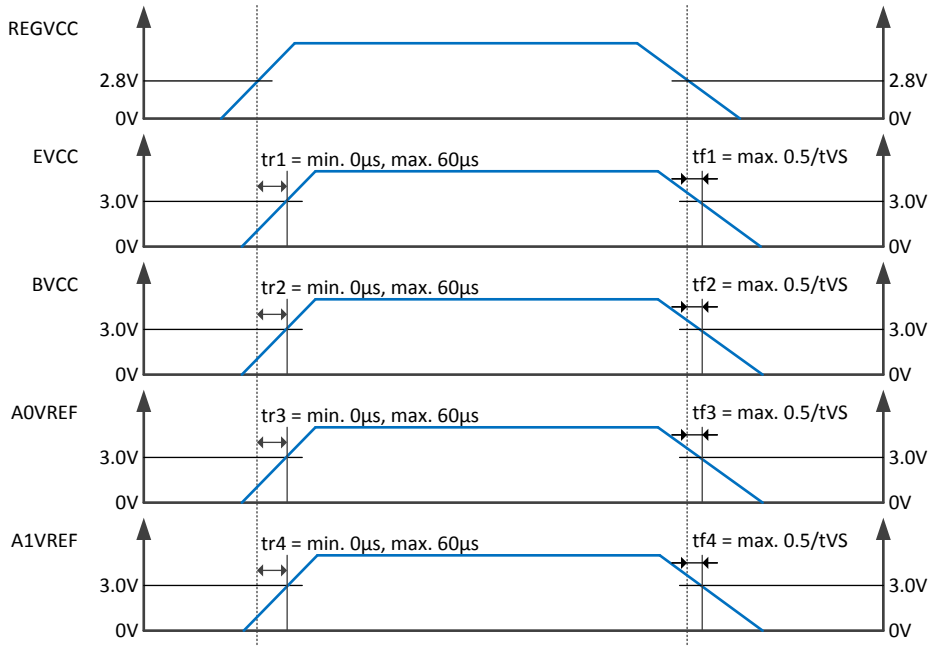


Figure 2 RH850/F1L Power up/down timing

Note: tVS is the timing of the voltage slope

2.2 Power Supply Overview of RH850/F1M Group

2.2.1 Power Supply Pin Overview of RH850/F1M Group

The devices of the RH850/F1M group have the following power supply pins.

Device	Power Supply Pins
RH850/F1M-233pin	REGVCC EVCC, EVSS BVCC, BVSS AnVREF, AnVSS (n = 0, 1)
RH850/F1M-176pin	REGVCC EVCC, EVSS BVCC, BVSS AnVREF, AnVSS (n = 0, 1)
RH850/F1M-144pin	REGVCC EVCC, EVSS BVCC, BVSS AnVREF, AnVSS (n = 0, 1)

The pins AWOVCL, AWOVSS and ISOVCL, ISOVSS are available on all devices to connect external capacitors.

2.2.2 Power Supply Pin Configuration of RH850/F1M Group

Depending on the device, the following power supply pin configuration applies:

The EVCC supply pins are internally connected.

The BVCC supply pins are internally connected.

2.2.3 Power Supply Pin Architecture of RH850/F1M Group

The RH850/F1M group supports different power supply architectures. The power supply architecture depends on the chosen RH850/F1M group device, application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1M group:

- REGVCC = EVCC = VPOC to 5.5V
- BVCC = VPOC to REGVCC
- A0VREF = 3.0V to 5.5V
- A1VREF = 3.0V to 5.5V
- AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

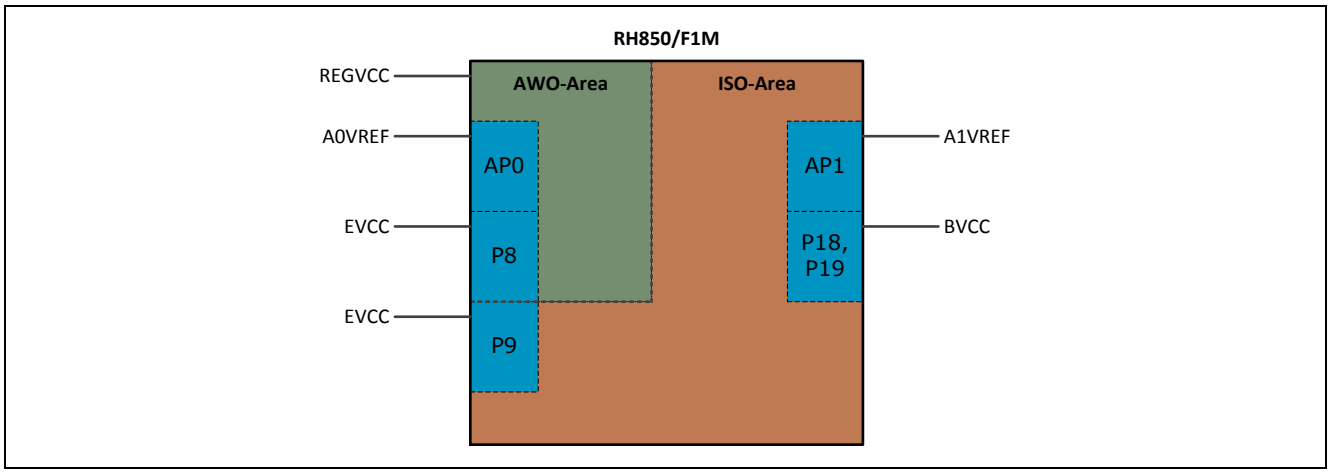


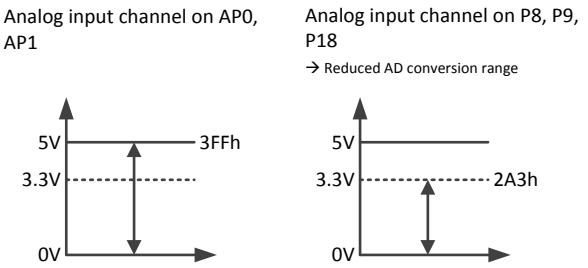
Figure 3 RH850/F1M Power supply architecture

Case 1 – Single Supply 5V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Case 2 – Single Supply 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Case 3 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V
Limitation	Analog port function limitation applies to P18
→	Operation permitted

Case 4 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function
Limitation	Common condition REGVCC = EVCC not met
→	Operation not permitted

Case 5 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9 and P18
→	Operation permitted

Case 6 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with digital function only P9 – Port usable with digital function only AP1 – Port usable with analog or digital function P18 – Port usable with digital function only
Limitation	No limitation applies to P8, P9 and P18 when these ports are used as digital port only.
→	Operation permitted

Case 7 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V
Limitation	Analog port function limitation applies to P8, P9 and P18.
→	Operation permitted

2.2.4 Power Supply Timing of RH850/F1M Group

The RH850/F1M group has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms.

For details on the electrical characteristics, please refer to the corresponding device data sheet.

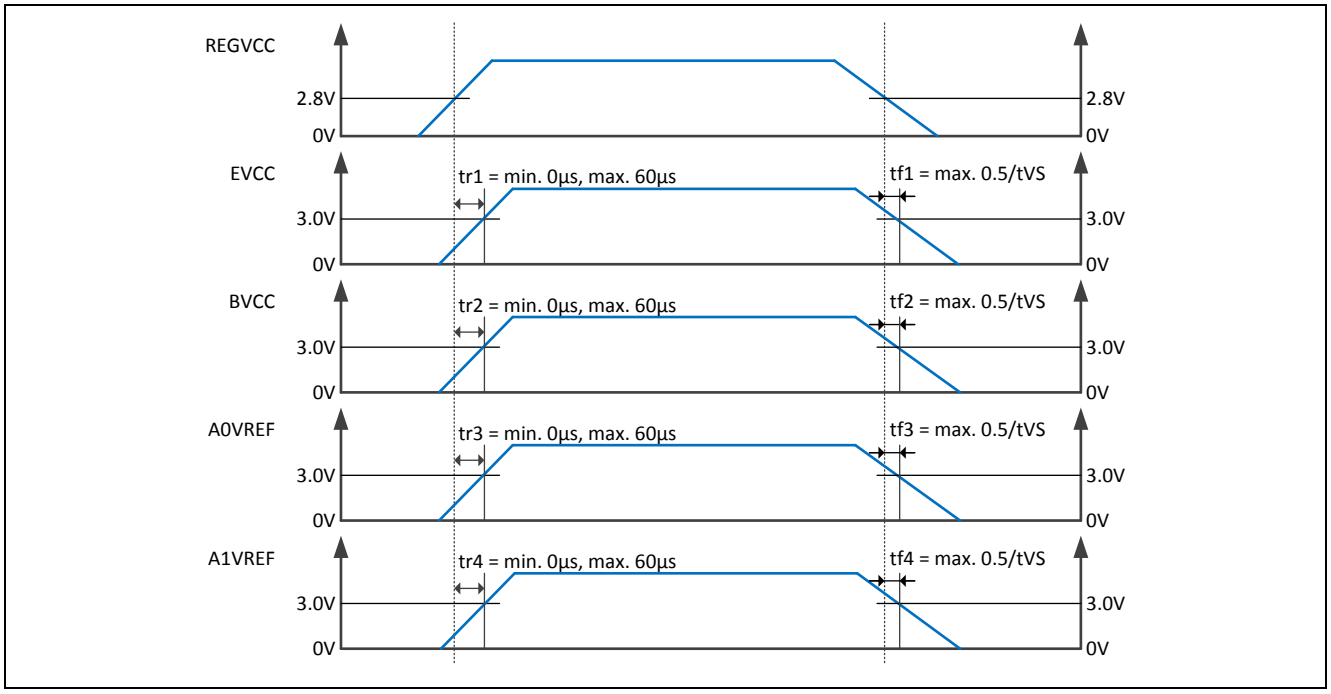


Figure 4 RH850/F1M Power up/down timing

Note: tVS is the timing of the voltage slope

2.3 Power Supply Overview of RH850/F1H Group

2.3.1 Power Supply Pin Overview of RH850/F1H Group

The devices of the RH850/F1H group have the following power supply pins.

Device	Power Supply Pins
RH850/F1H-272pin	REGVCC EVCC, EVSS BVCC, BVSS AnVREF, AnVSS (n = 0, 1) DVCC, DVSS (Debug device with trace interface only)
RH850/F1H-233pin	REGVCC EVCC, EVSS BVCC, BVSS AnVREF, AnVSS (n = 0, 1)
RH850/F1H-176pin	REGVCC EVCC, EVSS BVCC, BVSS AnVREF, AnVSS (n = 0, 1)

The pins AWOVCL, AWOVSS and ISOVCL, ISOVSS are available on all devices to connect external capacitors.

2.3.2 Power Supply Pin Configuration of RH850/F1H Group

Depending on the device, the following power supply pin configuration applies:

The EVCC supply pins are internally connected.

The BVCC supply pins are internally connected.

The DVCC supply pins are internally connected **(available on debug device with trace interface only)**.

2.3.3 Power Supply Handling at RH850/F1H-272pin

The RH850/F1H-272pin device has a different power supply configuration from the mass production (MP) and the debug device version (with trace interface). This has to be considered when designing the power supply of the ECU.

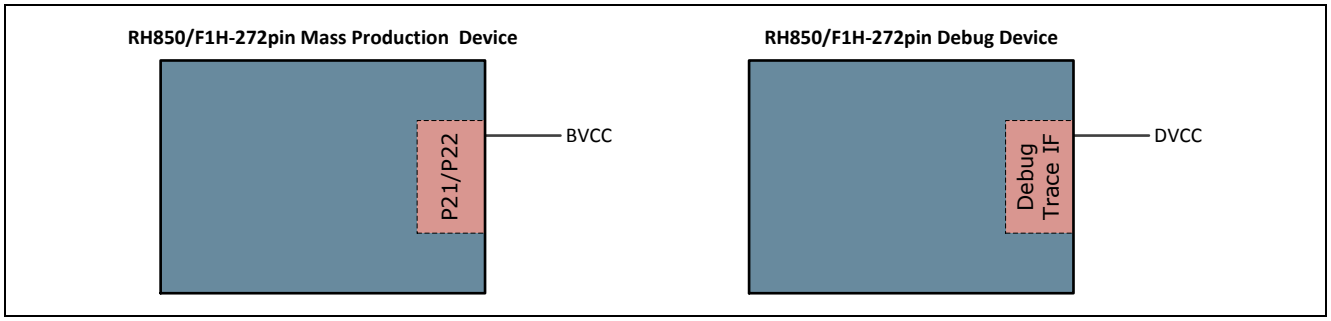


Figure 5 RH950/F1H-272pin Power supply pin difference between mass production and debug device

The following differences apply to the power supply of the RH850/F1H-272pin between the mass produciton (MP) device and the debug device with trace interface:

- Mass production device: BVCC = VPOC to REGVCC
- Debug device with trace interface: DVCC = 3.0V to 3.6V

When the RH850/F1H emulation adapter is used, the different supply voltage handling is already considered and realised.

2.3.4 Power Supply Pin Architecture of RH850/F1H Group

The RH850/F1H group supports different power supply architectures. The power supply architecture depends on the chosen RH850/F1H group device, application requirements and the use case.

Some common conditions apply to the supply of the RH850/F1H group:

- REGVCC = EVCC = VPOC to 5.5V
- BVCC = VPOC to REGVCC
- DVCC = 3.0V to 3.6V (available on debug device only)
- A0VREF = 3.0V to 5.5V
- A1VREF = 3.0V to 5.5V
- AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = DVSS = 0V

The following figure and the different cases describe the impact to the ADC ports and the ports with analog/digital function depending on the power supply architecture. In addition, it describes the limitations to these ports.

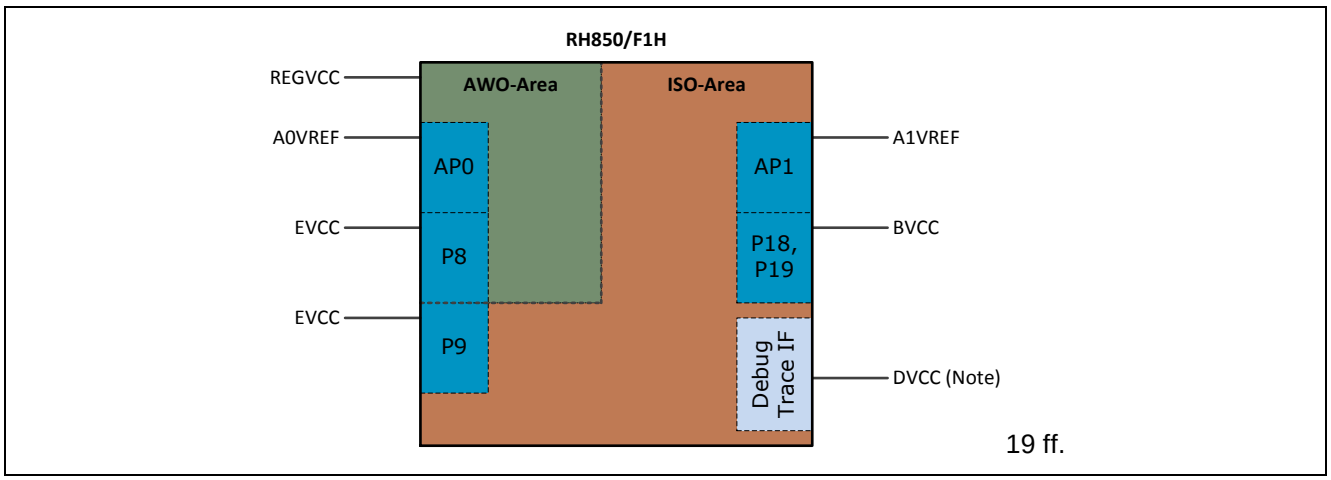


Figure 6 RH850/F1H Power supply architecture

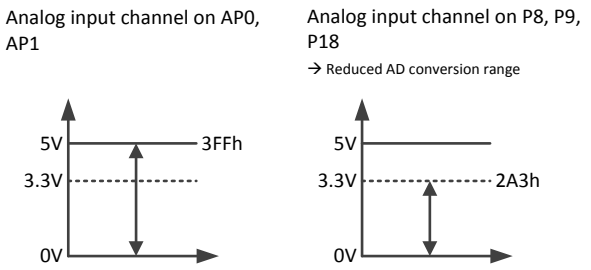
Note: The power supply pins DVCC are only available on the RH850/F1H (272pin) debug device. On the RH850/F1H (272pin) mass production device, these supply pins have to be connected and supplied by BVCC.

Case 1 – Single Supply 5V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Case 2 – Single Supply 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	No limitation applies
→	Operation permitted

Case 3 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V
Limitation	Analog port function limitation applies to P18 and P19
→	Operation permitted

Case 4 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function P9 – Port usable with analog or digital function AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function P19 – Port usable with analog or digital function
Limitation	Common condition REGVCC = EVCC not met
→	Operation not permitted

Case 5 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V, reduced AD conversion range between 0V to 3.3V  Note: Conversion range example based on 10-bit ADC resolution
Limitation	Analog port function limitation applies to P8, P9, P18 and P19
→	Operation permitted

Case 6 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 3.3V EVCC = 3.3V BVCC = 3.3V A0VREF = 5V A1VREF = 5V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with digital function only P9 – Port usable with digital function only AP1 – Port usable with analog or digital function P18 – Port usable with digital function only P19 – Port usable with digital function only
Limitation	No limitation applies to P8, P9, P18 and P19 when these ports are used as digital port only.
→	Operation permitted

Case 7 – Mixed Supply 5V & 3.3V	
Condition	REGVCC = 5V EVCC = 5V BVCC = 5V A0VREF = 3.3V A1VREF = 3.3V
Port Function	AP0 – Port usable with analog or digital function P8 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V P9 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V AP1 – Port usable with analog or digital function P18 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V P19 – Port usable with analog or digital function, analog input voltage limited to max. 3.3V
Limitation	Analog port function limitation applies to P8, P9, P18 and P19.
→	Operation permitted

2.3.5 Power Supply Timing of RH850/F1H Group

The RH850/F1H group has a recommended power supply timing.

The voltage slope of the different power supply pins is defined with min. 0.02V/ms and max. 500V/ms.

For details on the electrical characteristics, please refer to the corresponding device data sheet.

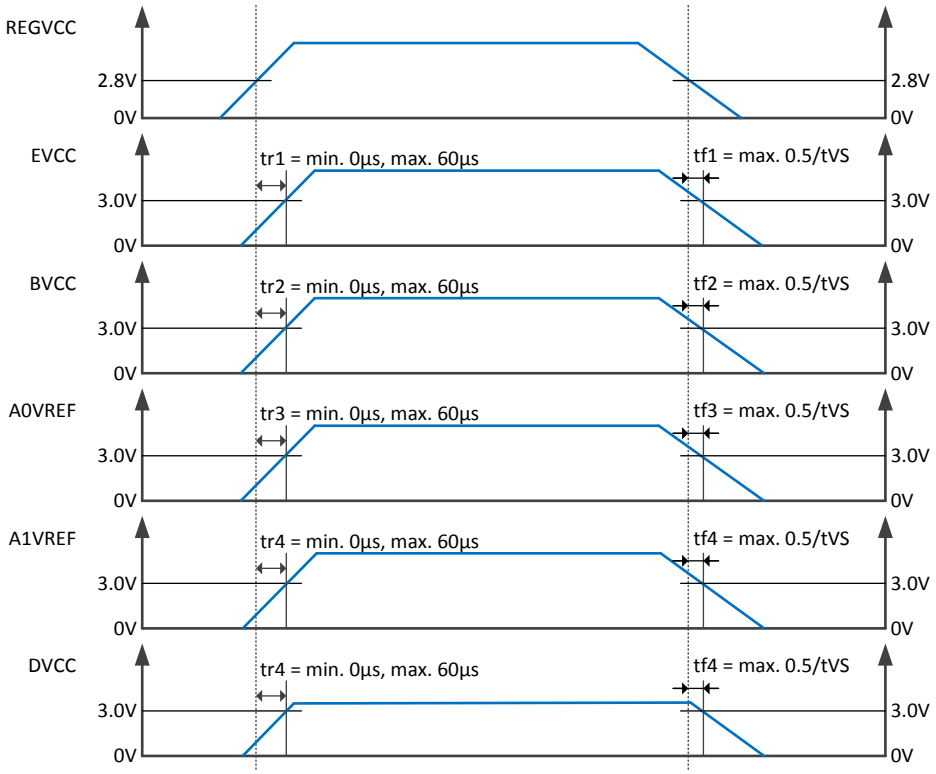


Figure 7 RH850/F1H Power up/down timing

Note: 1. tVS is the timing of the voltage slope

2. The power supply DVCC is only available on the RH850/F1H (272 pin) debug device (with trace interface). On the RH850/F1H (272pin) mass production device, these supply pins have to be connected and supplied by BVCC.

2.4 Principle Capacitor Placement at REGVCC of RH850/F1x Series

When the data flash of the RH850/F1x series will be used in the application it should be considered to add an additional capacitor to the REGVCC pin and to use a close component placement to the supply pin in order to optimize the EMI noise behaviour during the program and erase operation of the data flash.

The following recommendations shall be considered for the capacitor placement of the additional capacitor for EMI optimization during data flash operation at the REGVCC pin:

- Capacitor: 4.7µF to 10µF
- Pin: REGVCC
- Layout/distance: Capacitor within 10mm from mounting pad

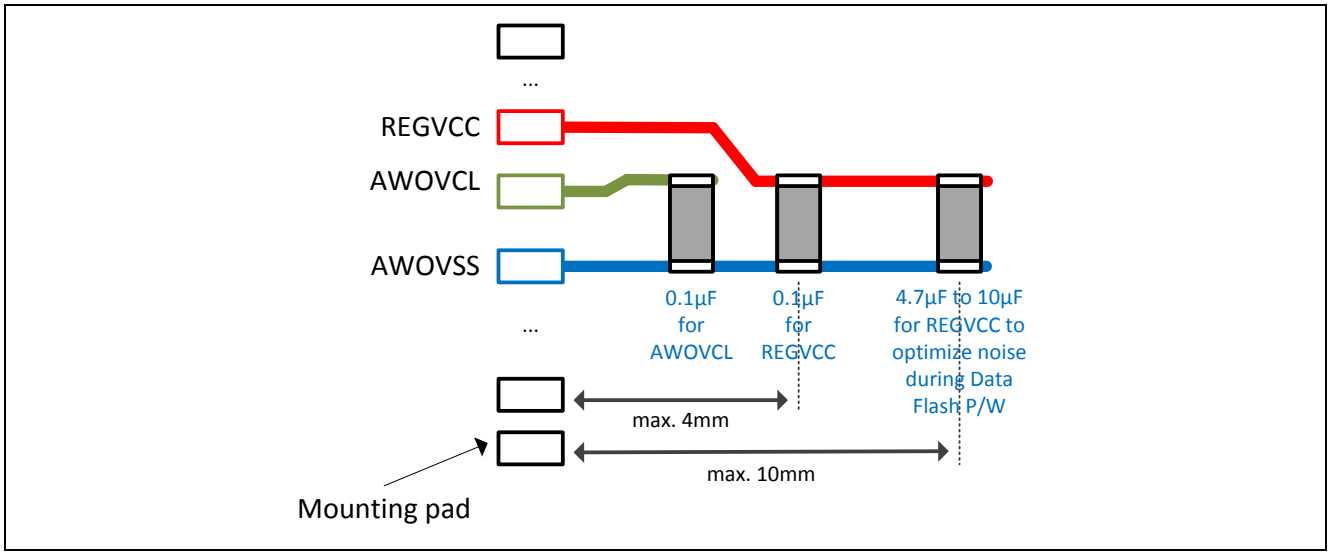


Figure 8 Principle capacitor placement at REGVCC for EMI at data flash operation

3. Minimum External Components

The RH850/F1x series requires a certain number of external connections and components for proper operation. The components are shown in different categories depending on the device operation and the use case.

3.1 Minimum External Components of RH850/F1L Group

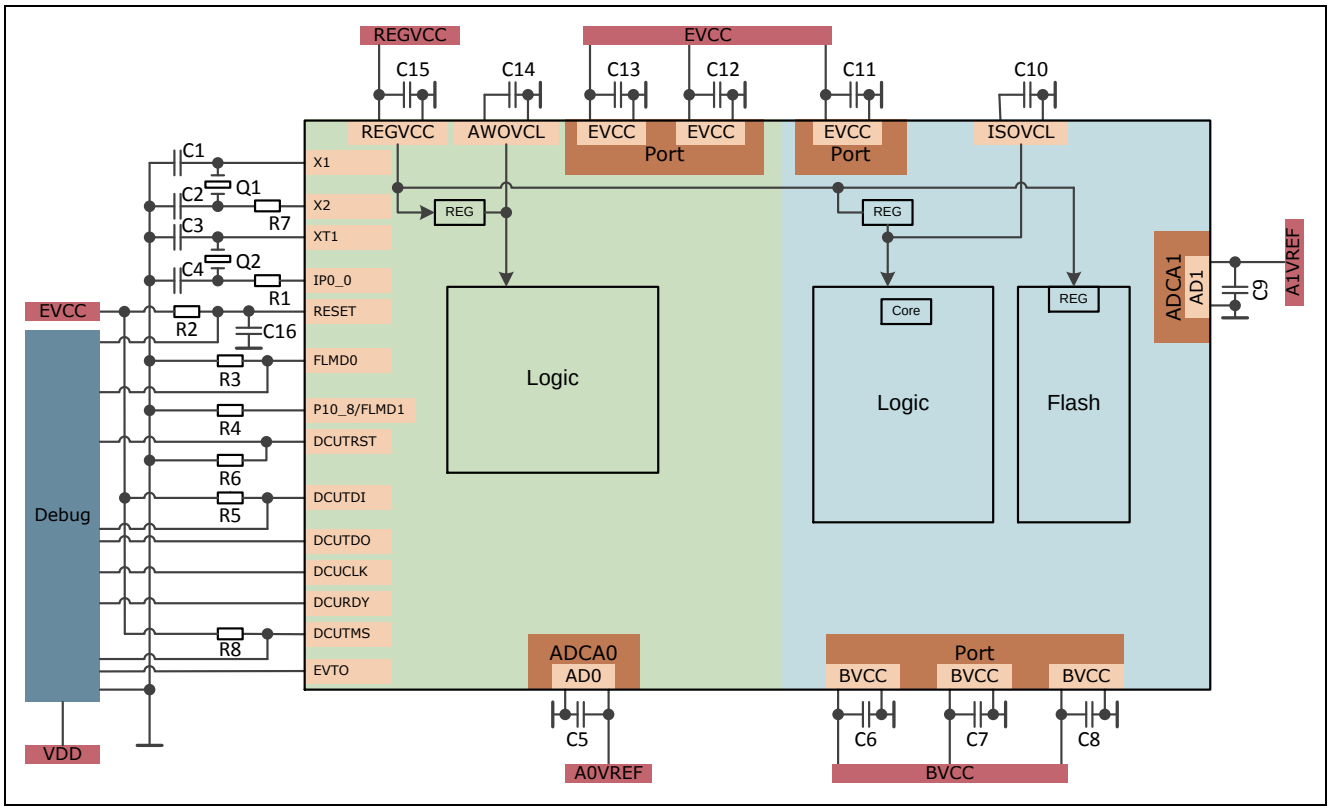


Figure 9 Minimum external components for RH850/F1L-176pin

Note: The debug interface connections shown covers Nexus, LPD 1pin and LPD 4pin. For details of the single debug connection, please refer to the corresponding debug interface connection chapter. For details of other external components, refer to their related chapters.

Component	Value			Category
	Min.	Typ.	Max.	
Q1	8MHz	-	24MHz	Typical
Q2	-	32.768kHz	-	Typical
R1	-	100kΩ Note 1	-	Typical
R2	1kΩ Note 3	4.7kΩ Note 3	6.6kΩ Note 3	Required
R3	95kΩ Note 6	100kΩ Note 7	105kΩ Note 6	Required
R4	-	10kΩ Note 5, 7	-	Typical
R5	-	1k to 4.7kΩ Note 4, 7, 8	-	Typical
R6	10kΩ Note 9	-	100kΩ Note 9	Required
R7	-	0Ω Note 1	-	Typical
R8	-	Optional Note 10	-	Typical
C1, C2	-	10pF Note 1	-	Typical
C3, C4	-	12pF Note 1	-	Typical
C5, C6, C7, C8, C9, C11, C12, C13, C15	-	100nF Note 2	-	Recommended
C10, C14	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required
C16	-	1nF to 10nF Note 3	-	Recommended

Notes 1. The shown values for reference only.
The final values must be evaluated (with the resonator manufacturer).

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the device datasheet.

3. See chapter RESET for details.

4. For values much smaller than the typical values, the connected devices might not be able to apply a low level to the signal. Additionally higher currents will flow through the resistor / device.

5. A low level must be applied to FLMD1 in case FLMD0 becomes ‘1’ for external flash programming.

   As a minimum value, a direct connection to VSS *can* be applied. *But* in case the related port (P10_8) is switched to output ‘1’, it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (E1) is not able to apply a high (‘1’) signal.

7. For values much higher than the typical value, the required signal timings might not be achieved due to the weaker currents. Additionally environmental effects (e.g. moisture and dirt) might generate other weak currents and therefore influence the signal.

8. See chapter Development and Test Tool Interface for details.

9. See chapter JP0_4/_DCUTRST and chapter Recommended Connection of Unused Pins for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See chapter Development and Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

In order to improve the electromagnetic interference and susceptibility it is recommended to add a capacitor of 4.7µF to 10µF in parallel to the capacitor C15 at REGVCC. The value of the parallel capacitor depends on the application requirements.

3.2 Minimum External Components of RH850/F1M Group

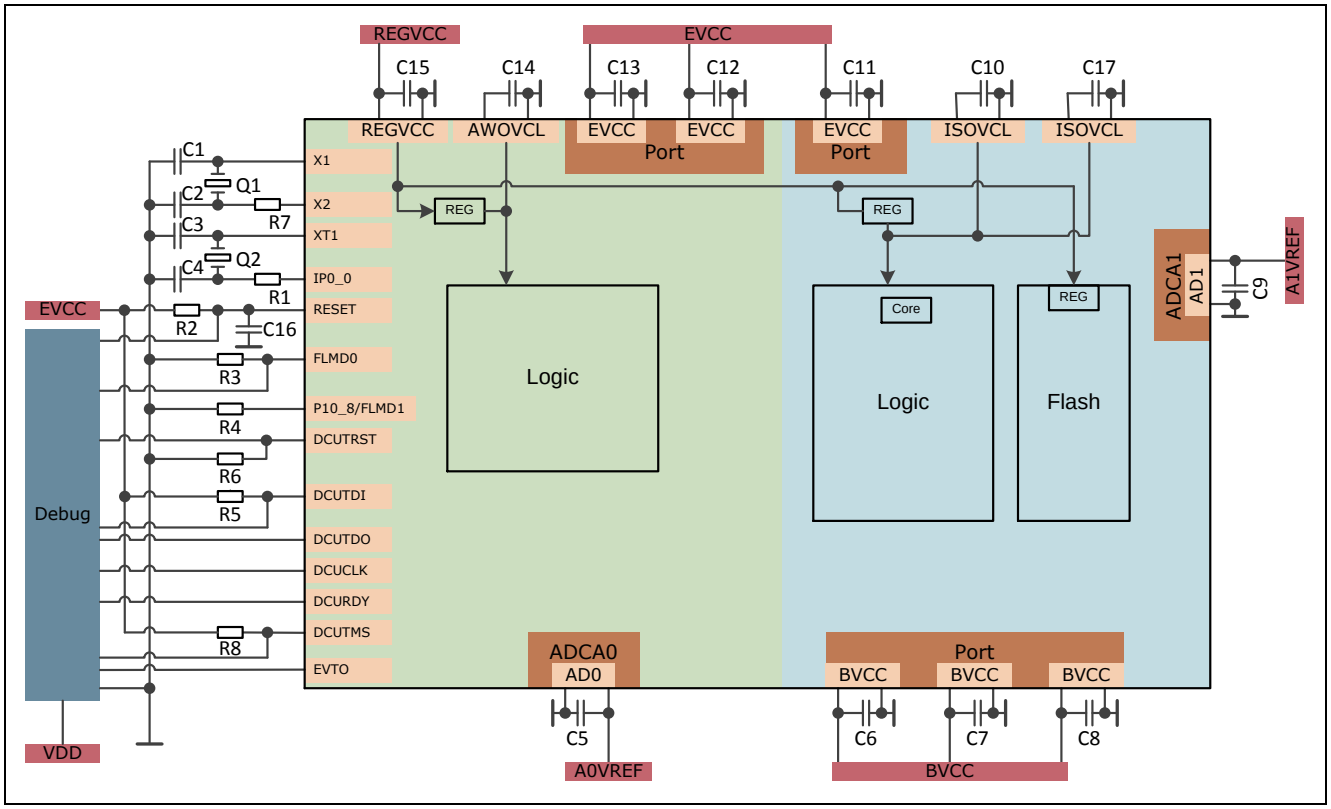


Figure 10 Minimum external components for RH850/F1M-233pin

Note: The debug interface connections shown covers Nexus, LPD 1pin and LPD 4pin. For details of the single debug connection, please refer to the corresponding debug interface connection chapter. For details of other external components, refer to their related chapters.

Component	Value			Category
	Min.	Typ.	Max.	
Q1	8MHz	-	24MHz	Typical
Q2	-	32.768kHz	-	Typical
R1	-	100kΩ[Note 1]	-	Typical
R2	1kΩ[Note 3]	4.7kΩ[Note 3]	6.6kΩ[Note 3]	Required
R3	86kΩ[Note 6]	100kΩ[Note 7]	105kΩ[Note 6]	Required
R4	-	10kΩ[Note 5, 7]	-	Typical
R5	-	1k to 4.7kΩ[Note 4, 7, 8]	-	Typical
R6	10kΩ[Note 9]	-	100kΩ[Note 9]	Required
R7	-	0Ω[Note 1]	-	Typical
R8	-	Optional[Note 10]	-	Typical
C1, C2	-	10pF[Note 1]	-	Typical
C3, C4	-	12pF[Note 1]	-	Typical
C5, C6, C7, C8, C9, C11, C12, C13, C15	-	100nF[Note 2]	-	Recommended
C10, C14, C17	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required
C16	-	1nF to 10nF[Note 3]	-	Recommended

Notes 1. The shown values for reference only.
The final values must be evaluated (with the resonator manufacturer).

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the device datasheet.

3. See chapter RESET for details.

4. For values much smaller than the typical values, the connected devices might not be able to apply a low level to the signal. Additionally higher currents will flow through the resistor / device.

5. A low level must be applied to FLMD1 in case FLMD0 becomes '1' for external flash programming.

   As a minimum value, a direct connection to VSS *can* be applied. *But* in case the related port (P10_8) is switched to output '1', it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (E1) is not able to apply a high ('1') signal.

7. For values much higher than the typical value, the required signal timings might not be achieved due to the weaker currents. Additionally environmental effects (e.g. moisture and dirt) might generate other weak currents and therefore influence the signal.

8. See chapter Development and Test Tool Interface for details.

9. See chapter JP0_4/_DCUTRST and chapter Recommended Connection of Unused Pins for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See chapter Development and Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

In order to improve the electromagnetic interference and susceptibility it is recommended to add a capacitor of 4.7µF to 10µF in parallel to the capacitor C15 at REGVCC. The value of the parallel capacitor depends on the application requirements.

3.3 Minimum External Components of RH850/F1H Group

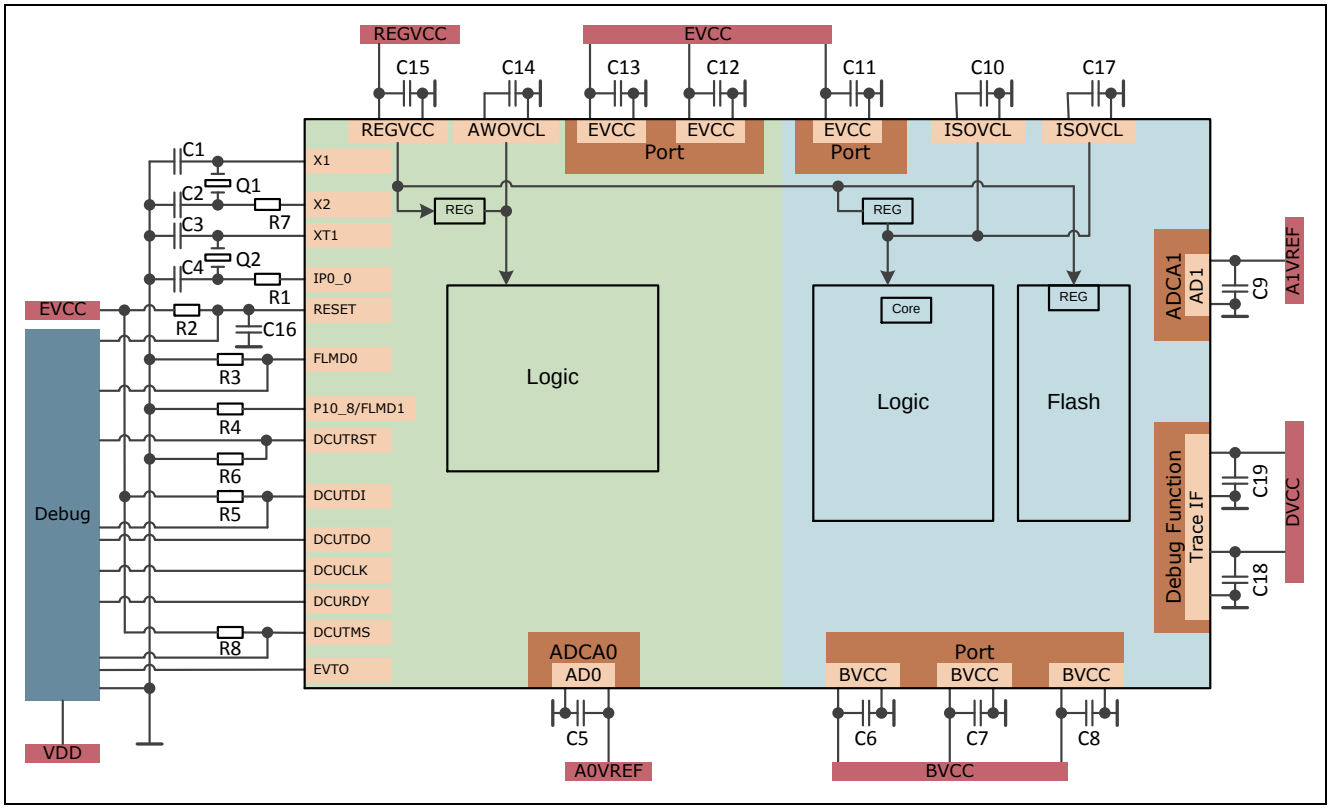


Figure 11 Minimum external components for RH850/F1H-272pin

Note: 1. The debug interface connections shown covers Nexus, LPD 1pin and LPD 4pin. For details of the single debug connection, please refer to the corresponding debug interface connection chapter. For details of other external components, refer to their related chapters.

2. The power supply pins DVCC are only available on the RH850/F1H (272pin) debug device. On the RH850/F1H (272pin) mass production device, these supply pins have to be connected to and supplied by BVCC.

Component	Value			Category
	Min.	Typ.	Max.	
Q1	8MHz	-	24MHz	Typical
Q2	-	32.768kHz	-	Typical
R1	-	100kΩ[Note 1]	-	Typical
R2	1kΩ[Note 3]	4.7kΩ[Note 3]	6.6kΩ[Note 3]	Required
R3	86kΩ[Note 6]	100kΩ[Note 7]	105kΩ[Note 6]	Required
R4	-	10kΩ[Note 5, 7]	-	Typical
R5	-	1k to 4.7kΩ[Note 4, 7, 8]	-	Typical
R6	10kΩ[Note 9]	-	100kΩ[Note 9]	Required
R7	-	0Ω[Note 1]	-	Typical
R8	-	Optional[Note 10]	-	Typical
C1, C2	-	10pF[Note 1]	-	Typical
C3, C4	-	12pF[Note 1]	-	Typical
C5, C6, C7, C8, C9, C11, C12, C13, C15, C18, C19	-	100nF[Note 2]	-	Recommended
C10, C14, C17	70nF ESR: max. 40 [mΩ]	100nF ESR: max. 40 [mΩ]	130nF ESR: max. 40 [mΩ]	Required
C16	-	1nF to 10nF[Note 3]	-	Recommended

Notes 1. The shown values for reference only.
The final values must be evaluated (with the resonator manufacturer).

2. The shown values are for reference only.
It must be ensured (by the schematic/PCB designer) that the voltage levels at the device pins always remain within the specified range of the device datasheet.

3. See chapter RESET for details.

4. For values much smaller than the typical values, the connected devices might not be able to apply a low level to the signal. Additionally higher currents will flow through the resistor / device.

5. A low level must be applied to FLMD1 in case FLMD0 becomes '1' for external flash programming.

   As a minimum value, a direct connection to VSS *can* be applied. *But* in case the related port (P10_8) is switched to output '1', it will damage the port/device.

6. In case of smaller values than the min. value, the typically connected device (E1) is not able to apply a high ('1') signal.

7. For values much higher than the typical value, the required signal timings might not be achieved due to the weaker currents. Additionally environmental effects (e.g. moisture and dirt) might generate other weak currents and therefore influence the signal.

8. See chapter Development and Test Tool Interface for details.

9. See chapter JP0_4/_DCUTRST and chapter Recommended Connection of Unused Pins for details.

10. The resistor is only required when the JTAG/Nexus interface is used for debugging and depends on the specification of the 3rd party development tool specification. See chapter Development and Test Tool Interface for details.

The definition of components categories is as follows:

- Required component

  Component that must be implemented as part of the device specification.

- Recommended component

  Component that is not required by the device specification, but is provided in order to secure the device operating conditions. The component value depends on the application requirements and must be evaluated with best engineering practice.

- Typical component

  Component that is not required by the device specification, but typically is provided in order to fulfil a use case. The component value depends on the application requirements and must be evaluated with best engineering practice.

In order to improve the electromagnetic interference and susceptibility it is recommended to add a capacitor of 4.7µF to 10µF in parallel to the capacitor C15 at REGVCC. The value of the parallel capacitor depends on the application requirements.

4. Oscillator

4.1 Recommended Oscillator Circuit

4.1.1 Main Oscillator

A crystal or ceramic resonator can be connected to the main clock input pins as shown below.

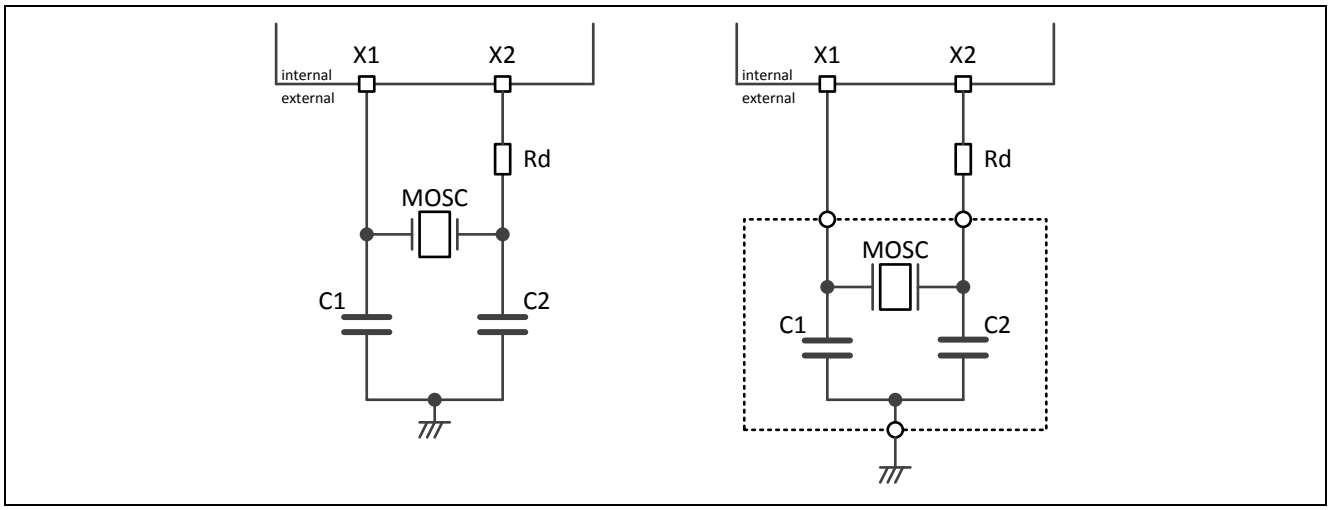


Figure 12 Recommended main oscillator circuit

General guidance values of the main oscillator circuit:

Component	Value
MOSC	8.00 to 24.00 MHz
C1	10pF
C2	10pF
Rd	0Ω

Caution

Values of C1, C2 and Rd depend on the use of ceramic or crystal resonator and must be specified in cooperation with ceramic or crystal resonator manufacturer.

4.1.2 Sub Oscillator

A crystal resonator can be connected to the sub clock input pins as shown below.

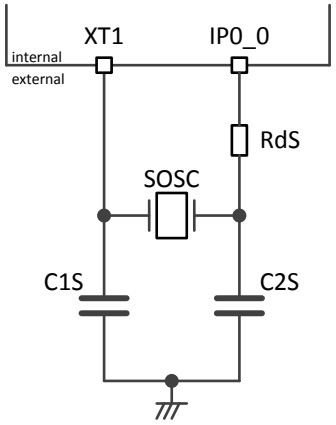


Figure 13 Recommended sub oscillator circuit

General guidance values of the sub oscillator circuit:

Component	Value
SOSC	32.768kHz
C1S	12pF
C2S	12pF
RdS	100kΩ

Caution

Values of C1S, C2S and RdS depend on the crystal resonator used and must be specified in cooperation with a crystal resonator manufacturer.

4.2 Recommended Oscillator Layout

General guidance for PCB layout:

- Keep the wiring length as short as possible
- Do not cross the wiring with other signal lines
- Do not route this circuit close to a signal line with high fluctuating current flow
- Always make the ground point of the oscillator capacitor the same potential as AWOVSS
- Do not ground the capacitor to a ground pattern with high current flow
- Do not tap signals from the oscillator

For further layout, related recommendations please refer to the application note “PCB-Design for Improved EMC” (R01AN0733EDxxxx).

5. Device Pins

5.1 RESET

5.1.1 Minimum RESET Circuit

The RH850/F1x series has an on-chip Power-on Clear (POC) circuit. Therefore, a specific external RESET circuit is not required and the minimum requirement of the RESET circuit is a resistor to EVCC for start-up of the device. The resistor should be dimensioned large enough to allow a RESET signal generated by development tool or flash programmer to control the RESET pin.

In addition, a capacitor should be added as protection against surges.

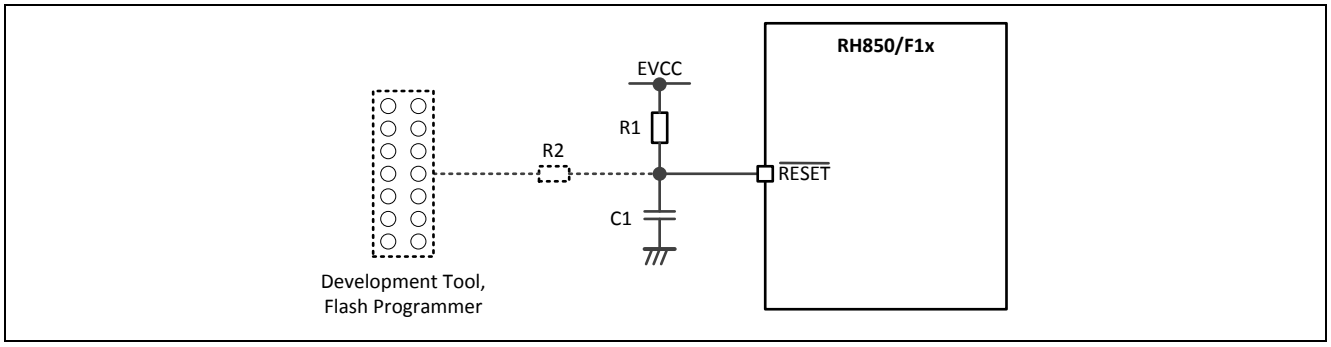


Figure 14 Minimum RESET circuit

General guidance values of the minimum RESET circuit:

Component	Value
R1	1 to 6.6kΩ
R2	100Ω
C1	1 to 10nF

The series resistor R2 is optional to suppress external signals from EMC point of view and depends on the application requirements.

The capacitor C1 can be adopted to a different value when the AC specification of the RESET (terminal) timing, the AC specification of the serial programmer setup timing and the EMC requirements of the ECU are fulfilled.

For further layout, related recommendations please refer to the application note “PCB-Design for Improved EMC” (R01AN0733EDxxxx).

5.1.2 RESET Input Characteristics

The RESET is passed through an internal analog noise filter to prevent erroneous resets due to spikes.

The following figure shows the timing when an external reset is performed. It explains the effect of the noise elimination.

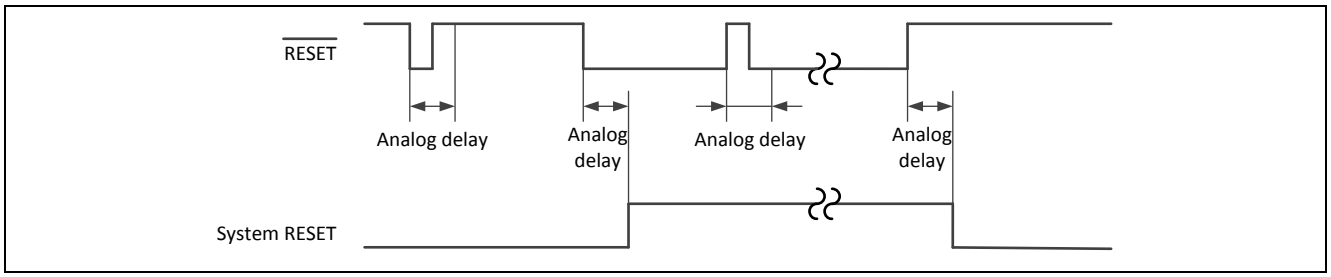


Figure 15 External RESET timing

The analog filter generates the analog delay. The filter regards pulses up to a certain width as noise and suppresses them.

For the minimum RESET pulse width, refer to the data sheet.

5.1.3 RESET Pin Input Characteristic during Power-On

During power-on of the device, an internal pull-down resistor is connected to the Pin / Terminal-RESET input until the internal state machine has finished initialization. The internal pull-down resistor is disabled automatically afterwards.

In case of a typical external circuit (like RC-combination) at the RESET pin, the voltage is rising with REGVCC. When the POC detection level is reached, a “plateau” phase occurs until the internal pull-down resistor is disabled and the charging curve of the RC-combination continues up to REGVCC.

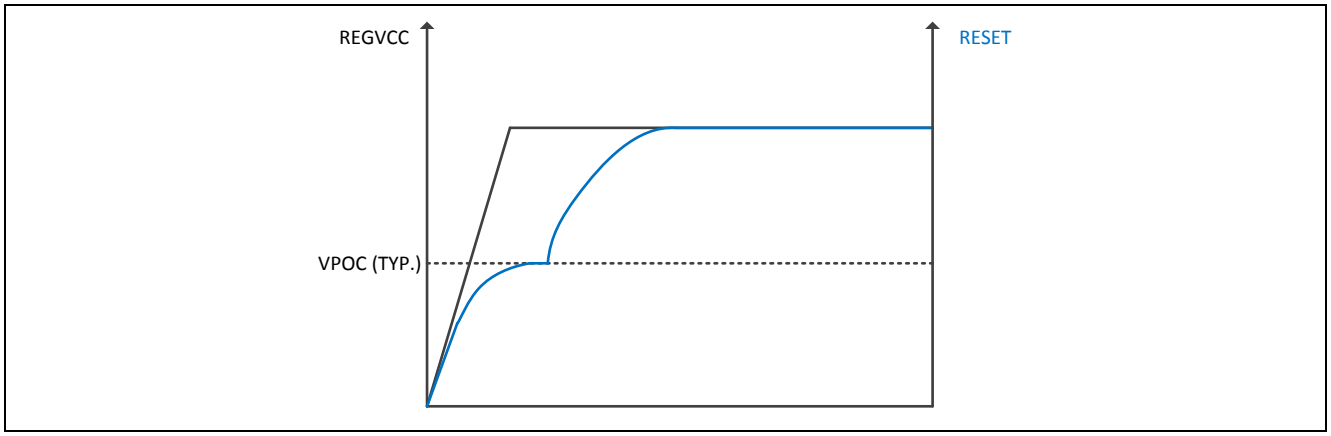


Figure 16 RESET Pin Input Behaviour at Power-on Clear

The shape of the signal curve at the RESET pin depends on the external circuit (e.g. use of reset generator, pull-up resistor, series resistor, series diode, etc.).

5.2 General Purpose I/O

5.2.1 RESET State of General Purpose I/O

During RESET state, all general-purpose I/O pins are in input mode with high-Z behaviour except the pin P0_0/_RESETOUT.

5.2.2 JP0_4/_DCUTRST

During power-on, RESET the pin JP0_4 should not be driven externally to high-level. Therefore, JP0_4/_DCUTRST has to be connected in all device operation modes to EVSS via a resistor.

5.2.3 P0_0/RESETOUT/CAN0TX/TAUD0I2/TAUD0O2/RLIN20RX/PWGA10O/DPO

P0_0 with alternate function

When P0_0 shall be used with an alternate function (e.g. CANTX, RLIN20RX, TAUD0O2, DPO, etc.) it has to be considered that the pin P0_0 is on low level after a Power-on RESET or any other device RESET source until it is released by the application software.

P0_0 and RESETOUT function

The pin P0_0 has an emulated RESETOUT function as default function. By this function, this pin drives an output low-level during and after reset, e.g. to reset an external ASIC. This function is realized by a special reset value of this pin being output mode by PM0_0=0, with an open-drain output buffer by PODC0_0=1 and with the output value being low by P0_0=0. This function is effective for any kind of reset.

Until being disabled by a write protected register the pin P0_0 drives an output low-level.

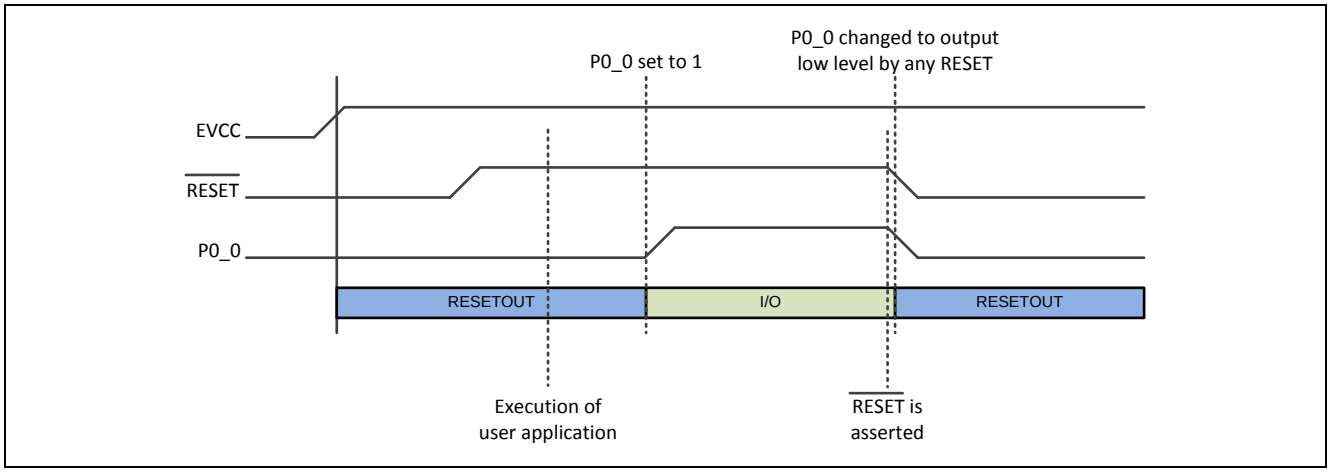


Figure 17 RESETOUT pin behaviour

Caution

Until being disabled by register settings, the pin P0_0 drives an output low-level after any kind of reset. To avoid a data collision, the outside circuit connected to the P0_0 pin must not drive high-level in any case.

5.2.4 Analog Filter Function

Depending on the alternative port functionality selected, some input signals of the device pins are passed through an analog filter - respectively analog delay stage - to remove noise and glitches from the input signal.

The detection level of the filtered input signal depends on the high-level/low-level input voltage of the port input buffer and its supported electrical characteristics.

After passing the external signal through an analog filter to eliminate noise and spikes, the event detection evaluates the level or any level change, i.e. an edge, of the signal and generates an output accordingly.

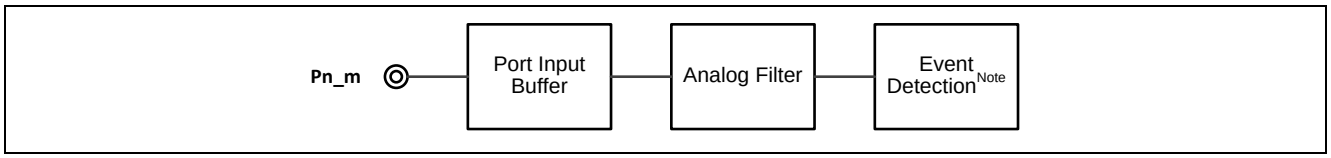


Figure 18 Analog Filter Function

Note: The event detection implementation depends on the analog filter type.

The input detection level as well as the pulse rejection of the analog filters are specified in the corresponding pin characteristics and peripheral chapters of the data sheet.

5.2.5 Behaviour during Low Power Mode

During the low power modes, different states apply for the ports and pins of the RH850/F1x series. The states depend on the chosen low-power mode and may not have the same behaviour for ports and pins.

- Port means that a pin works as a general-purpose input/output pin.
- Pin denotes the physical pin. Every pin is denoted by a unique pin number.

The following overview provides a summary of the port and pin behaviour during low-power modes:

	Always-on Area		Isolated Area	
	Ports	**Pins**	**Ports**	**Pins**
HALT Mode				
STOP Mode				
DEEP STOP Mode				
Cyclic RUN Mode				
Cyclic STOP Mode				

	Functional

	State before entering the mode is kept

	The ports are not powered and therefore not functional
	
	I/O hold function for isolated area
	• During the DEEP STOP mode, the state of the port pins on the isolated area can be held automatically. Thus, its input and/or output remain in the same state as before entering I/O buffer hold state. No external or internal signal can change its state until the I/O buffer hold state is terminated.
	• The I/O buffers in DEEP STOP mode are changing into I/O buffer hold state by default.
	• After the wake-up from DEEP STOP mode the I/O buffer hold state is terminated in the following steps:
	  ○ 1. Re-configure the peripheral or port function
	  ○ 2. Release I/O hold state by setting IOHOLD.IOHOLD = 0

5.3 Recommended Connection of unused Pins

5.3.1 Recommended Connection of unused Pins for RH850/F1L Group

Pin	Recommended Connection of Unused Pin
A0VREF, A1VREF	Connect to EVCC or BVCC
A0VSS, A1VSS	Connect to EVSS or BVSS
RESET	Connect to EVCC
XT1	Connect to AWOVSS
IP0_0/XT2	Leave open (IPIBC0.0 bit = 0) or connect to REGVCC or AWOVSS via a resistor (IPIBC0.0 bit = 1)
P0 (excluding P0_0) P1 P2 P8 P9 P20	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC of EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P0_0	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2 and P10_8) P11 P12 P18	Input state 48pin, 64, pin, 80pin and 100pin: - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC of EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) 144pin and 176pin: - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVCC of BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10_1 P10_2 P10_8	Input state 48pin, 64, pin, 80pin and 100pin: - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) 144pin and 176pin: - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open
AP1	Input state - Leave open (PIBCn_m = 0) - Connect to A1VREF or A1VSS via resistor (PIBCn_m = 1) Output state - Leave open
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note4
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note2	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Leave open Note3 _DCUTRST (JP0_4): Connect to EVSS via a resistor Note4 _DCURDY/LPDCLKOUT (JP0_5): Leave open _EVTO (JP0_6): Leave open

Notes
1. The pin availability depends on the selected device.
2. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, please refer to the chapter Debug Interface Connection.
3. A resistor between DCUTMS and EVCC is only required when the Nexus interface is used for debugging and depends on the 3rd party development tool specification.
4. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1L group, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

5.3.2 Recommended Connection of unused Pins for RH850/F1M Group

Pin	Recommended Connection of Unused Pin
A0VREF, A1VREF	Connect to EVCC or BVCC
A0VSS, A1VSS	Connect to EVSS or BVSS
RESET	Connect to EVCC
XT1	Connect to REGVCC or AWOVSS via a resistor (IPIBC0.0 bit = 1) or connect to AWOVSS (IPIBC0.0 bit = 0)Note5
IP0_0/XT2	Leave open (IPIBC0.0 bit = 0) or connect to REGVCC or AWOVSS via a resistor (IPIBC0.0 bit = 1)Note5
P0 (excluding P0_0) P1 P2 P8 P9 P20	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC of EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P0_0	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2 and P10_8) P11 P12 P13 P18 P19	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVCC of BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10_1 P10_2 P10_8	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open
AP1	Input state - Leave open (PIBCn_m = 0) - Connect to A1VREF or A1VSS via resistor (PIBCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note4
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note2	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Leave open Note3 _DCUTRST (JP0_4): Connect to EVSS via a resistor Note4 _DCURDY/LPDCLKOUT (JP0_5): Leave open _EVTO (JP0_6): Leave open

Notes
1. The pin availability depends on the selected device.
2. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, please refer to the chapter Debug Interface Connection.
3. A resistor between DCUTMS and EVCC is only required when the Nexus interface is used for debugging and depends on the 3rd party development tool specification.
4. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
5. XT1 is connected to IP0_0 (XT2) through an internal resistor. Therefore, it is necessary to maintain equal voltage level in order to avoid a current path.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1M group, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

5.3.3 Recommended Connection of unused Pins for RH850/F1H Group

Pin	Recommended Connection of Unused Pin
A0VREF, A1VREF	Connect to EVCC or BVCC
A0VSS, A1VSS	Connect to EVSS or BVSS
RESET	Connect to EVCC
XT1	Connect to REGVCC or AWOVSS via a resistor (IPIBC0.0 bit = 1) or connect to AWOVSS (IPIBC0.0 bit = 0)Note5
IP0_0/XT2	Leave open (IPIBC0.0 bit = 0) or connect to REGVCC or AWOVSS via a resistor (IPIBC0.0 bit = 1)Note5
P0 (excluding P0_0) P1 P2 P8 P9 P20	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC of EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P0_0	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10 (excluding P10_1, P10_2 and P10_8) P11 P12 P13 P18 P19	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVCC of BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
P10_1 P10_2 P10_8	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to BVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
AP0	Input state - Leave open (PIBCn_m = 0) - Connect to A0VREF or A0VSS via resistor (PIBCn_m = 1) Output state - Leave open
AP1	Input state - Leave open (PIBCn_m = 0) - Connect to A1VREF or A1VSS via resistor (PIBCn_m = 1) Output state - Leave open

Pin	Recommended Connection of Unused Pin
JP0 (excluding JP0_4) – **General-purpose I/O Mode**	Input state - Leave open (PIBCn_m = 0 and PMCn_m = 0) - Connect to EVCC or EVSS via resistor (PIBCn_m = 1 and PMCn_m = 1) Output state - Leave open
JP0_4 – **General-purpose I/O Mode**	Connect to EVSS via a resistor Note4
JP0 – **Debug Mode** (LPD IF / Nexus IF) Note2	DCUTDI/LPDI/LPDIO (JP0_0): Connect to EVCC via a resistor DCUTDO/LPDO (JP0_1): Leave open DCUTCK/LPDCLK (JP0_2): Leave open DCUTMS (JP0_3): Leave open Note3 _DCUTRST (JP0_4): Connect to EVSS via a resistor Note4 _DCURDY/LPDCLKOUT (JP0_5): Leave open _EVTO (JP0_6): Leave open
P21, P22 – **General purpose I/O Mode** (272pin mass production device)	Input state - Leave open (PIBCn_m = 0) - Connect to BVCC or BVSS via resistor (PIBCn_m = 1) Output state - Leave open
P21, P22 – **Debug Mode** (272pin debug device only)	_MSYN: Connect to DVCC via a resistor _DBINT: Connect to DVCC via a resistor MSEO0-1: Leave open MCKO: Leave open MDO0-15: Leave open

Notes
1. The pin availability depends on the selected device.
2. This part describes the handling of JP0 debug port pins during operation mode when the debug interface is not in operation. For details of the different interfaces, please refer to the chapter Debug Interface Connection.
3. A resistor between DCUTMS and EVCC is only required when the Nexus interface is used for debugging and depends on the 3rd party development tool specification.
4. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
5. XT1 is connected to IP0_0 (XT2) through an internal resistor. Therefore, it is necessary to maintain equal voltage level in order to avoid a current path.

Caution

When the debug mode is configured by OPBT0 on the RH850/F1H group, the corresponding pins of the JP0 port group are automatically switched to the selected debug interface. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function. Port usage details are described in the debug interface connection chapter.

5.4 Pin Assignment Differences

The pin assignment of the RH850/F1L-176pin, RH850/F1M-176pin and the RH850/F1H-176pin shows some differences because of to the fact that the RH850/F1M-176 and the RH850/F1H-176pin require additional pins for the external capacitor of the internal voltage regulator on the ISO area.

RH850/F1L-176pin	RH850/F1M-176pin		RH850/F1H-176pin	
Pin Assignment	**Pin Assignment**	**New Assignment of Alternate Functions**	**Pin Assignment**	**New Assignment of Alternate Functions**
P9_5 / CSIH0CSS6 / PWGA34O / TAUJ1I1 / TAUJ1O1 / ADCA0I12S	ISOVCL	P0_8 / RLIN21TX / DPIN6 / CSIH0CSS6 / CSIH1SSI / TAUB0I2 / TAUB0O2 / CAN3TX	ISOVCL	P0_8 / RLIN21TX / DPIN6 / CSIH0CSS6 / CSIH1SSI / TAUB0I2 / TAUB0O2 / CAN3TX
		P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / PWGA34O		P0_11 / RIIC0SDA / DPIN12 / CSIH1CSS2 / TAUB0I8 / TAUB0O8 / RLIN26RX / PWGA34O
		P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / ADCA0I10S		P9_3 / KR0I7 / PWGA21O / CSIH2CSS3 / TAUJ1I1 / TAUJ1O1 / ADCA0I10S
P9_6 / CSIH0CSS7 / PWGA35O / ADCA0I13S	ISOVSS	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O	ISOVSS	P0_6 / INTP2 / DPIN10 / SELDP2 / CSIH1SC / PWGA35O
		P11_1 / CSIH2SSI / FLX0TXDA / RLIN20RX / CSIH0CSS7 / PWGA26O / TAUB0I13 / TAUB0O13		P11_1 / CSIH2SSI / FLX0TXDA / RLIN20RX / CSIH0CSS7 / PWGA26O / TAUB0I13 / TAUB0O13 / MEMC0AD9

Note: The analog functionality (ADCA0I12S and ADCA0I13S) of the pins P9_5 and P9_6 of the RH850/F1L-176pin are not available on the RH850/F1M-176pin and the RH850/F1H-176pin.

5.5 Injected Current

The RH850/F1x series has different electrical characteristics for the injected current depending on the pin group and device pins of the different package variants.

For details, please refer to the corresponding product data sheet.

6. A/D-Converter

6.1 Conversion Time

The ADC conversion time consists of a number of timing parameters, which are summed-up to get the conversion timing depending on the application.

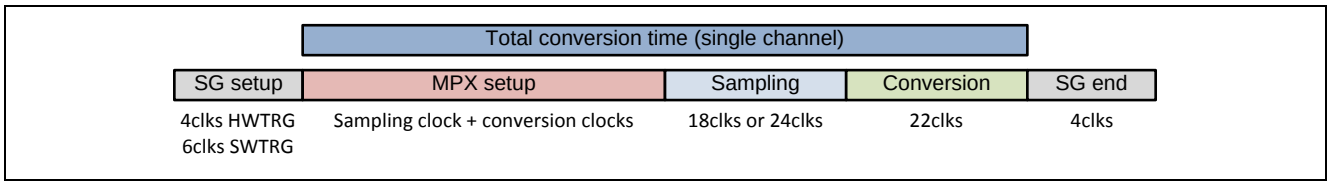


Figure 19 ADC conversion time

Notes: 1. SG - Scan Group
2. MPX - External multiplexer
3. HWTRG - Hardware trigger
4. SWTRG - Software trigger

The setting of the ADC clock and the sampling time results in the following conversion timing:

ADCLK [MHz]	Sampling time [clks]	MPX Setup time [µs]	Conversion time [µs]	Sampling time [µs]	Total conversion time (excluding MPX) [µs]	Total conversion time (including MPX) [µs]
40	24	1.15	0.55	0.60	1.15	2.30
32	18	1.25	0.69	0.56	1.25	2.50
32	24	1.44	0.69	0.75	1.44	2.88
24	18	1.67	0.92	0.75	1.67	3.33
24	24	1.92	0.92	1.00	1.92	3.83
8	18	5.00	2.75	2.25	5.00	10.00
8	24	5.75	2.75	3.00	5.75	11.50

Note: The sampling time is set by the ADCAnSMPCR.SMPT [7:0] bits.

6.2 External Multiplexer Wait Time

When an external multiplexer is used to extend the number of analogue input channels, a fixed wait time/set-up time of one conversion time has to be taken into account.

6.3 Equivalent Input Circuit

The A/D-converters have different options for the input with track & hold path or direct path only. Please refer to the user's manual, which A/D-converter is supported by the chosen device.

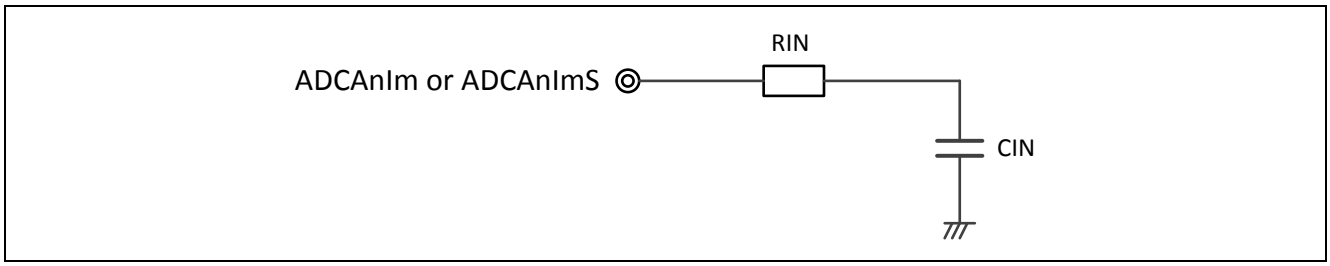


Figure 20 ADC equivalent input circuit

The ADC equivalent input circuit is given in the following tables according to the related RH850/F1x series product or group:

1.) RH850/F1L (176), RH850/F1L (144)

ADCA0			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA0I0 to ADCA0I5	Channel T&H is not used	5.0	2.1
ADCA0I0 to ADCA0I5	Channel T&H is used	14.1	2.2
ADCA0I6 to ADCA0I15		5.0	2.1
ADCA0I0S to ADCA0I3S, ADCA0I5S to ADCA0I16S		7.2	8.4
ADCA0I4S, ADCA0I17S to ADCA0I19S		10	8.4

ADCA1			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA1I0 to ADCA1I15		4.3	3.1
ADCA1I0S to ADCA1I17S		5.6	6.2

Caution

This specification is not tested during outgoing inspection. Therefore, RIN and CIN are reference values only and not guaranteed. In addition, these values are specified as maximum values.

2.) RH850/F1L (100), RH850/F1L (80), RH850/F1L (64), RH850/F1L (48)

ADCA0			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA0I0 to ADCA0I5	Channel T&H is not used	4.6	2.1
ADCA0I0 to ADCA0I5	Channel T&H is used	14.1	2.2
ADCA0I6 to ADCA0I15		4.6	2.1
ADCA0I0S to ADCA0I3S, ADCA0I5S to ADCA0I16S		6.8	8.8
ADCA0I4S, ADCA0I17S to ADCA0I19S		9.4	8.8

Caution

This specification is not tested during outgoing inspection. Therefore, RIN and CIN are reference values only and not guaranteed. In addition, these values are specified as maximum values.

3.) RH850/F1M

ADCA0			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA0I0 to ADCA0I5	Channel T&H is not used	4.5	2.2
ADCA0I0 to ADCA0I5	Channel T&H is used	13.9	2.6
ADCA0I6 to ADCA0I15		4.5	2.2
ADCA0I0S to ADCA0I3S, ADCA0I5S to ADCA0I11S, ADCA0I14S toADCA0I16S		6.1	9.4
ADCA0I4S, ADCA0I17S to ADCA0I19S		8.8	9.4

ADCA1			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA1I0 to ADCA1I15		4.2	2.2
ADCA1I0S to ADCA1I10S		8.3	8.5
ADCA1I11S to ADCA1I19S		6.0	8.6

Caution

This specification is not tested during outgoing inspection. Therefore, RIN and CIN are reference values only and not guaranteed. In addition, these values are specified as maximum values.

4.) RH850/F1H

ADCA0			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA0I0 to ADCA0I5	Channel T&H is not used	5.1	2.2
ADCA0I0 to ADCA0I5	Channel T&H is used	13.9	2.6
ADCA0I6 to ADCA0I15		5.1	2.2
ADCA0I0S to ADCA0I3S, ADCA0I5S to ADCA0I11S, ADCA0I14S to ADCA0I16S		6.1	9.4
ADCA0I4S, ADCA0I17S to ADCA0I19S		8.8	9.4

ADCA1			
Terminals	**Condition**	**RIN [kΩ]**	**CIN [pF]**
ADCA1I0 to ADCA1I15		4.5	2.2
ADCA1I0S to ADCA1I10S		8.3	8.5
ADCA1I11S to ADCA1I19S		6.0	8.6

Caution

This specification is not tested during outgoing inspection. Therefore, RIN and CIN are reference values only and not guaranteed. In addition, these values are specified as maximum values.

6.4 External Circuit on ADC Input

To preserve the accuracy of the A/D-converter, it is recommended that analog input pins have a low impedance. Therefore placing a capacitor at the analog input pin can provide an effective result. This capacitor contributes to noise filtering on the analog input pin. A basic filter can be realised by using a series resistor with a capacitor on the input pin (RC-filter).

The filter at the input pins should be designed taking into account the dynamic characteristics of the input signal, the equivalent input impedance of the ADC itself and the injected current specification of the analog input pins.

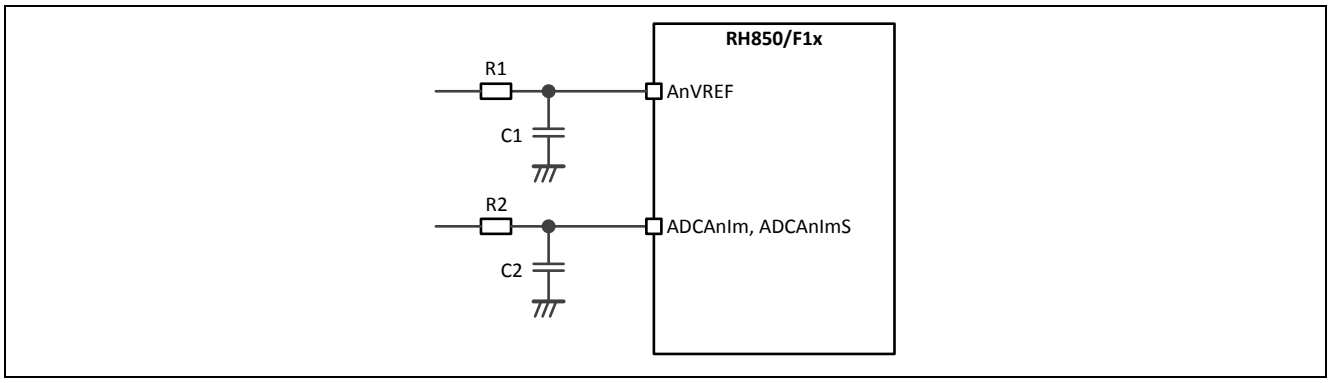


Figure 21 ADC external circuit on analog input

Note:	RH850/F1L (max. device group configuration)	n = 0, m = 0 to 15, 0S to 19S
		n = 1, m = 0 to 15, 0S to 7S
	RH850/F1M (max. device group configuration)	n = 0, m = 0 to 15, 0S to 11S, 14S to 17S
		n = 1, m = 0 to 15, 0S to 19S
	RH850/F1H (max. device group configuration)	n = 0, m = 0 to 15, 0S to 11S, 14S to 17S
		n = 1, m = 0 to 15, 0S to 19S

General guidance values of the basic external ADC input circuit:

Component	Value
R1	2.2 to 6.8Ω
R2	10kΩ
C1	100nF
C2	10nF

The values of the resistor and capacitor depend on the application requirements.

In order to improve the electromagnetic susceptibility it should be considered to add a series resistor (R1) to the supply line of AnVREF. The combination of series resistor and capacitor (C1) placed close to the supply pin AnVREF helps to improve the resistance against electromagnetic disturbance.

The resistor value influences the conversion accuracy and depends on the application requirements.

In order to improve the accuracy of the ADC it is recommended to add a capacitor of minimum 2µF (typical 4.7µF) in parallel to the capacitor C1 at AnVREF. The value of the parallel capacitor depends on the application requirements.

As guide line for the calculation of the external capacitor at the analog input pin the formula based on the internal equivalent capacitance and the ADC resolution of the corresponding AD-converter channel can be used:

$$Cexternal = CIN \times 2^{ADCresolution}$$

Cexternal: External capacitor at the analog input pin

CIN: Equivalent input capacitance

ADCresolution: AD-converter resolution for RH850/F1x either 12-bit or 10-bit resolution

7. Development and Test Tool Interface

The RH850/F1x series supports the following operation modes that are used for debugging, flash programming and test by using boundary scan.

FLMD0	P10_8 (FLMD1)	P10_1 (MODE0)	P10_2 (MODE1)	Operation Mode
0	x	x	x	Normal operation mode
1	0	x	x	Flash programming mode
1	1	0	1	Boundary scan mode

Note: x – Don't care

Operating Mode	Mode Description
Normal operating mode	Mode used for the execution of application software and during debugging.
Flash programming mode	Mode used during the flash memory program/erase of the device.
Boundary scan mode	Mode used for boundary scan test

7.1 Development Tool Interface of RH850/F1L Group

7.1.1 Debug Interface Connection of RH850/F1L Group

For the debugging environment, the following interface connections are supported:

- 1pin Low-pin debug interface (1pin LPD)
- 4pin Low-pin debug interface (4pin LPD)
- Nexus interface
  - The Nexus interface is only supported by 3rd party development tools.

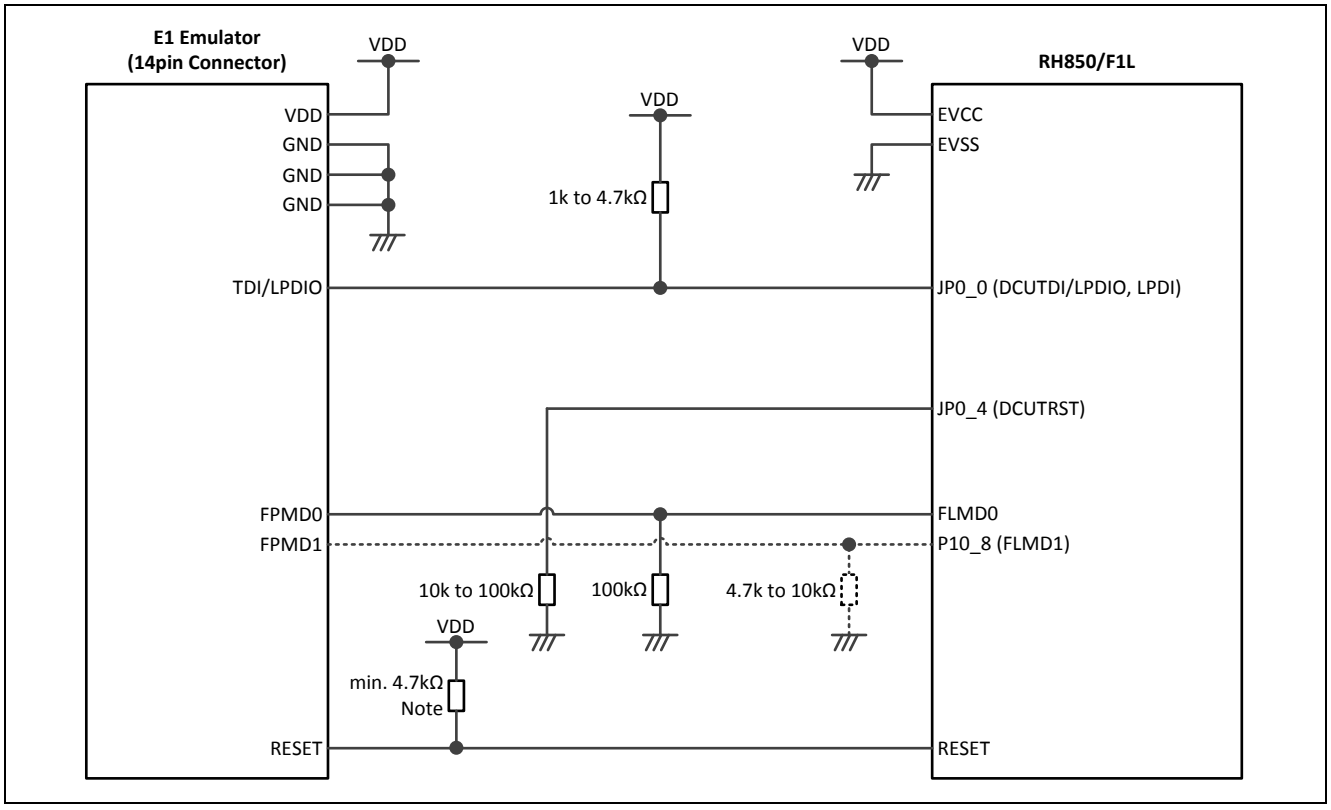


Figure 22 RH850/F1L 1pin Low-pin debug interface connection

Note: The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 1pin debug mode is used on the RH850/F1L group, the port of the JP0 port group is automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDIO input/output
- JP0_1: General-purpose I/O
- JP0_2: General-purpose I/O
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: General-purpose I/O
- JP0_6: General-purpose I/O

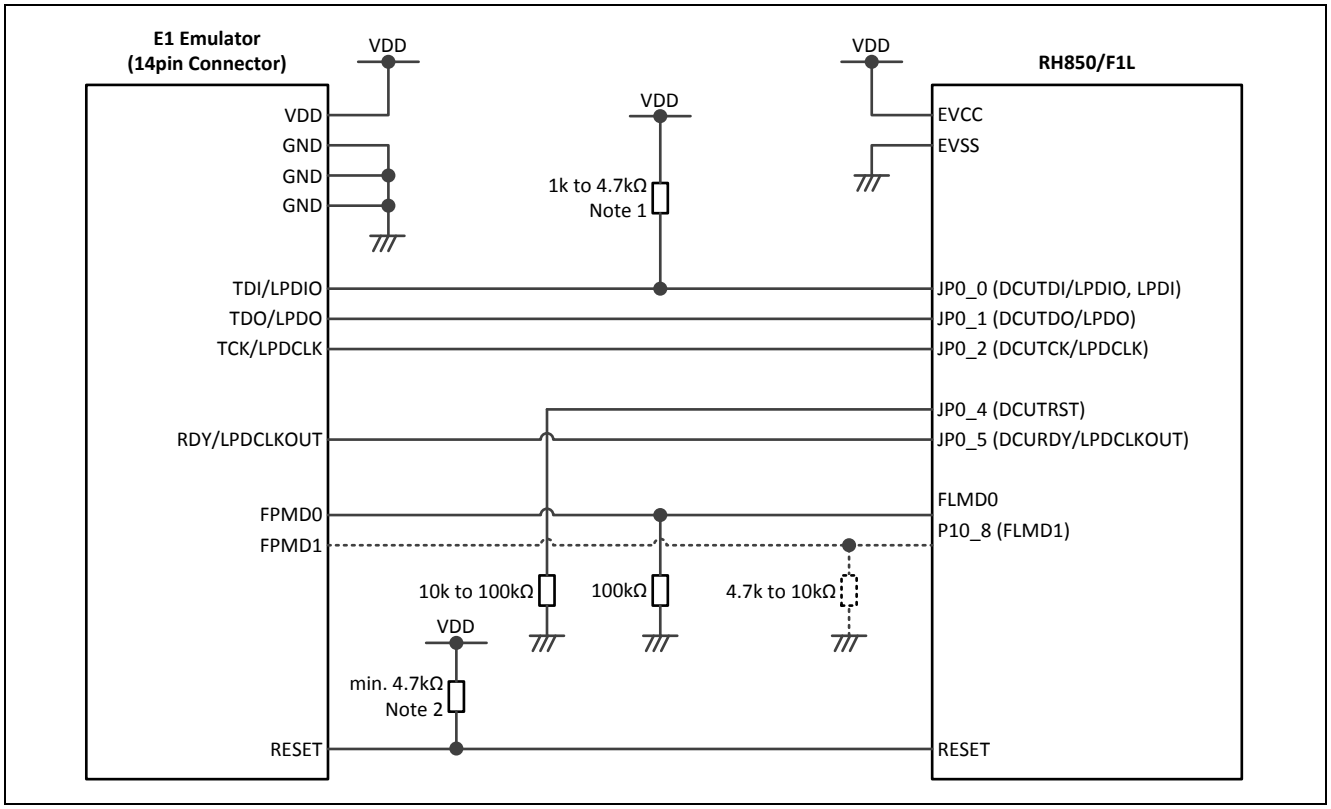


Figure 23 RH850/F1L 4pin Low-pin debug interface connection

Notes: 1. The resistor is optional in 4pin low-pin debug mode.

2. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 4pin debug mode is used on the RH850/F1L group, the ports of the JP0 port group are automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDI input
- JP0_1: LPDO output
- JP0_2: LPDCLK input
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: LPDCLKOUT output
- JP0_6: General-purpose I/O

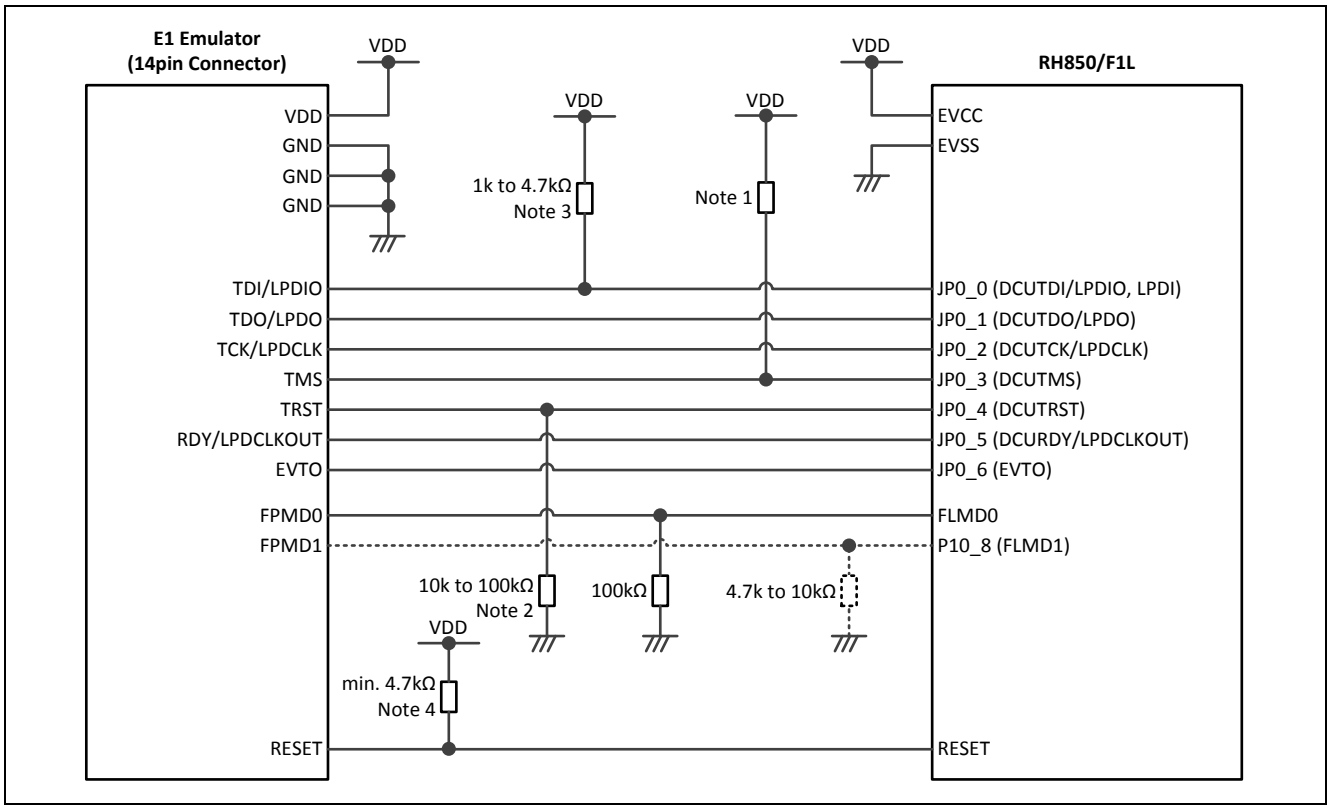


Figure 24 RH850/F1L Nexus, 4pin LPD and 1pin LPD debug interface connection

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the 4pin low-pin debug mode is used
4. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the Nexus debug mode is used on the RH850/F1L group, the ports of the JP0 port group are automatically switched to the debug interface mode.

- JP0_0: DCUTDI input
- JP0_1: DCUTDO output
- JP0_2: DCUTCK input
- JP0_3: DCUTMS input
- JP0_4: DCUTRST input
- JP0_5: DCUTRDY output
- JP0_6: EVTO

The debug interface signal connection of the E1 interface is given in the table below:

E1 Interface Connector	E1 Interface Signal	F1L Device Pin
1	LPDCLK/(DCUTCK)	JP0_2
2	GND	EVSS
3	(DCUTRST)	JP0_4
4	FPMD0/FLMD0	FLMD0
5	LPDO/(DCUTDO)	JP0_1
6	FPMD1	FLMD1
7	LPDI/LPDIO/(DCUTDI)	JP0_0
8	VDD	EVCC
9	(DCUTMS)	JP0_3
10	(EVTO)	JP0_6
11	LPDCLKOUT/(DCURDY)	JP0_5
12	GND	EVSS
13	RESET	RESET
14	GND	EVSS

Note: The Nexus interface signals marked with (*text*) are supported by 3rd party development tools and not by E1 emulator.

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

7.1.2 Flash Programming Interface Connection of RH850/F1L Group

For the programming environment the following connections are supported

- Single-wire asynchronous flash programming interface
- Two-wire asynchronous flash programming interface
- Synchronous flash programming interface

Flash Programming Interface	Function	F1L Device Pins
1-wire UART	RxD/TxD	JP0_0
2-wire UART	RxD	JP0_0
	TxD	JP0_1
CSI	SI	JP0_0
	SO	JP0_1
	SCK	JP0_2

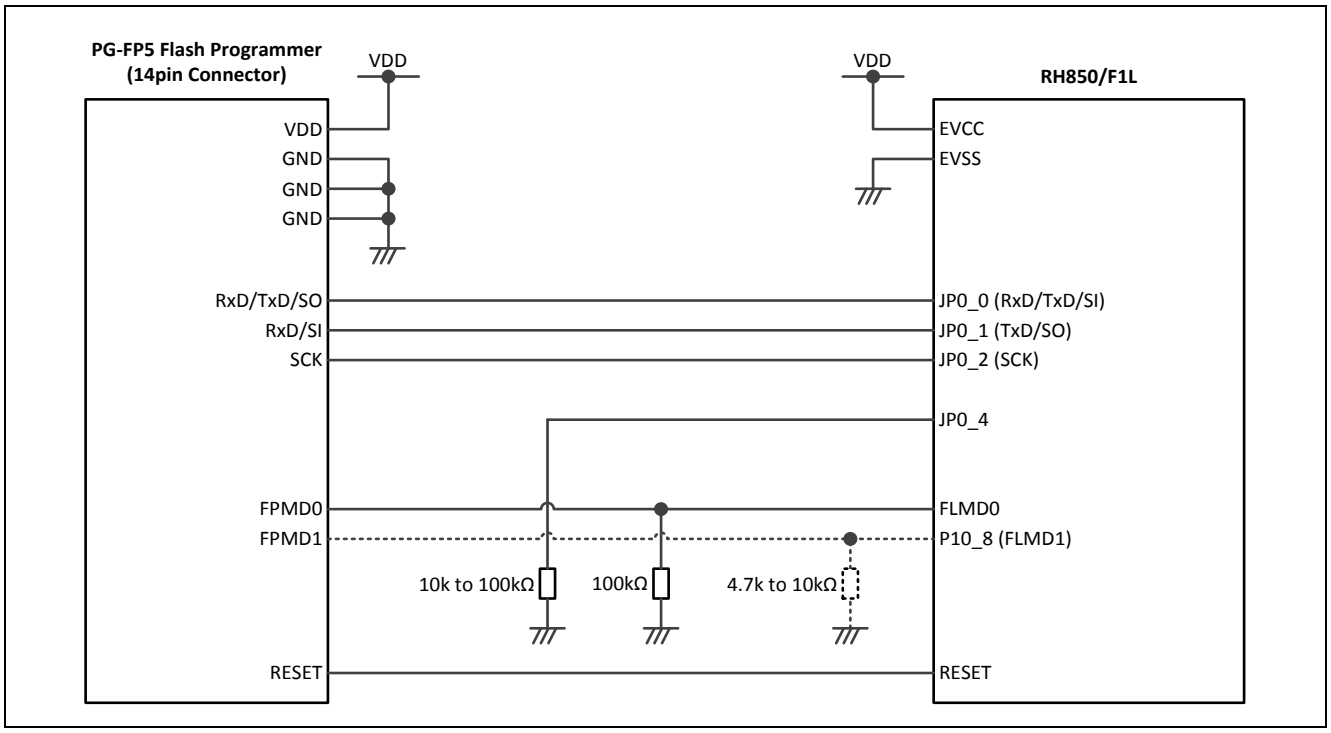


Figure 25 RH850/F1L PG-FP5 flash programming interface connection

The flash programming signal connection of the PG-FP5 interface is given in the table below:

PG-FP5 Interface Connector	PG-FP5 Signal	F1L Device Pin
1	SCK	JP0_2
2	GND	EVSS
3	-	-
4	FPMD0	FLMD0
5	SI/RxD	JP0_1
6	FPMD1	FLMD1
7	SO/TxD	JP0_0
8	VDD	EVCC
9	-	-
10	-	-
11	-	-
12	GND	EVSS
13	RESET	RESET
14	-	-

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

7.1.3 Combined Debug and Flash Programming Interface Connection of RH850/F1L Group

The following figure describes the combined connections for debugging and flash programming of the RH850/F1L group, supporting

- 1pin Low-pin debug interface (1pin LPD)
- 4pin Low-pin debug interface (4pin LPD)
- Nexus interface
- Single-wire asynchronous flash programming interface with PG-FP5
- Two-wire asynchronous flash programming interface with PG-FP5
- Synchronous flash programming interface with PG-FP5

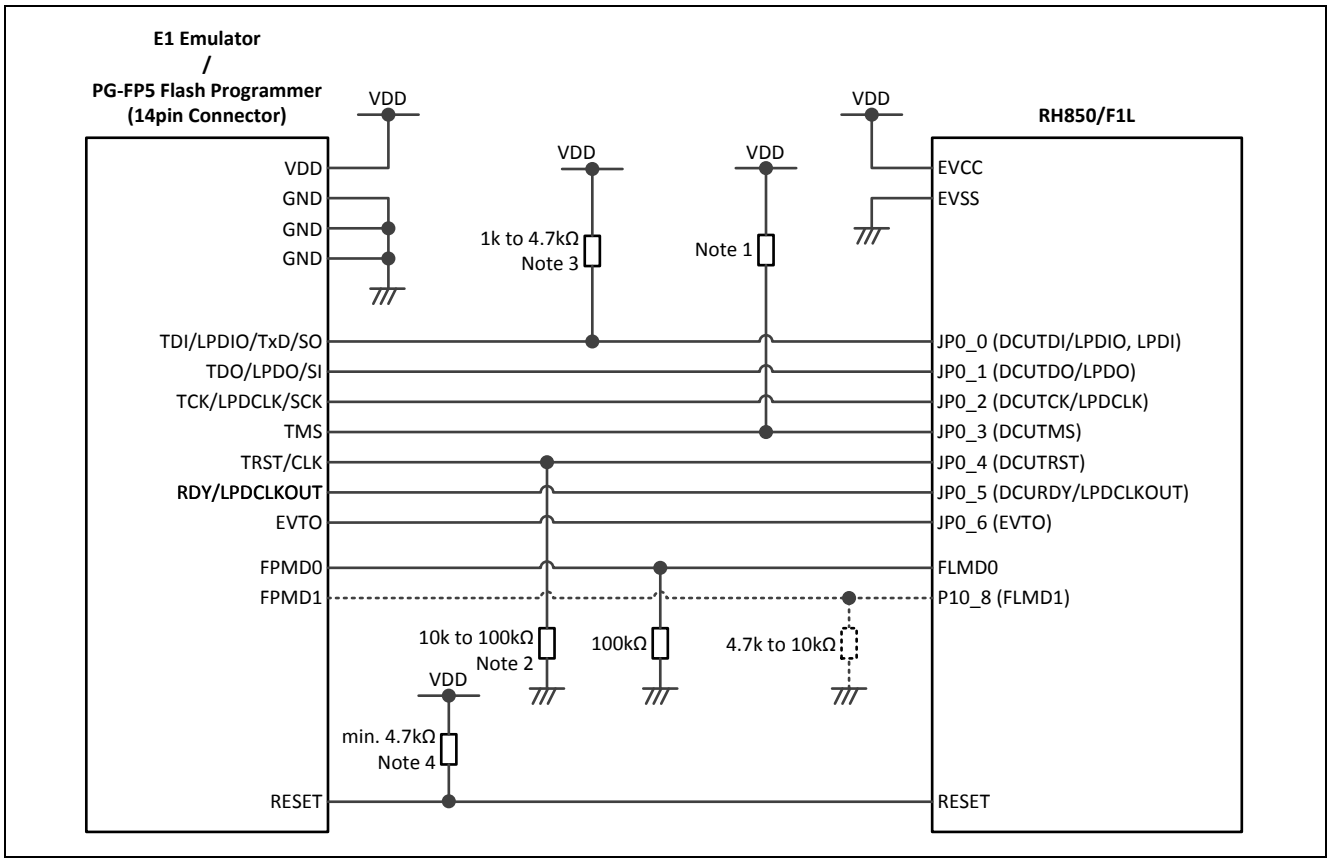


Figure 26 RH850/F1L Combined debug and flash programming interface connections

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the 4pin low-pin debug mode is used
4. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

7.2 Development Tool Interface of RH850/F1M Group

7.2.1 Debug Interface Connection of RH850/F1M Group

For the debugging environment, the following interface connections are supported:

- 1pin Low-pin debug interface (1pin LPD)
- 4pin Low-pin debug interface (4pin LPD)
- Nexus interface
  - The Nexus interface is only supported by 3rd party development tools.

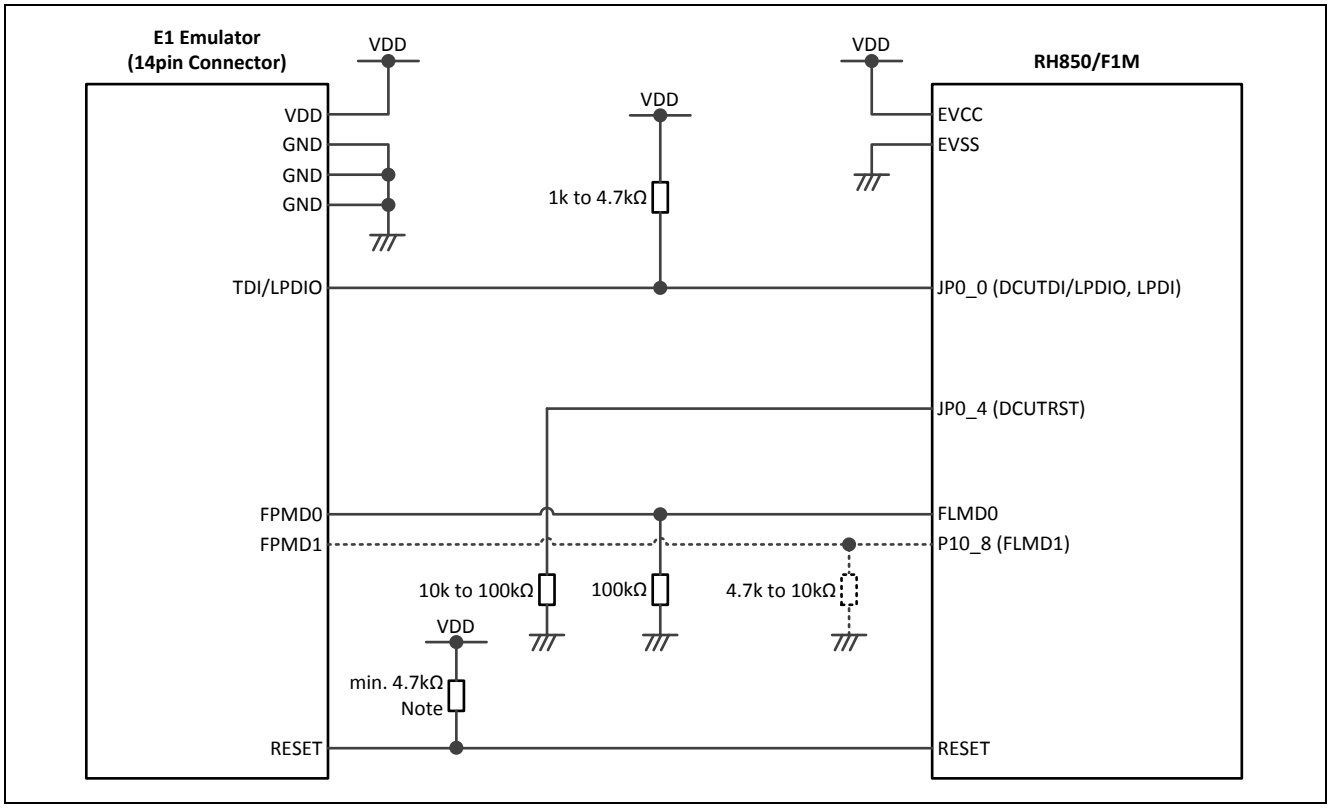


Figure 27 RH850/F1M 1pin Low-pin debug interface connection

Note: The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 1pin debug mode is used on the RH850/F1M group, the port of the JP0 port group is automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDIO input/output
- JP0_1: General-purpose I/O
- JP0_2: General-purpose I/O
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: General-purpose I/O
- JP0_6: General-purpose I/O

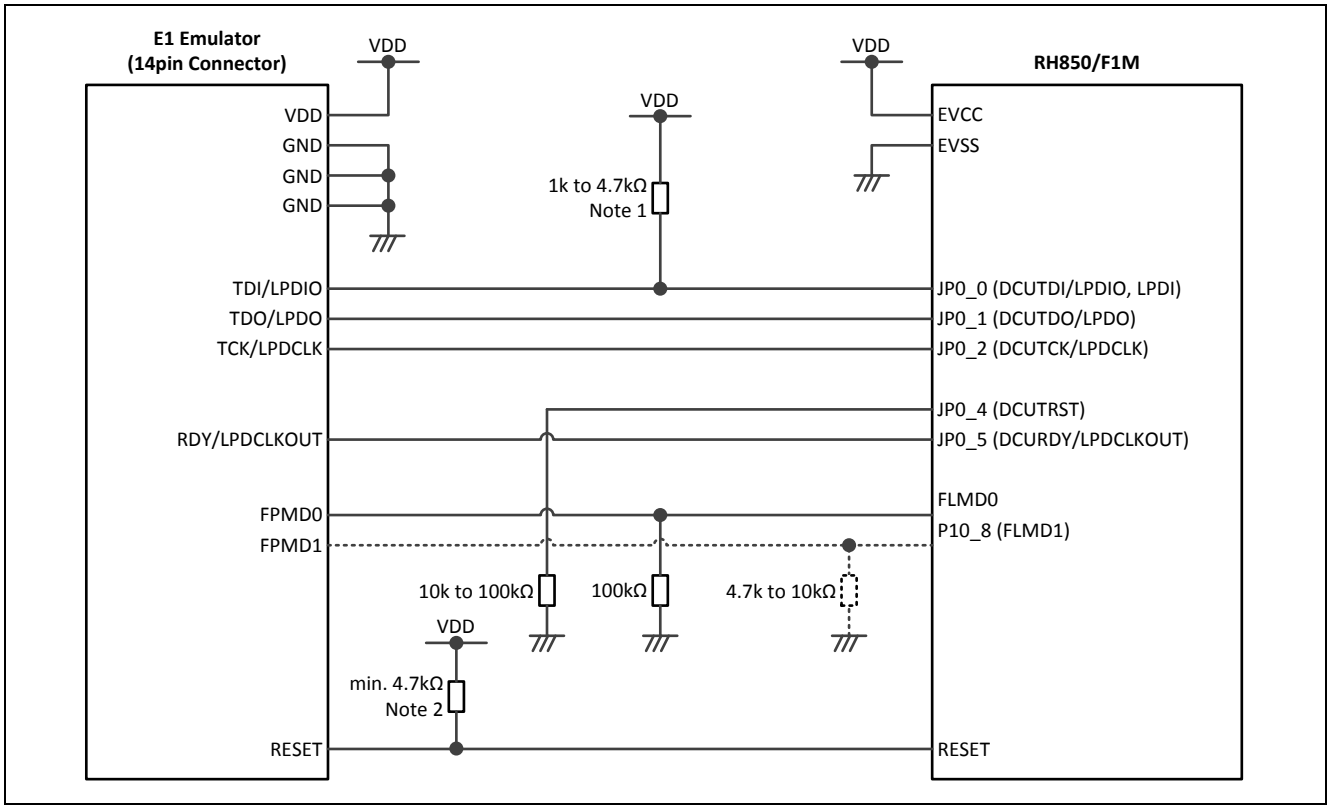


Figure 28 RH850/F1M 4pin Low-pin debug interface connection

Notes: 1. The resistor is optional in 4pin low-pin debug mode.

2. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 4pin debug mode is used on the RH850/F1M group, the ports of the JP0 port group are automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDI input
- JP0_1: LPDO output
- JP0_2: LPDCLK input
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: LPDCLKOUT output
- JP0_6: General-purpose I/O

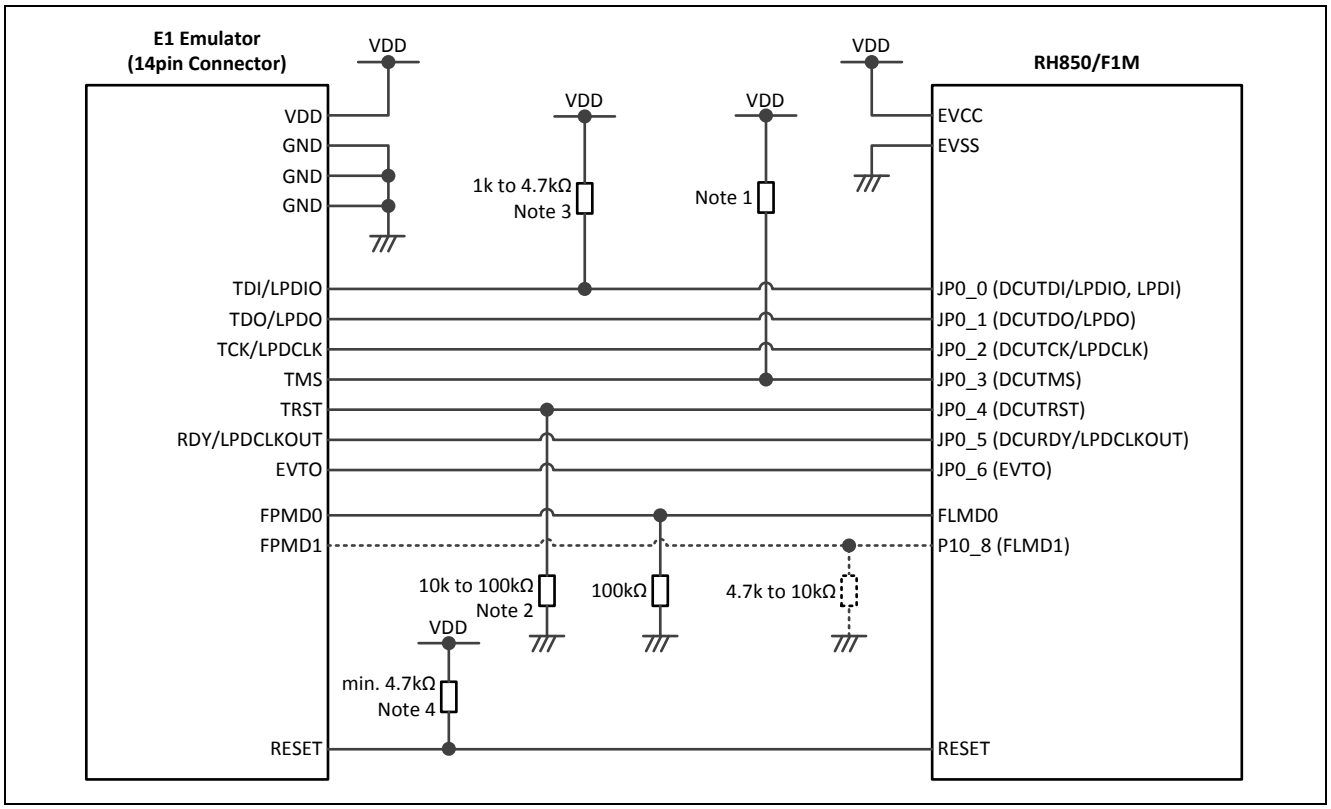


Figure 29 RH850/F1M Nexus, 4pin LPD and 1pin LPD debug interface connection

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the 4pin low-pin debug mode is used
4. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the Nexus debug mode is used on the RH850/F1M group, the ports of the JP0 port group are automatically switched to the debug interface mode.

- JP0_0: DCUTDI input
- JP0_1: DCUTDO output
- JP0_2: DCUTCK input
- JP0_3: DCUTMS input
- JP0_4: DCUTRST input
- JP0_5: DCUTRDY output
- JP0_6: EVTO

The debug interface signal connection of the E1 interface is given in the table below:

E1 Interface Connector	E1 Interface Signal	F1M Device Pin
1	LPDCLK/(DCUTCK)	JP0_2
2	GND	EVSS
3	(DCUTRST)	JP0_4
4	FPMD0/FLMD0	FLMD0
5	LPDO/(DCUTDO)	JP0_1
6	FPMD1	FLMD1
7	LPDI/LPDIO/(DCUTDI)	JP0_0
8	VDD	EVCC
9	(DCUTMS)	JP0_3
10	(EVTO)	JP0_6
11	LPDCLKOUT/(DCURDY)	JP0_5
12	GND	EVSS
13	RESET	RESET
14	GND	EVSS

Note: The Nexus interface signals marked with (*text*) are supported by 3rd party development tools and not by E1 emulator.

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

7.2.2 Flash Programming Interface Connection of RH850/F1M Group

For the programming environment the following connections are supported

- Single-wire asynchronous flash programming interface
- Two-wire asynchronous flash programming interface
- Synchronous flash programming interface

Flash Programming Interface	Function	F1M Device Pins
1-wire UART	RxD/TxD	JP0_0
2-wire UART	RxD	JP0_0
	TxD	JP0_1
CSI	SI	JP0_0
	SO	JP0_1
	SCK	JP0_2

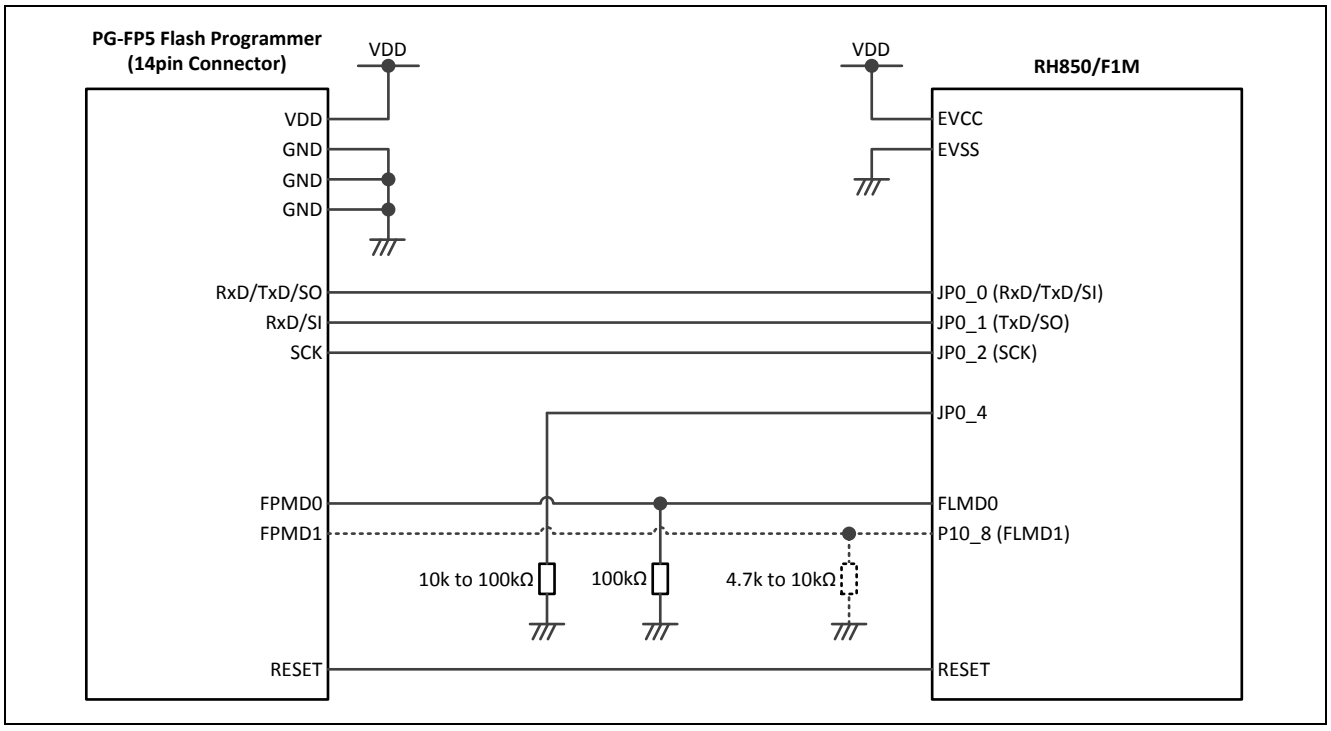


Figure 30 RH850/F1M PG-FP5 flash programming interface connection

The flash programming signal connection of the PG-FP5 interface is given in the table below:

PG-FP5 Interface Connector	PG-FP5 Signal	F1M Device Pin
1	SCK	JP0_2
2	GND	EVSS
3	-	-
4	FPMD0	FLMD0
5	SI/RxD	JP0_1
6	FPMD1	FLMD1
7	SO/TxD	JP0_0
8	VDD	EVCC
9	-	-
10	-	-
11	-	-
12	GND	EVSS
13	RESET	RESET
14	-	-

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

7.2.3 Combined Debug and Flash Programming Interface Connection of RH850/F1M Group

The following figure describes the combined connections for debugging and flash programming of the RH850/F1M group, supporting

- 1pin Low-pin debug interface (1pin LPD)
- 4pin Low-pin debug interface (4pin LPD)
- Nexus interface
- Single-wire asynchronous flash programming interface with PG-FP5
- Two-wire asynchronous flash programming interface with PG-FP5
- Synchronous flash programming interface with PG-FP5

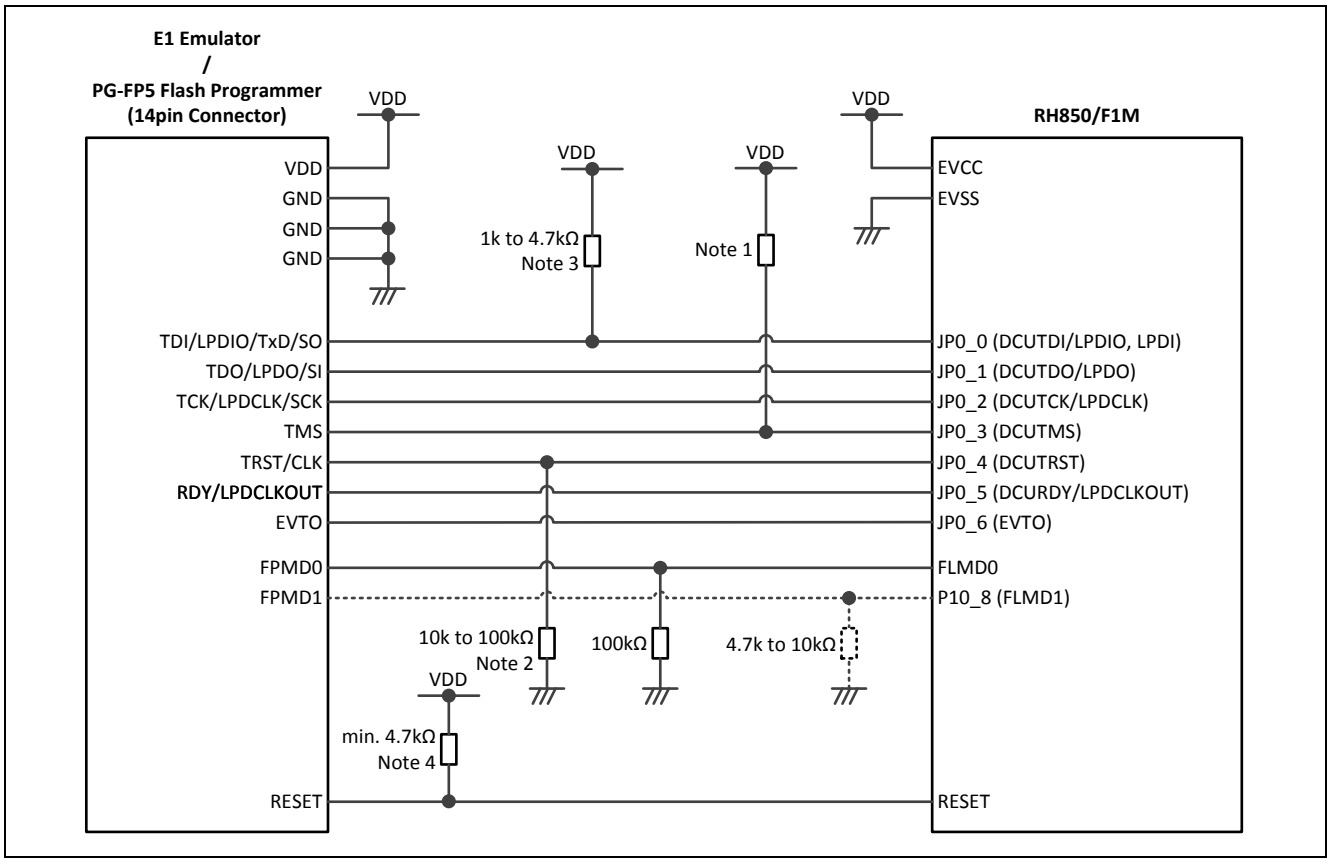


Figure 31 RH850/F1M Combined debug and flash programming interface connections

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the 4pin low-pin debug mode is used
4. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

7.3 Development Tool Interface of RH850/F1H Group

7.3.1 Debug Interface Connection of RH850/F1H Group

This chapter describes the debug interface connection of the RH850/F1H group with internal trace memory. The RH850/F1H (272pin) debug device with trace interface is NOT covered.

For the debugging environment, the following interface connections are supported:

- 1pin Low-pin debug interface (1pin LPD)
- 4pin Low-pin debug interface (4pin LPD)
- Nexus interface
  - The Nexus interface is only supported by 3rd party development tools.

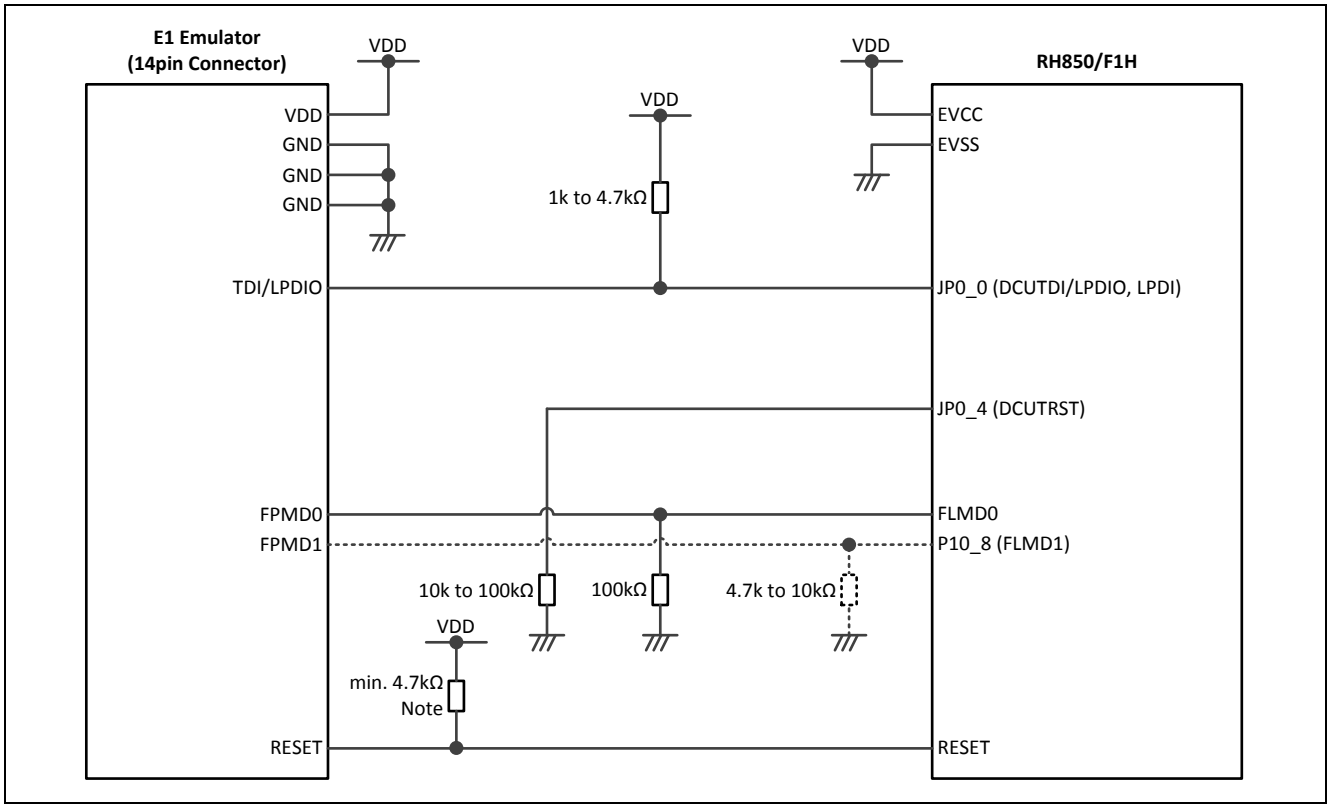


Figure 32 RH850/F1H 1pin Low-pin debug interface connection

Note: The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 1pin debug mode is used on the RH850/F1H group, the port of the JP0 port group is automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDIO input/output
- JP0_1: General-purpose I/O
- JP0_2: General-purpose I/O
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O

- JP0_5: General-purpose I/O
- JP0_6: General-purpose I/O

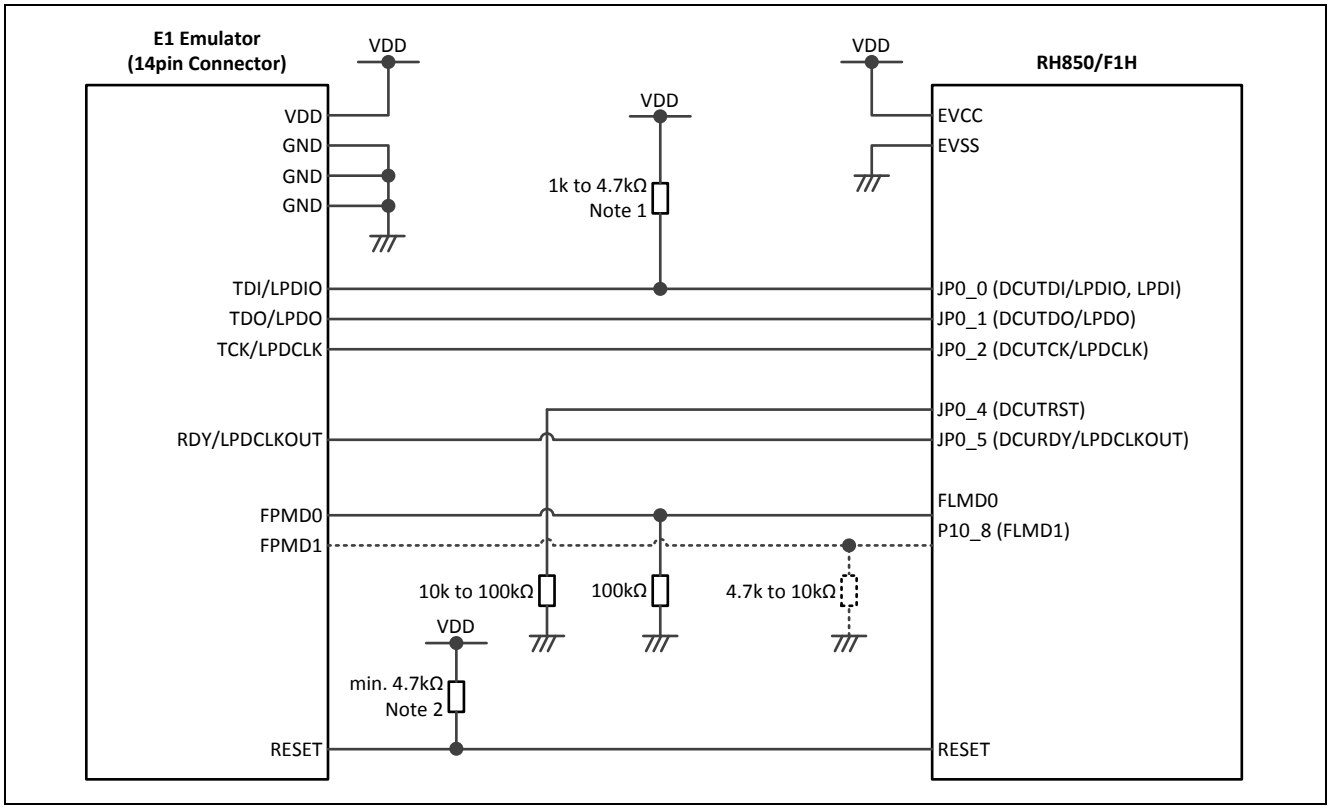


Figure 33 RH850/F1H 4pin Low-pin debug interface connection

Notes: 1. The resistor is optional in 4pin low-pin debug mode.

2. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the 4pin debug mode is used on the RH850/F1H group, the ports of the JP0 port group are automatically switched to the debug interface mode. The remaining pins of JP0 can be used as general-purpose I/O pin including its alternate function.

- JP0_0: LPDI input
- JP0_1: LPDO output
- JP0_2: LPDCLK input
- JP0_3: General-purpose I/O
- JP0_4: General-purpose I/O
- JP0_5: LPDCLKOUT output
- JP0_6: General-purpose I/O

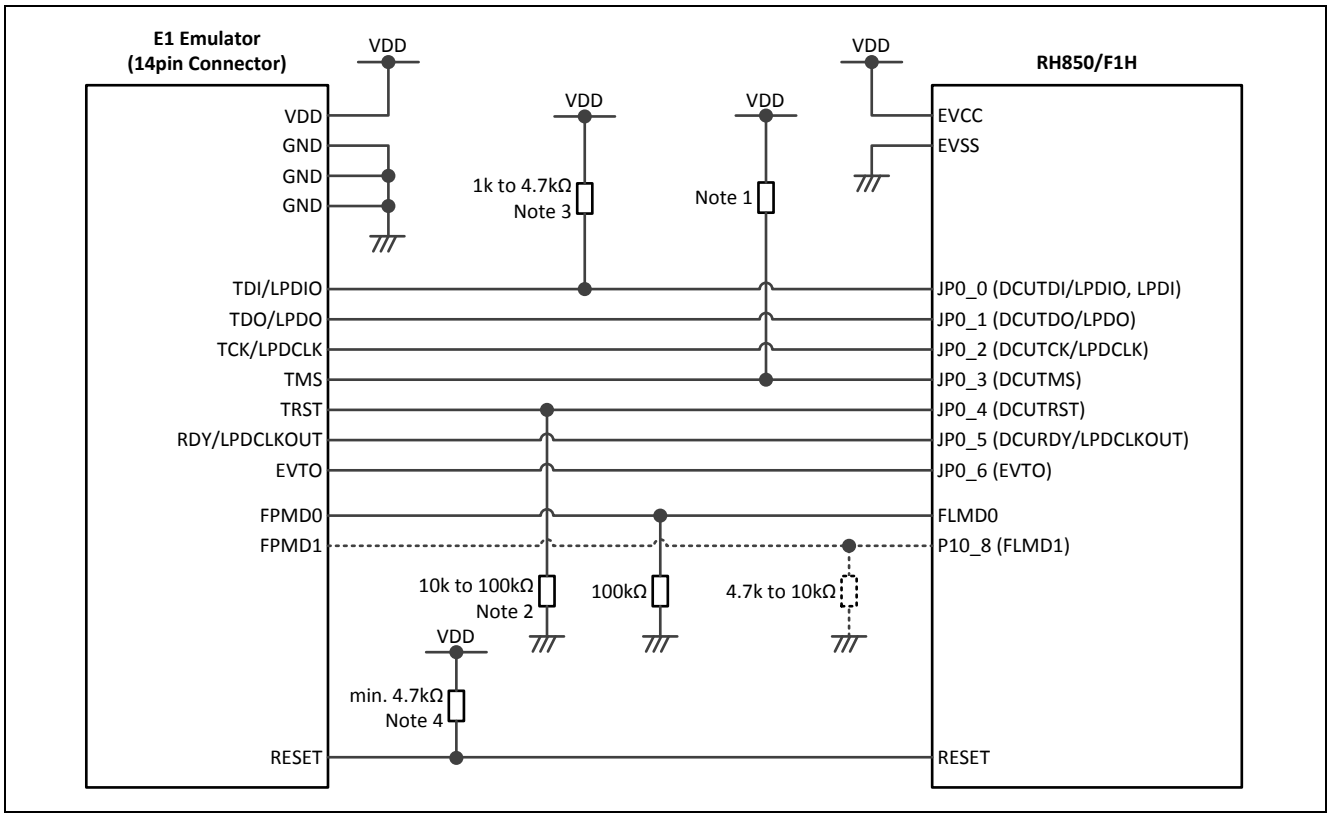


Figure 34 RH850/F1H Nexus, 4pin LPD and 1pin LPD debug interface connection

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the 4pin low-pin debug mode is used
4. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

When the Nexus debug mode is used on the RH850/F1H group, the ports of the JP0 port group are automatically switched to the debug interface mode.

- JP0_0: DCUTDI input
- JP0_1: DCUTDO output
- JP0_2: DCUTCK input
- JP0_3: DCUTMS input
- JP0_4: DCUTRST input
- JP0_5: DCUTRDY output
- JP0_6: EVTO

The debug interface signal connection of the E1 interface is given in the table below:

E1 Interface Connector	E1 Interface Signal	F1H Device Pin
1	LPDCLK/(DCUTCK)	JP0_2
2	GND	EVSS
3	(DCUTRST)	JP0_4
4	FPMD0/FLMD0	FLMD0
5	LPDO/(DCUTDO)	JP0_1
6	FPMD1	FLMD1
7	LPDI/LPDIO/(DCUTDI)	JP0_0
8	VDD	EVCC
9	(DCUTMS)	JP0_3
10	(EVTO)	JP0_6
11	LPDCLKOUT/(DCURDY)	JP0_5
12	GND	EVSS
13	RESET	RESET
14	GND	EVSS

Note: The Nexus interface signals marked with (*text*) are supported by 3rd party development tools and not by E1 emulator.

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

7.3.2 Flash Programming Interface Connection of RH850/F1H Group

For the programming environment the following connections are supported

- Single-wire asynchronous flash programming interface
- Two-wire asynchronous flash programming interface
- Synchronous flash programming interface

Flash Programming Interface	Function	F1H Device Pins
1-wire UART	RxD/TxD	JP0_0
2-wire UART	RxD	JP0_0
	TxD	JP0_1
CSI	SI	JP0_0
	SO	JP0_1
	SCK	JP0_2

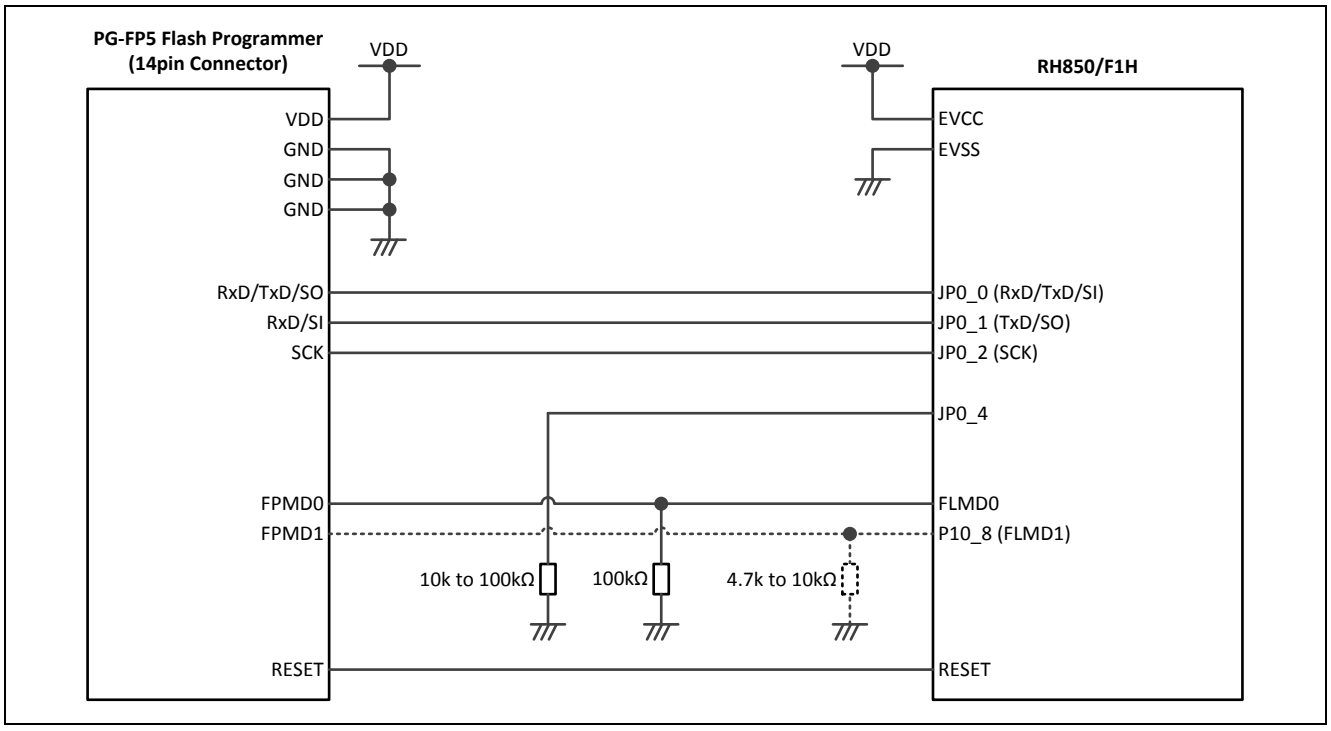


Figure 35 RH850/F1H PG-FP5 flash programming interface connection

The flash programming signal connection of the PG-FP5 interface is given in the table below:

PG-FP5 Interface Connector	PG-FP5 Signal	F1H Device Pin
1	SCK	JP0_2
2	GND	EVSS
3	-	-
4	FPMD0	FLMD0
5	SI/RxD	JP0_1
6	FPMD1	FLMD1
7	SO/TxD	JP0_0
8	VDD	EVCC
9	-	-
10	-	-
11	-	-
12	GND	EVSS
13	RESET	RESET
14	-	-

Caution:

When alternate port functions of P10_8/FLMD1 are used, please make sure not to drive a high level at reset.

When alternate port functions with pull-up resistor are used, please connect P10_8/FLMD1 to FPMD1 of emulator. In that case, it is kept at a low level by the emulator when the reset signal is released.

7.3.3 Combined Debug and Flash Programming Interface Connection of RH850/F1H Group

This chapter describes the debug interface connection of the RH850/F1H group with internal trace memory. The RH850/F1H (272pin) debug device with trace interface is NOT covered.

The following figure describes the combined connections for debugging and flash programming of the RH850/F1H group, supporting

- 1pin Low-pin debug interface (1pin LPD)
- 4pin Low-pin debug interface (4pin LPD)
- Nexus interface
- Single-wire asynchronous flash programming interface with PG-FP5
- Two-wire asynchronous flash programming interface with PG-FP5
- Synchronous flash programming interface with PG-FP5

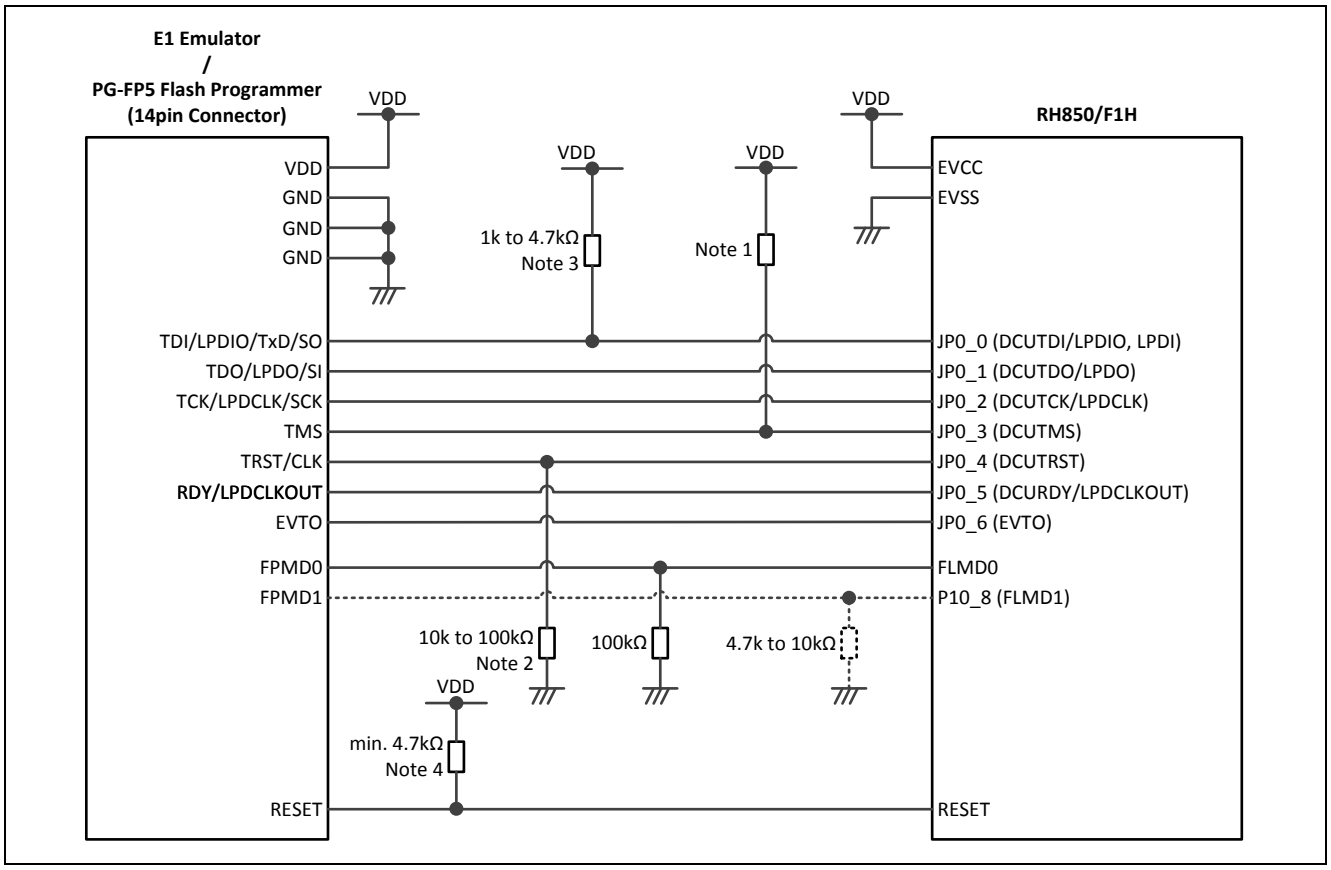


Figure 36 RH850/F1H Combined debug and flash programming interface connections

Notes:

1. The use of an external resistor is only required when the Nexus IF mode is used for debugging and depends on the hardware specification and implementation of the 3rd party development tool.
2. When the Nexus interface is used for debugging the value of the resistor depends on the 3rd party development tool specification.
3. The resistor is optional when the 4pin low-pin debug mode is used.
4. The maximum sink current of the RESET terminal of the E1 emulator is 2mA. The external pull-up circuit of the RESET pin has to be considered based on the applications requirement. When an external RESET component is used, the pull-up resistor value has to be selected appropriately.

7.4 Boundary Scan Mode Interface of RH850/F1L Group

The boundary scan test is compliant with IEEE Standard 1149.1 and certain boundary scan instructions are supported.

When the boundary scan mode shall be used, several connections have to be done between boundary scan test tool and the device. Especially the boundary scan mode selection pins have to be considered from application point of view as these pins are normally used for application related functions.

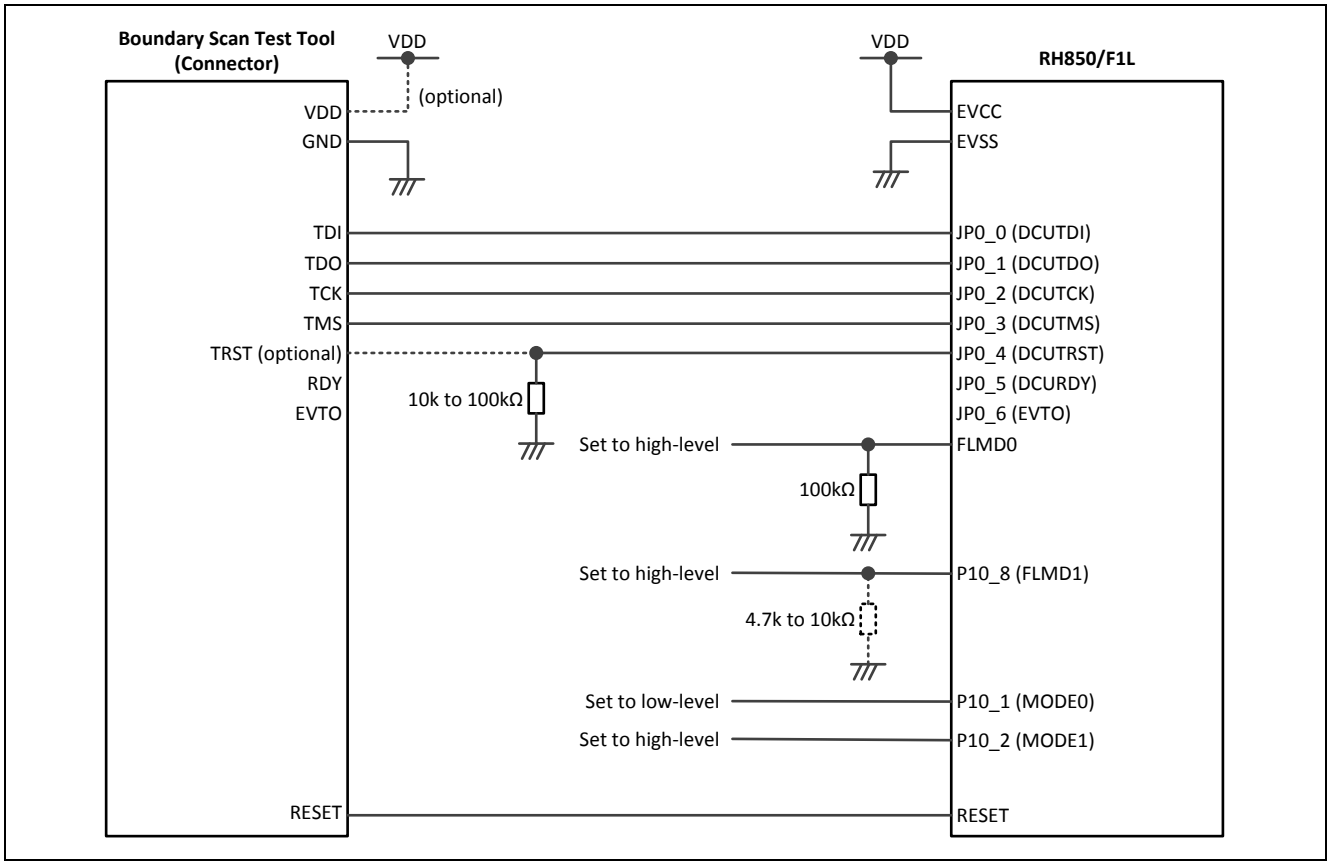


Figure 37 Boundary scan connection of RH850/F1L Group

Note: During boundary scan mode the level of the following pins must be fixed: P10_1: Low, P10_2: High, P10_8: High

In case of the digital I/O pins shared with an analog buffer the boundary scan function only applies to the general I/O function:

- ADCA0: AP0, P8 and P9
- ADCA1: AP1, P18

7.5 Boundary Scan Mode Interface of RH850/F1M Group

The boundary scan test is compliant with IEEE Standard 1149.1 and certain boundary scan instructions are supported.

When the boundary scan mode shall be used, several connections have to be done between boundary scan test tool and the device. Especially the boundary scan mode selection pins have to be considered from application point of view as these pins are normally used for application related functions.

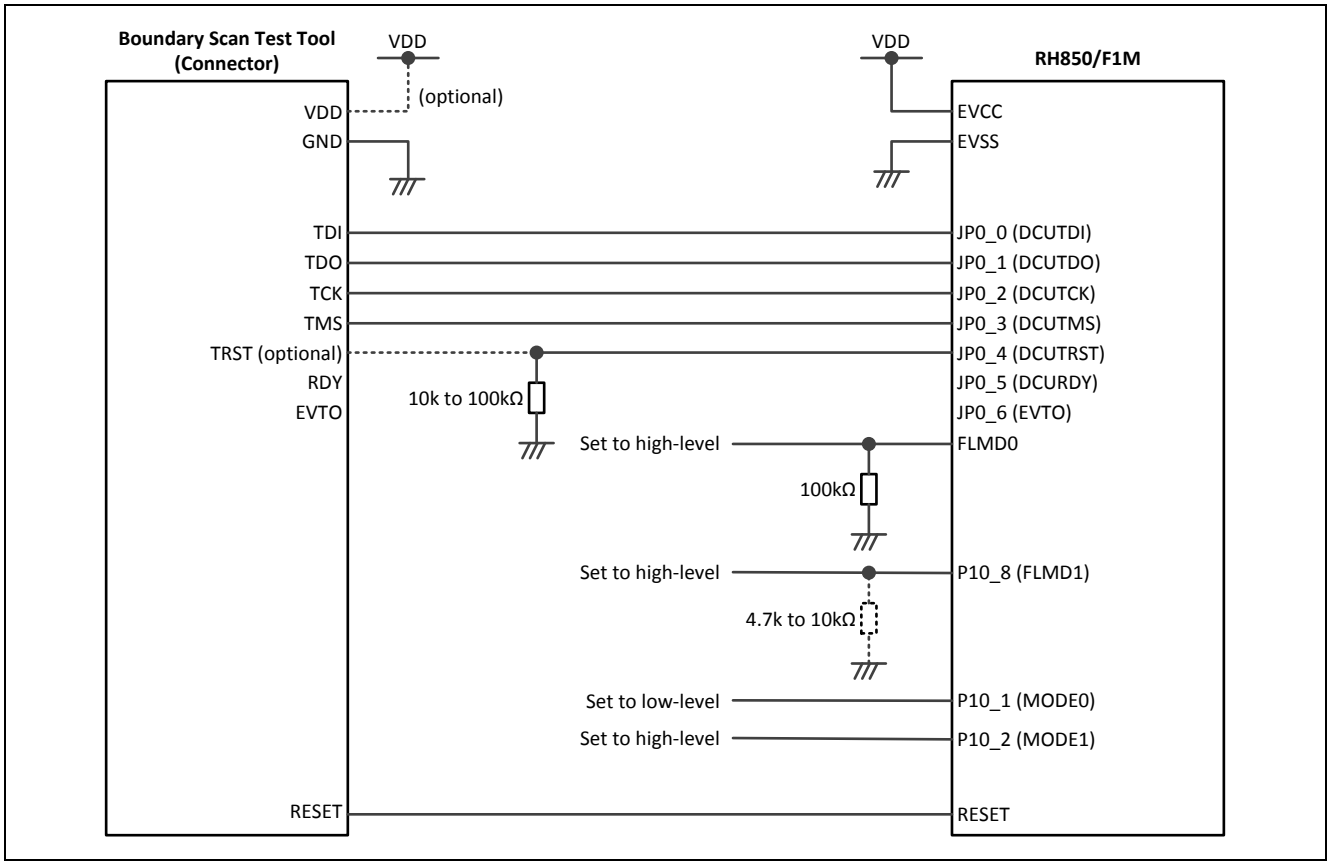


Figure 38 Boundary scan connection of RH850/F1M Group

Note: During boundary scan mode the level of the following pins must be fixed: P10_1: Low, P10_2: High, P10_8: High

In case of the digital I/O pins shared with an analog buffer the boundary scan function only applies to the general I/O function:

- ADCA0: AP0, P8 and P9
- ADCA1: AP1, P18

7.6 Boundary Scan Mode Interface of RH850/F1H Group

The boundary scan test is compliant with IEEE Standard 1149.1 and certain boundary scan instructions are supported.

When the boundary scan mode shall be used, several connections have to be done between boundary scan test tool and the device. Especially the boundary scan mode selection pins have to be considered from application point of view as these pins are normally used for application related functions.

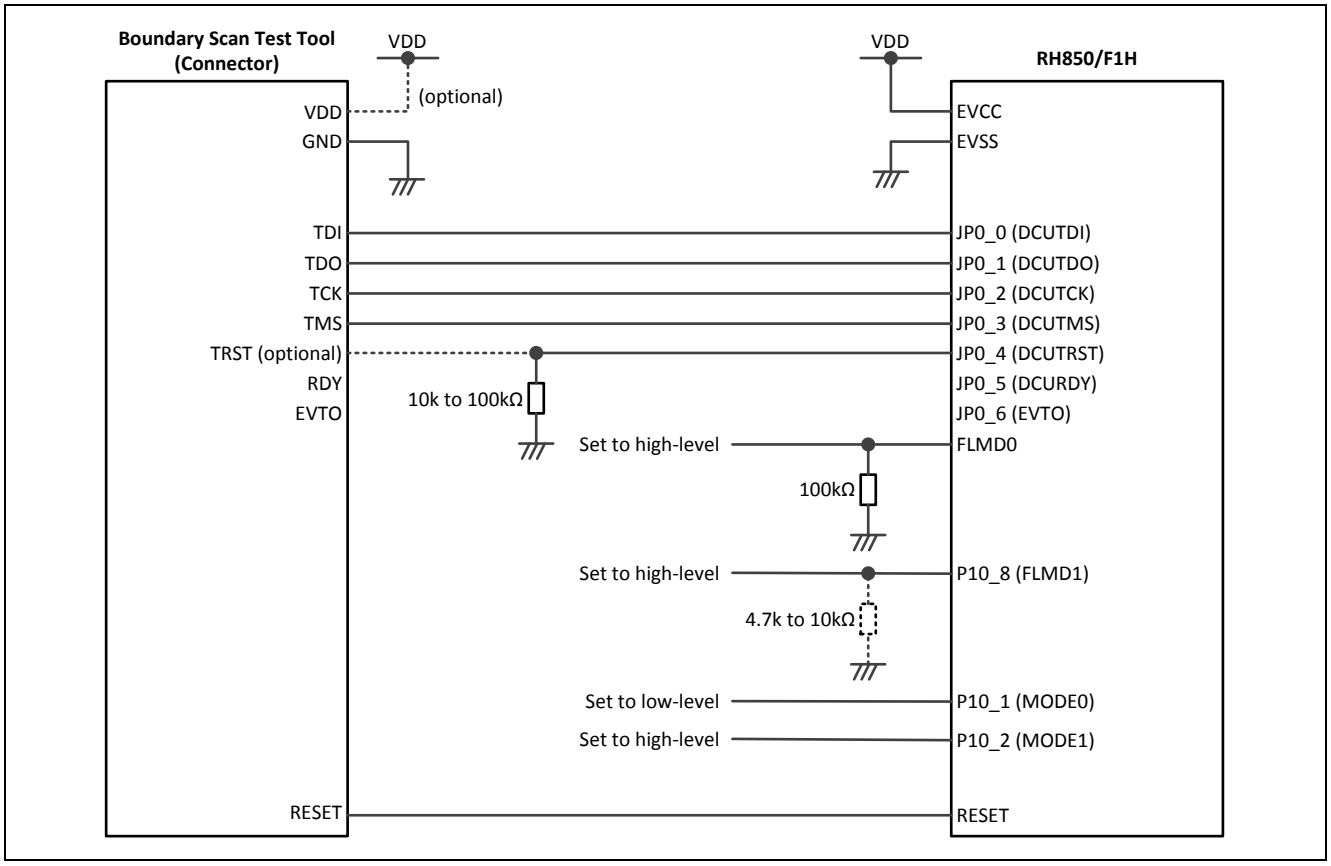


Figure 39 Boundary scan connection of RH850/F1H Group

Note: During boundary scan mode the level of the following pins must be fixed: P10_1: Low, P10_2: High, P10_8: High

In case of the digital I/O pins shared with an analog buffer the boundary scan function only applies to the general I/O function:

- ADCA0: AP0, P8 and P9
- ADCA1: AP1, P18

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Revision History

Rev.	Date	Description	
		Section	**Summary**
1.0	2012-11-21	-	Initial release
2.0	2013-05-15	-	• Update of wording
		-	• Reference Document – Added reference to data sheet
		-	• Power Supply Overview – Correction of supply pin names – Introduction of sub chapter
		-	• Power Supply Architecture – Added, new chapter
		-	• Power Supply Timing – Added, new chapter
		-	• Minimum External Components of RH850/F1L Group – Correction of supply pin names, DCUTMS connection – Correction of value for R1, C3, C4 – Added EVTO pin, added ESR value for C10, C14, R7, R8
		-	• Pin Supply Configuration – Correction of supply names
		-	• Recommended oscillator circuit – Added picture with recommended oscillator circuit with ceramic resonator – Corrected value of capacitor for 32kHz crystal
		-	• Minimum RESET Circuit – Corrected supply pin name
		-	• P0_0/RESETOUT – Corrected supply pin name
		-	• Behaviour during Low Power Mode – Adjustment of wording, change to table style outline
		-	• Recommended Connection of Unused Pins – Added description about connection of unused pins
		-	• ADC conversion time – Added description about ADC conversion, sampling and setup timing
		-	• Equivalent input circuit – Values of RIN and CIN corrected
		-	• Minimum external circuit on ADC input – Added sub chapter
		-	• Debug and Flash Programming Connection and Boundary Scan Mode Interface merged

Rev.	Date	Description	
		Section	**Summary**
		-	• Debug Interface Connection – Added EVTO pin, optional resistor and note to Figure X - Nexus, 4pin LPD and 1pin LPD debug interface connection – Corrected RH850/F1L supply pin name
		-	• Flash Programming Interface Connection – Corrected interface connection, added table with flash programming interface information – Corrected RH850/F1L supply pin name
		-	• Debug and Flash Programming Connection – Added EVTO pin, optional resistor and note to Figure X - Combined debug and flash programming interface connections – Corrected RH850/F1L supply pin name
		-	• Boundary Scan Mode Interface – Added EVTO pin to Figure X - Boundary scan connection – Corrected RH850/F1L supply pin name
2.10	2013-08-08	1.	• Reference Documents – Added RH850/F1L-144, RH850/F1L-100, RH850/F1L-80, RH850/F1L-64, RH850/F1L-48 data sheet document number – Added RH850/F1L-176, RH850/F1L-144, RH850/F1L-100, RH850/F1l-80 customer notification document number
		3.4	• Minimum External Components – Adjusted value of R3, R6
		5.3	• Recommended connection of unused pins – Adjusted condition for JP0_4
		6.1	• AD-Converter – Corrected conversion time header (excluding MPX, including MPX)
		7.1.1	• Debug Interface Connection – Adjusted resistor value for FLMD0 pin – Added pull-down resistor at JP0_4/DCUTRST
		7.1.2	• Flash Programming Interface Connection – Adjusted resistor value for FLMD0 pin – Added pull-down resistor at JP0_4/DCUTRST
		7.1.3	• Debug and Flash Programming Connection – Adjusted resistor value for FLMD0 pin – Added pull-down resistor at JP0_4/DCUTRST
		7.2	• Boundary Scan Mode Interface

Rev.	Date	Description	
		Section	**Summary**
			– Adjusted resistor value for FLMD0 pin – Added pull-down resistor at JP0_4/DCUTRST
2.20	2013-10-09	3.1	• Minimum External Components – Adjusted capacitor value for AWOVCL and ISOVCL pin – Corrected ESR value to max. 40 [mΩ]
		5.4	• Injected Current – New chapter added
3.00	2014-06-13	-	• Transfer to new template • Information added for RH850/F1H Group • Chapters added for F1M Group • Chapter assignment changed • Update of wording and coloring
		1.	• Reference Documents – Added RH850/F1M and RH850/F1H user's manual reference – Added RH850/F1M and RH850/F1H data sheet reference – Added RH850/F1M and RH850/F1H operating precaution reference
		2.4	• Recommended Capacitor Layout at REGVCC of RH850/F1L Group – Added chapter
		3.1	• Minimum External Components of RH850/F1L Group – Adjusted resistor value R1 to 100kΩ – Adjusted resistor value R5 to "1k to 4.7k" due to platform standardization
		3.3	• Minimum External Components of RH850/F1H Group – Adjusted resistor value R5 to "1k to 4.7k" due to platform standardization
		4.1.2	• Sub Oscillator – Adjusted resistor value RdS to 100kΩ
		5.2.3	• P0_0/RESETOUT/CAN0TX/TAUD0I2/TAUD0O2/RLIN20RX/PWGA10O/DPO – Added comment regarding pin behaviour after RESET
		6.4	• External Circuit on ADC Input – Added resistor R1 – Adopted resistor naming – Added sentence about R1 and EMS improvement

Rev.	Date	Description	
		Section	Summary
		7.1	Development Tool Interface of RH850/F1L Group Resistor in 4pin LPD mode defined as optional Adopted caution for handling of P10_8/FLMD1 pin Pull-up resistor added for RESET pin when E1 emulator is used
		7.3	Development Tool Interface of RH850/F1H Group Pull-up resistor added for RESET pin when E1 emulator is used
		7.4	Boundary Scan Mode Interface of RH850/F1L Group Added information about digital I/O pins of ADC
4.00	2014-09-19	-	Information added for RH850/F1M Group Update of wording and coloring
		1.	Reference Documents • Added RH850/F1M user's manual reference • Added F1H-272 OPC reference
		5.1.3	RESET Pin Input Characteristic during Power-On • Added chapter
		5.2.4	Analog Filter Function • Added chapter
4.10	2015-07-09	-	• Document number of RH850/F1M DS adjusted • Added document number of RH850/F1M-176 and RH850/F1H-233 • Wording adjustments, typing error corrections
		2.1.3	Power Supply Pin Architecture of RH850/F1L Group Re-phrased wording of limitation of case 6
		2.2.3	Power Supply Pin Architecture of RH850/F1M Group Re-phrased wording of limitation of case 6
		2.3.4	Power Supply Architecture of RH850/F1H Group • Added digital/analog port P19 to chapter • Re-phrased wording of limitation of case 6
		3.1	Minimum External Components of RH850/F1L Group • Corrected component list from "C10, C15" to "C10, C14" • Corrected maximum resistor value of R2 from 10k to 6.6k according to the the data sheet • Changed X1 of MOSC and X2 for SOSC to Q1 for MOSC and Q2 for SOSC to avoid misunderstanding with pins X1/X2 • Description added regarding parallel capacitor at REGVCC to improve EMI and EMS
		3.2	Minimum External Components of RH850/F1M Group • Corrected component list from "C10, C15" to "C10, C14" • Added C17 to figure and table • Corrected minimum resistor value of R3 from 96k to 86k • Corrected maximum resistor value of R2 from 10k to 6.6k according to the data sheet • Changed X1 of MOSC and X2 for SOSC to Q1 for MOSC and Q2 for SOSC to avoid misunderstanding with pins X1/X2 • Description added regarding parallel capacitor at REGVCC to improve EMI and EMS

Rev.	Date	Description	
		Section	**Summary**
		3.3	Minimum External Components of RH850/F1H Group • Corrected component list from “C10, C15” to “C10, C14” • Corrected C17 in table • Corrected minimum resistor value of R3 from 95k to 86k • Corrected maximum resistor value of R2 from 10k to 6.6k according to the data sheet • Changed X1 of MOSC and X2 for SOSC to Q1 for MOSC and Q2 for SOSC to avoid misunderstanding with pins X1/X2 • Description added regarding parallel capacitor at REGVCC to improve EMI and EMS
		5.1.1	Minimum RESET Circuit • Resistor value for R1of the RH850/F1x groups adjusted according to the corresponding data sheets • Added desciption when a different capacitor value for C1 is used
		5.3.2	Recommended Connection of unused Pins for RH850/F1M Group • Adjusted recommended setting for XT1 according to RH850/F1M user’s manual • Recommended setting of P21 and P21 removed as this is not applicable for RH850/F1M group
		5.3.3	Recommended Connection of unused Pins for RH850/F1H Group • Adjusted recommended setting for XT1 according to RH850/F1H user’s manual
		5.4	Pin Assignement Differences Added “…fact that the RH850/F1M-176 and the RH850/F1H-176pin require …”
		6.2	External Multiplexer Wait Time Reference to data sheet removed
		6.3	Equivalent Input Circuit Added pin name ADCAnImS to figure
		6.4	External Circuit on ADC Input • Adjusted value for series resistor R1 and re-prased wording of description for clarification • Adjusted wording regarding Cexternal for clarification that it is related to analog input pin • Added ADCAnImS to figure • Separated ADC channel numer in note for RH850/F1x groups
4.20	2016-01-26	6.3	ADC equivalent input circuit values corrected for RH850/F1L and added for RH850/F1M and RH850/F1H
		7	EVTO pins added to tables describing the debug interface signals for RH850/F1L, RH850/F1M and RH850/F1H

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 LanGao Rd., Putuo District, Shanghai, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 3.0