RH850/F1x Series

F1Kx Migration Information

R01AN2917ED0310
Rev. 3.10

Introduction

This document provides information on the differences between the new **RH850/F1Kx** devices and their predecessors, the members of the RH850/F1x series: F1L, F1M, F1H and F1K.
It is intended to support the migration of SW from the F1x devices to the new F1Kx devices.

Differences / similarities between the device series are shown function by function on register level.
Differences on bit level are not part of this documentation, e.g.
- same register on F1Kx vs. F1M but added bits on F1Kx,
- same bits differences on usage / specification.

This document is intended as a supplement to the valid device specification, the corresponding RH850/F1Kx and RH850/F1x series User's Manuals and Datasheets (see below).
This document itself is not part of the device specification.
This document can be changed at any time.

At the release time of this document the following User's Manuals and Datasheets are available:

Document	DocNr	Version	Release date
F1KM/F1KH Group User's Manual: Hardware	R01UH0684EJ0110	1.10	Dec, 2018
F1K Group User's Manual: Hardware	R01UH0562EJ0110	1.10	Nov, 2016
F1K Group User's Manual V1.11 Errata	TN-RH8-B168A/E	1.00	Sep, 2018
F1L User's Manual: Hardware	R01UH0390EJ0133	1.33	Apr, 2016
F1L User's Manual: Hardware Rev.1.33 Errata	TN-RH8-B102A/E	1.00	Oct, 2017
F1L Datasheet (176 pin version)	R01DS0170EJ0131	1.31	Apr, 2016
F1L Datasheet Rev.1.31 Errata	TN-RH8-B103A/E	1.00	Oct, 2017
F1M User's Manual: Hardware	R01UH0518EJ0103	1.03	May, 2016
F1M Datasheet (176 pin version)	R01DS0250EJ0111	1.11	May, 2016
F1H User's Manual: Hardware	R01UH0445EJ0112	1.12	May, 2016
F1H Datasheet	R01DS0234EJ0111	1.11	May, 2016
RH850/F1M and F1H User's Manual: Hardware Errata	TN-RH8-B140A/E	1.00	Apr, 2018
RH850/F1M and F1H DATASHEET Errata	TN-RH8-B141A/E	1.00	Apr, 2018

Disclaimer

How to use this manual

In this document the following naming convention is used to distinguish between the different F1x series:

Document wording	Related RH850/F1x series
F1Kx	F1KM, F1KH
F1KH	F1KH-D8
F1KM	F1KM-S4, F1KM-S1
-D8	F1KH-D8
-S4	F1KM-S4
-S1	F1KM-S1

The tables in this document are using the following words/symbols to describe the similarities and differences of the RH850/F1x devices.

Symbol	Description
Yes	This register / function is available on the F1x device.
-	This register / function is not available.
Same	This register / function is available with the same functionality on the F1K device and the related F1x device.
√	This register / function is available on the related F1x device.
←	Same function/(content) as shown to the left.

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1. Overview

This document shall provide a thorough overview of the differences between the following RH850/F1x devices:

- RH850/F1KH Series: F1KH-D8
- RH850/F1KM Series: F1KM-S4, F1KM-S1
- RH850/F1K Series: F1K
- RH850/F1x Series: F1H, F1M, F1L

The major differences (and similarities) of the devices are shown below:

- CPU

	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1L	F1M / F1H
System [1)]	2x G3KH CPU	G3KH CPU	←	←	G3K CPU	2x G3M CPU
Frequency (max)	2x 240MHz	240MHz	120MHz	80MHz (ECO) 120MHz (ADVANCED/PREMIUM)	80/96MHz	120MHz
Pipeline	5-stages	←	←	←	←	7-stages
Cache	No	←	←	←	←	Yes
Coprocessor	Single-precision	←	←	←	No	Double-precision
Interrupt priority levels	16 priority levels	←	←	←	8 priority levels	16 priority levels

Notes:
[1)] The G3KH CPU can be considered rather a subset of the G3M CPU than a superset of the G3K CPU.
[2)] The F1Kx has additional interrupts for new interrupt sources

- Security function

Pin Pairs	F1KM-S4 F1KH-D8	F1H	F1KM-S1	F1K	F1M	F1L
ICU	ICUMD	ICUMB	ICUSE	←	ICUSC	ICUSB

- Power supply

Pin Pairs	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1L	F1M / F1H
EVCC	Yes	←	←	←	←	←
BVCC	Yes	←	No	←	Yes	←
REGVCC	-	2	1	←	←	←
REG0VCC	Yes	-	-	-	-	-
REG1VCC	Yes	-	-	-	-	-
ISOVCL	3	3	1	←	←	2

Due to the increase of REGVCC and ISOVCL supply pin pairs on the F1Kx compared to the other devices, the number of available pin for port functions is decreased. Therefore some ports are not available on the F1Kx device compared to the other devices of the same pin count.

- Clock

Function	F1KM-S4 F1KH-D8	F1KM-S1	F1K	F1L	F1M / F1H
PLL	2	1	←	←	2
SSCG	Yes	No	←	←	Yes
MainOSC frequency [MHz]	8, 16, 20, 24	←	16, 20, 24	8-24	←
HS IntOSC calibration	Yes	←	←	No	←
HS IntOSC as PLL input	Yes	←	←	No	←

- Clock distribution
  - On the F1Kx and F1K, the HSINTOSC and ExtOSC can be used as clock source for CSI
  - On the F1Kx and F1K, the HSINTOSC can be used as LIN clock source
  - The F1Kx and F1K have a reduced selection for clock distribution compared to F1L, F1M or F1H
- Memory overview

Memory	F1KH-D8	F1KM-S4	F1K-S1	F1K	F1L	F1M	F1H
DataFlash:	256KB	128KB	64KB	64KB	32KB and 64KB	64KB	64KB
CPU RAM	LocalRAM, GlobalRAM	←	Local RAM	Local RAM	LocalRAM and SecondaryRAM	LocalRAM	LocalRAM, GlobalRAM
RetentionRAM	64KB	64KB	32KB	64KB	32KB	64KB	128KB, 64KB

- DMA
  - F1KH and F1K implement the same DMA functionality as F1M / F1H.
  - Differences are found in the added DMA trigger factors.
- Ports and port alternative functions
  - F1Kx and F1K add SHMT1 functionality (via PIS register) for all wakeup pins (expect IP0_0 and APx)
  - F1Kx and F1K add / move the RESETOUT functionality to P8_6.
- Improved safety features

Function	F1KM-S4 F1KH-D8	F1KM-S1	F1K	F1L	F1M	F1H
MPU areas (per core)	16	16	16	4	16	16
PEG	Yes	←	←	No	Yes	←
IPG	Yes	←	No	←	←	←
GRG	Yes	No	←	←	Yes	←
PBG	Yes	←	←	No	←	Yes
HBG	Yes	No	←	←	←	Yes
PBGC	Yes	←	←	No	←	←

  - F1Kx, F1K: Added interrupt and address capture on SED in DataFlash and CSIH RAM and RSCAN RAM
- Improved peripheral functions:
  - CSIG0 can operate during CyclicRUN mode
  - Updated CAN functionality

Function	F1KM-S4 F1KM-D8	F1KM-S1	F1K	F1L	F1M	F1H
CAN-FD	Yes	Yes	Yes	No	No	Partly
CAN-FD Macro Version	V3	V3	V2	-	-	V2

  - F1Kx, F1K LPS:
    - LPS can support multiplexer for ADCA inputs
    - LPS supports interrupts in case of an analog or digital error
  - Added CAN channels, Added CAN-FD function (on PREMIUM devices)
  - F1Kx ADCA:
    - Increase number of upper/lower limit pairs to 8
    - Add configurable stabilization time for multiplexed analog input.
    - Add Upper/Lower limit error gathering register.
    - Add stop trigger setting for each SG.
    - ADCMUX pin added to P8

  - F1KM PWM-Diagnostic:
    - Added ADC trigger control functions
    - Added ADC conversion result registers
    - Added function to increase PWM period frequency above 4.8 kHz

- New peripheral functions:
  - RSENT: Single Edge Nibble Transmission
  - SFMA: Serial Flash Memory IF (F1KH and F1KM-S4 only)
  - MMCA: Memory Card I/F (F1KH-D8 324 pins only)

2. Pin Function

2.1 Overview

The functionality of the port registers is not changed between the device versions.

The F1K devices adds additional port function control register due to added alternative function selectivity.

The F1K adds port input buffer selection registers for the added selection of the SHMT1 functionality.

Note:
Unless otherwise highlighted, references to the F1H device are based on the specification of the F1H Premium device.

2.2 Registers Base Address

Base Address Name	F1KH	F1KM	F1K	F1L	F1M	F1H
<PORTn_base>	FFC1 0000H	←	←	←	←	←
<JPORT0_base>	FFC2 0000H	←	←	←	←	←

2.3 Registers overview

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
PMCn	<PORTn_base> + 0400H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPMC0	<JPORT0_base> + 0040H	Yes	Yes	Yes	Yes	Yes	Yes
PMCSRn	<PORTn_base> + 0900H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPMCSR0	<JPORT0_base> + 0090H	Yes	Yes	Yes	Yes	Yes	Yes
PIPCn	<PORTn_base> + 4200H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
PMn	<PORTn_base> + 0300H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
APMn	<PORTn_base> + 03C8H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPM0	<JPORT0_base> + 0030H	Yes	Yes	Yes	Yes	Yes	Yes
PMSRn	<PORTn_base> + 0800H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
APMSRn	<PORTn_base> + 08C8H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPMSR0	<JPORT0_base> + 0080H	Yes	Yes	Yes	Yes	Yes	Yes
PIBCn	<PORTn_base> + 4000H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
APIBCn	<PORTn_base> + 40C8H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPIBC0	<JPORT0_base> + 0400H	Yes	Yes	Yes	Yes	Yes	Yes
IPIBC0	<PORTn_base> + 40F0H	Yes	Yes	Yes	Yes	Yes	Yes
PFCn	<PORTn_base> + 0500H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPFC0	<JPORT0_base> + 0050H	Yes	Yes	Yes	Yes	Yes	Yes
PFCEn	<PORTn_base> + 0600H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPFCE0	<JPORT0_base> + 0060H	Yes	Yes	Yes	n.a.	n.a.	n.a.
PFCAEn	<PORTn_base> + 0A00H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
PBDCn	<PORTn_base> + 4100H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
APBDCn	<PORTn_base> + 41C8H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPBDC0	<JPORT0_base> + 0410H	Yes	Yes	Yes	Yes	Yes	Yes
PPRn	<PORTn_base> + 0200H + n×4	Yes	Yes	Yes	Yes	Yes	Yes

APPRn	<PORTn_base> + 02C8H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPPR0	<JPORT0_base> + 0020H	Yes	Yes	Yes	Yes	Yes	Yes
IPPR0	<PORTn_base> + 02F0H	Yes	Yes	Yes	Yes	Yes	Yes
Pn	<PORTn_base> + 0000H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
APn	<PORTn_base> + 00C8H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JP0	<JPORT0_base> + 0000H	Yes	Yes	Yes	Yes	Yes	Yes
PNOTn	<PORTn_base> + 0700H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
APNOTn	<PORTn_base> + 07C8H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPNOT0	<JPORT0_base> + 0070H	Yes	Yes	Yes	Yes	Yes	Yes
PSRn	<PORTn_base> + 0100H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
APSRn	<PORTn_base> + 01C8H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPSR0	<JPORT0_base> + 0010H	Yes	Yes	Yes	Yes	Yes	Yes
PUn	<PORTn_base> + 4300H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPU0	<JPORT0_base> + 0430H	Yes	Yes	Yes	Yes	Yes	Yes
PDn	<PORTn_base> + 4400H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPD0	<JPORT0_base> + 0440H	Yes	Yes	Yes	Yes	Yes	Yes
PDSCn	<PORTn_base> + 4600H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPDSC0	<JPORT0_base> + 0460H	Yes	Yes	Yes	n.a.	n.a.	n.a.
PODCn	<PORTn_base> + 4500H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPODC0	<JPORT0_base> + 0450H	Yes	Yes	Yes	Yes	Yes	Yes
PISn	<PORTn_base> + 4700H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPIS0	<JPORT0_base> + 0470H	Yes	Yes	Yes	n.a.	n.a.	n.a.
PISAn	<PORTn_base> + 4A00H + n×4	Yes	Yes	n.a.	n.a.	n.a.	n.a.
JPISAn	<PORTn_base> + 04A0H	Yes	Yes	Yes	n.a.	Yes	Yes
PPCMDn	<PORTn_base> + 4C00H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPPCMD0	<JPORT0_base> + 04C0H	Yes	Yes	Yes	Yes	Yes	Yes
PPROTSn	<PORTn_base> + 4B00H + n×4	Yes	Yes	Yes	Yes	Yes	Yes
JPPROTS0	<JPORT0_base> + 04B0H	Yes	Yes	Yes	Yes	Yes	Yes

2.4 48-pin device comparisons

2.4.1 F1KM-S1 vs. F1L

The package pin assignment between the 48-pin F1KM-S1 and the 48-pin F1L does not differ.

The functional differences (and similarities) are shown below:

Port Name	F1KM-S1 (48pin)	F1L (48pin)
AP0_m (m=0 to 7)	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Added RTCAOUT	-
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P8_0	Added SENT0RX, RIIC1SDA	-
P8_1	Added SENT0SPCO, RIIC1SCL	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Same	Same
P10_5	Same	Same
P10_6	MODE2	-
P10_7	Added TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-

2.5 64-pin device comparisons

2.5.1 F1KM-S1 vs. F1L

The package pin assignment between the 64-pin F1KM-S1 and the 64-pin F1L does not differ.

The functional differences (and similarities) are shown below:

Port Name	F1KM-S1 (64pin)	F1L (64pin)
AP0_m (m=0 to 9)	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Added RTCA0OUT	-
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Same	Same
P0_5	Same	Same
P0_6	Same	Same
P8_0	Added SENT0RX, RIIC1SDA	-
P8_1	Added SENT0SPCO,RIIC1SCL	-
P8_2	Same	Same
P8_3	Same	Same
P8_4	Same	Same
P8_5	Added NMI	-
P8_6	Added RTCA0OUT, _RESETOUT	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added TAUJ1I1, TAUJ1O	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Same	Same
P10_5	Same	Same
P10_6	Added MODE2	-
P10_7	Added TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same

Port Name	F1KM-S1 (64pin)	F1L (64pin)
P10_12	Same	Same
P10_13	Same	Same
P10_14	Same	Same

2.6 80-pin device comparisons

2.6.1 F1KM-S1 vs. F1L

The package pin assignment between the 80-pin F1KM-S1 and the 80-pin F1L does not differ.

The functional differences (and similarities) are shown below:

Port Name	F1KM-S1 (80pin)	F1L (80pin)
AP0_m (m=0 to 10)	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Added RTCA0OUT	-
P0_0	Added DPO, TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_10	Added TAUB0I6, TAUB0O6	-
P0_11	Added TAUB0I8, TAUB0O8	-
P0_12	Added TAUB0I10, TAUB0O10, CSIG0SI	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added CSIH0SO, TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Added TAUB0I0, TAUB0O0	-
P0_8	Added TAUB0I2, TAUB0O2	-
P0_9	Added TAUB0I4, TAUB0O4	-
P8_0	Added SENT0RX, RIIC1SDA	-
P8_1	Added SENT0SPCO, RIIC1SCL	-
P8_2	Same	Same
P8_3	Same	Same
P8_4	Same	Same
P8_5	Added NMI	-
P8_6	Added RTCA0OUT, _RESETOUT	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added TAUJ1I1, TAUJ1O1	-
P9_4	Added TAUJ1I0, TAUJ1O0	-
P9_5	Added TAUJ1I1, TAUJ1O1	-
P9_6	Same	Same
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same

Port Name	F1KM-S1 (80pin)	F1L (80pin)
P10_3	Same	Same
P10_4	Same	Same
P10_5	Same	Same
P10_6	Added MODE2	-
P10_7	Added TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Added TAUB0I1, TAUB0O1	-
P10_12	Added TAUB0I3, TAUB0O3	-
P10_13	Added TAUB0I5, TAUB0O5	-
P10_14	Added TAUB0I7, TAUB0O7	-
P10_15	Added TAUB0I9, TAUB0O9	-
P11_0	Added TAUB0I11, TAUB0O11	-
P11_1	Added CSIH0CSS7, TAUB0I13, TAUB0O13	-
P11_2	Added INTP12, RLIN32TX, TAUB0I15, TAUB0O15	-
P11_3	Added RLIN32TX	-
P11_4	Same	Same

2.7 100-pin device comparisons

2.7.1 F1KM-S1 vs. F1L

The package pin assignment between the 100-pin F1KM-S1 and the 100-pin F1L does not differ.

The functional differences (and similarities) are shown below:

Port Name	F1KM-S1 (100pin)	F1L (100pin)
AP0_m (m=0 to 15)	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Added RTCA0OUT	-
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Added PWGA35O	-
P0_7	Same	Same
P0_8	Added CSIH0CSS6	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	PWGA34O	-
P0_12	Same	Same
P8_0	Added SENT0RX, RIIC1SDA	-
P8_1	Added SENT0SPCO, RIIC1SCL	-
P8_2	Same	Same
P8_3	Same	Same
P8_4	Same	Same
P8_5	Added NMI	-
P8_6	Added RTCA0OUT, _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1	-
P8_9	Added ADCA0SEL2	-
P8_10	Same	Same
P8_11	Same	Same
P8_12	Same	Same
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added TAUJ1I1, TAUJ1O1	-

Port Name	F1KM-S1 (100pin)	F1L (100pin)
P9_4	Same	Same
P9_5	Same	Same
P9_6	Same	Same
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Same	Same
P10_5	Same	Same
P10_6	Added MODE2	-
P10_7	Added TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same
P10_12	Same	Same
P10_13	Same	Same
P10_14	Same	Same
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added CSIH0CSS7	-
P11_2	Added RLIN32RX, INTP12	-
P11_3	Added RLIN32TX	-
P11_4	Same	Same
P11_5	Same	Same
P11_6	Same	Same
P11_7	Same	Same

2.7.2 F1KM-S1 vs. F1K

The package pin assignment between the 100-pin F1KM-S1 and the 100-pin F1K does not differ.

The functional differences (and similarities) are shown below:

Port Name	F1KM-S1 (100pin)	F1K (100pin)
AP0_m (m=0 to 15)	Same	Same
JP0_0	Added TAUJ2I0, TAUJ2O0	-
JP0_1	Same	Same
JP0_2	Same	Same
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Added RTCA0OUT	-
P0_0	Added TAUJ2I1, TAUJ2O1	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Same	Same
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Same	Same
P8_0	Added SENT0RX, RIIC1SDA	-
P8_1	Added SENT0SPCO, RIIC1SCL	-
P8_2	Same	Same
P8_3	Same	Same
P8_4	Same	Same
P8_5	Same	Same
P8_6	Added RTCA0OUT	-
P8_7	Added RTCA0OUT	-
P8_8	Same	Same
P8_9	Same	Same
P8_10	Same	Same
P8_11	Same	Same
P8_12	Same	Same
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same

Port Name	F1KM-S1 (100pin)	F1K (100pin)
P9_3	Same	Same
P9_4	Same	Same
P9_5	Same	Same
P9_6	Same	Same
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Same	Same
P10_5	Same	Same
P10_6	Same	Same
P10_7	Added TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same
P10_12	Same	Same
P10_13	Same	Same
P10_14	Same	Same
P10_15	Same	Same
P11_0	Same	Same
P11_1	Same	Same
P11_2	Same	Same
P11_3	Same	Same
P11_4	Same	Same
P11_5	Same	Same
P11_6	Same	Same
P11_7	Same	Same

2.7.3 F1KM-S4 vs F1L

The package pin assignment between the 100-pin F1KM-S4 and the 100-pin F1L differs at the following pins:

Pin Number	F1KM-S4 (100pin)	F1L (100pin)
4	ISOVCL	P10_15
5	ISOVSS	P11_0
42	ISOVSS	P8_0
43	ISOVCL	P8_1
74	ISOVSS	P9_5
75	REGVCC	P9_6

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (100pin)	F1L (100pin)
AP0_m (m=0 to 15)	Same	Same
JP0_0	Added TAUJ2I0, TAUJ2O0	-
JP0_1	Same	Same
JP0_2	Same	Same
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Added RTCA0OUT	-
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Added PWGA35O	-
P0_7	Same	Same
P0_8	Added CSIH0CSS6	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	Added PWGA34O	-
P0_12	Same	Same
P0_13	Same	Same
P0_14	Same	Same
P8_0	Replaced by ISOVSS	-
P8_1	Replaced by ISOVCL	-
P8_2	Same	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI, INTP9	-
P8_6	Added RTCA0OUT, _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1	-
P8_9	Added ADCA0SEL2	-
P8_10	Same	Same

Port Name	F1KM-S4 (100pin)	F1L (100pin)
P8_11	Same	Same
P8_12	Same	Same
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added TAUJ1I1, TAUJ1O1	-
P9_4	Same	Same
P9_5	Replaced by ISOVSS	-
P9_6	Replaced by REGVCC	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Added CAN6TX	-
P10_5	Added CAN6RX, INTP6	-
P10_6	Added MODE2	-
P10_7	Added TAUJ3I1, TAUJ3O1	-
P10_8	Added FLXA0TXDB, TAUJ3I2, TAUJ3O2	-
P10_9	Added FLXA0RXDB	-
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Added FLXA0TXENA	-
P10_12	Added FLXA0STPWT	-
P10_13	Added FLXA0TXENB, CAN7TX	-
P10_14	Added FLXA0RXDA, CAN7RX, INTP9	-
P10_15	Replaced by ISOVCL	-
P11_0	Replaced by ISOVSS	-
P11_1	Added FLXA0TXDA, CSIH0CSS7	-
P11_2	Added INTP12, RLIN32RX	-
P11_3	Added RLIN32TX	-
P11_4	Same	Same
P11_5	Removed RLIN33TX	-
P11_6	Removed RLIN33RX	-
P11_7	Same	Same

2.7.4 F1KM-S4 vs F1K

The package pin assignment between the 100-pin F1KM-S4 and the 100-pin F1K differs at the following pins:

Pin Number	F1KM-S4 (100pin)	F1K (100pin)
4	ISOVCL	P10_15
5	ISOVSS	P11_0
42	ISOVSS	P8_0
43	ISOVCL	P8_1
74	ISOVSS	P9_5
75	REGVCC	P9_6

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (100pin)	F1K (100pin)
AP0_m (m=0 to 15)	Same	Same
JP0_0	Added TAUJ2I0, TAUJ2O0	-
JP0_1	Same	Same
JP0_2	Same	Same
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Added RTCA0OUT	-
P0_0	Added TAUJ2I1, TAUJ2O1	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Same	Same
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Same	Same
P8_0	Replaced by ISOVSS	-
P8_1	Replaced by ISOVCL	-
P8_2	Same	Same
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added INTP9	-
P8_6	Added RTCA0OUT	-
P8_7	Added RTCA0OUT	-
P8_8	Same	Same
P8_9	Same	Same
P8_10	Same	Same
P8_11	Same	Same

Port Name	F1KM-S4 (100pin)	F1K (100pin)
P8_12	Same	Same
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Same	Same
P9_4	Same	Same
P9_5	Replaced by ISOVSS	-
P9_6	Replaced by REGVCC	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Added CAN6TX	-
P10_5	Added CAN6RX, INTP6	-
P10_6	Same	Same
P10_7	Added TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2, FLXA0TXDB	-
P10_9	Added FLXA0RXDB	-
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Added FLXA0TXENA	-
P10_12	Added FLXA0STPWT	-
P10_13	Added CAN7TX, FLXA0TXENB	-
P10_14	Added CAN7RX, INTP9, FLXA0RXDA	-
P10_15	Replaced by ISOVCL	-
P11_0	Replaced by ISOVSS	-
P11_1	Added FLXA0TXDA	-
P11_2	Same	Same
P11_3	Same	Same
P11_4	Same	Same
P11_5	Removed RLIN33TX	-
P11_6	Removed RLIN33RX	-
P11_7	Same	Same

2.8 144-pin device comparisons

2.8.1 F1KM-S4 vs. F1L

The package pin assignment between the 144-pin F1KM-S4 and the 144-pin F1L differs at the following pins:

Pin Number	F1KM-S4 (144pin)	F1L (144pin)
11	ISOVCL	P11_13
12	ISOVSS	P11_14
60	ISOVSS	P1_7
61	ISOVCL	P1_6
97	ISOVSS	P9_5
98	REGVCC	P9_6

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (144pin)	F1L (144pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 7)	Same	Same
IP0_0	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Added PWGA35O	-
P0_7	Same	Same
P0_8	Added INTP16, CSIH0CSS6	-
P0_9	Same	Same
P0_10	Added CAN4TX	1)
P0_11	Added PWGA34O	-
P0_12	Same	Same
P0_13	Added CAN5TX	1)
P0_14	Added CAN5TX Added INTP17	1) -
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added INTP19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	Exchanged to ISOVCL	-
P1_7	Exchanged to ISOVSS	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21 Removed RLIN34TX	-
P1_10	Added INTP22, ADCA1TRG1	-

Port Name	F1KM-S4 (144pin)	F1L (144pin)
P1_11	Added INTP14	-
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Same	Same
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Same	Same
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added TAUJ1I1, TAUJ1O1, INTP16	-
P9_4	Added INTP17	-
P9_5	Exchanged to ISOVSS	-
P9_6	Exchanged to REGVCC	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added TAUJ3I0, TAUJ3O0, INTP18	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Added CAN6TX, PWGA53O	-
P10_5	Added CAN6RX, INTP6, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added FLXA0TXDB, TAUJ3I2, TAUJ3O2	-
P10_9	Added FLXA0RXDB	-
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Added FLXA0TXENA	-
P10_12	Added FLXA0STPWT	-
P10_13	Added FLXA0TXENB, CAN7TX	-
P10_14	Added FLXA0RXDA, CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added FLXA0TXDA, CSIH0CSS7, INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added SFMA0IO1, INTP21	-
P11_5	Added SFMA0IO0, Added CAN5RX	- 1)
P11_6	Added SFMA0SSL, Added CAN5TX	- 1)

Port Name	F1KM-S4 (144pin)	F1L (144pin)
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_13	Replaced to ISOVCL	-
P11_14	Replaced to ISOVSS	-
P11_15	Same	Same
P12_0	Same	Same
P12_1	Same	Same
P12_2	Added INTP19	-
P18_0	Added TAUJ3I0, TAUJ3O0	-
P18_1	Added TAUJ3I1, TAUJ3O1	-
P18_2	Added TAUJ3I2, TAUJ3O2	-
P18_3	Added TAUJ3I3, TAUJ3O3	-
P20_4	Added INTP22, CAN7RX, INTP9	-
P20_5	Added INTP23, CAN7TX	-

1) Already available in devices with 1.5- and 2-MB code flash memories.

2.8.2 F1KM-S4 vs. F1M

The package pin assignment between the 144-pin F1KM-S4 and the 144-pin F1M differs at the following pins:

Pin Number	F1KM-S4 (144pin)	F1M (144pin)
11	ISOVCL	P11_13
12	ISOVSS	P11_14
60	ISOVSS	P1_7
61	ISOVCL	P1_6
97	ISOVSS	ISOVCL
98	REGVCC	ISOVSS

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (144pin)	F1M (144pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 7)	Same	Same
IP0_0	Same	Same
JP0_0	Added FPDR, FPDT	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	- -
P0_1	Added TAUJ2I2, TAUJ2O2, CAN0RX	-
P0_2	Added TAUJ2I3, TAUJ2O3, CAN1RX	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14, CAN2RX	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added INTP19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	Exchanged to ISOCVL	-
P1_7	Exchanged to ISOVSS	-

Port Name	F1KM-S4 (144pin)	F1M (144pin)
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	-
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Same	Same
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Same	Same
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added INTP18, TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Added CAN6TX, PWGA53O	-
P10_5	Added CAN6RX, INTP6, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_13	Added CAN7TX	-
P10_14	Added CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added INTP20	-
P11_2	Added SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-
P11_5	Added SFMA0IO0	-

Port Name	F1KM-S4 (144pin)	F1M (144pin)
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_13	Exchanged to ISOVCL	-
P11_14	Exchanged to ISOVSS	-
P11_15	Same	Same
P12_0	Same	Same
P12_1	Same	Same
P12_2	Added INTP19	-
P18_0	Added TAUJ3I0, TAUJ3O0	-
P18_1	Added TAUJ3I1, TAUJ3O1	-
P18_2	Added TAUJ3I2, TAUJ3O2	-
P18_3	Added TAUJ3I3, TAUJ3O3	-
P20_4	Added INTP22, CAN7RX, INTP9	-
P20_5	Added INTP23, CAN7TX	-

2.8.3 F1KM-S4 vs. F1K

The package pin assignment between the 144-pin F1KM-S4 and the 144-pin F1K differs at the following pins:

Pin Number	F1KM-S4 (144pin)	F1K (144pin)
11	ISOVCL	P11_13
12	ISOVSS	P11_14
60	ISOVSS	P1_7
61	ISOVCL	P1_6
97	ISOVSS	P9_5
98	REGVCC	P9_6
112	BVCC	EVCC
119	BVSS	EVSS
140	BVCC	EVCC
141	BVSS	EVSS

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (144pin)	F1K (144pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 7)	Same	Same
IP0_0	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	- -
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	-
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added INTP19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-

Port Name	F1KM-S4 (144pin)	F1K (144pin)
P1_6	Exchanged to ISOVCL	-
P1_7	Exchanged to ISOVSS	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	-
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Same	Same
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Same	Same
P8_6	Same	Same
P8_7	Same	Same
P8_8	Added RLIN34RX, INTP14	-
P8_9	Added RLIN34TX	-
P8_10	Same	Same
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P9_5	Exchanged to ISOVSS	-
P9_6	Exchanged to REGVCC	-
P10_0	TAUJ1I3, TAUJ1O3	-
P10_1	INTP18, TAUJ3I0, TAUJ3O0	-
P10_2	Same	Same
P10_3	Same	Same
P10_4	Added CAN6TX, PWGA53O	-
P10_5	Added CAN6RX, INTP6, PWGA54O	-
P10_6	Added RLIN24RX	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added FLXA0TXDB, TAUJ3I2, TAUJ3O2	-
P10_9	Added FLXA0RXDB	-
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Added FLXA0TXENA	-
P10_12	Added FLXA0STPWT	-
P10_13	Added FLXA0TXENB, CAN7TX	-
P10_14	Added FLXA0RXDA, CAN7RX, INTP9	-

Port Name	F1KM-S4 (144pin)	F1K (144pin)
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added FLXA0TXDA, INTP20	-
P11_2	Added SFMA0IO3	-
P11_3	Added SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-
P11_5	Added SFMA0IO0	-
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_13	Exchanged to ISOVCL	-
P11_14	Exchanged to ISOVSS	-
P11_15	Same	Same
P12_0	Same	Same
P12_1	Same	Same
P12_2	Added INTP19	-
P18_0	Added TAUJ3I0, TAUJ3O0	-
P18_1	Added TAUJ3I1, TAUJ3O1	-
P18_2	Added TAUJ3I2, TAUJ3O2	-
P18_3	Added TAUJ3I3, TAUJ3O3	-
P20_4	Added INTP22, CAN7RX, INTP9	-
P20_5	Added INTP23, CAN7TX	-

2.9 176-pin devices comparison

2.9.1 F1KM-S4 vs. F1L

The package pin assignment between the 176-pin F1KM-S4 and the 176-pin F1L differs at the following pins:

Pin Number	F1KM-S4 (176pin)	F1L (176pin)
13	ISOVCL	P11_13
14	ISOVSS	P11_14
72	ISOVSS	P1_7
73	ISOVCL	P1_6
113	ISOVSS	P9_5
114	REGVCC	P9_6

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (176pin)	F1L (176pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	- -
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added INTP10, TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Added PWGA35O	-
P0_7	Same	Same
P0_8	Added INTP16, CSIH0CSS6	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	Added PWGA34O	-
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added INTP18, TAUJ2I2, TAUJ2O2	-
P1_3	Added INTP19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	Exchanged to ISOVCL	-

Port Name	F1KM-S4 (176pin)	F1L (176pin)
P1_7	Exchanged to ISOVSS	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	- -
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Added CAN7RX, INTP9	-
P1_15	Added CAN7TX	-
P2_0	Added INTP6, CAN6RX	-
P2_1	Added CAN6TX	-
P2_2	Same	Same
P2_3	Same	Same
P2_4	Added ADCA0SEL0	-
P2_5	Added ADCA0SEL1	-
P2_6	Added ADCA0SEL2	-
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Added RLIN37TX	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added TAUJ1I1, TAUJ1O1, INTP16	-
P9_4	Added INTP17	-
P9_5	Exchanged to ISOVSS	-
P9_6	Exchanged to REGVCC	-
P10_0	Added ETNB0RXCLK, TAUJ1I3, TAUJ1O3	-
P10_1	Added INTP18, ETNB0RXD0, MEMC0A20, TAUJ3I0, TAUJ3O0	-
P10_2	Added ETNB0RXD1, MEMC0A21, RLIN37TX	-
P10_3	Added RLIN37RX, INTP17	-

Port Name	F1KM-S4 (176pin)	F1L (176pin)
P10_4	Added PWGAO53, CAN6TX, ETNB0RXD2, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, ETNB0RXD3, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added FLXA0TXDB, TAUJ3I2, TAUJ3O2	-
P10_9	Added FLXA0RXDB	-
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Added FLXA0TXENA	-
P10_12	Added FLXA0STPWT	-
P10_13	Added FLXA0TXENB, CAN7TX	-
P10_14	Added FLXA0RXDA, CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added FLXA0TXDA, CSIH0CSS7, INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-
P11_5	Added SFMA0IO0	-
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Added ETNB0RXDV	-
P11_12	Same	Same
P11_13	Exchanged to ISOVCL	-
P11_14	Exchanged to ISOVSS	-
P11_15	Added ETNB0RXERR, RLIN36TX	-
P12_0	Added _CSIG2SSI, RLIN36RX, INTP16	-
P12_1	Same	Same
P12_2	Added INTP19, CSIG2RYI, CSIG2RYO	-
P12_3	Added CSIG2SI, _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added CSIG2SC, ETNB0MDIO, _MEMC0BEN1	-
P12_5	Added ETNB0MDC, CSIG2SO, TAUB1I4, TAUB1O4	-
P18_0	Added ETNB0LINK, TAUJ3I0, TAUJ3O0	-
P18_1	Added ETNB0TXD0, TAUJ3I1, TAUJ3O1	-
P18_2	Added ETNB0TXD1, TAUJ3I2, TAUJ3O2	-
P18_3	Added ETNB0TXD2, TAUJ3I3, TAUJ3O3	-
P18_4	Added ETNB0TXD3	-
P18_5	Added ETNB0TXEN	-
P18_6	Same	Same

Port Name	F1KM-S4 (176pin)	F1L (176pin)
P18_7	Added ETNB0TXCLK	-
P20_0	Added CAN6RX, INTP6, CSIG3SI	-
P20_1	Added CAN6TX, CSIG3SO	-
P20_2	Added RLIN29RX, CSIG3SC	-
P20_3	Added RLIN29TX, CSIG3RYI, CSIG3RYO	-
P20_4	Added INTP22, CAN7RX, INTP9, _CSIG3SSI	-
P20_5	Added INTP23, CAN7TX	-

2.9.2 F1KM-S4 vs. F1M

The package pin assignment between the 176-pin F1KM-S4 and the 176-pin F1M differs at the following pins:

Pin Number	F1KM-S4 (176pin)	F1M (176pin)
13	ISOVCL	P11_13
14	ISOVSS	P11_14
72	ISOVSS	P1_7
73	ISOVCL	P1_6
113	ISOVSS	ISOVCL
114	REGVCC	ISOVSS

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (176pin)	F1M (176pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added FPDR, FPDT	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	- -
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	Same
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added INTP19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	Exchanged to ISOVCL	-
P1_7	Exchanged to ISOVCC	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	- -
P1_10	Added INTP22, ADCA1TRG1	-

Port Name	F1KM-S4 (176pin)	F1M (176pin)
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Added CAN7RX, INTP9	-
P1_15	Added CAN7TX	-
P2_0	Added CAN6RX, INTP6	-
P2_1	Added CAN6TX	-
P2_2	Same	Same
P2_3	Same	Same
P2_4	Same	Same
P2_5	Same	Same
P2_6	Same	Same
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Added RLIN37TX	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P10_0	Added TAUJ1I3, TAUJ1O3, ETNB0RXCLK	-
P10_1	Added INTP18, TAUJ3I0, TAUJ3O0, ETNB0RXD0, MEMC0A20	-
P10_2	Added ETNB0RXD1, MEMC0A21, RLIN37TX	-
P10_3	Added RLIN37RX, INTP17	-
P10_4	Added CAN6TX, PWGA53O, ETNB0RXD2, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, ETNB0RXD3, PWGA54O	-
P10_6	Added MODE2, RLIN24RX	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Added RLIN30RX	-
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Added RLIN31RX	-
P10_12	Same	Same
P10_13	Added CAN7TX	-

Port Name	F1KM-S4 (176pin)	F1M (176pin)
P10_14	Added CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added SFMA0IO1, INTP21	-
P11_5	Added SFMA0IO0	
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Added ETNB0RXDV	-
P11_12	Same	Same
P11_13	Exchanged to ISOVCL	-
P11_14	Exchanged to ISOVSS	-
P11_15	Added ETNB0RXERR, RLIN36TX	-
P12_0	Added _CSIG2SSI, RLIN36RX, INTP16	-
P12_1	Same	Same
P12_2	Added INTP19, CSIG2RYI, CSIG2RYO	-
P12_3	Added CSIG2SI, _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added CSIG2SC, ETNB0MDIO, _MEMC0BEN1	-
P12_5	Added ETNB0MDC, CSIG2SO, TAUB1I4, TAUB1O4	-
P18_0	Added ETNB0LINK, TAUJ3I0, TAUJ3O0	-
P18_1	Added ETNB0TXD0, TAUJ3I1, TAUJ3O1	-
P18_2	Added ETNB0TXD1, TAUJ3I2, TAUJ3O2	-
P18_3	Added ETNB0TXD2, TAUJ3I3, TAUJ3O3	-
P18_4	Added ETNB0TXD3	-
P18_5	Added ETNB0TXEN	-
P18_6	Same	Same
P18_7	Added ETNB0TXCLK	-
P20_0	Added CAN6RX, INTP6, CSIG3SI	-
P20_1	Added CAN6TX, CSIG3SO	-
P20_2	Added CSIG3SC, CAN4RX	-
P20_3	Added CSIG3RYI, CSIG3RYO	-
P20_4	Added INTP22, CAN7RX, INTP9, _CSIG3SSI	-
P20_5	Added INTP23, CAN7TX	-

2.9.3 F1KM-S4 vs. F1H

The package pin assignment between the 176-pin F1KM-S4 and the 176-pin F1H differs at the following pins:

Pin Number	F1KM-S4 (176pin)	F1H (176pin)
13	ISOVCL	P11_13
14	ISOVSS	P11_14
72	ISOVSS	P1_7
73	ISOVCL	P1_6
113	ISOVSS	ISOVCL
114	REGVCC	ISOVSS

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (176pin)	F1H (176pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	- -
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added INTP19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	Exchanged to ISOVCL	-
P1_7	Exchanged to ISOVSS	-

Port Name	F1KM-S4 (176pin)	F1H (176pin)
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	- -
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Added CAN7RX, INTP9	-
P1_15	Added CAN7TX	-
P2_0	Same	Same
P2_1	Same	Same
P2_2	Same	Same
P2_3	Same	Same
P2_4	Same	Same
P2_5	Same	Same
P2_6	Same	Same
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Added RLIN37TX	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added INTP18, TAUJ3I0, TAUJ3O0, MEMC0A20	-
P10_2	Added MEMC0A21, RLIN37TX	-
P10_3	Added RLIN37RX, INTP17	-
P10_4	Added CAN6TX, PWGA53O, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-

Port Name	F1KM-S4 (176pin)	F1H (176pin)
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same
P10_12	Same	Same
P10_13	Added CAN7TX	-
P10_14	Added CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-
P11_5	Added SFMA0IO0	-
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_13	Exchanged to ISOVCL	-
P11_14	Exchanged to ISOVSS	-
P11_15	Added ETNB0RXERR, RLIN36TX	-
P12_0	Added _CSIG2SSI, RLIN36RX, INTP16	-
P12_1	Same	Same
P12_2	Added INTP19, CSIG2RYI, CSIG2RYO	-
P12_3	Added _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added _MEMC0BEN1	-
P12_5	Added TAUB1I4, TAUB1O4	-
P18_0	Added TAUJ3I0, TAUJ3O0	-
P18_1	Added TAUJ3I1, TAUJ3O1	-
P18_2	Added TAUJ3I2, TAUJ3O2	-
P18_3	Added TAUJ3I3, TAUJ3O3	-
P18_4	Same	Same
P18_5	Same	Same
P18_6	Removed ETNB0TXERR	-
P18_7	Same	Same
P20_0	Same	Same
P20_1	Same	Same
P20_2	Same	Same
P20_3	Same	Same
P20_4	Added INTP22, CAN7RX, INTP9	-
P20_5	Added INTP23, CAN7TX	-

2.9.4 F1KM-S4 vs. F1K

The package pin assignment between the 176-pin F1KM-S4 and the 176-pin F1K differs at the following pins:

Pin Number	F1KM-S4 (176pin)	F1K (176pin)
4	BVCC	EVCC
5	BVSS	EVSS
13	ISOVCL	P11_13
14	ISOVSS	P11_14
72	ISOVSS	P1_7
73	ISOVCL	P1_6
113	ISOVSS	P9_5
114	REGVCC	P9_6
140	BVCC	EVCC
151	BVSS	EVSS
172	BVCC	EVCC
173	BVSS	EVSS

The functional differences (and similarities) are shown below:

Port Name	F1KM-S4 (176pin)	F1K (176pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added TAUJ2I0, TAUJ2O0	-
JP0_1	Same	Same
JP0_2	Same	Same
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added INTP19, TAUJ2I3, TAUJ2O3	-

Port Name	F1KM-S4 (176pin)	F1K (176pin)
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	Exchanged to ISOVCL	-
P1_7	Exchanged to ISOVSS	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	- -
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Added CAN7RX, INTP9	-
P1_15	Added CAN7TX	-
P2_0	Same	Same
P2_1	Same	Same
P2_2	Same	Same
P2_3	Same	Same
P2_4	Same	Same
P2_5	Same	Same
P2_6	Same	Same
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Added RLIN37TX	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Same	Same
P8_6	Same	Same
P8_7	Same	Same
P8_8	Added RLIN34RX, INTP14	-
P8_9	Added RLIN34TX	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P9_5	Exchanged to ISOVSS	-
P9_6	Exchanged to REGVCC	-
P10_0	Added TAUJ1I3, TAUJ1O3, MEMC0A19, ETNB0RXCLK	-

Port Name	F1KM-S4 (176pin)	F1K (176pin)
P10_1	Added INTP18, TAUJ3I0, TAUJ3O0, ETNB0RXD0, MEMC0A20	-
P10_2	Added ETNB0RXD1, MEMC0A21, RLIN37TX	-
P10_3	Added MEMC0CLK, RLIN37RX, INTP17	-
P10_4	Added CAN6TX, PWGA53O, ETNB0RXD2, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, ETNB0RXD3, PWGA54O	-
P10_6	Added MEMC0AD0, RLIN24RX	-
P10_7	Added MEMC0AD1, RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added FLXA0TXDB, MEMC0AD2, TAUJ3I2, TAUJ3O2	-
P10_9	Added MEMC0AD3, FLXA0RXDB	-
P10_10	Added MEMC0AD4, TAUJ3I3, TAUJ3O3	-
P10_11	Added MEMC0AD5, FLXA0TXENA	-
P10_12	Added MEMC0AD6, FLXA0STPWT	-
P10_13	Added MEMC0AD7, FLXA0TXENB, CAN7TX	-
P10_14	Added MEMC0AD8, FLXA0RXDA, CAN7RX, INTP9	-
P10_15	Added _MEMC0RD	-
P11_0	Added _MEMC0WR	-
P11_1	Added MEMC0AD9, FLXA0TXDA, INTP20	-
P11_2	Added MEMC0AD10, SFMA0IO3	-
P11_3	Added MEMC0AD11, SFMA0IO2	-
P11_4	Added MEMC0AD12, SFMA0IO1, INTP21	-
P11_5	Added MEMC0AD13, SFMA0IO0	-
P11_6	Added MEMC0AD14, SFMA0SSL	-
P11_7	Added MEMC0AD15, SFMA0CLK	-
P11_8	Added _MEMC0CS0	-
P11_9	Added _MEMC0CS1	-
P11_10	Added _MEMC0CS2	-
P11_11	Added _MEMC0CS3, ETNB0RXDV	-
P11_12	Added MEMC0WAIT	-
P11_13	Exchanged to ISOVCL	-
P11_14	Exchanged to ISOVSS	-
P11_15	Added _MEMC0ASTB, ETNB0RXERR, RLIN36TX	-
P12_0	Added _CSIG2SSI, MEMC0A16, RLIN36RX, INTP16	-
P12_1	Added MEMC0A17	-
P12_2	Added MEMC0A18, INTP19, CSIG2RYI, CSIG2RYO	-

Port Name	F1KM-S4 (176pin)	F1K (176pin)
P12_3	Added CSIG2SI, _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added CSIG2SC, ETNB0MDIO, _MEMC0BEN1	-
P12_5	Added ETNB0MDC, CSIG2SO, TAUB1I4, TAUB1O4	-
P18_0	Added ETNB0LINK, TAUJ3I0, TAUJ3O0	-
P18_1	Added ETNB0TXD0, TAUJ3I1, TAUJ3O1	-
P18_2	Added ETNB0TXD1, TAUJ3I2, TAUJ3O2	-
P18_3	Added ETNB0TXD2, TAUJ3I3, TAUJ3O3	-
P18_4	Added ETNB0TXD3	-
P18_5	Added ETNB0TXEN	-
P18_6	Same	Same
P18_7	Added ETNB0TXCLK	-
P20_0	Added CSIG3SI	-
P20_1	Added CSIG3SO	-
P20_2	Added CSIG3SC	-
P20_3	Added CSIG3RYI, CSIG3RYO	-
P20_4	Added INTP22, CAN7RX, INTP9, _CSIG3SSI	-
P20_5	Added INTP23, CAN7TX	-

2.9.5 F1KH-D8 vs. F1H

The package pin assignment between the 176-pin F1KH-D8 and the 176-pin F1H differs at the following pins:

Pin Number	F1KH-D8 (176pin)	F1H (176pin)
13	ISOVCL	P11_13
14	ISOVSS	P11_14
60	REG0VCC	REGVCC
72	ISOVSS	P1_7
73	ISOVLC	P1_6
113	ISOVSS	ISOVCL
114	REG1VCC	ISOVSS

The functional differences (and similarities) are shown below:

Port Name	F1KH-D8 (176pin)	F1H (176pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added TAUJ2I0, TAUJ2O0, FPDR, FPDT	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added RLIN33RX, TAUJ2I0, TAUJ2O0, _CSIG4SSI	-
P1_1	Added INTP18, RLIN33TX, CSIG4SC, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2, CSIG4SI	-
P1_3	Added INTP19, CSIG4SO, TAUJ2I3, TAUJ2O3	-

Port Name	F1KH-D8 (176pin)	F1H (176pin)
P1_4	Added RLIN35RX, DPIN18, CSIH4SI	-
P1_5	Added INTP20, CSIH4SC	-
P1_6	Exchanged to ISOVCL	-
P1_7	Exchanged to ISOVSS	-
P1_8	Removed INTP14	-
P1_9	Added INTP21 Removed RLIN34TX	-
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Added CSIH4RYI, CSIH4RYO	-
P1_15	Same	Same
P2_0	Same	Same
P2_1	Same	Same
P2_2	Added CSIH4CSS0	-
P2_3	Added CSIH4CSS1	-
P2_4	Added CSIH4SO	-
P2_5	Added _CSIH4SSI	-
P2_6	Added CSIG4RYI, CSIG4RYO	-
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P8_2	Added RLIN37TX	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added INTP18, TAUJ3I0, TAUJ3O0, MEMC0A20	-
P10_2	Added MEMC0A21, RLIN37TX	-
P10_3	Added RLIN37RX, INTP17	-

Port Name	F1KH-D8 (176pin)	F1H (176pin)
P10_4	Added CAN6TX, PWGA53O, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same
P10_12	Same	Same
P10_13	Added CAN7TX	-
P10_14	Added CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-
P11_5	Added SFMA0IO0	-
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_13	Exchanged to ISOVCL	-
P11_14	Exchanged to ISOVSS	-
P11_15	Added ETNB0RXERR, RLIN36TX	-
P12_0	Added _CSIG2SSI, RLIN36RX, INTP16	-
P12_1	Same	Same
P12_2	Added INTP19, CSIG2RYI, CSIG2RYO	-
P12_3	Added _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added _MEMC0BEN1	-
P12_5	Added TAUB1I4, TAUB1O4	-
P18_0	Added TAUJ3I0, TAUJ3O0	-
P18_1	Added TAUJ3I1, TAUJ3O1	-
P18_2	Added TAUJ3I2, TAUJ3O2	-
P18_3	Added TAUJ3I3, TAUJ3O3	-
P18_4	Same	Same
P18_5	Same	Same
P18_6	Removed ETNB0TXERR	-
P18_7	Same	Same
P20_0	Same	Same
P20_1	Same	Same

Port Name	F1KH-D8 (176pin)	F1H (176pin)
P20_2	Same	Same
P20_3	Same	Same
P20_4	Added INTP22	-
P20_5	Added INTP23	-

2.9.6 F1KH-D8 vs. F1KM-S4

The package pin assignment between the 176-pin F1KH-D8 and the 176-pin F1KM-S4 differs at the following pins:

Pin Number	F1KH-D8 (176pin)	F1KM-S4 (176pin)
60	REG0VCC	REGVCC
114	REG1VCC	REGVCC

The functional differences (and similarities) are shown below:

Port Name	F1KH-D8 (176pin)	F1KM-S4 (176pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Same	Same
JP0_1	Same	Same
JP0_2	Same	Same
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Same	Same
P0_1	Same	Same
P0_2	Same	Same
P0_3	Same	Same
P0_4	Same	Same
P0_5	Same	Same
P0_6	Same	Same
P0_7	Same	Same
P0_8	Same	Same
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Same	Same
P1_0	Added _CSIG4SSI	-
P1_1	Added CSIG4SC	-
P1_2	Added CSIG4SI	-
P1_3	Added CSIG4SO	-
P1_4	Added CSIH4SI	-
P1_5	Added CSIH4SC	-
P1_8	Same	Same
P1_9	Same	Same
P1_10	Same	Same
P1_11	Same	Same
P1_12	Same	Same
P1_13	Same	Same

Port Name	F1KH-D8 (176pin)	F1KM-S4 (176pin)
P1_14	Added CSIH4RYI, CSIH4RYO	-
P1_15	Same	Same
P2_0	Same	Same
P2_1	Same	Same
P2_2	Added CSIH4CSS0	-
P2_3	Added CSIH4CSS1	-
P2_4	Added CSIH4SO	-
P2_5	Added _CSIH4SSI	-
P2_6	Added CSIG4RYI, CSIG4RYO	-
P8_0	Same	Same
P8_1	Same	Same
P8_2	Same	Same
P8_3	Same	Same
P8_4	Same	Same
P8_5	Same	Same
P8_6	Same	Same
P8_7	Same	Same
P8_8	Same	Same
P8_9	Same	Same
P8_10	Same	Same
P8_11	Same	Same
P8_12	Same	Same
P9_0	Same	Same
P9_1	Same	Same
P9_2	Same	Same
P9_3	Same	Same
P9_4	Same	Same
P10_0	Same	Same
P10_1	Same	Same
P10_2	Same	Same
P10_3	Same	Same
P10_4	Same	Same
P10_5	Same	Same
P10_6	Same	Same
P10_7	Same	Same
P10_8	Same	Same
P10_9	Same	Same
P10_10	Same	Same
P10_11	Same	Same
P10_12	Same	Same
P10_13	Same	Same
P10_14	Same	Same
P10_15	Same	Same
P11_0	Same	Same

Port Name	F1KH-D8 (176pin)	F1KM-S4 (176pin)
P11_1	Same	Same
P11_2	Same	Same
P11_3	Same	Same
P11_4	Same	Same
P11_5	Same	Same
P11_6	Same	Same
P11_7	Same	Same
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_15	Same	Same
P12_0	Same	Same
P12_1	Same	Same
P12_2	Same	Same
P12_3	Same	Same
P12_4	Same	Same
P12_5	Same	Same
P18_0	Same	Same
P18_1	Same	Same
P18_2	Same	Same
P18_3	Same	Same
P18_4	Same	Same
P18_5	Same	Same
P18_6	Same	Same
P18_7	Same	Same
P20_0	Same	Same
P20_1	Same	Same
P20_2	Same	Same
P20_3	Same	Same
P20_4	Same	Same
P20_5	Same	Same

2.10 233-pin devices comparison

2.10.1 F1KM-S4 vs. F1M

The following BGA ball pads differ on the functional or electrical assignment on the F1KM than on the F1M device

BGA pad	F1KM-S4 (233pin)	F1M (233pin)
F1	P13_3	P13_2
F2	P13_2	P11_13
G1	P12_3	P13_5
G2	P13_4	P13_3
G3	P13_5	P11_14
G4	ISOVCL	P13_4
H2	P13_7	P12_3
H3	P13_6	P13_7
H4	ISOVSS	P13_6
J14	REGVCC	ISOVCL
P11	ISOVSS	P0_7
P12	ISOVCL	P1_15
R6	P1_10	P1_8
R11	P0_7	P1_6
R12	P2_5	P1_4
R13	P1_15	P1_14
U5	P1_8	P1_10
U12	P1_5	P1_7
U13	P1_4	P1_5
U14	P1_14	P2_5
U17	A0VSS	EVSS

The following table shows the functional differences or similarities of the ports on the F1KM compared to the F1M device

Port Name	F1KM-S4 (233pin)	F1M (233pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUB0I12, TAUB0O12	-
P0_4	Added TAUB0I12, TAUB0O12	-

Port Name	F1KM-S4 (233pin)	F1M (233pin)
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	-
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added DPIN19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	n.a.	-
P1_7	n.a.	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21 Removed RLIN34TX	-
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Added CAN7RX, INTP9	-
P1_15	Added CAN7TX	-
P2_0	Added CAN6RX, INTP6	-
P2_1	Added CAN6TX	-
P2_2	Same	Same
P2_3	Same	Same
P2_4	Same	Same
P2_5	Same	Same
P2_6	Same	Same
P2_7	Added RLIN210RX	-
P2_8	Added RLIN210TX	-
P2_9	Same	Same
P2_10	Same	Same
P2_11	Same	Same
P2_12	Added RLIN211RX	Same
P2_13	Added RLIN211TX	Same
P2_14	Same	Same
P2_15	Same	Same
P3_0	Same	Same

Port Name	F1KM-S4 (233pin)	F1M (233pin)
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Added RLIN37TX	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added __RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P10_0	Added ETNB0RXCLK, TAUJ1I3, TAUJ1O3	-
P10_1	Added INTP18, ETNB0RXD0, MEMC0A20, TAUJ3I0, TAUJ3O0	-
P10_2	Added ETNB0RXD1, MEMC0A21, RLIN37TX	-
P10_3	Added RLIN37RX, INTP17	-
P10_4	Added CAN6TX, PWGA53O, ETNB0RXD2, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, ETNB0RXD3, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same
P10_12	Same	Same
P10_13	Added CAN7TX	-
P10_14	Added CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-

Port Name	F1KM-S4 (233pin)	F1M (233pin)
P11_5	Added SFMA0IO0	-
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Added ETNB0RXDV	-
P11_12	Same	Same
P11_13	n.a.	-
P11_14	n.a.	-
P11_15	Added RLIN36TX, ETNB0RXERR	-
P12_0	Added _CSIG2SSI, RLIN36RX, INTP16	-
P12_1	Same	Same
P12_2	Added INTP19, CSIG2RYI, CSIG2RYO	-
P12_3	Added CSIG2SI, _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added CSIG2SC, ETNB0MDIO, _MEMC0BEN1	-
P12_5	Added ETNB0MDC, CSIG2SO, TAUB1I4, TAUB1O4	-
P13_0	Same	Same
P13_1	Added MEMC0A20	-
P13_2	Added ETNB0RXDV	-
P13_3	Added ETNB0RXERR	-
P13_4	Same	Same
P13_5	Added MEMC0A21	-
P13_6	Added MEMC0A22	-
P13_7	Same	Same
P18_0	Added ETNB0LINK, TAUJ3I0, TAUJ3O0	-
P18_1	Added ETNB0TXD0, TAUJ3I1, TAUJ3O1	-
P18_2	Added ETNB0TXD1, TAUJ3I2, TAUJ3O2	-
P18_3	Added ETNB0TXD2, TAUJ3I3, TAUJ3O3	-
P18_4	Added ETNB0TXD3	-
P18_5	Added ETNB0TXEN	-
P18_6	Same	Same
P18_7	Added ETNB0TXCLK	-
P18_8	Same	Same
P18_9	Same	Same
P18_10	Same	Same
P18_11	Same	Same
P18_12	Same	Same
P18_13	Same	Same
P18_14	Same	Same
P18_15	Same	Same
P19_0	Same	Same

Port Name	F1KM-S4 (233pin)	F1M (233pin)
P19_1	Same	Same
P19_2	Same	Same
P19_3	Same	Same
P20_0	Added CAN6RX, INTP6, CSIG3SI	-
P20_1	Added CAN6TX, CSIG3SO	-
P20_2	Added CSIG3SC	-
P20_3	Added CSIG3RYI, CSIG3RYO	-
P20_4	Added INTP22, CAN7RX, INTP9, _CSIG3SSI	-
P20_5	Added INTP23, CAN7TX	-

2.10.2 F1KM-S4 vs. F1H

The following BGA ball pads differ on the functional or electrical assignment on the F1KM than on the F1H device

BGA pad	F1KM-S4 (233pin)	F1H (233pin)
F1	P13_3	P13_2
F2	P13_2	P11_13
G1	P12_3	P13_5
G2	P13_4	P13_3
G3	P13_5	P11_14
G4	ISOVCL	P13_4
H2	P13_7	P12_3
H3	P13_6	P13_7
H4	ISOVSS	P13_6
J14	REGVCC	ISOVCL
P11	ISOVSS	P0_7
P12	ISOVCL	P1_15
R6	P1_10	P1_8
R11	P0_7	P1_6
R12	P2_5	P1_4
R13	P1_15	P1_14
U5	P1_8	P1_10
U12	P1_5	P1_7
U13	P1_4	P1_5
U14	P1_14	P2_5
U17	A0VSS	EVSS

The following table shows the functional differences or similarities of the ports on the F1KM compared to the F1H Premium device:

Port Name	F1KM-S4 (233pin)	F1H Premium (233pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added FPDR, FPDT, TAUJ2I0, TAUJ2O0	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUB0I12, TAUB0O12	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-

Port Name	F1KM-S4 (233pin)	F1H Premium (233pin)
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added DPIN19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	n.a.	-
P1_7	n.a.	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	- -
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Same	Same
P1_15	Same	Same
P2_0	Same	Same
P2_1	Same	Same
P2_2	Same	Same
P2_3	Same	Same
P2_4	Same	Same
P2_5	Same	Same
P2_6	Same	Same
P2_7	Same	Same
P2_8	Same	Same
P2_9	Same	Same
P2_10	Same	Same
P2_11	Same	Same
P2_12	Same	Same
P2_13	Same	Same
P2_14	Same	Same
P2_15	Same	Same
P3_0	Same	Same
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-

Port Name	F1KM-S4 (233pin)	F1H Premium (233pin)
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Added RLIN37TX	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added __RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added INTP18, MEMC0A20, TAUJ3I0, TAUJ3O0	-
P10_2	Added MEMC0A21, RLIN37TX	-
P10_3	Added RLIN37RX, INTP17	-
P10_4	Added CAN6TX, PWGA53O, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same
P10_12	Same	Same
P10_13	Added CAN7TX	-
P10_14	Added CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-
P11_5	Added SFMA0IO0	-
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same

Port Name	F1KM-S4 (233pin)	F1H Premium (233pin)
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_13	n.a.	-
P11_14	n.a.	-
P11_15	Added RLIN36TX, ETNB0RXERR	-
P12_0	Added _CSIG2SSI, RLIN36RX, INTP16	
P12_1	Same	Same
P12_2	Added INTP19, CSIG2RYI, CSIG2RYO	-
P12_3	Added _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added _MEMC0BEN1	-
P12_5	Added TAUB1I4, TAUB1O4	-
P13_0	Same	Same
P13_1	Added MEMC0A20	-
P13_2	Same	-
P13_3	Same	Same
P13_4	Same	Same
P13_5	Added MEMC0A21	-
P13_6	Added MEMC0A22	-
P13_7	Same	Same
P18_0	Added TAUJ3I0, TAUJ3O0	-
P18_1	Added TAUJ3I1, TAUJ3O1	-
P18_2	Added TAUJ3I2, TAUJ3O2	-
P18_3	Added TAUJ3I3, TAUJ3O3	-
P18_4	Same	Same
P18_5	Same	Same
P18_6	Removed ETNB0TXERR	-
P18_7	Same	Same
P18_8	Same	Same
P18_9	Same	Same
P18_10	Same	Same
P18_11	Same	Same
P18_12	Same	Same
P18_13	Same	Same
P18_14	Same	Same
P18_15	Same	Same
P19_0	Same	Same
P19_1	Same	Same
P19_2	Same	Same
P19_3	Same	Same
P20_0	Same	Same
P20_1	Same	Same
P20_2	Same	Same

Port Name	F1KM-S4 (233pin)	F1H Premium (233pin)
P20_3	Same	Same
P20_4	INTP22	-
P20_5	INTP23	-

2.10.3 F1KH-D8 vs. F1H

The package pin assignment between the 233-pin F1KH-D8 and the 233-pin F1H Premium differs at the following pins:

Pin Number	F1KH-D8 (233pin)	F1H (233pin)
F1	P13_3	P13_2
F2	P13_2	P11_13
G1	P12_3	P13_5
G2	P13_4	P13_3
G3	P13_5	P11_14
G4	ISOVCL	P13_4
H2	P13_7	P12_3
H3	P13_6	P13_7
H4	ISOVSS	P13_6
J14	REG1VCC	ISOVCL
P10	REG0VCC	REGVCC
P11	ISOVSS	P0_7
P12	ISOVCL	P1_15
R6	P1_10	P1_8
R11	P0_7	P1_6
R12	P2_5	P1_4
R13	P1_15	P1_14
U5	P1_8	P1_10
U12	P1_5	P1_7
U13	P1_4	P1_5
U14	P1_14	P2_5
U17	A0VSS	EVSS

The functional differences (and similarities) are shown below:

Port Name	F1KH-D8 (233pin)	F1H Premium (233pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added TAUJ2I0, TAUJ2O0, FPDR, FPDT	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1, Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	-
P0_9	Same	Same

Port Name	F1KH-D8 (233pin)	F1H Premium (233pin)
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0, _CSIG4SSI	-
P1_1	Added INTP18, CSIG4SC, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2, CSIG4SI	-
P1_3	Added INTP19, CSIG4SO, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18, CSIH4SI	-
P1_5	Added INTP20, CSIH4SC	-
P1_6	n.a.	-
P1_7	n.a.	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	-
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Added CSIH4RYI, CSIH4RYO	-
P1_15	Same	Same
P2_0	Same	Same
P2_1	Same	Same
P2_2	Added CSIH4CSS0	-
P2_3	Added CSIH4CSS1	-
P2_4	Added CSIH4SO	-
P2_5	Added _CSIH4SSI	-
P2_6	Added CSIG4RYI, CSIG4RYO	-
P2_7	Same	Same
P2_8	Same	Same
P2_9	Same	Same
P2_10	Same	Same
P2_11	Same	Same
P2_12	Same	Same
P2_13	Same	Same
P2_14	Same	Same
P2_15	Same	Same
P3_0	Same	Same
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Added RLIN37TX	-

Port Name	F1KH-D8 (233pin)	F1H Premium (233pin)
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added _RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added INTP18, TAUJ3I0, MEMC0A20, TAUJ3O0	-
P10_2	Added MEMC0A21, RLIN37TX	-
P10_3	Added RLIN37RX, INTP17	-
P10_4	Added CAN6TX, PWGA53O, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same
P10_12	Same	Same
P10_13	Added CAN7TX	-
P10_14	Added CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-
P11_5	Added SFMA0IO0	-
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same

Port Name	F1KH-D8 (233pin)	F1H Premium (233pin)
P11_11	Same	Same
P11_12	Same	Same
P11_13	n.a.	-
P11_14	n.a.	-
P11_15	Added ETNB0RXERR, RLIN36TX	-
P12_0	Added _CSIG2SSI, RLIN36RX, INTP16	-
P12_1	Same	Same
P12_2	Added INTP19, CSIG2RYI, CSIG2RYO	-
P12_3	Added _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added _MEMC0BEN1	-
P12_5	Added TAUB1I4, TAUB1O4	-
P13_0	Same	Same
P13_1	Added MEMC0A20	-
P13_2	Same	Same
P13_3	Same	Same
P13_4	Same	Same
P13_5	Added MEMC0A21	-
P13_6	Added MEMC0A22	-
P13_7	Same	Same
P18_0	Added TAUJ3I0, TAUJ3O0	-
P18_1	Added TAUJ3I1, TAUJ3O1	-
P18_2	Added TAUJ3I2, TAUJ3O2	-
P18_3	Added TAUJ3I3, TAUJ3O3	-
P18_4	Same	Same
P18_5	Same	Same
P18_6	Removed ETNB0TXERR	-
P18_7	Same	Same
P18_8	Same	Same
P18_9	Same	Same
P18_10	Same	Same
P18_11	Same	Same
P18_12	Same	Same
P18_13	Same	Same
P18_14	Same	Same
P18_15	Same	Same
P19_0	Same	Same
P19_1	Same	Same
P19_2	Same	Same
P19_3	Same	Same
P20_0	Same	Same
P20_1	Same	Same
P20_2	Same	Same
P20_3	Same	Same
P20_4	Added INTP22	-

Port Name	F1KH-D8 (233pin)	F1H Premium (233pin)
P20_5	Added INTP23	-

2.10.4 F1KH-D8 vs. F1KM-S4

The following BGA ball pads differ on the functional or electrical assignment on the F1KH-D8 than on the F1KM-S4 device

BGA pad	F1KH-D8 (233pin)	F1KM-S4 (233pin)
J14	REG1VCC	REGVCC
P10	REG0VCC	REGVCC

The following table shows the functional differences or similarities of the ports on the F1KH-D8 compared to the F1KM-S4 device:

Port Name	F1KH-D8 (233pin)	F1KM-S4 (233pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Same	Same
JP0_1	Same	Same
JP0_2	Same	Same
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Same	Same
P0_1	Same	Same
P0_2	Same	Same
P0_3	Same	Same
P0_4	Same	Same
P0_5	Same	Same
P0_6	Same	Same
P0_7	Same	Same
P0_8	Same	Same
P0_9	Same	Same
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Same	Same
P1_0	Added _CSIG4SSI	-
P1_1	Added CSIG4SC	-
P1_2	Added CSIG4SI	-
P1_3	Added CSIG4SO	-
P1_4	Added CSIH4SI	-
P1_5	Added CSIH4SC	-
P1_8	Same	Same
P1_9	Same	Same
P1_10	Same	Same
P1_11	Same	Same

Port Name	F1KH-D8 (233pin)	F1KM-S4 (233pin)
P1_12	Same	Same
P1_13	Same	Same
P1_14	Added CSIH4RYI, CSIH4RYO	-
P1_15	Same	Same
P2_0	Same	Same
P2_1	Same	Same
P2_2	Added CSIH4CSS0	-
P2_3	Added CSIH4CSS1	-
P2_4	Added CSIH4SO	-
P2_5	Added _CSIH4SSI	-
P2_6	Added CSIG4RYI, CSIG4RYO	-
P2_7	Same	Same
P2_8	Same	Same
P2_9	Same	Same
P2_10	Same	Same
P2_11	Same	Same
P2_12	Same	Same
P2_13	Same	Same
P2_14	Same	Same
P2_15	Same	Same
P3_0	Same	Same
P8_0	Same	Same
P8_1	Same	Same
P8_2	Same	Same
P8_3	Same	Same
P8_4	Same	Same
P8_5	Same	Same
P8_6	Same	Same
P8_7	Same	Same
P8_8	Same	Same
P8_9	Same	Same
P8_10	Same	Same
P8_11	Same	Same
P8_12	Same	Same
P9_0	Same	Same
P9_1	Same	Same
P9_2	Same	Same
P9_3	Same	Same
P9_4	Same	Same
P10_0	Same	Same
P10_1	Same	Same
P10_2	Same	Same
P10_3	Same	Same
P10_4	Same	Same

Port Name	F1KH-D8 (233pin)	F1KM-S4 (233pin)
P10_5	Same	Same
P10_6	Same	Same
P10_7	Same	Same
P10_8	Same	Same
P10_9	Same	Same
P10_10	Same	Same
P10_11	Same	Same
P10_12	Same	Same
P10_13	Same	Same
P10_14	Same	Same
P10_15	Same	Same
P11_0	Same	Same
P11_1	Same	Same
P11_2	Same	Same
P11_3	Same	Same
P11_4	Same	Same
P11_5	Same	Same
P11_6	Same	Same
P11_7	Same	Same
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_15	Same	Same
P12_0	Same	Same
P12_1	Same	Same
P12_2	Same	Same
P12_3	Same	Same
P12_4	Same	Same
P12_5	Same	Same
P13_0	Same	Same
P13_1	Same	Same
P13_2	Same	Same
P13_3	Same	Same
P13_4	Same	Same
P13_5	Same	Same
P13_6	Same	Same
P13_7	Same	Same
P18_0	Same	Same
P18_1	Same	Same
P18_2	Same	Same
P18_3	Same	Same
P18_4	Same	Same

Port Name	F1KH-D8 (233pin)	F1KM-S4 (233pin)
P18_5	Same	Same
P18_6	Same	Same
P18_7	Same	Same
P18_8	Same	Same
P18_9	Same	Same
P18_10	Same	Same
P18_11	Same	Same
P18_12	Same	Same
P18_13	Same	Same
P18_14	Same	Same
P18_15	Same	Same
P19_0	Same	Same
P19_1	Same	Same
P19_2	Same	Same
P19_3	Same	Same
P20_0	Same	Same
P20_1	Same	Same
P20_2	Same	Same
P20_3	Same	Same
P20_4	Same	Same
P20_5	Same	Same

2.11 272-pin devices comparison

2.11.1 F1KM-S4 vs F1H

The following BGA ball pads differ on the functional or electrical assignment on the F1KM-S4 than on the F1H device

BGA pad	F1KM-S4 (272pin)	F1H ECO (272pin)
E1	P11_0	P22_2
F1	P22_2	P22_0
G1	P22_0	P21_4
H1	P21_4	P11_13
H2	P11_12	P21_3
H4	ISOVCL	P11_0
J2	P21_3	P11_14
J4	ISOVSS	P11_12
L17	REGVCC	ISOVCL
U11	ISOVSS	P0_7
U12	ISOVCL	P1_4
V11	P0_7	P1_6
W6	P2_14	P1_8
W12	P1_4	P1_7
Y6	P1_8	P2_14
Y20	A0VSS	EVSS

The following table shows the functional differences or similarities of the ports on the F1KM-S4 compared to the F1H device:

Port Name	F1KM-S4 (272pin)	F1H ECO (272pin)
AP0_m (m=0 to 15)	Same	Same
AP1_m (m=0 to 15)	Same	Same
IP0_0	Same	Same
JP0_0	Added TAUJ2I0, TAUJ2O0, FPDR, FPDT	-
JP0_1	Added FPDT	-
JP0_2	Added FPCK	-
JP0_3	Same	Same
JP0_4	Same	Same
JP0_5	Same	Same
JP0_6	Same	Same
P0_0	Added TAUJ2I1, TAUJ2O1 Removed _RESETOUT	-
P0_1	Added TAUJ2I2, TAUJ2O2	-
P0_2	Added TAUJ2I3, TAUJ2O3	-
P0_3	Added TAUJ1I0, TAUJ1O0	-
P0_4	Added TAUB0I12, TAUB0O12	-
P0_5	Added TAUB0I14, TAUB0O14	-
P0_6	Same	Same
P0_7	Same	Same
P0_8	Added INTP16	-
P0_9	Same	Same

Port Name	F1KM-S4 (272pin)	F1H ECO (272pin)
P0_10	Same	Same
P0_11	Same	Same
P0_12	Same	Same
P0_13	Same	Same
P0_14	Added INTP17	-
P1_0	Added TAUJ2I0, TAUJ2O0	-
P1_1	Added INTP18, TAUJ2I1, TAUJ2O1	-
P1_2	Added DPIN19, TAUJ2I2, TAUJ2O2	-
P1_3	Added INTP19, TAUJ2I3, TAUJ2O3	-
P1_4	Added DPIN18	-
P1_5	Added INTP20	-
P1_6	n.a.	-
P1_7	n.a.	-
P1_8	Removed RLIN34RX, INTP14	-
P1_9	Added INTP21, Removed RLIN34TX	- -
P1_10	Added INTP22, ADCA1TRG1	-
P1_11	Added INTP14	-
P1_12	Added RLIN36TX	-
P1_13	Added RLIN36RX, INTP16	-
P1_14	Added CAN7RX, INTP9	-
P1_15	Added CAN7TX	-
P2_0	Same	Same
P2_1	Same	Same
P2_2	Same	Same
P2_3	Same	Same
P2_4	Same	Same
P2_5	Same	Same
P2_6	Same	Same
P2_7	Same	Same
P2_8	Same	Same
P2_9	Same	Same
P2_10	Same	Same
P2_11	Same	Same
P2_12	Same	Same
P2_13	Same	Same
P2_14	Same	Same
P2_15	Same	Same
P3_0	Same	Same
P3_1	Same	Same
P3_2	Same	Same
P3_3	Same	Same
P3_4	Same	Same
P3_5	Same	Same
P3_6	Same	Same

Port Name	F1KM-S4 (272pin)	F1H ECO (272pin)
P3_7	Same	Same
P3_8	Same	Same
P3_9	Same	Same
P3_10	Same	Same
P8_0	Added CAN6RX, INTP6, RIIC1SDA, SENT0RX	-
P8_1	Added CAN6TX, RIIC1SCL, SENT0SPCO	-
P8_2	Added RLIN37TX	-
P8_3	Added CAN7TX	-
P8_4	Added CAN7RX, INTP9	-
P8_5	Added NMI	-
P8_6	Added __RESETOUT	-
P8_7	Added ADCA0SEL0, RTCA0OUT	-
P8_8	Added ADCA0SEL1, RLIN34RX, INTP14	-
P8_9	Added ADCA0SEL2, RLIN34TX	-
P8_10	Added RLIN37RX, INTP17	-
P8_11	Added RLIN25RX	-
P8_12	Added INTP23, RLIN25TX	-
P9_0	Added TAUJ1I1, TAUJ1O1, SENT1RX, RIIC1SDA	-
P9_1	Added TAUJ1I2, TAUJ1O2, SENT1SPCO, RIIC1SCL	-
P9_2	Same	Same
P9_3	Added INTP16	-
P9_4	Added INTP17	-
P10_0	Added TAUJ1I3, TAUJ1O3	-
P10_1	Added INTP18, TAUJ3I0, TAUJ3O0, MEMC0A20	-
P10_2	Added MEMC0A21, RLIN37TX	-
P10_3	Added RLIN37RX, INTP17	-
P10_4	Added CAN6TX, PWGA53O, MEMC0A22	-
P10_5	Added CAN6RX, INTP6, PWGA54O	-
P10_6	Added RLIN24RX, MODE2	-
P10_7	Added RLIN24TX, TAUJ3I1, TAUJ3O1	-
P10_8	Added TAUJ3I2, TAUJ3O2	-
P10_9	Same	Same
P10_10	Added TAUJ3I3, TAUJ3O3	-
P10_11	Same	Same
P10_12	Same	Same
P10_13	Added CAN7TX	-
P10_14	Added CAN7RX, INTP9	-
P10_15	Same	Same
P11_0	Same	Same
P11_1	Added INTP20	-
P11_2	Added RLIN32RX, INTP12, SFMA0IO3	-

Port Name	F1KM-S4 (272pin)	F1H ECO (272pin)
P11_3	Added RLIN32TX, SFMA0IO2	-
P11_4	Added INTP21, SFMA0IO1	-
P11_5	Added SFMA0IO0	-
P11_6	Added SFMA0SSL	-
P11_7	Added SFMA0CLK	-
P11_8	Same	Same
P11_9	Same	Same
P11_10	Same	Same
P11_11	Same	Same
P11_12	Same	Same
P11_13	n.a.	-
P11_14	n.a.	-
P11_15	Added ETNB0RXERR, RLIN36TX	-
P12_0	Added _CSIG2SSI, RLIN36RX, INTP16	-
P12_1	Same	Same
P12_2	Added INTP19, CSIG2RYI, CSIG2RYO	-
P12_3	Added _MEMC0BEN0, TAUB1I6, TAUB1O6	-
P12_4	Added _MEMC0BEN1	-
P12_5	Added TAUB1I4, TAUB1O4	-
P13_0	Same	Same
P13_1	Same	Same
P13_2	Same	Same
P13_3	Same	Same
P13_4	Same	Same
P13_5	Same	Same
P13_6	Same	Same
P13_7	Same	Same
P18_0	Added TAUJ3I0, TAUJ3O0	-
P18_1	Added TAUJ3I1, TAUJ3O1	-
P18_2	Added TAUJ3I2, TAUJ3O2	-
P18_3	Added TAUJ3I3, TAUJ3O3	-
P18_4	Same	Same
P18_5	Same	Same
P18_6	Removed ETNB0TXERR	-
P18_7	Same	Same
P18_8	Same	Same
P18_9	Same	Same
P18_10	Same	Same
P18_11	Same	Same
P18_12	Same	Same
P18_13	Same	Same
P18_14	Same	Same
P18_15	Same	Same
P19_0	Same	Same

Port Name	F1KM-S4 (272pin)	F1H ECO (272pin)
P19_1	Same	Same
P19_2	Same	Same
P19_3	Same	Same
P20_0	Same	Same
P20_1	Same	Same
P20_2	Same	Same
P20_3	Same	Same
P20_4	Added INTP22, CAN7RX, INTP9	-
P20_5	Added INTP23, CAN7TX	-
P20_6	Same	Same
P20_7	Same	Same
P20_8	Same	Same
P20_9	Same	Same
P20_10	Same	Same
P20_11	Same	Same
P20_12	Same	Same
P20_13	Same	Same
P20_14	Same	Same
P21_0	Same	Same
P21_1	Same	Same
P21_2	Same	Same
P21_3	Same	Same
P21_4	Same	Same
P22_0	Same	Same
P22_1	Same	Same
P22_2	Same	Same
P22_3	Same	Same
P22_4	Same	Same
P22_5	Same	Same
P22_6	Same	Same
P22_7	Same	Same
P22_8	Same	Same
P22_9	Same	Same
P22_10	Same	Same
P22_11	Same	Same
P22_12	Same	Same
P22_13	Same	Same
P22_14	Same	Same
P22_15	Same	Same

2.12 Input Buffer Control (PISn/JPIS0, PISAn/JPISA0)

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	48		64		80	
				F1KM-S1	F1L	F1KM-S1	F1L	F1KM-S1	F1L
P0_0	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_1	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_2	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_3	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_4	SHMT1	SHMT4	—	—	—	√	√	√	√
P0_5	SHMT1	SHMT4	—	—	—	√	√	√	√
P0_6	SHMT1	SHMT4	—	—	—	√	√	√	√
P0_7	SHMT1	SHMT4	—	—	—	—	—	√	√
P0_8	SHMT1	SHMT4	—	—	—	—	—	√	—
P0_9	SHMT1	SHMT4	—	—	—	—	—	√	√
P0_10	SHMT1	SHMT4	—	—	—	—	—	√	—
P0_11	SHMT1	SHMT4	—	—	—	—	—	√	√
P0_12	SHMT1	SHMT4	—	—	—	—	—	√	√
P8_0	SHMT1	SHMT4	—	√	—	√	—	√	—
P8_1	SHMT1	SHMT4	—	√	—	√	—	√	—
P8_2	SHMT1	SHMT4	—	—	—	√	—	√	—
P8_3	SHMT1	SHMT4	—	—	—	√	—	√	—
P8_4	SHMT1	SHMT4	—	—	—	√	—	√	—
P8_5	SHMT1	SHMT4	—	—	—	√	—	√	—
P8_6	SHMT1	SHMT4	—	—	—	√	—	√	—
P9_0	SHMT1	SHMT4	—	√	—	√	—	√	—
P9_1	SHMT1	SHMT4	—	√	—	√	—	√	—
P9_2	SHMT1	SHMT4	—	—	—	√	—	√	—
P9_3	SHMT1	SHMT4	—	—	—	√	—	√	—
P9_4	SHMT1	SHMT4	—	—	—	—	—	√	—
P9_5	SHMT1	SHMT4	—	—	—	—	—	√	—
P9_6	SHMT1	SHMT4	—	—	—	—	—	√	—
P10_0	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_1	SHMT1	SHMT4	—	√	—	√	—	√	—
P10_2	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_3	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_4	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_5	SHMT1	SHMT4	—	√	—	√	—	√	—
P10_6	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_7	SHMT1	SHMT4	—	√	—	√	—	√	—
P10_8	SHMT1	SHMT4	—	√	—	√	—	√	—
P10_9	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_10	SHMT1	SHMT4	—	√	—	√	—	√	—
P10_11	SHMT1	SHMT4	—	—	—	√	√	√	√
P10_12	SHMT1	SHMT4	—	—	—	√	—	√	—
P10_13	SHMT1	SHMT4	—	—	—	√	√	√	√
P10_14	SHMT1	SHMT4	—	—	—	√	—	√	—
P10_15	SHMT1	SHMT4	—	—	—	—	—	√	√
P11_0	SHMT1	SHMT4	—	—	—	—	—	√	—
P11_1	SHMT1	SHMT4	—	—	—	—	—	√	√
P11_2	SHMT1	SHMT4	—	—	—	—	—	√	—
P11_3	SHMT1	SHMT4	—	—	—	—	—	√	√
P11_4	SHMT1	SHMT4	—	—	—	—	—	√	—

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	100			144				176					
				F1KM	F1K	F1L	F1KM	F1K	F1L	F1M	F1KH	F1KM	F1K	F1L	F1M	F1H
P0_0	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_1	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_2	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_3	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_4	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_5	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_6	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_7	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_8	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P0_9	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_10	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P0_11	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_12	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_13	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P0_14	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P1_0	SHMT1	SHMT4	—	—	—	—	√	√	√	√	√	√	√	√	√	√[5]
P1_1	SHMT1	SHMT4	—	—	—	—	√	—	—	—	√	√	—	—	—	—
P1_2	SHMT1	SHMT4	—	—	—	—	√	√	√	√	√	√	√	√	√	√
P1_3	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P1_4	SHMT1	SHMT4	—	—	—	—	√	√	√	√	√	√	√	√	√	√[5]
P1_5	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P1_6	SHMT1	SHMT4	—	—	—	—	—	√	√	√	—	—	√	√	√	√
P1_7	SHMT1	SHMT4	—	—	—	—	—	√	—	—	—	—	√	—	—	—
P1_8	SHMT1	SHMT4	—	—	—	—	√	√	√	√	√	√	√	√	√	√[5]
P1_9	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P1_10	SHMT1	SHMT4	—	—	—	—	√	√	√	√	√	√	√	√	√	√
P1_11	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P1_12	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	√	√	√
P1_13	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P1_14	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	√	√	√
P1_15	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P2_0	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	√	√	√
P2_1	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P2_2	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	√	√	√
P2_3	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P2_4	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	√	√	√
P2_5	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P2_6	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P2_7	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2_8	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2_9	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2_10	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2_11	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2_12	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2_13	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2_14	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P2_15	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_0	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_1	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_2	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_3	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_4	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_5	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	100			144				176					
				F1KM	F1K	F1L	F1KM	F1K	F1L	F1M	F1KH	F1KM	F1K	F1L	F1M	F1H
P3_6	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_7	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_8	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_9	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_10	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_11	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P3_12	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P8_0	SHMT1	SHMT4	—	√[4]	√	—	√	√	—	—	√	√	√	—	—	—
P8_1	SHMT1	SHMT4	—	√[4]	√	—	√	√	—	—	√	√	√	—	—	—
P8_2	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_3	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_4	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_5	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_6	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_7	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_8	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_9	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_10	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_11	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P8_12	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P9_0	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P9_1	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P9_2	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P9_3	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P9_4	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P9_5	SHMT1	SHMT4	—	√[4]	√	—	—	√	—	—	—	—	√	—	—	—
P9_6	SHMT1	SHMT4	—	√[4]	√	—	—	√	—	—	—	—	√	—	—	—
P10_0	SHMT1	SHMT4	—	√	√	√	√	√	√	√	—	—	√	√	√	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	√
P10_1	SHMT1	SHMT4	—	√	√	—	√	√	—	—	—	—	√	—	—	—
	—	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	—
P10_2	SHMT1	SHMT4	—	√	√	√	√	√	√	√	—	—	√	√	√	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	√
P10_3	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P10_4	SHMT1	SHMT4	—	√	√	√	√	√	√	√	—	—	√	√	√	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	√
P10_5	SHMT1	SHMT4	—	√	√	—	√	√	—	—	—	—	√	—	—	—
	—	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	—
P10_6	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P10_7	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P10_8	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P10_9	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P10_10	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	—
P10_11	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	—
P10_12	SHMT1	SHMT4	—	√	√	—	√	√	—	√	√	√	√	—	√	√
P10_13	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P10_14	SHMT1	SHMT4	—	√	√	—	√	√	—	√	√	√	√	—	√	√
P10_15	SHMT1	SHMT4	—	√[4)]	√	√	√	√	√	√	√	√	√	√	√	√
P11_0	SHMT1	SHMT4	—	√[4)]	√	—	√	√	—	—	√	√	√	—	—	—

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	100			144				176					
				F1KM	F1K	F1L	F1KM	F1K	F1L	F1M	F1KH	F1KM	F1K	F1L	F1M	F1H
P11_1	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P11_2	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P11_3	SHMT1	SHMT4	—	√	√	√1)	√	√	√	√	√	√	√	√	√	√
P11_4	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P11_5	SHMT1	SHMT4	—	√	√	√1)	√	√	√2)	√	√	√	√	√	√	√
P11_6	SHMT1	SHMT4	—	√	√	√	√	√	√	√	√	√	√	√	√	√
P11_7	SHMT1	SHMT4	—	√	√	—	√	√	—	—	√	√	√	—	—	—
P11_8	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P11_9	SHMT1	SHMT4	—	—	—	—	√	√	√	√	√	√	√	√	√	√
P11_10	SHMT1	SHMT4	—	—	—	—	√	√	—	—	—	—	√	—	—	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	—
	—	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
P11_11	SHMT1	SHMT4	—	—	—	—	√	√	—	—	—	—	√	—	—	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	—
	—	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
P11_12	SHMT1	SHMT4	—	—	—	—	√	√	√	√	—	—	√	√	√	√
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	—
P11_13	SHMT1	SHMT4	—	—	—	—	—	√	√	√	—	—	√	√	√	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
P11_14	SHMT1	SHMT4	TTL	—	—	—	—	√	—	—	—	—	√	—	—	—
	—	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
P11_15	SHMT1	SHMT4	—	—	—	—	√	√	√	√	—	—	√	√	√	√
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	—
P12_0	SHMT1	SHMT4	—	—	—	—	√	—	—	—	√	√	—	—	—	—
P12_1	SHMT1	SHMT4	—	—	—	—	√	√	√	√	√	√	√	√	√	√
P12_2	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P12_3	SHMT1	SHMT4	—	—	—	—	—	—	—	√	√	√	√	√	√	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
P12_4	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	√	—	—	—
	—	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
P12_5	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P13_0	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P13_1	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P13_2	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	—
P13_3	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	—
P13_4	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P13_5	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	—
P13_6	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P13_7	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P18_0	SHMT1	SHMT4		—	—	—	√	√	—	—	—	—	√	—	—	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	—
	—	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
P18_1	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P18_2	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P18_3	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P18_4	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P18_5	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P18_6	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P18_7	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	√	—	—	—
	SHMT1	SHMT4	TTL	—	—	—	—	—	—	—	√	√	—	—	—	—
	—	SHMT4	TTL	—	—	—	—	—	—	—	—	—	—	—	—	√
P19_0	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P19_1	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	100			144				176					
				F1KM	F1K	F1L	F1KM	F1K	F1L	F1M	F1KH	F1KM	F1K	F1L	F1M	F1H
P19_2	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P19_3	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_0	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	√	√	√
P20_1	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P20_2	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	√	√	√
P20_3	SHMT1	SHMT4	—	—	—	—	—	—	—	—	√	√	√	—	—	—
P20_4	SHMT1	SHMT4	—	—	—	—	√	√	√	√	√	√	√	√	√	√
P20_5	SHMT1	SHMT4	—	—	—	—	√	√	—	—	√	√	√	—	—	—
P20_6	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_7	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_8	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_9	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_10	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_11	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_12	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_13	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P20_14	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P21_0	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P21_1	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P21_2	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P21_3	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P21_4	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_0	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_1	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_2	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_3	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_4	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_5	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_6	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_7	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_8	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_9	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_10	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_11	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_12	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_13	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_14	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
P22_15	SHMT1	SHMT4	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Note 1. Only available in F1L for Gateway
Note 2. Only available in devices with 1.5- and 2-MB code flash memories
Note 3. -
Note 4. Not F1KM-S4
Note 5. Not on F1H GW

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	233pin				272pin	
				F1KH	F1KM	F1H	F1H	F1KM	F1H
P0_0	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_1	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_2	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_3	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_4	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_5	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_6	SHMT1	SHMT4	—	√	√	√	√	√	√

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	233pin				272pin	
				F1KH	F1KM	F1H	F1H	F1KM	F1H
P0_7	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_8	SHMT1	SHMT4	—	√	√	—	—	√	—
P0_9	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_10	SHMT1	SHMT4	—	√	√	—	—	√	—
P0_11	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_12	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_13	SHMT1	SHMT4	—	√	√	√	√	√	√
P0_14	SHMT1	SHMT4	—	√	√	—	—	√	—
P1_0	SHMT1	SHMT4	—	√	√	√	√	√	√
P1_1	SHMT1	SHMT4	—	√	√	—	—	√	—
P1_2	SHMT1	SHMT4	—	√	√	√	√	√	√
P1_3	SHMT1	SHMT4	—	√	√	—	—	√	—
P1_4	SHMT1	SHMT4	—	√	√	√	√	√	√
P1_5	SHMT1	SHMT4	—	√	√	—	—	√	—
P1_6	SHMT1	SHMT4	—	—	—	√	√	—	√
P1_7	SHMT1	SHMT4	—	—	—	—	—	—	—
P1_8	SHMT1	SHMT4	—	√	√	√	√	√	√
P1_9	SHMT1	SHMT4	—	√	√	—	—	√	—
P1_10	SHMT1	SHMT4	—	√	√	√	√	√	√
P1_11	SHMT1	SHMT4	—	√	√	—	—	√	—
P1_12	SHMT1	SHMT4	—	√	√	√	√	√	√
P1_13	SHMT1	SHMT4	—	√	√	—	—	√	—
P1_14	SHMT1	SHMT4	—	√	√	√	√	√	√
P1_15	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_0	SHMT1	SHMT4	—	√	√	√	√	√	√
P2_1	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_2	SHMT1	SHMT4	—	√	√	√	√	√	√
P2_3	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_4	SHMT1	SHMT4	—	√	√	√	√	√	√
P2_5	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_6	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_7	SHMT1	SHMT4	—	√	√	—	√	√	√
P2_8	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_9	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_10	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_11	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_12	SHMT1	SHMT4	—	√	√	—	√	√	√
P2_13	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_14	SHMT1	SHMT4	—	√	√	—	—	√	—
P2_15	SHMT1	SHMT4	—	√	√	—	—	√	—
P3_0	SHMT1	SHMT4	—	√	√	—	—	√	—
P3_1	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_2	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_3	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_4	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_5	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_6	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_7	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_8	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_9	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_10	SHMT1	SHMT4	—	—	—	—	—	√	—
P3_11	SHMT1	SHMT4	—	—	—	—	—	—	—
P3_12	SHMT1	SHMT4	—	—	—	—	—	—	—

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	233pin				272pin	
				F1KH	F1KM	F1H	F1H	F1KM	F1H
P8_0	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_1	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_2	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_3	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_4	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_5	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_6	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_7	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_8	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_9	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_10	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_11	SHMT1	SHMT4	—	√	√	—	—	√	—
P8_12	SHMT1	SHMT4	—	√	√	—	—	√	—
P9_0	SHMT1	SHMT4	—	√	√	—	—	√	—
P9_1	SHMT1	SHMT4	—	√	√	—	—	√	—
P9_2	SHMT1	SHMT4	—	√	√	—	—	√	—
P9_3	SHMT1	SHMT4	—	√	√	—	—	√	—
P9_4	SHMT1	SHMT4	—	√	√	—	—	√	—
P10_0	SHMT1	SHMT4	—	—	—	√	—	—	—
	SHMT1	SHMT4	TTL	√	√	—	√	√	√
P10_1	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P10_2	SHMT1	SHMT4	—	—	—	√	—	—	—
	SHMT1	SHMT4	TTL	√	√	—	√	√	√
P10_3	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_4	SHMT1	SHMT4	—	—	—	√	—	—	—
	SHMT1	SHMT4	TTL	√	√	—	√	√	√
P10_5	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P10_6	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_7	SHMT1	SHMT4	—	√	√	—	—	√	—
P10_8	SHMT1	SHMT4	—	√	√	—	—	√	—
P10_9	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_10	SHMT1	SHMT4	—	√	√	—	—	√	—
P10_11	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_12	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_13	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_14	SHMT1	SHMT4	—	√	√	√	√	√	√
P10_15	SHMT1	SHMT4	—	√	√	√	√	√	√
P11_0	SHMT1	SHMT4	—	√	√	—	—	√	—
P11_1	SHMT1	SHMT4	—	√	√	√	√	√	√
P11_2	SHMT1	SHMT4	—	√	√	—	—	√	—
P11_3	SHMT1	SHMT4	—	√	√	√	√	√	√
P11_4	SHMT1	SHMT4	—	√	√	—	—	√	—
P11_5	SHMT1	SHMT4	—	√	√	√	√	√	√
P11_6	SHMT1	SHMT4	—	√	√	√	√	√	√
P11_7	SHMT1	SHMT4	—	√	√	—	—	√	—
P11_8	SHMT1	SHMT4	—	√	√	—	—	√	—
P11_9	SHMT1	SHMT4	—	√	√	√	√	√	√
P11_10	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P11_11	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	233pin				272pin	
				F1KH	F1KM	F1H	F1H	F1KM	F1H
P11_12	SHMT1	SHMT4	—	—	—	√	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P11_13	SHMT1	SHMT4	TTL	—	—	√	√	—	√
P11_14	—	SHMT4	TTL	—	—	—	√	—	√
P11_15	SHMT1	SHMT4	—	—	—	√	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P12_0	SHMT1	SHMT4	—	√	√	—	—	√	—
P12_1	SHMT1	SHMT4	—	√	√	√	√	√	√
P12_2	SHMT1	SHMT4	—	√	√	—	—	√	—
P12_3	SHMT1	SHMT4	—	√	√	√	—	√	—
	SHMT1	SHMT4	TTL	—	—	—	√	—	√
P12_4	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P12_5	SHMT1	SHMT4	—	√	√	—	—	√	—
P13_0	SHMT1	SHMT4	—	√	√	—	—	√	—
P13_1	SHMT1	SHMT4	—	√	√	—	—	√	—
P13_2	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P13_3	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P13_4	SHMT1	SHMT4	—	√	√	—	—	√	—
P13_5	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P13_6	SHMT1	SHMT4	—	√	√	—	—	√	—
P13_7	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_0	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P18_1	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_2	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_3	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_4	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_5	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_6	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_7	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P18_8	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P18_9	—	SHMT4	TTL	—	—	—	√	—	√
	SHMT1	SHMT4	TTL	√	√	—	—	√	—
P18_10	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_11	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_12	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_13	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_14	SHMT1	SHMT4	—	√	√	—	—	√	—
P18_15	SHMT1	SHMT4	—	√	√	—	—	√	—
P19_0	SHMT1	SHMT4	—	√	√	—	—	√	—
P19_1	SHMT1	SHMT4	—	√	√	—	—	√	—
P19_2	SHMT1	SHMT4	—	√	√	—	—	√	—
P19_3	SHMT1	SHMT4	—	√	√	—	—	√	—
P20_0	SHMT1	SHMT4	—	√	√	√	√	√	√
P20_1	SHMT1	SHMT4	—	√	√	—	—	√	—
P20_2	SHMT1	SHMT4	—	√	√	√	√	√	√
P20_3	SHMT1	SHMT4	—	√	√	—	—	√	—
P20_4	SHMT1	SHMT4	—	√	√	√	√	√	√

Name	Type 1 (PISn_m=0, PISAn_m=0)	Type 2 (PISn_m=1, PISAn_m=0)	Type 5 (PISAn_m=1)	233pin				272pin	
				F1KH	F1KM	F1H	F1H	F1KM	F1H
P20_5	SHMT1	SHMT4	—	√	√	—	—	√	—
P20_6	SHMT1	SHMT4	—	—	—	—	—	√	—
P20_7	SHMT1	SHMT4	—	—	—	—	—	√	—
P20_8	SHMT1	SHMT4	—	—	—	—	—	√	—
P20_9	SHMT1	SHMT4	—	—	—	—	—	√	—
P20_10	SHMT1	SHMT4	—	—	—	—	—	√	—
P20_11	SHMT1	SHMT4	—	—	—	—	—	√	—
P20_12	SHMT1	SHMT4	—	—	—	—	—	√	—
P20_13	SHMT1	SHMT4	—	—	—	—	—	√	—
P20_14	SHMT1	SHMT4	—	—	—	—	—	√	—
P21_0	SHMT1	SHMT4	—	—	—	—	—	√	—
P21_1	SHMT1	SHMT4	—	—	—	—	—	√	—
P21_2	SHMT1	SHMT4	—	—	—	—	—	√	—
P21_3	SHMT1	SHMT4	—	—	—	—	—	√	—
P21_4	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_0	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_1	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_2	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_3	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_4	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_5	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_6	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_7	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_8	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_9	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_10	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_11	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_12	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_13	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_14	SHMT1	SHMT4	—	—	—	—	—	√	—
P22_15	SHMT1	SHMT4	—	—	—	—	—	√	—

3. CPU System

3.1 Overview

The main differences between the G3KH CPU of the F1KM devices and the G3M CPU core of the F1M/F1H are:

- Removed registers related to the cache operation
- Note the G3KH is very similar to the G3M core used in the F1M/F1H, whereas the G3KH differs more to the G3K core used in the F1L.

3.2 Program Registers

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
r0	√	√	√	√	√	√
r1	√	√	√	√	√	√
r2	√	√	√	√	√	√
r3	√	√	√	√	√	√
r4	√	√	√	√	√	√
r5	√	√	√	√	√	√
r6 to r29	√	√	√	√	√	√
r30	√	√	√	√	√	√
r31	√	√	√	√	√	√
PC	√	√	√	√	√	√

3.3 Basic System Registers

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
EIPC	√	√	√	√	√	√
EIPSW	√	√	√	√	√	√
FEPC	√	√	√	√	√	√
FEPSW	√	√	√	√	√	√
PSW	√	√	√	√	√	√
FPSR	√	√	√	—	√	√
FPEPC	√	√	√	—	√	√
FPST	√	√	√	—	√	√
FPCC	√	√	√	—	√	√
FPCFG	√	√	√	—	√	√
FPEC	√	√	√	—	√	√
EIIC	√	√	√	√	√	√
FEIC	√	√	√	√	√	√
CTPC	√	√	√	√	√	√
CTPSW	√	√	√	√	√	√
CTBP	√	√	√	√	√	√
EIWR	√	√	√	√	√	√
FEWR	√	√	√	√	√	√
MCFG0	√	√	√	√	√	√
RBASE	√	√	√	√	√	√
EBASE	√	√	√	√	√	√
INTBP	√	√	√	√	√	√
MCTL	√	√	√	√	√	√
PID	√	√	√	√	√	√
SCCFG	√	√	√	√	√	√
SCBP	√	√	√	√	√	√
HTCFG0	√	√	√	√	√	√
MEA	√	√	√	√	√	√

ASID	√	√	√	√	√	√
MEI	√	√	√	√	√	√

3.4 Interrupt Function Registers

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
FPIPR	√	√	√	—	√	√
ISPR	√	√	√	√	√	√
PMR	√	√	√	√	√	√
ICSR	√	√	√	√	√	√
INTCFG	√	√	√	√	√	√

3.5 FPU Function Registers

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
FPSR	√	√	√	—	√	√
FPEPC	√	√	√	—	√	√
FPST	√	√	√	—	√	√
FPCC	√	√	√	—	√	√
FPCFG	√	√	√	—	√	√
FPEC	√	√	√	—	√	√

3.6 MPU Function Registers

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
MPM	√	√	√	√	√	√
MPRC	√	√	√	√	√	√
MPBRGN	√	√	√	√	√	√
MPTRGN	√	√	√	√	√	√
MCA	√	√	√	—	√	√
MCS	√	√	√	—	√	√
MCC	√	√	√	—	√	√
MCR	√	√	√	—	√	√
MPLA0	√	√	√	√	√	√
MPUA0	√	√	√	√	√	√
MPAT0	√	√	√	√	√	√
MPLA1	√	√	√	√	√	√
MPUA1	√	√	√	√	√	√
MPAT1	√	√	√	√	√	√
MPLA2	√	√	√	√	√	√
MPUA2	√	√	√	√	√	√
MPAT2	√	√	√	√	√	√
MPLA3	√	√	√	√	√	√
MPUA3	√	√	√	√	√	√
MPAT3	√	√	√	√	√	√
MPLA4	√	√	√	—	√	√

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
MPUA4	√	√	√	—	√	√
MPAT4	√	√	√	—	√	√
MPLA5	√	√	√	—	√	√
MPUA5	√	√	√	—	√	√
MPAT5	√	√	√	—	√	√
MPLA6	√	√	√	—	√	√
MPUA6	√	√	√	—	√	√
MPAT6	√	√	√	—	√	√
MPLA7	√	√	√	—	√	√
MPUA7	√	√	√	—	√	√
MPAT7	√	√	√	—	√	√
MPLA8	√	√	√	—	√	√
MPUA8	√	√	√	—	√	√
MPAT8	√	√	√	—	√	√
MPLA9	√	√	√	—	√	√
MPUA9	√	√	√	—	√	√
MPAT9	√	√	√	—	√	√
MPLA10	√	√	√	—	√	√
MPUA10	√	√	√	—	√	√
MPAT10	√	√	√	—	√	√
MPLA11	√	√	√	—	√	√
MPUA11	√	√	√	—	√	√
MPAT11	√	√	√	—	√	√
MPLA12	√	√	√	—	√	√
MPUA12	√	√	√	—	√	√
MPAT12	√	√	√	—	√	√
MPLA13	√	√	√	—	√	√
MPUA13	√	√	√	—	√	√
MPAT13	√	√	√	—	√	√
MPLA14	√	√	√	—	√	√
MPUA14	√	√	√	—	√	√
MPAT14	√	√	√	—	√	√
MPLA15	√	√	√	—	√	√
MPUA15	√	√	√	—	√	√
MPAT15	√	√	√	—	√	√

3.7 Cache Operation Function Registers

The RH850/ F1KM does not include a cache operation function, so all the following registers return a value of 0 when read, and writing to these registers is ignored.

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
BWERRL	—	—	—	—	—	—
BWERRH	—	—	—	—	—	—
BRERRL	—	—	—	—	—	—
BRERRH	—	—	—	—	—	—
ICTAGL	—	—	—	—	√	√
ICTAGH	—	—	—	—	√	√

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
ICDATL	—	—	—	—	√	√
ICDATH	—	—	—	—	√	√
DCTAGL	—	—	—	—	—	—
DCTAGH	—	—	—	—	—	—
DCDATL	—	—	—	—	—	—
DCDATH	—	—	—	—	—	—
ICCTRL	—	—	—	—	√	√
DCCTRL	—	—	—	—	—	—
ICCFG	—	—	—	—	√	√
DCCFG	—	—	—	—	—	—
ICERR	—	—	—	—	√	√
DCERR	—	—	—	—	—	—

3.8 Registers for Buffer Control

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
FBUFCCTL	√	√	√	—	—	—
CDBCR	—	—	—	—	√	√

3.9 List of PEG Protection Setting Registers

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
PEGSP	√	√	√	—	√	√
PEGG0MK	√	√	√	—	√	√
PEGG0BA	√	√	√	—	√	√
PEGG1MK	√	√	√	—	√	√
PEGG1BA	√	√	√	—	√	√
PEGG2MK	√	√	√	—	√	√
PEGG2BA	√	√	√	—	√	√
PEGG3MK	√	√	√	—	√	√
PEGG3BA	√	√	√	—	√	√

3.10 IPG – Internal Peripheral Guards

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
IPGECRUM	√	√	—	—	—	—
IPGADRUM	√	√	—	—	—	—
IPGENUM	√	√	—	—	—	—
IPGPMTUM0	√	√	—	—	—	—
IPGPMTUM2	√	√	—	—	—	—
IPGPMTUM3	√	√	—	—	—	—
IPGPMTUM4	√	√	—	—	—	—

3.11 SEG — System Error Generator Function

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
SEGCONT	√	√	√	√	√	√
SEGFLAG	√	√	√	√	√	√
SEGADDR	√	√	√	—	—	—

3.12 Inter-Processor Interrupt Control Registers

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
IPIR_CH0	√	—	—	—	—	√
IPIR_CH1	√	—	—	—	—	√
IPIR_CH2	√	—	—	—	—	√
IPIR_CH3	√	—	—	—	—	√

3.13 Inter-CPU Functions

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
G0MEV0	√	—	—	—	—	√
G0MEV0	√	—	—	—	—	√
...	√	—	—	—	—	√
G0MEV31	√	—	—	—	—	√

3.14 CPU2 Boot Up Operation

Symbol	F1KH	F1KM	F1K	F1L	F1M	F1H
BOOTCTRL	√	—	—	—	—	—

4. Address Space

4.1 Overview

Differences in the address space are related to the following memory specification of the devices:

- GlobalRAM is available only on F1H, F1KM-S4 and F1KH-D8.
- CodeFlash Bank A, B are available only on F1H and F1KH-D8.
  Other devices have a single CodeFlash area.
- Local RAM is available as
  - a single address space (F1L, F1K).
  - primary and secondary LocalRAM (F1L).
  - Local RAM CPU1 and Local RAM CPU2 (F1H and F1KH-D8).
- External Memory Interface is not available on F1K

4.2 Address map

Address Space type	F1KH-D8 (8MB)	F1KM-S4 (4MB)	F1KM-S1 (1MB)	F1K (2MB)	F1L (2MB)	F1M (4MB)	F1H (4MB)
Code Flash	0000 0000$_H$ to 003F FFFF$_H$ (4 MB) 0080 0000H to 00BF FFFFH (4 MB)	0000 0000$_H$ to 003F FFFF$_H$ (4 MB)	0000 0000$_H$ to 000F FFFF$_H$ (1 MB)	0000 0000$_H$ to 001F FFFF$_H$ (2 MB)	0000 0000$_H$ to 001F FFFF$_H$ (2 MB)	0000 0000$_H$ to 003F FFFF$_H$ (4 MB)	0000 0000$_H$ to 001F FFFF$_H$ (2 MB) 0080 0000H to 009F FFFFH (2 MB)
Code Flash Extended User area (32KB)	0100 0000$_H$ to 0100 7FFF$_H$	0100 0000$_H$ to 0100 7FFF$_H$	0100 0000$_H$ to 0100 7FFF$_H$	0100 0000$_H$ to 0100 7FFF$_H$	0100 0000$_H$ to 0100 7FFF$_H$	0100 0000$_H$ to 0100 7FFF$_H$	0100 0000H to 0100 7FFFH
On-Chip Peripheral I/O area	1002 0000H to 1002 1FFFH	1002 0000H to 1002 1FFFH	-	-	-	1002 0000H to 1002 1FFFH	1002 0000H to 1002 1FFFH
On-Chip Peripheral I/O area	1003 0000H to 1003 03FFH	1003 0000H to 1003 03FFH	-	-	-	1003 0000H to 1003 03FFH	1003 0000H to 1003 03FFH
On-Chip Peripheral I/O area	1004 0000H to 1004 0FFFH	1004 0000H to 1004 0FFFH	-	-	-	-	-
External memory area (CS0)	2000 0000$_H$ to 20FF FFFF$_H$	2000 0000$_H$ to 20FF FFFF$_H$	-	-	0200 0000$_H$ to 020F FFFF$_H$	2000 0000$_H$ to 200F FFFF$_H$	2000 0000H to 20FF FFFF$_H$
External memory area (CS1)	2200 0000$_H$ to 22FF FFFF$_H$	2200 0000$_H$ to 22FF FFFF$_H$	-	-	0240 0000$_H$ to 024F FFFF$_H$	2200 0000$_H$ to 220F FFFF$_H$	2200 0000H to 22FF FFFF$_H$
External memory area (CS2)	2400 0000$_H$ to 24FF FFFF$_H$	2400 0000$_H$ to 24FF FFFF$_H$	-	-	0280 0000$_H$ to 028F FFFF$_H$	2400 0000$_H$ to 240F FFFF$_H$	2400 0000H to 24FF FFFF$_H$
External memory area (CS3)	2800 0000$_H$ to 28FF FFFF$_H$	2800 0000$_H$ to 28FF FFFF$_H$	-	-	0300 0000$_H$ to 030F FFFF$_H$	2800 0000$_H$ to 280F FFFF$_H$	2800 0000H to 28FF FFFF$_H$
External Serial Flash Memory Area (SFMA)	3000 0000$_H$ to 33FF FFFF$_H$	3000 0000$_H$ to 33FF FFFF$_H$	-	-	-	-	-
Local RAM (CPU2 area)	FE9D 0000H to FE9F FFFFH	-	-	-	-	-	FE9E 0000H to FE9F FFFFH
Local RAM (CPU1 area)	FEBD 0000H to FEBF FFFFH (192KB)	FEBC 0000$_H$ to FEBF FFFF$_H$ (256KB)	FEBE 0000$_H$ to FEBF 7FFF$_H$ (96KB)	FEBD 0000$_H$ to FEBE FFFF$_H$	FEDD 8000$_H$ to FEDD FFFF$_H$ (32KB)	FEBC 0000$_H$ to FEBF FFFF$_H$ (256KB)	FEBE 0000H to FEBF FFFFH (128KB)

Address Space type	F1KH-D8 (8MB)	F1KM-S4 (4MB)	F1KM-S1 (1MB)	F1K (2MB)	F1L (2MB)	F1M (4MB)	F1H (4MB)
					FEDE 0000$_H$ to FEDF FFFF$_H$ (128KB)		FEBC 0000H to FEBF FFFFH (256KB)
RetentionRAM (CPU1 area)	-	FEF0 0000$_H$ to FEF0 FFFF$_H$ (64KB)	FEBF 8000$_H$ to FEBF FFFF$_H$ (32KB)	FEBF 0000$_H$ to FEBF FFFF$_H$	FEE0 0000$_H$ to FEE0 7FFF$_H$ (32KB)	-	-
Local RAM (Self area)	FEDD 0000$_H$ to FEDF FFFF$_H$ (192KB)	FEDC 0000$_H$ to FEDF FFFF$_H$ (256KB)	FEDE 0000 $_H$ to FEDF 7FFF $_H$ (96KB)	FEDD 0000$_H$ to FEDE FFFF$_H$ (128 KB)	-	FEDC 0000$_H$ to FEDF FFFF$_H$ (256KB)	FEDE 0000H to FEDF FFFFH (128KB) FEDC 0000H to FEDF FFFFH (256KB)
Global RAM (Bank A)	FEEB 8000H to FEEF FFFFH (288KB)	FEEE 8000H to FEEF FFFFH (96KB)	-	-	-	-	FEEF 8000H to FEEF FFFFH (32KB)
Retention RAM	FEF0 0000H to FEF0 FFFFH (64KB)	FEF0 0000H to FEF0 FFFFH (64KB)	FEDF 8000$_H$ to FEDF FFFF$_H$ (32KB)	FEDF 0000 $_H$ to FEDF FFFF$_H$ (64 KB)	-	FEF0 0000$_H$ to FEF0 FFFF$_H$ (64KB)	FEF0 0000H to FEF0 FFFFH (64KB)
Global RAM (Bank B)	FEFB 8000H to FEFF FFFFH (288KB)	FEFE 8000H to FEFF FFFFH (96KB)	-	-	-	-	FEFF 8000H to FEFF FFFFH
Data Flash	FF20 0000H to FF23 FFFFH (256KB)	FF20 0000H to FF21 FFFFH (128KB)	FF20 0000$_H$ to FF20 FFFF$_H$ (64KB)	FF20 0000$_H$ to FF20 FFFF$_H$ (64 KB)	FF20 0000$_H$ to FF20 7FFF$_H$ (32 KB)	FF20 0000$_H$ to FF20 FFFF$_H$ (64 KB)	FF20 0000$_H$ to FF20 FFFF$_H$ (64 KB)
On-Chip Peripheral I/O area	FFA0 0000$_H$ to FFFD FFFF$_H$ (6MB – 128KB)	FFA0 0000$_H$ to FFFD FFFF$_H$ (6MB – 128KB)	FFA0 0000$_H$ to FFFD FFFF$_H$ (6MB – 128KB)	FFA0 0000$_H$ to FFFD FFFF$_H$ (6MB – 128KB)	FF40 0000$_H$ to FFFF 7FFF$_H$ (11.97MB)	FFA0 0000$_H$ to FFFD FFFF$_H$ (6MB – 128KB)	FF00 0000H to FFFD FFFFH (16MB – 128KB)
On-Chip Peripheral I/O area (self)	FFFE E000$_H$ to FFFE FFFF$_H$ (8 KB)	FFFE E000$_H$ to FFFE FFFF$_H$ (8 KB)	FFFE E000$_H$ to FFFE FFFF$_H$ (8 KB)	FFFE E000$_H$ to FFFE FFFF$_H$ (8 KB)	-	FFFE E000$_H$ to FFFE FFFF$_H$ (8 KB)	FFFE E000$_H$ to FFFE FFFF$_H$ (8 KB)
On-Chip Peripheral I/O area	FFFF 5000$_H$ to FFFF FFFF$_H$ (44 KB)	FFFF 5000$_H$ to FFFF FFFF$_H$ (44 KB)	FFFF 5000$_H$ to FFFF FFFF$_H$ (44 KB)	FFFF 5000$_H$ to FFFF FFFF$_H$ (44 KB)	-	FFFF 5000$_H$ to FFFF FFFF$_H$ (44 KB)	FFFF 5000$_H$ to FFFF FFFF$_H$ (44 KB)
DMA / INTC		-	-	-	FFFF 8000$_H$ to FFFF AFFF$_H$ (12KB)	-	-

1) 1 MB for some device version only.

5. DMA

5.1 Overview

The F1KM uses the same DMA macro as the F1K/F1M/F1H.

Therefore, differences between F1KM and F1L are same as differences between F1L and F1K/F1M/F1H.

- DMA number of channels:
  - F1KM-S1, F1L, F1M, F1K: 16 channels
  - F1KM-S4, F1H: 32 channels
  - F1KH-D8: 64 channels
- F1KM adds DMA triggers for CAN FD (when available).

5.2 Registers Overview

The DMA base addresses are indicated in the following table.

Base Address Name	F1KH	F1KM	F1K	F1L	F1M	F1H
<DMA0_base>	FFFF 8000 H	FFFF 8000 H	FFFF 8000 H	FFFF 8300H	FFFF 8000 H	FFFF 8000 H
<DMA1_base>	FFFF 9000 H	-	-	-	-	-

Registers are identical between F1K, F1M and F1H. Note the different number of channels between F1K/F1M and F1H.

Due to low similarity between DMA registers of F1L vs. F1K/F1M/F1H a detailed description is not given in this document.

5.3 Interrupt Requests

Base Address Name	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
INTDMA0..15	Yes	Yes	Yes	Yes	Yes	Yes	Yes
INTDMA16..31	Yes	Yes	No	No	No	No	Yes
INTDMA32..63	Yes	No	No	No	No	No	No

Please note that the actual interrupt number may differ between the products.

5.4 DMA Trigger factors

Trigger Number	Name	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
DMACTRG[0]	TAUD0REQSEL0	Yes	Yes	Yes	INTTAUD0I0	←	←	←
DMACTRG[1]	TAUD0REQSEL1	Yes	Yes	Yes	INTTAUD0I4	←	←	←
DMACTRG[2]	TAUD0REQSEL2	Yes	Yes	Yes	INTTAUD0I8	←	←	←
DMACTRG[3]	TAUD0REQSEL3	Yes	Yes	Yes	INTTAUD0I12	←	←	←
DMACTRG[4]	INTADCA0I0	Yes	Yes	Yes	←	←	←	←
DMACTRG[5]	INTADCA0I1	Yes	Yes	Yes	←	←	←	←
DMACTRG[6]	INTADCA0I2	Yes	Yes	Yes	←	←	←	←
DMACTRG[7]	ADC_CONV_END0	Yes	Yes	Yes	←	←	←	←
DMACTRG[8]	INTCSIG0IC	Yes	Yes	Yes	←	←	←	←

Trigger Number	Name	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
DMACTRG[9]	INTCSIG0IR	Yes	Yes	Yes	←	←	←	←
DMACTRG[10]	INTRLIN30UR0	Yes	Yes	Yes	←	←	←	←
DMACTRG[11]	INTRLIN30UR1	Yes	Yes	Yes	←	←	←	←
DMACTRG[12]	INTP0	Yes	Yes	Yes	←	←	←	←
DMACTRG[13]	INTP2	Yes	Yes	Yes	←	←	←	←
DMACTRG[14]	INTP4	Yes	Yes	Yes	←	←	←	←
DMACTRG[15]	See →	RSCANFDRF12	No	No	INTTAUD0I1	←	←	←
DMACTRG[16]	INTRLIN37UR0	Yes	Yes	No	INTTAUD0I5	←	←	←
DMACTRG[17]	TAUD0REQSEL4	Yes	Yes	Yes	INTTAUD0I9	←	←	←
DMACTRG[18]	TAUD0REQSEL5	Yes	Yes	Yes	INTTAUD0I13	←	←	←
DMACTRG[19]	INTRIIC0TI	Yes	Yes	Yes	←	←	←	←
DMACTRG[20]	INTRIIC0RI	Yes	Yes	Yes	←	←	←	←
DMACTRG[21]	INTTAUJ0I0	Yes	Yes	Yes	←	←	←	←
DMACTRG[22]	INTTAUJ0I3	Yes	Yes	Yes	←	←	←	←
DMACTRG[23]	RSCANFDCF0	Yes	Yes	Yes	←	←	Setting prohibited	←
DMACTRG[24]	RSCANFDCF1	Yes	Yes	Yes	←	←	Setting prohibited	←
DMACTRG[25]	See →	RSCANFDRF13	No	No	←	←	Setting prohibited	←
DMACTRG[26]	RSCANFDCF2	Yes	Yes	Yes	←	←	Setting prohibited	←
DMACTRG[27]	RSCANFDCF3	Yes	Yes	Yes	←	←	Setting prohibited	←
DMACTRG[28]	INTCSIH1IC	Yes	Yes	Yes	←	←	←	←
DMACTRG[29]	INTCSIH1IR	Yes	Yes	Yes	←	←	←	←
DMACTRG[30]	INTCSIH1IJC	Yes	Yes	Yes	←	←	←	←
DMACTRG[31]	INTP6	Yes	Yes	Yes	←	←	←	←
DMACTRG[32]	INTP8	Yes	Yes	Yes	←	←	←	←
DMACTRG[33]	TAUB0REQSEL0	Yes	Yes	Yes	INTTAUB0I0	←	←	←
DMACTRG[34]	TAUB0REQSEL1	Yes	Yes	Yes	INTTAUB0I2	←	←	←
DMACTRG[35]	TAUB0REQSEL2	Yes	Yes	Yes	INTTAUB0I4	←	←	←
DMACTRG[36]	TAUB0REQSEL3	Yes	Yes	Yes	INTTAUB0I6	←	←	←
DMACTRG[37]	TAUB0REQSEL4	Yes	Yes	Yes	INTTAUB0I9	←	←	←
DMACTRG[38]	TAUB0REQSEL5	Yes	Yes	Yes	INTTAUB0I11	←	←	←
DMACTRG[39]	See →	INTCSIG4IC	No	No	INTTAUB0I13	←	←	←
DMACTRG[40]	See →	INTCSIG4IR	No	No	INTTAUB0I15	←	←	←
DMACTRG[41]	INTCSIH3IC	Yes	Yes	Yes	←	←	←	←
DMACTRG[42]	INTCSIH3IR	Yes	Yes	Yes	←	←	←	←
DMACTRG[43]	INTCSIH3IJC	Yes	Yes	Yes	←	←	←	←
DMACTRG[44]	INTRLIN32UR0	Yes	Yes	Yes	←	←	←	←
DMACTRG[45]	INTRLIN32UR1	Yes	Yes	Yes	←	←	←	←
DMACTRG[46]	INTTAUJ1I0	Yes	Yes	Yes	←	←	←	←
DMACTRG[47]	INTTAUJ1I2	Yes	Yes	Yes	←	←	←	←
DMACTRG[48]	RSCANFDCF4	Yes	Yes	Yes	←	←	Setting prohibited	←
DMACTRG[49]	RSCANFDCF5	Yes	Yes	Yes	←	←	Setting prohibited	←
DMACTRG[50]	INTRLIN34UR0	Yes	Yes	No	Yes	←	←	←

Trigger Number	Name	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
DMACTRG[51]	INTRLIN34UR1	Yes	Yes	No	Yes	←	←	←
DMACTRG[52]	TAUB1REQSEL0	Yes	Yes	No	INTTAUB1I0	←	←	←
DMACTRG[53]	TAUB1REQSEL1	Yes	Yes	No	INTTAUB1I2	←	←	←
DMACTRG[54]	TAUB1REQSEL2	Yes	Yes	No	INTTAUB1I4	←	←	←
DMACTRG[55]	TAUB1REQSEL3	Yes	Yes	No	INTTAUB1I6	←	←	←
DMACTRG[56]	TAUB1REQSEL4	Yes	Yes	No	INTTAUB1I9	←	←	←
DMACTRG[57]	TAUB1REQSEL5	Yes RSCANFDRF15[*1]	Yes	No	INTTAUB1I11	←	←	←
DMACTRG[58]	See →	INTCSIH4IC	No	No	INTTAUB1I13	←	←	←
DMACTRG[59]	See →	INTCSIH4IR	No	No	INTTAUB1I15	←	←	←
DMACTRG[60]	RSCANFDRF0	Yes	Yes	←	←	←	Setting prohibited	←
DMACTRG[61]	RSCANFDRF1	Yes	Yes	←	←	←	Setting prohibited	←
DMACTRG[62]	RSCANFDRF2	Yes	Yes	←	←	←	Setting prohibited	←
DMACTRG[63]	RSCANFDRF3	Yes	Yes	←	←	←	Setting prohibited	←
DMACTRG[64]	RSCANFDCF6	Yes	Yes	No	INTTAUD0I2	←	←	←
DMACTRG[65]	RSCANFDCF7	Yes	Yes	No	INTTAUD0I6	←	←	←
DMACTRG[66]	INTCSIG1IC	Yes	Yes	No	INTTAUD0I10	←	←	←
DMACTRG[67]	INTCSIG1IR	Yes	Yes	No	INTTAUD0I14	←	←	←
DMACTRG[68]	RSCANFDRF4	Yes	Yes	No	←	←	Setting prohibited	←
DMACTRG[69]	RSCANFDRF5	Yes	Yes	No	←	←	Setting prohibited	←
DMACTRG[70]	INTCSIH0IC	Yes	Yes	←	←	←	←	←
DMACTRG[71]	INTCSIH0IR	Yes	Yes	←	←	←	←	←
DMACTRG[72]	INTCSIH0IJC	Yes	Yes	←	←	←	←	←
DMACTRG[73]	INTP1	Yes	Yes	←	←	←	←	←
DMACTRG[74]	INTP3	Yes	Yes	←	←	←	←	←
DMACTRG[75]	INTP5	Yes	Yes	←	←	←	←	←
DMACTRG[76]	See →	INTCSIH4IJC	No	No	INTTAUD0I3	←	←	←
DMACTRG[77]	INTRLIN37UR1	Yes	Yes	No	INTTAUD0I7	←	←	←
DMACTRG[78]	INTCSIG2IC	Yes	Yes	No	INTTAUD0I11	←	←	←
DMACTRG[79]	INTCSIG2IR	Yes	Yes	No	INTTAUD0I15	←	←	←
DMACTRG[80]	INTTAUJ0I1	Yes	Yes	←	←	←	←	←
DMACTRG[81]	INTTAUJ0I2	Yes	Yes	←	←	←	←	←
DMACTRG[82]	RSCANFDRF6	Yes	Yes	No	Yes	←	Setting prohibited	←
DMACTRG[83]	RSCANFDRF7	Yes	Yes	No	Yes	←	Setting prohibited	←
DMACTRG[84]	See →	RSCANFDRF14	No	←	←	←	Setting prohibited	←
DMACTRG[85]	INTDMAFL	Yes	Yes	←	←	←	←	←
DMACTRG[86]	INTRLIN31UR0	Yes	Yes	←	←	←	←	←
DMACTRG[87]	INTRLIN31UR1	Yes	Yes	←	←	←	←	←
DMACTRG[88]	INTP7	Yes	Yes	←	←	←	←	←
DMACTRG[89]	INTCSIH2IC	Yes	Yes	←	←	←	←	←
DMACTRG[90]	INTCSIH2IR	Yes	Yes	←	←	←	←	←

Trigger Number	Name	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
DMACTRG[91]	INTCSIH2IJC	Yes	Yes	←	←	←	←	←
DMACTRG[92]	See →	No	←	←	INTTAUB0I1	←	←	←
DMACTRG[93]	See →	No	←	←	INTTAUB0I3	←	←	←
DMACTRG[94]	See →	No	←	←	INTTAUB0I5	←	←	←
DMACTRG[95]	See →	No	←	←	INTTAUB0I7	←	←	←
DMACTRG[96]	See →	RSCANFDRF8	No	←	INTTAUB0I8	←	←	←
DMACTRG[97]	See →	RSCANFDRF9	No	←	INTTAUB0I10	←	←	←
DMACTRG[98]	See →	RSCANFDRF10	No	←	INTTAUB0I12	←	←	←
DMACTRG[99]	See →	RSCANFDRF11	No	←	INTTAUB0I14	←	←	←
DMACTRG[100]	INTTAUJ1I1	Yes	Yes	←	←	←	←	←
DMACTRG[101]	INTTAUJ1I3	Yes	Yes	←	←	←	←	←
DMACTRG[102]	INTP9	Yes	Yes	No	Yes	←	←	←
DMACTRG[103]	INTTAUJ2I0	Yes	Yes	←	INTADCA1I0	←	←	←
DMACTRG[104]	INTTAUJ2I1	Yes	Yes	←	INTADCA1I1	←	←	←
DMACTRG[105]	INTTAUJ2I2	Yes	Yes	←	INTADCA1I2	←	←	←
DMACTRG[106]	INTTAUJ2I3	Yes	Yes	←	ADC_CONV_END1	←	←	←
DMACTRG[107]	INTTAUJ3I0	Yes	Yes	←	Setting prohibited	←	←	←
DMACTRG[108]	INTTAUJ3I1	Yes	Yes	←	Setting prohibited	←	←	←
DMACTRG[109]	INTTAUJ3I2	Yes	Yes	←	INTCSIG1IC	←	←	←
DMACTRG[110]	INTTAUJ3I3	Yes	Yes	←	INTCSIG1IR	←	←	←
DMACTRG[111]	INTRLIN33UR0	Yes	Yes	No	Yes	←	←	←
DMACTRG[112]	INTRLIN33UR1	Yes	Yes	No	Yes	←	←	←
DMACTRG[113]	INTRIIC1TI	Yes	Yes	←	INTRLIN35UR0	←	←	←
DMACTRG[114]	INTRIIC1RI	Yes	Yes	←	INTRLIN35UR1	←	←	←
DMACTRG[115]	INTADCA1I0	Yes	Yes	No	INTTAUB1I1	←	←	←
DMACTRG[116]	INTADCA1I1	Yes	Yes	No	INTTAUB1I3	←	←	←
DMACTRG[117]	INTADCA1I2	Yes	Yes	No	INTTAUB1I5	←	←	←
DMACTRG[118]	ADC_CONV_END1	Yes	Yes	No	INTTAUB1I7	←	←	←
DMACTRG[119]	INTRLIN36UR0	Yes	Yes	No	INTTAUB1I8	←	←	←
DMACTRG[120]	INTRLIN36UR1	Yes	Yes	No	INTTAUB1I10	←	←	←
DMACTRG[121]	INTRLIN35UR0	Yes	Yes	No	INTTAUB1I12	←	←	←
DMACTRG[122]	INTRLIN35UR1	Yes	Yes	No	INTTAUB1I14	←	←	←
DMACTRG[123]	INTSENT0RI	Yes	←	←	Setting prohibited	INTCSIG2IC	Setting prohibited	←
DMACTRG[124]	INTSENT1RI	Yes	←	←	Setting prohibited	INTCSIG2IR	Setting prohibited	←
DMACTRG[125]	INTCSIG3IC	Yes	Yes	No	Setting prohibited	INTCSIG3IC	Setting prohibited	←
DMACTRG[126]	INTCSIG3IR	Yes	Yes	No	Setting prohibited	INTCSIG3IR	Setting prohibited	←
DMACTRG[127]	See →	No	←	←	Setting prohibited	←	Setting prohibited	←

6. Reset Controller

6.1 Overview

Device differences for the Reset controller are described in this chapter.

The basic functionality and operation of the Reset Controller is very similar between the F1Kx series and the F1K/F1H/F1M/F1L devices.

The devices have the following Reset sources:

Reset Source	Symbol	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
External reset	$\overline{\text{RESET}}$	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Power-On Clear	POCRES	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Watchdog timer reset	WDTA0RES	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	WDTA1RES	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	WDTA2RES	Yes	-	-	-	-	-	Yes
Clock monitor reset	$\overline{\text{CLMA0RES}}$	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	$\overline{\text{CLMA1RES}}$	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	$\overline{\text{CLMA2RES}}$	Yes	Yes	-	Yes	Yes	Yes	Yes
	$\overline{\text{CLMA3RES}}$	Yes	Yes	Yes	-	-	-	-
Low-voltage indicator reset	$\overline{\text{LVIRES}}$	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Software reset	SWRES	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Debugger reset	$\overline{\text{DBRES}}$	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Core voltage monitor reset	$\overline{\text{CVMRES}}$	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Transition to DeepSTOP mode		Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.2 Reset Controller Registers Overview

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
RESF	FFF8 0760H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
RESFC	FFF8 0768H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
RESFR	FFF8 0860H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
RESFCR	FFF8 0868H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SWRESA	FFF8 0A04H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CYCRBASE	FFF8 3600H	-	-	Yes	Yes	-	-	-

7. Clock Controller

7.1 Overview

Device differences for the clock generation and clock distribution are described in this chapter.
The main differences are:

- PLL(0) control register (PLL(0)C) is different on F1L vs. F1M/F1H vs. F1KM/F1KH due to the different PLL feature set (e.g. SSCG).
- PLL1 only is available on F1KH-D8/F1KM-S4/F1M/F1H
- F1KH/F1KM/F1K cannot output CPUCLK on FOUT.
- F1KH/F1KM/F1K add a clock divider for the CPUCLK.
- On F1KH/F1KM/F1K the CPUCLK is removed as source clock for several peripheral clock domains:
  - Peripheral clock C_ISO_PERIn (n=1,2).
  - LIN
  - CAN
  - CSI
  - IIC

  As a result, the CPU frequency can be scaled without affecting the peripheral operating frequency.
- CSI can select the HSINTOSC as clock source.

7.2 Clock Oscillator Registers Overview

Yes: The register is available
Different: Register content is different depending on device
No: Register is not available on this device
New: Register is added to the device

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
MOSCE	FFF8 1100H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MOSCS	FFF8 1104H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MOSCC	FFF8 1108H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MOSCST	FFF8 110CH	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MOSCSTPM	FFF8 1118H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MOSCM	FFF8 1118H	Yes	Yes	Yes	Yes	No	No	No
SOSCE	FFF8 1200H	Yes	Yes	No	Yes	Yes	Yes	Yes
SOSCS	FFF8 1204H	Yes	Yes	No	Yes	Yes	Yes	Yes
SOSCST	FFF8 120CH	Yes	Yes	No	Yes	Yes	Yes	Yes
ROSCE	FFF8 1000H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ROSCS	FFF8 1004H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ROSCSTPM	FFF8 1018H	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PLL(0)E	FFF8 9000H	Yes	Yes	No	Yes	Yes	Yes	Yes
PLL(0)S	FFF8 9004H	Yes	Yes	No	Yes	Yes	Yes	Yes
PLL(0)C	FFF8 9008H	Yes	Yes	No	Different	Different	Different	Different
PLL0ST	FFF8 900CH	Yes	Yes	No	No	No	Different	Different
PLL1E	FFF8 9100H	Yes	Yes	No	No	No	Yes	Yes
	FFF8 9000H	No	No	Yes	No	No	No	No
PLL1S	FFF8 9104H	Yes	Yes	No	No	No	Yes	Yes
	FFF8 9004H	No	No	Yes	No	No	No	No
PLL1C	FFF8 9108H	Yes	Yes	No	No	No	Yes	Yes
	FFF8 9008H	No	No	Yes	No	No	No	No
CKSC_PLL(0)IS_CTL	FFF8 A700H	Yes	Yes	No	Yes	No	No	No
CKSC_PLL(0)IS_ACT	FFF8 A708H	Yes	Yes	No	Yes	No	No	No
CKSC_PLL1IS_CTL	FFF8 A710H	New	New	No	No	No	No	No
	FFF8 A700H	No	No	Yes	No	No	No	No
CKSC_PLL1IS_ACT	FFF8 A718H	New	New	No	No	No	No	No
	FFF8 A708H	No	No	Yes	No	No	No	No
CKSC_PPLLCLKS_CTL	FFF8 A010H	Yes	Yes	Yes	Yes	No	No	No

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
CKSC_PPLLCLKS_ACT	FFF8 A018H	Yes	Yes	Yes	Yes	No	No	No
ROSCUT	FFF8 101C H	Yes	Yes	Yes	Yes	No	No	No

7.3 Clock Selector Control Register Overview

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
CKSC_AWDTAD_CTL	FFF8 2000H	Same	Same	Same	Same	Same	Same
CKSC_AWDTAD_ACT	FFF8 2008H	Same	Same	Same	Same	Same	Same
CKSC_AWDTAD_STPM	FFF8 2018H	Same	Same	Same	Same	Same	Same
CKSC_ATAUJS_CTL	FFF8 2100H	Same	Same	Same	Same	Same	Same
CKSC_ATAUJS_ACT	FFF8 2108H	Same	Same	Same	Same	Same	Same
CKSC_ATAUJD_CTL	FFF8 2200H	Same	Same	Same	Same	Same	Same
CKSC_ATAUJD_ACT	FFF8 2208H	Same	Same	Same	Same	Same	Same
CKSC_ATAUJD_STPM	FFF8 2218H	Same	Same	Same	Same	Same	Same
CKSC_ARTCAS_CTL	FFF8 2300H	Same	Same	Same	Same	Same	Same
CKSC_ARTCAS_ACT	FFF8 2308H	Same	Same	Same	Same	Same	Same
CKSC_ARTCAD_CTL	FFF8 2400H	Same	Same	Same	Same	Same	Same
CKSC_ARTCAD_ACT	FFF8 2408H	Same	Same	Same	Same	Same	Same
CKSC_ARTCAD_STPM	FFF8 2418H	Same	Same	Same	Same	Same	Same
CKSC_AADCAS_CTL	FFF8 2500H	Same	Same	Same	Same	Same	Same
CKSC_AADCAS_ACT	FFF8 2508H	Same	Same	Same	Same	Same	Same
CKSC_AADCAD_CTL	FFF8 2600H	Same	Same	Same	Same	Same	Same
CKSC_AADCAD_ACT	FFF8 2608H	Same	Same	Same	Same	Same	Same
CKSC_AADCAD_STPM	FFF8 2618H	Same	Same	Same	Same	Same	Same
CKSC_AFOUTS_CTL	FFF8 2700H	Same	Same	Same	Same	Same	Same
CKSC_AFOUTS_ACT	FFF8 2708H	Same	Same	Same	Same	Same	Same
CKSC_AFOUTS_STPM	FFF8 2718H	Same	Same	Same	Same	Same	Same
CKSC_CPUCLKS_CTL	FFF8 A000H	Same	Same	Same	Same	Same	Same
CKSC_CPUCLKS_ACT	FFF8 A008H	Same	Same	Same	Same	Same	Same
CKSC_CPUCLKD_CTL	FFF8 A100H	Changed	Changed	Changed	Same	Same	Same
CKSC_CPUCLKD_ACT	FFF8 A108H	Changed	Changed	Changed	Same	Same	Same
CKSC_IPERI1S_CTL	FFF8 A200H	Changed	Changed	Changed	Same	Same	Same
CKSC_IPERI1S_ACT	FFF8 A208H	Same	Same	Same	Same	Same	Same
CKSC_IPERI2S_CTL	FFF8 A300H	Changed	Changed	Changed	Same	Same	Same
CKSC_IPERI2S_ACT	FFF8 A308H	Same	Same	Same	Same	Same	Same
CKSC_ILINS_CTL	FFF8 A400H	Changed	Changed	Changed	Same	Same	Same
CKSC_ILINS_ACT	FFF8 A408H	Changed	Changed	Changed	Same	Same	Same
CKSC_IADCAS_CTL	FFF8 A500H	Same	Same	Same	Same	Same	Same
CKSC_IADCAS_ACT	FFF8 A508H	Same	Same	Same	Same	Same	Same
CKSC_IADCAD_CTL	FFF8 A600H	Same	Same	Same	Same	Same	Same

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
CKSC_IADCAD_ACT	FFF8 A608H	Same	Same	Same	Same	Same	Same
CKSC_ILIND_CTL	FFF8 A800H	Same	Same	Same	Same	Same	Same
CKSC_ILIND_ACT	FFF8 A808H	Same	Same	Same	Same	Same	Same
CKSC_ILIND_STPM	FFF8 A818H	Same	Same	Same	Same	Same	Same
CKSC_ICANS_CTL	FFF8 A900H	Changed	Changed	Changed	Same	Same	Same
CKSC_ICANS_ACT	FFF8 A908H	Same	Same	Same	Same	Same	Same
CKSC_ICANS_STPM	FFF8 A918H	Same	Same	Same	Same	Same	Same
CKSC_ICANOSCD_CTL	FFF8 AA00H	Same	Same	Same	Same	Same	Same
CKSC_ICANOSCD_ACT	FFF8 AA08H	Same	Same	Same	Same	Same	Same
CKSC_ICANOSCD_STPM	FFF8 AA18H	Same	Same	Same	Same	Same	Same
CKSC_ICSIS_CTL	FFF8 AB00H	Changed	Changed	Changed	Same	Same	Same
CKSC_ICSIS_ACT	FFF8 AB08H	Changed	Changed	Changed	Same	Same	Same
CKSC_IIICS_CTL	FFF8 AC00H	Changed	Changed	Changed	No	Same	Same
CKSC_IIICS_ACT	FFF8 AC08H	Same	Same	Same	No	Same	Same

8. Stand-By Controller

8.1 Overview

Device differences related to the stand-by controller are described in this chapter.

The main differences are:

- The ADCA0 interrupts (INTADCA0In (n=0..2)) can be selected as a ‘Wake-Up Factor 2’ in order to switch from DEEPSTOP mode to Cyclic RUN mode when using the LPS.
- CSIG0 can operate in CyclicRUN mode.
- Depending on stand-by mode, the CPU clock source after wake-up from standby mode can be different.

8.2 Registers overview

Name	Address	F1KH F1KM	F1K	F1L	F1M	F1H
STBC0PSC	FFF8 0100H	Same	Same	Same	Same	Same
STBC0STPT	FFF8 0110H	Same	Same	Same	Same	Same
WUF0	FFF8 0400H	Same	Same	Same	Same	Same
WUF1	FFF8 0410H	New	-	-	-	-
WUF20	FFF8 0520H	Same	Same	Same	Same	Same
WUF_ISO0	FFF8 8110H	Same	Same	Same	Same	Same
WUFMSK0	FFF8 0404H	Same	Same	Same	Same	Same
WUFMSK1	FFF8 0414H	New	-	-	-	-
WUFMSK20	FFF8 0524H	Same	Same	Same	Same	Same
WUFMSK_ISO0	FFF8 8114H	Same	Same	Same	Same	Same
WUFC0	FFF8 0408H	Same	Same	Same	Same	Same
WUFC1	FFF8 0418H	New	-	-	-	-
WUFC20	FFF8 0528H	Same	Same	Same	Same	Same
WUFC_ISO0	FFF8 8118H	Same	Same	Same	Same	Same
IOHOLD	FFF8 0B00H	Same	Same	Same	Same	Same

8.3 CPU clock source after wake-up from standby mode

When leaving the DEEPSTOP mode the CPU clock source is different on F1KH/F1KM/F1K than on F1L/F1M/F1H.
The CPU always starts on the HS IntOSC.

8.3.1 STOP mode and CYCLICSTOP mode

There are no differences between F1KH/F1KM/F1K and F1L/F1M/F1H.
The CPU will re-start on the same clock source that it used when entering the STOP mode or CYCLICSTOP mode

8.3.2 DEEPSTOP

On F1L/F1M/F1H the CPU will start on the same clock source that it used when entering the DEEPSTOP mode.

On F1KH/F1KM/F1K the CPU will always start on the HSINTOSC.
The MAINOSC will be started automatically when leaving the DEEPSTOP mode. CPU will start operation after the

MAINOSC becomes stable (if the MAINOSC is started automatically).
The PLL must be enabled by SW.

8.4 Wake-up factors 1 (WUF0)

Number	Name	F1KH-D8 F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
0	TNMI	Yes	←	←	←	←	←
1	WDTA0NMI	Yes	←	←	←	←	←
2	INTLVIL	Yes	←	←	←	←	←
5	INTP0	Yes	←	←	←	←	←
6	INTP1	Yes	←	←	←	←	←
7	INTP2	Yes	←	←	←	←	←
8	INTWDTA0	Yes	←	←	←	←	←
9	INTP3	Yes	←	←	←	←	←
10	INTP4	Yes	←	←	←	←	←
11	INTP5	Yes	←	←	←	←	←
12	INTP10	Yes	←	←	←	←	←
13	INTP11	Yes	←	←	←	←	←
14	WUTRG1	Yes	←	←	←	←	←
15	INTTAUJ0I0	Yes	←	←	←	←	←
16	INTTAUJ0I1	Yes	←	←	←	←	←
17	INTTAUJ0I2	Yes	←	←	←	←	←
18	INTTAUJ0I3	Yes	←	←	←	←	←
19	WUTRG0	Yes	←	←	←	←	←
20	INTP6	Yes	←	←	←	←	←
21	INTP7	Yes	←	←	←	←	←
22	INTP8	Yes	←	←	←	←	←
23	INTP12	Yes	←	←	←	←	←
24	INTP9	Yes	←	←	←	←	←
25	INTP13	Yes	←	←	←	←	←
26	INTP14	Yes	No	Yes	←	←	←
27	INTP15	Yes	No	Yes	←	←	←
28	INTRTCA01S	Yes	←	←	←	←	←
29	INTRTCA0AL	Yes	←	←	←	←	←
30	INTRTCA0R	Yes	←	←	←	←	←
31	INTDCUTDI	Yes	←	←	←	←	←

8.5 Wake-up factors 1 (WUF1)

Number	Name	F1KH-D8 F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
0	INTP16	Yes	-	-	-	-	-
1	INTP17	Yes	-	-	-	-	-
2	INTP18	Yes	-	-	-	-	-

Number	Name	F1KH-D8 F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
3	INTP19	Yes	-	-	-	-	-
4	INTP20	Yes	-	-	-	-	-
5	INTP21	Yes	-	-	-	-	-
6	INTP22	Yes	-	-	-	-	-
7	INTP23	Yes	-	-	-	-	-
8	INTTAUJ2I0	Yes	Yes	-	-	-	-
9	INTTAUJ2I1	Yes	Yes	-	-	-	-
10	INTTAUJ2I2	Yes	Yes	-	-	-	-
11	INTTAUJ2I3	Yes	Yes	-	-	-	-

8.6 Wake-up factors 1 (WUF_ISO0)

Number	Name	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
1	INTKR0	Yes	Yes	Yes	←	←	←	←
2	INTRCANGRECC0	Yes	Yes	Yes	←	←	←	←
3	INTRCAN0REC	Yes	Yes	Yes	←	←	←	←
4	INTRCAN1REC	Yes	Yes	Yes	←	←	←	←
5	INTRCAN2REC	Yes	Yes	Yes	←	←	←	←
6	INTRCAN3REC	Yes	Yes	Yes	←	←	←	←
7	INTRCAN4REC	Yes	Yes	Yes	←	←	←	←
8	INTRCAN5REC	Yes	Yes	Yes	←	←	←	←
9	INTRCAN6REC	Yes	Yes	-	Yes	Yes	-	INTRCANGRECC1
10	INTRCAN7REC	Yes	Yes	-	-	-	-	INTRCAN6REC
11	INTRCANGRECC1	-	-	-	-	-	-	INTRCAN7REC
12	INTRCAN8REC	-	-	-	-	-	-	-
13	INTRCAN9REC	-	-	-	-	-	-	-
14	INTRCAN10REC	-	-	-	-	-	-	-
15	INTRCAN11REC	-	-	-	-	-	-	-

8.7 Wake-up factors 2

Number	Name	F1KH-D8 F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
0	INTADCA0I0	Yes	←	←	←	←	←
1	INTADCA0I1	Yes	←	←	←	←	←
2	INTADCA0I2	Yes	←	←	←	←	←
3	INTRLIN30	Yes	←	←	←	←	←
4	INTTAUJ0I0	Yes	←	←	←	←	←
5	INTTAUJ0I1	Yes	←	←	←	←	←
6	INTTAUJ0I2	Yes	←	←	←	←	←
7	INTTAUJ0I3	Yes	←	←	←	←	←
8	INTRLIN31	Yes	←	←	←	←	←

Number	Name	F1KH-D8 F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
9	INTRLIN32	Yes	←	←	←	←	←
10	INTRTCA01S	Yes	←	←	←	←	←
11	INTRTCA0AL	Yes	←	←	←	←	←
12	INTRTCA0R	Yes	←	←	←	←	←
13	INTRLIN33	Yes	←	←	←	←	←
14	INTRLIN34	Yes	-	Yes	←	←	←
15	INTRLIN35	Yes	-	Yes	←	←	←
16	INTRLIN36	Yes	-	-	-	-	-
17	INTRLIN37	Yes	-	-	-	-	-
18	INTTAUJ2I0	Yes	←	-	-	-	-
19	INTTAUJ2I1	Yes	←	-	-	-	-
20	INTTAUJ2I2	Yes	←	-	-	-	-
21	INTTAUJ2I3	Yes	←	-	-	-	-

9. Low-Power Sampler (LPS)

9.1 Overview

Device differences for the Low-Power Sampler (LPS) are described in this chapter.

For the F1KM/F1K several features have been added to the LPS. These are

- Added interrupts for digital or analog port comparisons
- Added support for pins of analog multiplexer

9.2 Register Base Address

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
<LPS_base>	FFF8 3000H	←	←	←	FFBC 2000H

9.3 Clock Supply

Unit Clock Name	F1Kx	F1K	F1H	F1M	F1L
Register access clock	CPUCLK_L, EMCLK	CPUCLK2 EMCLK	EMCLK	←	←
Operating clock	EMCLK	←	-	-	-

9.4 Interrupt Requests

Interrupt signal	Interrupt Number					DMA Trigger Number				
	F1Kx	F1K	F1H	F1M	F1L	F1KM	F1K	F1L	F1M	F1H
INTCWEND	112	←	←	←	104	-	-	-	-	-
INTADCA0I0	18	←	←	←	10	4	←	←	←	←
INTADCA0I1	19	←	←	←	11	5	←	←	←	←
INTADCA0I2	20, 32	←	←	←	12	6	←	←	←	←
INTDPE	356	←	-	-	-	-	-	-	-	-
INTAPE	357	←	-	-	-	-	-	-	-	-

9.5 External Input/Output Signals

Unit Signal Name	External Input/Output Signals				
	F1Kx	F1K	F1H	F1M	F1L
DPO	DPO	←	←	←	←
DPSELk	SELDPk	←	←	←	←
DPINm	DPINm	←	←	←	←
APO	APO	←	←	←	←
ADCA0SELk	ADCA0SELk	←	-	-	-
ADCA0Im	ADCA0Im	←	←	←	←

Note: The configuration of the pins for the analog multiplexer is part of the port configuration.

9.6 Registers overview

Name	Address	F1Kx	F1K	F1H	F1M	F1L
SCTLR	<LPS0_base > + 00H	Same	Same	Same	Same	Same
EVFR	<LPS0_base > + 04H	Same	Same	Same	Same	Same
DPSELR0	<LPS0_base > + 08H	Same	Same	Same	Same	Same
DPSELRM	<LPS0_base > + 0CH	Same	Same	Same	Same	Same
DPSELRH	<LPS0_base > + 10H	Same	Same	Same	Same	Same
DPDSR0	<LPS0_base > + 14H	Same	Same	Same	Same	Same
DPDSRM	<LPS0_base > + 18H	Same	Same	Same	Same	Same
DPDSRH	<LPS0_base > + 1CH	Same	Same	Same	Same	Same
DPDIMR0	<LPS0_base > + 20H	Same	Same	Same	Same	Same
DPDIMR1	<LPS0_base > + 24H	Same	Same	Same	Same	Same
DPDIMR2	<LPS0_base > + 28H	Same	Same	Same	Same	Same
DPDIMR3	<LPS0_base > + 2CH	Same	Same	Same	Same	Same
DPDIMR4	<LPS0_base > + 30H	Same	Same	Same	Same	Same
DPDIMR5	<LPS0_base > + 34H	Same	Same	Same	Same	Same
DPDIMR6	<LPS0_base > + 38H	Same	Same	Same	Same	Same
DPDIMR7	<LPS0_base > + 3CH	Same	Same	Same	Same	Same
CNTVAL	<LPS0_base > + 40H	Same	Same	Same	Same	Same
SOSTR	<LPS0_base > + 44H	Same	Same	Same	Same	Same

10. Clocked Serial Interface G (CSIG)

10.1 Overview

The functional feature set of the CSIG between F1Kx/F1K and F1L/F1M/F1H is identical.

Applicable differences may result in the modified clock selection on F1Kx/F1K.

10.2 Register Base Address

Base Address Name	F1KH	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
<CSIG0_base>	FFD8 8000$_H$	←	←	←	←	←	FFDB 0000$_H$
<CSIG1_base>	FFD8 A000$_H$	←	-	←	←	←	FFDB 2000$_H$
<CSIG2_base>	FFD8 C000H	←	-	-	FFD8 C000H	-	-
<CSIG3_base>	FFD8 E000H	←	-	-	FFD8 E000H	-	-
<CSIG4_base>	FFD9 2000H	-	-	-	-	-	-

10.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1H	F1M	F1L
CSIGn	PCLK	CKSCLK_ICSI	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_ICSI	CPUCLK2, CKSCLK_ICSI	CKSCLK_ICSI	←	←

10.4 Interrupt Requests

Base Address Name	Request / Trigger	F1KH	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
CSIG0								
INTCSIGTIC	Interrupt	27,118	←	←	27,118	←	←	19,110
	DMA Trigger	8	←	←	←	←	←	←
INTCSIGTIR	Interrupt	28,119	←	←	28,119	←	←	20,111
	DMA Trigger	9	←	←	←	←	←	←
INTCSIGTIRE	Interrupt	57	←	←	←	←	←	49
	DMA Trigger	-	-	-	-	-	-	-
CSIG1								
INTCSIGTIC	Interrupt	223	←	-	223	←	←	215
	DMA Trigger	66	←	-	109	←	←	45
INTCSIGTIR	Interrupt	224	←	-	224	←	←	216
	DMA Trigger	67	←	-	110	←	←	46
INTCSIGTIRE	Interrupt	225	←	-	225	←	←	217
	DMA Trigger	-	-	-	-	-	-	-
CSIG2								
INTCSIGTIC	Interrupt	326	←	-	-	326	-	-

Base Address Name	Request / Trigger	F1KH	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
	DMA Trigger	78	←	-	123	←	-	-
INTCSIGTIR	Interrupt	327	←	-	-	327	-	-
	DMA Trigger	79	←	-	124	←	-	-
INTCSIGTIRE	Interrupt	328	←	-	-	328	-	-
	DMA Trigger	-	-	-	-	-	-	-
CSIG3								
INTCSIGTIC	Interrupt	329	←	-	329	←	-	-
	DMA Trigger	125	←	-	125	←	-	-
INTCSIGTIR	Interrupt	330	←	-	330	←	-	-
	DMA Trigger	126	←	-	126	←	-	-
INTCSIGTIRE	Interrupt	331	←	-	331	←	-	-
	DMA Trigger	-	-	-	-	-	-	-
CSIG4								
INTCSIGTIC	Interrupt	98	-	-	-	-	-	-
	DMA Trigger	39	-	-	-	-	-	-
INTCSIGTIR	Interrupt	99	-	-	-	-	-	-
	DMA Trigger	40	-	-	-	-	-	-
INTCSIGTIRE	Interrupt	100	-	-	-	-	-	-
	DMA Trigger	-	-	-	-	-	-	-

10.5 Reset Sources

Base Address Name	F1Kx	F1K	F1L	F1M	F1H
CSIGn	All reset sources (ISORES)	←	←	←	←

10.6 Registers overview

Name	Address	F1Kx	F1K	F1L	F1M	F1H
CSIGnCTL0	<CSIGn_base> + 0000H	Same	Same	Same	Same	Same
CSIGnCTL1	<CSIGn_base> + 0010H	Same	Same	Same	Same	Same
CSIGnCTL2	<CSIGn_base> + 0014H	Same	Same	Same	Same	Same
CSIGnSTR0	<CSIGn_base> + 0004H	Same	Same	Same	Same	Same
CSIGnSTCR0	<CSIGn_base> + 0008H	Same	Same	Same	Same	Same
CSIGnBCTL0	<CSIGn_base> + 1000H	Same	Same	Same	Same	Same
CSIGnCFG0	<CSIGn_base> + 1010H	Same	Same	Same	Same	Same
CSIGnTX0W	<CSIGn_base> + 1004H	Same	Same	Same	Same	Same
CSIGnTX0H	<CSIGn_base> + 1008H	Same	Same	Same	Same	Same
CSIGnRX0	<CSIGn_base> + 100CH	Same	Same	Same	Same	Same
CSIGnEMU	<CSIGn_base> + 0018H	Same	Same	Same	Same	Same

11. Clocked Serial Interface H (CSIH)

11.1 Overview

The functional feature set of the CSIH between F1Kx/F1K and F1L/F1M/F1H is identical.

Applicable differences may result in the modified clock selection on F1Kx/F1K.

11.2 Register Base Address

Base Address Name	F1KH	F1KM	F1K	F1H	F1M	F1L
<CSIH0_base>	FFD8 0000$_H$	←	←	←	←	←
<CSIH1_base>	FFD8 2000$_H$	←	←	←	←	←
<CSIH2_base>	FFD8 4000$_H$	←	←	←	←	←
<CSIH3_base>	FFD8 6000$_H$	←	←	←	←	←
<CSIH4_base>	FFD9 0000$_H$	-	-	-	-	-

11.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1H	F1M	F1L
CSIHn	PCLK	CKSCLK_ICSI	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_ICSI	CPUCLK2 CKSCLK_ICSI	CKSCLK_ICSI	←	←

11.4 Interrupt Requests

Base Address Name	Request / Trigger	F1KH	F1KM	F1K	F1H	F1M	F1L
CSIH0							
INTCSIHTIC	Interrupt	29	←	←	←	←	21
	DMA Trigger	70	←	70	←	←	6
INTCSIHTIR	Interrupt	30	←	←	←	←	22
	DMA Trigger	71	←	71	←	←	7
INTCSIHTIRE	Interrupt	31	←	←	←	←	23
	DMA Trigger	-	-	-	-	-	-
INTCSIHTIJC	Interrupt	20, 32	←	20, 32	←	←	24
	DMA Trigger	72	←	72	←	←	8
CSIH1							
INTCSIHTIC	Interrupt	16,116	←	←	←	←	8, 108
	DMA Trigger	28	←	←	←	←	←
INTCSIHTIR	Interrupt Number	17,117	←	←	←	←	9, 109
	DMA Trigger	29	←	←	←	←	←
INTCSIHTIRE	Interrupt Number	27, 118	←	←	←	←	19, 110
	DMA Trigger	-	-	-	-	-	-
INTCSIHTIJC	Interrupt Number	28, 119	←	←	←	←	20, 111
	DMA Trigger	30	←	←	←	←	←
CSIH2							
INTCSIHTIC	Interrupt	8, 132	←	←	←	←	0, 124

	DMA Trigger	89	←	←	←	←	25
INTCSIHTIR	Interrupt	10, 133	←	←	←	←	29, 125
	DMA Trigger	90	←	←	←	←	26
INTCSIHTIRE	Interrupt	11, 134	←	←	←	←	30, 126
	DMA Trigger	-	←	-	-	-	-
INTCSIHTIJC	Interrupt	12, 135	←	←	←	←	31, 127
	DMA Trigger	91	←	←	←	←	27
CSIH3							
INTCSIHTIC	Interrupt	9, 158	←	←	←	←	1, 150
	DMA Trigger	41	←	←	←	←	←
INTCSIHTIR	Interrupt	13, 159	←	←	←	←	5, 151
	DMA Trigger	42	←	←	←	←	←
INTCSIHTIRE	Interrupt	14, 160	←	←	←	←	6, 152
	DMA Trigger	-	-	-	-	-	-
INTCSIHTIJC	Interrupt	15, 161	←	←	←	←	7, 153
	DMA Trigger	43	←	←	←	←	←
CSIH4							
INTCSIHTIC	Interrupt	124	-	-	-	-	-
	DMA Trigger	58	-	-	-	-	-
INTCSIHTIR	Interrupt	125	-	-	-	-	-
	DMA Trigger	59	-	-	-	-	-
INTCSIHTIRE	Interrupt	126	-	-	-	-	-
	DMA Trigger	-	-	-	-	-	-
INTCSIHTIJC	Interrupt	127	-	-	-	-	-
	DMA Trigger	76	-	-	-	-	-

11.5 Reset Sources

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
CSIHn	All reset sources (ISORES)	←	←	←	←

11.6 Registers overview

Name	Address	F1Kx	F1K	F1L	F1M	F1H
CSIHnCTL0	<CSIHn_base> + 0000H	Same	Same	Same	Same	Same
CSIHnCTL1	<CSIHn_base> + 0010H	Same	Same	Same	Same	Same
CSIHnCTL2	<CSIHn_base> + 0014H	Same	Same	Same	Same	Same
CSIHnSTR0	<CSIHn_base> + 0004H	Same	Same	Same	Same	Same
CSIHnSTCR0	<CSIHn_base> + 0008H	Same	Same	Same	Same	Same
CSIHnMCTL0	<CSIHn_base> + 1040H	Same	Same	Same	Same	Same
CSIHnMCTL1	<CSIHn_base> + 1000H	Same	Same	Same	Same	Same
CSIHnMCTL2	<CSIHn_base> + 1004H	Same	Same	Same	Same	Same
CSIHnMRWP0	<CSIHn_base> + 1018H	Same	Same	Same	Same	Same
CSIHnCFG0	<CSIHn_base> + 1044H	Same	Same	Same	Same	Same
CSIHnCFG1	<CSIHn_base> + 1048H	Same	Same	Same	Same	Same
CSIHnCFG2	<CSIHn_base> + 104CH	Same	Same	Same	Same	Same
CSIHnCFG3	<CSIHn_base> + 1050H	Same	Same	Same	Same	Same
CSIHnCFG4	<CSIHn_base> + 1054H	Same	Same	Same	Same	Same
CSIHnCFG5	<CSIHn_base> + 1058H	Same	Same	Same	Same	Same

Name	Address	F1Kx	F1K	F1L	F1M	F1H
CSIHnCFG6	<CSIHn_base> + 105CH	Same	Same	Same	Same	Same
CSIHnCFG7	<CSIHn_base> + 1060H	Same	Same	Same	Same	Same
CSIHnTX0W	<CSIHn_base> + 1008H	Same	Same	Same	Same	Same
CSIHnTX0H	<CSIHn_base> + 100CH	Same	Same	Same	Same	Same
CSIHnRX0W	<CSIHn_base> + 1010H	Same	Same	Same	Same	Same
CSIHnRX0H	<CSIHn_base> + 1014H	Same	Same	Same	Same	Same
CSIHnEMU	<CSIHn_base> + 0018H	Same	Same	Same	Same	Same
CSIHnBRS0	<CSIHn_base> + 1068H	Same	Same	Same	Same	Same
CSIHnBRS1	<CSIHn_base> + 106CH	Same	Same	Same	Same	Same
CSIHnBRS2	<CSIHn_base> + 1070H	Same	Same	Same	Same	Same
CSIHnBRS3	<CSIHn_base> + 1074H	Same	Same	Same	Same	Same

12. LIN/UART Interface 2 (RLIN2)

12.1 Overview

The F1KM/F1K uses the same RLIN2 macro as the F1M/F1H.

The main differences between the device versions are

- F1KM/F1K uses a different interrupt naming than F1M/F1H.
- Naming for RLIN2 channels 8 and 9 is different between F1L (RLIN21n) and F1M/F1H/F1K/F1KM (RLIN242)

12.2 Register Base Address

Base Address Name	F1KH	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
<RLIN240_base>	FFCE 0000H	←	←	←	←	←	←
<RLIN241_base>	FFCE 0080H	←	-	FFCE 0080H	←	←	←
<RLIN242_base>	FFCE 0100H	←	-	FFCE 0100H	←	←	-
<RLIN243_base>	FFCE 0180H	-	-	-	-	-	-
<RLIN210_base>	-	-	-	-	-	-	FFCE 0100H
<RLIN211_base>	-	-	-	-	-	-	FFCE 0120H

12.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1H	F1M	F1L
RLIN24n	LIN communication clock sources	CKSCLK_ILIN	←	←	←	←
	Register access	CPUCLK_L CKSCLK_ILIN	CPUCLK2 CKSCLK_ILIN	CKSCLK_ILIN	←	←
RLIN21n	LIN communication clock sources	-	-	-	-	CKSCLK_ILIN
	Register access	-	-	-	-	CKSCLK_ILIN

12.4 Interrupt Requests

Unit Interrupt Signal	F1KH	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
RLIN240							
INTRLIN20	58	←	←	-	58	←	-
INTRLIN0	-	-	-	58	-	-	50
INTRLIN21	59	←	←	-	59	←	-
INTRLIN1	-	-	-	59	-	-	51
INTRLIN22	162	←	←	-	162	←	-
INTRLIN2	-	-	-	162	-	-	154
INTRLIN23	163	←	-	-	163	←	-
INTRLIN3	-	-	-	163	-	-	155
RLIN241							
INTRLIN24	226	←	-	-	226	←	-
INTRLIN4	-	-	-	226	-	-	218
INTRLIN25	227	←	-	-	227	←	-
INTRLIN5	-	-	-	227	-	-	219
INTRLIN26	275	←	-	-	275	←	-
INTRLIN6	-	-	-	275	-	-	267
INTRLIN27	276	←	-	-	276	←	-
INTRLIN7	-	-	-	276	-	-	268
RLIN242							

Unit Interrupt Signal	F1KH	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
INTRLIN28	285	←	-	-	285	←	-
INTRLIN8	-	-	-	285	-	-	-
INTRLIN29	286	←	-	-	286	←	-
INTRLIN9	-	-	-	286	-	-	-
INTRLIN210	324	←	-	-	324	-	-
INTRLIN211	325	←	-	-	325	-	-
RLIN243							
INTRLIN212	184	-	-	-	-	-	-
INTRLIN213	185	-	-	-	-	-	-
INTRLIN214	186	-	-	-	-	-	-
INTRLIN215	187	-	-	-	-	-	-
RLIN210							
INTRLIN8		-	-	-	-	-	277
RLIN211							
INTRLIN9		-	-	-	-	-	278

12.5 Reset Sources

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
RLIN24n RLIN21n	All reset sources (ISORES)	←	←	←	←

12.6 External Input/Output Signals

Unit Signal Name	F1KH	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
RLIN240							
RLIN2mRX (m = 0 to 3)	Yes	Yes	-	Yes	←	←	←
RLIN2mTX (m = 0 to 3)	Yes	Yes	-	Yes	←	←	←
RLIN2mRX (m = 0 to 2)	-	-	Yes	-	-	-	-
RLIN2mTX (m = 0 to 2)	-	-	Yes	-	-	-	-
RLIN241							
RLIN2mRX (m = 4 to 7)	Yes	Yes	-	Yes	←	←	←
RLIN2mTX (m = 4 to 7)	Yes	Yes	-	Yes	←	←	←
RLIN242							
RLIN2mRX (m = 8, 9)	Yes	Yes	-	Yes	←	←	-
RLIN2mTX (m = 8, 9)	Yes	Yes	-	Yes	←	←	-
RLIN2mRX (m = 10 to 11)	Yes	Yes	-	-	Yes	-	-
RLIN2mTX (m = 10 to 11)	Yes	Yes	-	-	Yes	-	-
RLIN243							
RLIN2mRX (m = 12 to 15)	Yes	-	-	-	-	-	-
RLIN2mTX (m = 12 to 15)	Yes	-	-	-	-	-	-
RLIN210							
RLIN2mRX (m = 8)	-	-	-	-	-	-	Yes
RLIN2mTX (m = 8)	-	-	-	-	-	-	Yes
RLIN211							
RLIN2mRX (m = 9)	-	-	-	-	-	-	Yes
RLIN2mTX (m = 9)	-	-	-	-	-	-	Yes

12.7 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H. Note the registers related to RLIN21 only are available on F1L.

Name	Address	F1Kx	F1K	F1H	F1M	F1L
RLN24nGLWBR	<RLIN24n_base> + 01H	Yes	Yes	Yes	Yes	Yes
RLN21nGLWBR	<RLIN21n_base> + 01H	-	-	-	-	Yes
RLN24nGLBRP0	<RLIN24n_base> + 02H	Yes	Yes	Yes	Yes	Yes
RLN21nGLBRP0	<RLIN21n_base> + 02H	-	-	-	-	Yes
RLN24nGLBRP1	<RLIN24n_base> + 03H	Yes	Yes	Yes	Yes	Yes
RLN21nGLBRP1	<RLIN21n_base> + 03H	-	-	-	-	Yes
RLN24nGLSTC	<RLIN24n_base> + 04H	Yes	Yes	Yes	Yes	Yes
RLN21nGLSTC	<RLIN21n_base> + 04H	-	-	-	-	Yes
RLN24nmLiMD	<RLIN24n_base> + 08H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiMD	<RLIN21n_base> + 08H + i × 20H	-	-	-	-	Yes
RLN24nmLiBFC	<RLIN24n_base> + 09H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiBFC	<RLIN21n_base> + 09H + i × 20H	-	-	-	-	Yes
RLN24nmLiSC	<RLIN24n_base> + 0AH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiSC	<RLIN21n_base> + 0AH + i × 20H	-	-	-	-	Yes
RLN24nmLiWUP	<RLIN24n_base> + 0BH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiWUP	<RLIN21n_base> + 0BH + i × 20H	-	-	-	-	Yes
RLN24nmLiIE	<RLIN24n_base> + 0CH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiIE	<RLIN21n_base> + 0CH + i × 20H	-	-	-	-	Yes
RLN24nmLiEDE	<RLIN24n_base> + 0DH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiEDE	<RLIN21n_base> + 0DH + i × 20H	-	-	-	-	Yes
RLN24nmLiCUC	<RLIN24n_base> + 0EH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiCUC	<RLIN21n_base> + 0EH + i × 20H	-	-	-	-	Yes
RLN24nmLiTRC	<RLIN24n_base> + 10H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiTRC	<RLIN21n_base> + 10H + i × 20H	-	-	-	-	Yes
RLN24nmLiMST	<RLIN24n_base> + 11H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiMST	<RLIN21n_base> + 11H + i × 20H	-	-	-	-	Yes
RLN24nmLiST	<RLIN24n_base> + 12H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiST	<RLIN21n_base> + 12H + i × 20H	-	-	-	-	Yes
RLN24nmLiEST	<RLIN24n_base> + 13H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiEST	<RLIN21n_base> + 13H + i × 20H	-	-	-	-	Yes
RLN24nmLiDFC	<RLIN24n_base> + 14H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDFC	<RLIN21n_base> + 14H + i × 20H	-	-	-	-	Yes
RLN24nmLiIDB	<RLIN24n_base> + 15H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiIDB	<RLIN21n_base> + 15H + i × 20H	-	-	-	-	Yes
RLN24nmLiCBR	<RLIN24n_base> + 16H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiCBR	<RLIN21n_base> + 16H + i × 20H	-	-	-	-	Yes
RLN24nmLiDBR1	<RLIN24n_base> + 18H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDBR1	<RLIN21n_base> + 18H + i × 20H	-	-	-	-	Yes
RLN24nmLiDBR2	<RLIN24n_base> + 19H + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDBR2	<RLIN21n_base> + 19H + i × 20H	-	-	-	-	Yes
RLN24nmLiDBR3	<RLIN24n_base> + 1AH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDBR3	<RLIN21n_base> + 1AH + i × 20H	-	-	-	-	Yes
RLN24nmLiDBR4	<RLIN24n_base> + 1BH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDBR4	<RLIN21n_base> + 1BH + i × 20H	-	-	-	-	Yes

Name	Address	F1Kx	F1K	F1H	F1M	F1L
RLN24nmLiDBR5	<RLIN24n_base> + 1CH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDBR5	<RLIN21n_base> + 1CH + i × 20H	-	-	-	-	Yes
RLN24nmLiDBR6	<RLIN24n_base> + 1DH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDBR6	<RLIN21n_base> + 1DH + i × 20H	-	-	-	-	Yes
RLN24nmLiDBR7	<RLIN24n_base> + 1EH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDBR7	<RLIN21n_base> + 1EH + i × 20H	-	-	-	-	Yes
RLN24nmLiDBR8	<RLIN24n_base> + 1FH + i × 20H	Yes	Yes	Yes	Yes	Yes
RLN21nmLiDBR8	<RLIN21n_base> + 1FH + i × 20H	-	-	-	-	Yes

13. LIN/UART Interface 3 (RLIN3)

13.1 Overview

The F1Kx/F1K uses the same RLIN3 implementation as the F1L/F1M/F1H.

The main differences between the device versions are

- F1L interrupt number assignment is different to F1M/F1H/F1K/F1Kx.
- F1L register base addresses are different to F1M/F1H/F1K/F1Kx.

13.2 Register Base Address

Base Address Name	F1KH F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
<RLIN30_base>	FFCE 2000H	←	←	←	←	FFCF 0000H
<RLIN31_base>	FFCE 2040H	←	←	←	←	FFCF 0040H
<RLIN32_base>	FFCE 2080H	←	←	←	←	FFCF 0080H
<RLIN33_base>	FFCE 20C0H	←	←	←	←	FFCF 00C0H
<RLIN34_base>	FFCE 2100H	-	FFCE 2100H	←	←	FFCF 0100H
<RLIN35_base>	FFCE 2140H	-	FFCE 2140H	←	←	FFCF 0140H
<RLIN36_base>	FFCE 2180H	-	-	-	-	-
<RLIN37_base>	FFCE 21C0H	-	-	-	-	-

13.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1H	F1M	F1L
RLIN3n	LIN communication clock sources	CKSCLK_ILIN	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_ILIN	CPUCLK2 CKSCLK_ILIN	CKSCLK_ILIN	←	←

13.4 Interrupt Requests

Unit Interrupt Signal	Interrupt Number						DMA Trigger Number					
	F1KH / F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H	F1KH / F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
RLIN30												
INTRLIN3n (n = 0)	33	33	33	25	33	33	-	-	-	-	-	-
INTRLIN3nUR0 (n = 0)	34	34	34	26	34	34	10	10	10	10[1)]	10	10
INTRLIN3nUR1 (n = 0)	35	35	35	27	35	35	11	11	11	11[1)]	11	11
INTRLIN3nUR2 (n = 0)	36	36	36	28	36	36	-	-	-	-	-	-
RLIN31												
INTRLIN3n (n = 1)	120	120	120	112	120	120	-	-	-	-	-	-
INTRLIN3nUR0 (n = 1)	121	121	121	113	121	121	86	86	86	22[2)]	86	86
INTRLIN3nUR1 (n = 1)	122	122	122	114	122	122	87	87	87	23[2)]	87	87

Unit Interrupt Signal	Interrupt Number						DMA Trigger Number					
	F1KH / F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H	F1KH / F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
INTRLIN3nUR2 (n = 1)	123	123	123	115	123	123	-	-	-	-	-	-
RLIN32												
INTRLIN3n (n = 2)	164	164	164	156	164	164	-	-	-	-	-	-
INTRLIN3nUR0 (n = 2)	165	165	165	157	165	165	44	44	44	44[1)]	44	44
INTRLIN3nUR1 (n = 2)	166	166	166	158	166	166	45	45	45	45[1)]	45	45
INTRLIN3nUR2 (n = 2)	167	167	167	159	167	167	-	-	-	-	-	-
RLIN33												
INTRLIN3n (n = 3)	228	228	228	220	228	228	-	-	-	-	-	-
INTRLIN3nUR0 (n = 3)	229	229	229	221	229	229	111	111	111	47[2)]	111	111
INTRLIN3nUR1 (n = 3)	230	230	230	222	230	230	112	112	112	48[2)]	112	112
INTRLIN3nUR2 (n = 3)	231	231	231	223	231	231	-	-	-	-	-	-
RLIN34												
INTRLIN3n (n = 4)	232	-	224	224	232	232	-	-	-	-	-	-
INTRLIN3nUR0 (n = 4)	233	-	225	225	233	233	50	-	50	50[1)]	50	50
INTRLIN3nUR1 (n = 4)	234	-	226	226	234	234	51	-	51	51[1)]	51	51
INTRLIN3nUR2 (n = 4)	235	-	227	227	235	235	-	-	-	-	-	-
RLIN35												
INTRLIN3n (n = 5)	236	-	228	228	236	236	-	-	-	-	-	-
INTRLIN3nUR0 (n = 5)	237	-	229	229	237	237	121	-	113	49[2)]	113	113
INTRLIN3nUR1 (n = 5)	238	-	230	230	238	238	122	-	114	50[2)]	114	114
INTRLIN3nUR2 (n = 5)	239	-	231	231	239	239	-	-	-	-	-	-
RLIN36												
INTRLIN3n (n = 6)	360	-	-	-	-	-	-	-	-	-	-	-
INTRLIN3nUR0 (n = 6)	361	-	-	-	-	-	119	-	-	-	-	-
INTRLIN3nUR1 (n = 6)	362	-	-	-	-	-	120	-	-	-	-	-
INTRLIN3nUR2 (n = 6)	363	-	-	-	-	-	-	-	-	-	-	-
RLIN37												
INTRLIN3n (n = 7)	364	-	-	-	-	-	-	-	-	-	-	-
INTRLIN3nUR0 (n = 7)	365	-	-	-	-	-	16	-	-	-	-	-
INTRLIN3nUR1 (n = 7)	366	-	-	-	-	-	77	-	-	-	-	-
INTRLIN3nUR2 (n = 7)	367	-	-	-	-	-	-	-	-	-	-	-

[1)] (channels 0 to 7)

[2)] (channels 8 to 15)

13.5 Reset Sources

Base Address Name	F1Kx	F1K	F1L	F1M	F1H
RLIN3n	All reset sources (ISORES)	←	←	←	←

13.6 External Input/Output Signals

Unit Signal Name	F1KH F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
RLIN30						
RLIN3nRX (n = 0)	Yes	Yes	Yes	Yes	Yes	Yes
RLIN3nTX (n = 0)	Yes	Yes	Yes	Yes	Yes	Yes
RLIN31						
RLIN3nRX (n = 1)	Yes	Yes	Yes	Yes	Yes	Yes
RLIN3nTX (n = 1)	Yes	Yes	Yes	Yes	Yes	Yes
RLIN32						
RLIN3nRX (n = 2)	Yes	Yes	Yes	Yes	Yes	Yes
RLIN3nTX (n = 2)	Yes	Yes	Yes	Yes	Yes	Yes
RLIN33						
RLIN3nRX (n = 3)	Yes	Yes	Yes	Yes	Yes	Yes
RLIN3nTX (n = 3)	Yes	Yes	Yes	Yes	Yes	Yes
RLIN34						
RLIN3nRX (n = 4)	Yes	No	Yes	Yes	Yes	Yes
RLIN3nTX (n = 4)	Yes	No	Yes	Yes	Yes	Yes
RLIN35						
RLIN3nRX (n = 5)	Yes	No	Yes	Yes	Yes	Yes
RLIN3nTX (n = 5)	Yes	No	Yes	Yes	Yes	Yes
RLIN36						
RLIN3nRX (n = 6)	Yes	No	-	-	-	-
RLIN3nTX (n = 6)	Yes	No	-	-	-	-
RLIN37						
RLIN3nRX (n = 7)	Yes	No	-	-	-	-
RLIN3nTX (n = 7)	Yes	No	-	-	-	-

13.7 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1H	F1M	F1L
RLN3nLWBR	<RLIN3n_base> + 01H	Same	Same	Same	Same	Same
RLN3nLBRP01	<RLIN3n_base> + 02H	Same	Same	Same	Same	Same
RLN3nLBRP0	<RLIN3n_base> + 02H	Same	Same	Same	Same	Same
RLN3nLBRP1	<RLIN3n_base> + 03H	Same	Same	Same	Same	Same
RLN3nLSTC	<RLIN3n_base> + 04H	Same	Same	Same	Same	Same
RLN3nLMD	<RLIN3n_base> + 08H	Same	Same	Same	Same	Same
RLN3nLBFC	<RLIN3n_base> + 09H	Same	Same	Same	Same	Same
RLN3nLSC	<RLIN3n_base> + 0AH	Same	Same	Same	Same	Same
RLN3nLWUP	<RLIN3n_base> + 0BH	Same	Same	Same	Same	Same
RLN3nLIE	<RLIN3n_base> + 0CH	Same	Same	Same	Same	Same
RLN3nLEDE	<RLIN3n_base> + 0DH	Same	Same	Same	Same	Same
RLN3nLCUC	<RLIN3n_base> + 0EH	Same	Same	Same	Same	Same
RLN3nLTRC	<RLIN3n_base> + 10H	Same	Same	Same	Same	Same
RLN3nLMST	<RLIN3n_base> + 11H	Same	Same	Same	Same	Same
RLN3nLST	<RLIN3n_base> + 12H	Same	Same	Same	Same	Same

Name	Address	F1Kx	F1K	F1H	F1M	F1L
RLN3nLEST	<RLIN3n_base> + 13H	Same	Same	Same	Same	Same
RLN3nLDFC	<RLIN3n_base> + 14H	Same	Same	Same	Same	Same
RLN3nLIDB	<RLIN3n_base> + 15H	Same	Same	Same	Same	Same
RLN3nLCBR	<RLIN3n_base> + 16H	Same	Same	Same	Same	Same
RLN3nLUDB0	<RLIN3n_base> + 17H	Same	Same	Same	Same	Same
RLN3nLDBR1	<RLIN3n_base> + 18H	Same	Same	Same	Same	Same
RLN3nLDBR2	<RLIN3n_base> + 19H	Same	Same	Same	Same	Same
RLN3nLDBR3	<RLIN3n_base> + 1AH	Same	Same	Same	Same	Same
RLN3nLDBR4	<RLIN3n_base> + 1BH	Same	Same	Same	Same	Same
RLN3nLDBR5	<RLIN3n_base> + 1CH	Same	Same	Same	Same	Same
RLN3nLDBR6	<RLIN3n_base> + 1DH	Same	Same	Same	Same	Same
RLN3nLDBR7	<RLIN3n_base> + 1EH	Same	Same	Same	Same	Same
RLN3nLDBR8	<RLIN3n_base> + 1FH	Same	Same	Same	Same	Same
RLN3nLUOER	<RLIN3n_base> + 20H	Same	Same	Same	Same	Same
RLN3nLUOR1	<RLIN3n_base> + 21H	Same	Same	Same	Same	Same
RLN3nLUTDR	<RLIN3n_base> + 24H	Same	Same	Same	Same	Same
RLN3nLUTDRL	<RLIN3n_base> + 24H	Same	Same	Same	Same	Same
RLN3nLUTDRH	<RLIN3n_base> + 25H	Same	Same	Same	Same	Same
RLN3nLURDR	<RLIN3n_base> + 26H	Same	Same	Same	Same	Same
RLN3nLURDRL	<RLIN3n_base> + 26H	Same	Same	Same	Same	Same
RLN3nLURDRH	<RLIN3n_base> + 27H	Same	Same	Same	Same	Same
RLN3nLUWTDR	<RLIN3n_base> + 28H	Same	Same	Same	Same	Same
RLN3nLUWTDRL	<RLIN3n_base> + 28H	Same	Same	Same	Same	Same
RLN3nLUWTDRH	<RLIN3n_base> + 29H	Same	Same	Same	Same	Same

14. I2C Bus Interface (RIIC)

14.1 Overview

The functional feature set of the RIIC between F1Kx/F1K and F1L/F1M/F1H is identical.

The F1Kx devices add a second channel, compared to all previous F1x devices.

14.2 Register Base Address

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
<RIIC0_base>	FFCA 0000H	←	←	←	←
<RIIC1_base>	FFCA 0080H	-	-	-	-

14.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1H	F1M	F1L
RIICn	PCLK	CKSCLK_IIIC	←	←	←	CPUCLK2
	Register access	CPUCLK_L CKSCLK_IIIC	CPUCLK2 CKSCLK_IIIC	CKSCLK_IIIC	CKSCLK_IIIC	CPUCLK2

14.4 Interrupt Requests

Unit Interrupt Signal	Interrupt Number					DMA Trigger Number				
	F1Kx	F1K	F1H	F1M	F1L	F1Kx	F1K	F1H	F1M	F1L
RIIC0										
INTRIIC0EE	77	←	←	←	71	-	-	-	-	-
INTRIIC0RI	78	←	←	←	70	20	←	←	←	←
INTRIIC0TI	76	←	←	←	68	19	←	←	←	←
INTRIIC0TEI	79	←	←	←	69	-	-	-	-	-
RIIC1										
INTRIIC1EE	241	-	-	-	-	-	-	-	-	-
INTRIIC1RI	242	-	-	-	-	114	-	-	-	-
INTRIIC1TI	240	-	-	-	-	113	-	-	-	-
INTRIIC1TEI	243	-	-	-	-	-	-	-	-	-

14.5 Reset Sources

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
RIICn	All reset sources (ISORES)	←	←	←	←

14.6 External Input/Output Signals

Unit Signal Name	F1Kx	F1K	F1H	F1M	F1L
RIICn					
RIICnSCL	Yes	Yes	Yes	Yes	Yes
RIICnSDA	Yes	Yes	Yes	Yes	Yes

14.7 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1H	F1M	F1L
RIICnCR1	<RIICn_base> + 0000H	Same	Same	Same	Same	Same
RIICnCR2	<RIICn_base> + 0004H	Same	Same	Same	Same	Same
RIICnMR1	<RIICn_base> + 0008H	Same	Same	Same	Same	Same
RIICnMR2	<RIICn_base> + 000CH	Same	Same	Same	Same	Same
RIICnMR3	<RIICn_base> + 0010H	Same	Same	Same	Same	Same
RIICnFER	<RIICn_base> + 0014H	Same	Same	Same	Same	Same
RIICnSER	<RIICn_base> + 0018H	Same	Same	Same	Same	Same
RIICnIER	<RIICn_base> + 001CH	Same	Same	Same	Same	Same
RIICnSR1	<RIICn_base> + 0020H	Same	Same	Same	Same	Same
RIICnSR2	<RIICn_base> + 0024H	Same	Same	Same	Same	Same
RIICnSAR0	<RIICn_base> + 0028H	Same	Same	Same	Same	Same
RIICnSAR1	<RIICn_base> + 002CH	Same	Same	Same	Same	Same
RIICnSAR2	<RIICn_base> + 0030H	Same	Same	Same	Same	Same
RIICnBRL	<RIICn_base> + 0034H	Same	Same	Same	Same	Same
RIICnBRH	<RIICn_base> + 0038H	Same	Same	Same	Same	Same
RIICnDRT	<RIICn_base> + 003CH	Same	Same	Same	Same	Same
RIICnDRR	<RIICn_base> + 0040H	Same	Same	Same	Same	Same

15. CAN Interface (RS-CANFD / RS-CAN)

Whereas the RSCAN implementation on F1L, F1M and F1H are identical (*), the F1Kx/F1K enhancements result in the following differences:

- For support of the CANFD functionality the register known from the RSCAN implementation are used with changed name and additional registers are added.
- F1K adds triggers for DMA supported memory transfers.

The CAN interrupt assignment on F1K is similar to F1M/F1H and differs from F1L.

(*) The RSCAN1 macro is only available on the F1H.
The interrupt assignment on F1L is different than on F1M/F1H.

15.1 Register Base Address

Base Address Name	F1KH	F1KM	F1K	F1L	F1M	F1H
<RSCAN0_base> <RCFDC0_base>	— FFD0 0000H	— FFD0 0000H	FFD0 0000H —	Same —	Same —	Same —
<RCFDC1_base>	FFD2 0000H	—	—	—	—	—
<ECCCAN0_base> for MB RAM	—	—	FFC7 1300H	—	—	—
<ECCCANFD0_base> for AFL RAM	—	—	FFC7 1400H	—	—	—
<RSCAN1_base>	—	—	FFD0 8000H	—	—	FFD0 8000H
<ECCCAN1_base>	—	—	FFC7 1020H	—	—	—

15.2 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
RCFDCn RSCANn	clk_xincan	CKSCLK_ICANOSC	←	Same	Same	Same
	clkc	CKSCLK_IPERI2	←	Same	Same	Same
	pclk	CKSCLK_ICAN	←	Same	Same	Same
	Register access clock	CPUCLK_M, CKSCLK_ICAN	CPUCLK2, CKSCLK_ICAN	CKSCLK_ICAN	←	←

15.3 Interrupt Requests

Unit Interrupt Signal	Interrupt Number							DMA Trigger Number						
	-D8	-S4	-S1	F1K	F1L	F1M	F1H	-D8	-S4	-S1	F1K	F1L	F1M	F1H
INTRCANGERR0	22	←	←	←	—	22	22	—	—	—	—	—	—	—
INTRCANGERR	—	—	—	—	14	—	—	—	—	—	—	—	—	—
INTRCANGRECC0	23	←	←	←		23	23	—	—	—	—	—	—	—
INTRCANGRECC	—	—	—	—	15	—	—	—	—	—	—	—	—	—
INTRCANGERR1	—	—	—	—	—	—	319	—	—	—	—	—	—	—

Unit Interrupt Signal	Interrupt Number							DMA Trigger Number						
	-D8	-S4	-S1	F1K	F1L	F1M	F1H	-D8	-S4	-S1	F1K	F1L	F1M	F1H
INTRCANGRECC1	—	—	—	—	—	—	320	—	—	—	—	—	—	—
RSCANFDRF0	—	—	—	—	—	—	—	60	←	←	—	—	—	—
RSCANFDRF1	—	—	—	—	—	—	—	61	←	←	—	—	—	—
RSCANFDRF2	—	—	—	—	—	—	—	62	←	←	—	—	—	—
RSCANFDRF3	—	—	—	—	—	—	—	63	←	←	—	—	—	—
RSCANFDRF4	—	—	—	—	—	—	—	68	←	←	—	—	—	—
RSCANFDRF5	—	—	—	—	—	—	—	69	←	←	—	—	—	—
RSCANFDRF6	—	—	—	—	—	—	—	82	←	—	—	—	—	—
RSCANFDRF7	—	—	—	—	—	—	—	83	←	—	—	—	—	—
INTRCAN0ERR	24	←	←	←	16	24	24	—	—	—	—	—	—	—
INTRCAN0REC	25	←	←	←	17	25	25	—	—	—	—	—	—	—
INTRCAN0TRX	26	←	←	←	18	26	26	—	—	—	—	—	—	—
RSCANFDCF0	—	—	—	—	—	—	—	23	←	←	←	—	—	—
INTRCAN1ERR	113	←	←	←	105	113	113	—	—	—	—	—	—	—
INTRCAN1REC	114	←	←	←	106	114	114	—	—	—	—	—	—	—
INTRCAN1TRX	115	←	←	←	107	115	115	—	—	—	—	—	—	—
RSCANFDCF1	—	—	—	—	—	—	—	24	←	←	←	—	—	—
INTRCAN2ERR	217	←	←	←	209	217	217	—	—	—	—	—	—	—
INTRCAN2REC	218	←	←	←	210	218	218	—	—	—	—	—	—	—
INTRCAN2TRX	219	←	←	←	211	219	219	—	—	—	—	—	—	—
RSCANFDCF2	—	—	—	—	—	—	—	26	←	←	←	—	—	—
INTRCAN3ERR	220	←	←	←	212	220	220	—	—	—	—	—	—	—
INTRCAN3REC	221	←	←	←	213	221	221	—	—	—	—	—	—	—
INTRCAN3TRX	222	←	←	←	214	222	222	—	—	—	—	—	—	—
RSCANFDCF3	—	—	—	—	—	—	—	27	←	←	←	—	—	—
INTRCAN4ERR	272	←	←	←	264	272	272	—	—	—	—	—	—	—
INTRCAN4REC	273	←	←	←	265	273	273	—	—	—	—	—	—	—
INTRCAN4TRX	274	←	←	←	266	274	274	—	—	—	—	—	—	—
RSCANFDCF4	—	—	—	—	—	—	—	48	←	←	←	—	—	—
INTRCAN5ERR	287	←	←	←	279	287	287	—	—	—	—	—	—	—
INTRCAN5REC	288	←	←	←	280	288	288	—	—	—	—	—	—	—
INTRCAN5TRX	289	←	←	←	281	289	289	—	—	—	—	—	—	—
RSCANFDCF5	—	—	—	—	—	—	—	49	←	←	←	—	—	—
INTRCAN6ERR	321	←	—	—	—	—	321	—	—	—	—	—	—	—
INTRCAN6REC	322	←	—	—	—	—	322	—	—	—	—	—	—	—
INTRCAN6TRX	323	←	—	—	—	—	323	—	—	—	—	—	—	—

Unit Interrupt Signal	Interrupt Number							DMA Trigger Number						
	-D8	-S4	-S1	F1K	F1L	F1M	F1H	-D8	-S4	-S1	F1K	F1L	F1M	F1H
RSCANFDCF6	—	—	—	—	—	—	—	64	←	—	—	—	—	—
INTRCAN7ERR	332	←	—	—	—	—	332	—	—	—	—	—	—	—
INTRCAN7REC	333	←	—	—	—	—	333	—	—	—	—	—	—	—
INTRCAN7TRX	334	←	—	—	—	—	334	—	—	—	—	—	—	—
RSCANFDCF7	—	—	—	—	—	—	—	65	←	—	—	—	—	—
INTRCANGERR1	319	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCANGRECC1	320	—	—	—	—	—	—	—	—	—	—	—	—	—
RSCANFDRF8	—	—	—	—	—	—	—	96	—	—	—	—	—	—
RSCANFDRF9	—	—	—	—	—	—	—	97	—	—	—	—	—	—
RSCANFDRF10	—	—	—	—	—	—	—	98	—	—	—	—	—	—
RSCANFDRF11	—	—	—	—	—	—	—	99	—	—	—	—	—	—
RSCANFDRF12	—	—	—	—	—	—	—	15	—	—	—	—	—	—
RSCANFDRF13	—	—	—	—	—	—	—	25	—	—	—	—	—	—
RSCANFDRF14	—	—	—	—	—	—	—	84	—	—	—	—	—	—
RSCANFDRF15	—	—	—	—	—	—	—	57	—	—	—	—	—	—
INTRCAN8ERR	244	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCAN8REC	245	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCAN8TRX	246	—	—	—	—	—	—	—	—	—	—	—	—	—
RSCANFDCF8	—	—	—	—	—	—	—	92	—	—	—	—	—	—
INTRCAN9ERR	247	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCAN9REC	248	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCAN9TRX	249	—	—	—	—	—	—	—	—	—	—	—	—	—
RSCANFDCF9	—	—	—	—	—	—	—	93	—	—	—	—	—	—
INTRCAN10ERR	250	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCAN10REC	251	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCAN10TRX	252	—	—	—	—	—	—	—	—	—	—	—	—	—
RSCANFDCF10	—	—	—	—	—	—	—	94	—	—	—	—	—	—
INTRCAN11ERR	253	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCAN11REC	254	—	—	—	—	—	—	—	—	—	—	—	—	—
INTRCAN11TRX	255	—	—	—	—	—	—	—	—	—	—	—	—	—
RSCANFDCF11	—	—	—	—	—	—	—	95	—	—	—	—	—	—

15.4 Reset Sources

Base Address Name	F1Kx	F1K	F1L	F1M	F1H
RSCANn (n = 0)	-	All reset sources (ISORES)	←	←	←
RCFDCn	All reset sources (ISORES)	-	-	-	-

15.5 Registers overview

Name	Address (Offset to <RSCANn_base>)	F1Kx	F1K	F1L	F1M	F1H
RSCFDnCFDGRMCFG	+ 04FCH	—	Yes	—	—	Yes
RSCANnCmCFG	+ 0000H + (10H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCmNCFG	same	—	Yes	—	—	—
RCFDCnCFDCmNCFG	same	Yes	—	—	—	—
RSCANnCmCTR	+ 0004H + (10H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCmCTR	same	—	Yes	—	—	—
RCFDCnCFDCmCTR	same	Yes	—	—	—	—
RSCANnCmSTS	+ 0008H + (10H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCmSTS	same	—	Yes	—	—	—
RCFDCnCFDCmSTS	same	Yes	—	—	—	—
RSCANnCmERFL	+ 000CH + (10H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCmERFL	same	—	Yes	—	—	—
RCFDCnCFDCmERFL	same	Yes	—	—	—	—
RSCFDnCFDCmDCFG	+ 0500H + (20H × m)	—	Yes	—	—	—
RCFDCnCFDCmDCFG	+ 0700H + (20H × m)	Yes	—	—	—	—
RSCFDnCFDCmFDCFG	+ 0504H + (20H × m)	—	Yes	—	—	—
RCFDCnCFDCmFDCFG	+ 0704H + (20H × m)	Yes	—	—	—	—
RSCANnCFDCmFDCTR	+ 0508H + (20H × m)	—	Yes	—	—	—
RCFDCnCFDCmFDCTR	+ 0708H + (20H × m)	Yes	—	—	—	—
RSCFDnCFDCmFDSTS	+ 050CH + (20H × m)	—	Yes	—	—	—
RCFDCnCFDCmFDSTS	+ 070CH + (20H × m)	Yes	—	—	—	—
RSCFDnCFDCmFDCRC	+ 0510H + (20H × m)	—	Yes	—	—	—
RCFDCnCFDCmFDCRC	+ 0710H + (20H × m)	Yes	—	—	—	—
RSCANnGCFG	+ 0084H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGCFG	same	—	Yes	—	—	—
RCFDCnCFDGCFG	same	Yes	—	—	—	—
RSCANnGCTR	+ 0088H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGCTR	same	—	Yes	—	—	—
RCFDCnCFDGCTR	same	Yes	—	—	—	—
RSCANnGSTS	+ 008CH	—	Yes	Yes	Yes	Yes
RSCFDnCFDGSTS	same	—	Yes	—	—	—
RCFDCnCFDGSTS	same	Yes	—	—	—	—
RSCANnGERFL	+ 0090H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGERFL	same	—	Yes	—	—	—
RCFDCnCFDGERFL	same	Yes	—	—	—	—
RSCANnGTSC	+ 0094H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGTSC	same	—	Yes	—	—	—
RCFDCnCFDGTSC	same	Yes	—	—	—	—

Name	Address (Offset to <RSCANn_base>)	F1Kx	F1K	F1L	F1M	F1H
RSCANnGTINTSTS0	+ 0460H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGTINTSTS0	same	—	Yes	—	—	—
RCFDCnCFDGTINTSTS0	+610H	Yes	—	—	—	—
RSCANnGTINTSTS1	+ 0464H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGTINTSTS1	same	—	Yes	—	—	—
RCFDCnCFDGTINTSTS1	+614H	Yes	—	—	—	—
RSCANnGFDCFG	+ 0474H	—	Yes	—	—	Yes
RSCFDnCFDGFDCFG	same	—	Yes	—	—	—
RCFDCnCFDGFDCFG	+624H	Yes	—	—	—	—
RSCANnGAFLECTR	+ 0098H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGAFLECTR	same	—	Yes	—	—	—
RCFDCnCFDGAFLECTR	same	Yes	—	—	—	—
RSCANnGAFLCFG0	+ 009CH	—	Yes	Yes	Yes	Yes
RSCFDnCFDGAFLCFG0	same	—	Yes	—	—	—
RCFDCnCFDGAFLCFG0	same	Yes	—	—	—	—
RSCANnGAFLCFG1	+ 00A0H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGAFLCFG1	same	—	Yes	—	—	—
RCFDCnCFDGAFLCFG1	same	Yes	—	—	—	—
RSCANnGAFLIDj	+ 0500H + (10H × j)	—	Yes	Yes	Yes	Yes
RSCFDnCFDGAFLIDj	+ 1000H + (10H × j)	—	Yes	—	—	—
RCFDCnCFDGAFLIDj	same	Yes	—	—	—	—
RSCANnGAFLMj	+ 0504H + (10H × j)	—	Yes	Yes	Yes	Yes
RSCFDnCFDGAFLMj	+ 1004H + (10H × j)	—	Yes	—	—	—
RCFDCnCFDGAFLMj	same	Yes	—	—	—	—
RSCANnGAFLP0_j	+ 0508H + (10H × j)	—	Yes	Yes	Yes	Yes
RSCFDnCFDGAFLP0_j	+ 1008H + (10H × j)	—	Yes	—	—	—
RCFDCnCFDGAFLP0_j	same	Yes	—	—	—	—
RSCANnGAFLP1_j	+ 050CH + (10H × j)	—	Yes	Yes	Yes	Yes
RSCFDnCFDGAFLP1_j	+ 100CH + (10H × j)	—	Yes	—	—	—
RCFDCnCFDGAFLP1_j	same	Yes	—	—	—	—
RSCANnRMNB	+ 00A4H	—	Yes	Yes	Yes	Yes
RSCFDnCFDRMNB	same	—	Yes	—	—	—
RCFDCnCFDRMNB	same	Yes	—	—	—	—
RSCANnRMNDy	+ 00A8H + (04H × y)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRMNDy	same	—	Yes	—	—	—
RCFDCnCFDRMNDy	same	Yes	—	—	—	—
RSCANnRMIDq	+ 0600H + (10H × q)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRMIDq	+ 2000H + (20H × q)	—	Yes	—	—	—
RCFDCnCFDRMIDq	+ 2000H + (80H × q)	Yes	—	—	—	—
RSCANnRMPTRq	+ 0604H + (10H × q)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRMPTRq	+ 2004H + (20H × q)	—	Yes	—	—	—
RCFDCnCFDRMPTRq	+ 2004H + (80H × q)	Yes	—	—	—	—
RSCANnRMDF0q	+ 0608H + (10H × q)	—	Yes	Yes	Yes	Yes
RSCANnRMDF1q	+ 060CH + (10H × q)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRMFDSTSq	+ 2008H + (20H × q)	—	Yes	—	—	—
RCFDCnCFDRMFDSTSq	+ 2008H + (80H × q)	Yes	—	—	—	—
RSCFDnCFDRMDFb_q	+ 200CH + (04H × b) + (20H × q)	—	Yes	—	—	—
RCFDCnCFDRMDFb_q	+ 200CH + (04H × b) + (80H × q)	Yes	—	—	—	—
RSCANnRFCCx	+ 00B8H + (04H × x)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRFCCx	same	—	Yes	—	—	—

Name	Address (Offset to <RSCANn_base>)	F1Kx	F1K	F1L	F1M	F1H
RCFDCnCFDRFCCx	same	Yes	—	—	—	—
RSCANnRFSTSx	+ 00D8H + (04H × x)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRFSTSx	same	—	Yes	—	—	—
RCFDCnCFDRFSTSx	same	Yes	—	—	—	—
RSCANnRFPCTRx	+ 00F8H + (04H × x)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRFPCTRx	same	—	Yes	—	—	—
RCFDCnCFDRFPCTRx	same	Yes	—	—	—	—
RSCANnRFIDx	+ 0E00H + (10H × x)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRFIDx	+ 3000H + (80H × x)	—	Yes	—	—	—
RCFDCnCFDRFIDx	+ 6000H + (80H × x)	Yes	—	—	—	—
RSCANnRFPTRx	+ 0E04H + (10H × x)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRFPTRx	+ 3004H + (80H × x)	—	Yes	—	—	—
RCFDCnCFDRFPTRx	+ 6004H + (80H × x)	Yes	—	—	—	—
RSCFDnCFDRFFDSTSx	+ 3008H + (80H × x)	—	Yes	—	—	—
RCFDCnCFDRFFDSTSx	+ 6008H + (80H × x)	Yes	—	—	—	—
RSCANnRFDF0x	+ 0E08H + (10H × x)	—	Yes	Yes	Yes	Yes
RSCANnRFDF1x	+ 0E0CH + (10H × x)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRFDFd_x	+ 300CH + (04H × d) + (80H × x)	—	Yes	—	—	—
RCFDCnCFDRFDFd_x	+ 600CH + (04H × d) + (80H × x)	Yes	—	—	—	—
RSCANnCFCCk	+ 0118H + (04H × k)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCFCCk	same	—	Yes	—	—	—
RCFDCnCFDCFCCk	same	Yes	—	—	—	—
RSCANnCFSTSk	+ 0178H + (04H × k)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCFSTSk	same	—	Yes	—	—	—
RCFDCnCFDCFSTSk	same	Yes	—	—	—	—
RSCANnCFPCTRk	+ 01D8H + (04H × k)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCFPCTRk	same	—	Yes	—	—	—
RCFDCnCFDCFPCTRk	same	Yes	—	—	—	—
RSCANnCFIDk	+ 0E80H + (10H × k)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCFIDk	+ 3400H + (80H × k)	—	Yes	—	—	—
RCFDCnCFDCFIDk	+ 6400H + (80H × k)	Yes	—	—	—	—
RSCANnCFPTRk	+ 0E84H + (10H × k)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCFPTRk	+ 3404H + (80H × k)	—	Yes	—	—	—
RCFDCnCFDCFPTRk	+ 6404H + (80H × k)	Yes	—	—	—	—
RSCFDnCFDCFFDCSTSk	+ 3408H + (80H × k)	—	Yes	—	—	—
RCFDCnCFDCFFDCSTSk	+ 6408H + (80H × k)	Yes	—	—	—	—
RSCANnCFDF0k	+ 0E88H + (10H × k)	—	Yes	Yes	Yes	Yes
RSCANnCFDF1k	+ 0E8CH + (10H × k)	—	Yes	Yes	Yes	Yes
RSCFDnCFDCFDFd_k	+ 340CH + (04H × d) + (80H × k)	—	Yes	—	—	—
RCFDCnCFDCFDFd_k	+ 640CH + (04H × d) + (80H × k)	Yes	—			
RSCANnFESTS	+ 0238H	—	Yes	Yes	Yes	Yes
RSCFDnCFDFESTS	same	—	Yes	—	—	—
RCFDCnCFDFESTS	same	Yes	—	—	—	—
RSCANnFFSTS	+ 023CH	—	Yes	Yes	Yes	Yes
RSCFDnCFDFFSTS	same	—	Yes	—	—	—
RCFDCnCFDFFSTS	same	Yes	—	—	—	—
RSCANnFMSTS	+ 0240H	—	Yes	Yes	Yes	Yes
RSCFDnCFDFMSTS	same	—	Yes	—	—	—
RCFDCnCFDFMSTS	same	Yes	—	—	—	—

Name	Address (Offset to <RSCANn_base>)	F1Kx	F1K	F1L	F1M	F1H
RSCANnRFISTS	+ 0244H	—	Yes	Yes	Yes	Yes
RSCFDnCFDRFISTS	same	—	Yes	—	—	—
RCFDCnCFDRFISTS	same	Yes	—	—	—	—
RSCANnCFRISTS	+ 0248H	—	Yes	Yes	Yes	Yes
RSCFDnCFDCFRISTS	same	—	Yes	—	—	—
RCFDCnCFDCFRISTS	same	Yes	—	—	—	—
RSCANnCFTISTS	+ 024CH	—	Yes	Yes	Yes	Yes
RSCFDnCFDCFTISTS	same	—	Yes	—	—	—
RCFDCnCFDCFTISTS	same	Yes	—	—	—	—
RSCFDnCFDCDTCT	+ 0490H	—	Yes	—	—	—
RCFDCnCFDCDTCT	+ 0640H	Yes	—	—	—	—
RSCFDnCFDCDTSTS	+ 0494H	—	Yes	—	—	—
RCFDCnCFDCDTSTS	+ 0644H	Yes	—	—	—	—
RSCANnTMCp	+ 0250H + (01H × p)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMCp	same	—	Yes	—	—	—
RCFDCnCFDTMCp	same	Yes	—	—	—	—
RSCANnTMSTSp	+ 02D0H + (01H × p)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMSTSp	same	—	Yes	—	—	—
RCFDCnCFDTMSTSp	+ 0350H + (01H × p)	Yes	—	—	—	—
RSCANnTMIDp	+ 1000H + (10H × p)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMIDp	+ 4000H + (20H × p)	—	Yes	—	—	—
RCFDCnCFDTMIDp	+ 8000H + (80H × p)	Yes	—	—	—	—
RSCANnTMPTRp	+ 1004H + (10H × p)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMPTRp	+ 4004H + (20H × p)	—	Yes	—	—	—
RCFDCnCFDTMPTRp	+ 8004H + (80H × p)	Yes	—	—	—	—
RSCFDnCFDTMFDCTRp	+ 4008H + (20H × p)	—	Yes	—	—	—
RCFDCnCFDTMFDCTRp	+ 8008H + (80H × p)	Yes	—	—	—	—
RSCANnTMDF0p	+ 1008H + (10H × p)	—	Yes	Yes	Yes	Yes
RSCANnTMDF1p	+ 100CH + (10H × p)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMDFb_p	+ 400CH + (04H × b)+ (20H × p)	—	Yes	—	—	—
RCFDCnCFDTMDFb_p	+ 800CH + (04H × b)+ (80H × p)	Yes	—	—	—	—
RSCANnTMIECy	+ 0390H + (04H × y)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMIECy	same	—	Yes	—	—	—
RCFDCnCFDTMIECm	+ 04D0H + (04H × m)	Yes	—	—	—	—
RSCANnTMTRSTSy	+ 0350H + (04H × y)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMTRSTSy	same	—	Yes	—	—	—
RCFDCnCFDTMTRSTSm	+ 0450H + (04H × m)	Yes	—	—	—	—
RSCANnTMTARSTSy	+ 0360H + (04H × y)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMTARSTSy	same	—	Yes	—	—	—
RCFDCnCFDTMTARSTSm	+ 0470H + (04H × m)	Yes	—	—	—	—
RSCANnTMTCSTSy	+ 0370H + (04H × y)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMTCSTSy	same	—	Yes	—	—	—
RCFDCnCFDTMTCSTSm	+ 0490H + (04H × m)	Yes	—	—	—	—
RSCANnTMTASTSy	+ 0380H + (04H × y)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTMTASTSy	same	—	Yes	—	—	—
RCFDCnCFDTMTASTSm	+ 04B0H + (04H × m)	Yes	—	—	—	—
RSCANnTXQCCm	+ 03A0H + (04H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTXQCCm	same	—	Yes	—	—	—
RCFDCnCFDTXQCCm	+ 0550H + (04H × m)	Yes	—	—	—	—

Name	Address (Offset to <RSCANn_base>)	F1Kx	F1K	F1L	F1M	F1H
RSCANnTXQSTSm	+ 03C0H + (04H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTXQSTSm	same	—	Yes	—	—	—
RCFDCnCFDTXQSTSm	+ 0570H + (04H × m)	Yes	—	—	—	—
RSCANnTXQPCTRm	+ 03E0H + (04H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTXQPCTRm	same	—	Yes	—	—	—
RCFDCnCFDTXQPCTRm	+ 0590H + (04H × m)	Yes	—	—	—	—
RSCANnTHLCCm	+ 0400H + (04H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTHLCCm	same	—	Yes	—	—	—
RCFDCnCFDTHLCCm	+ 05B0H + (04H × m)	Yes	—	—	—	—
RSCANnTHLSTSm	+ 0420H + (04H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTHLSTSm	same	—	Yes	—	—	—
RCFDCnCFDTHLSTSm	+ 05D0H + (04H × m)	Yes	—	—	—	—
RSCANnTHLPCTRm	+ 0440H + (04H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTHLPCTRm	same	—	Yes	—	—	—
RCFDCnCFDTHLPCTRm	+ 05F0H + (04H × m)	Yes	—	—	—	—
RSCANnTHLACCm	+ 1800H + (04H × m)	—	Yes	Yes	Yes	Yes
RSCFDnCFDTHLACCm	+ 6000H + (04H × m)	—	Yes	—	—	—
RCFDCnCFDTHLACC0m	+ 10000H + (08H × m)	Yes	—	—	—	—
RCFDCnCFDTHLACC1m	+ 10004H + (08H × m)	Yes	—	—	—	—
RSCANnGTSTCFG	+ 0468H	—	Yes	Yes	Yes	Yes
RSCFDnCFDGTSTCFG	same	—	Yes	—	—	—
RCFDCnCFDGTSTCFG	+ 0618H	Yes	—	—	—	—
RSCANnGTSTCTR	+ 046CH	—	Yes	Yes	Yes	Yes
RSCFDnCFDGTSTCTR	same	—	Yes	—	—	—
RCFDCnCFDGTSTCTR	+ 061CH	Yes	—	—	—	—
RSCANnGLOCKK	+ 047CH	—	Yes	Yes	Yes	Yes
RSCFDnCFDGLOCKK	same	—	Yes	—	—	—
RCFDCnCFDGLOCKK	+ 062CH	Yes	—	—	—	—
RSCANnRPGACCr	+ 1900H + (04H × r)	—	Yes	Yes	Yes	Yes
RSCFDnCFDRPGACCr	+ 6400H + (04H × r)	—	Yes	—	—	—
RCFDCnCFDRPGACCr	+ 10400H + (04H × r)	Yes	—	—	—	—

16. FlexRay Interface (FLXA)

16.1 Overview

The functional feature set of the FLXA between F1KH/F1KM-S4 and F1M/F1H is identical.

16.2 Register Base Address

Base Address Name	F1KH / F1KM_S4	F1KM-S1	F1K	F1L	F1M	F1H
<FLXA0_base>	1002 0000H	-	-	-	1002 0000H	←

16.3 Clock Supply

Base Address Name	Clock for the Unit	F1KH / F1KM_S4	F1K	F1L	F1M	F1H
FLXA0	hclk	CPUCLK_L	-	-	CPUCLK2	←
	clkc	CKSCLK_PPLLCLK	-	-	PPLLCLK	←
	Register access clock	CPUCLK_L	-	-	CPUCLK2	←

16.4 Interrupt Requests

Unit Interrupt Signal	Interrupt Number					
	F1KH / F1KM_S4	F1KM-S1	F1K	F1L	F1M	F1H
FLXA0						
INTFLXA0LINE0	179	-	-	-	179	←
INTFLXA0LINE1	180	-	-	-	180	←
INTFLXA0TIM0	181	-	-	-	181	←
INTFLXA0TIM1	182	-	-	-	182	←
INTFLXA0TIM2	183	-	-	-	183	←
INTFLXA0FDA	173	-	-	-	173	←
INTFLXA0FW	174	-	-	-	174	←
INTFLXA0OW	178	-	-	-	178	←
INTFLXA0OT	177	-	-	-	177	←
INTFLXA0IQF	176	-	-	-	176	←
INTFLXA0IQE	175	-	-	-	175	←

16.5 Reset Sources

Unit Name	F1KH / F1KM_S4	F1KM-S1	F1L	F1M	F1H
FLXA0	All reset sources (ISORES)	-	-	All reset sources (ISORES)	←

16.6 Registers overview

The registers are identical on the devices.

17. Window Watchdog Timer (WDTA)

17.1 Overview

The functional feature set of the WDTA between F1Kx and F1L/F1M/F1H/F1K is identical.

17.2 Register Base Address

Base Address Name	F1KH	F1KM	F1K	F1L	F1M	F1H
<WDTA0_base>	FFED 0000H	←	←	←	←	←
<WDTA1_base>	FFED 1000H	←	←	←	←	←
<WDTA2_base>	FFED 2000H	-	-	-	-	FFED 2000H

17.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
WDTA0	PCLK	CKSCLK_AWDTA	←	←	←	←
	Register access	CPUCLK_L	CPUCLK2	←	←	←
WDTA1 WDTA2	PCLK	LS IntOSC	←	←	←	←
	Register access	CPUCLK_L	CPUCLK2	←	←	←

17.4 Interrupt Requests

Unit Interrupt Signal (FENMI interrupt)	Interrupt Request				
	F1Kx	F1K	F1L	F1M	F1H
WDTA0					
WDTA0TNMI	WDTA0NMI	←	←	←	←
WDTA1					
WDTA1TNMI	WDTA1NMI	←	←	←	←
WDTA2					
WDTA2TNMI	WDTA2NMI	-	-	-	WDTA2NMI

17.5 Reset Sources

Unit Name	F1Kx	F1K	F1L	F1M	F1H
WDTA0	Reset sources (AWORES)	←	←	←	←
WDTA1	All reset sources (ISORES)	←	←	←	←
WDTA2	All reset sources (ISORES)	←	-	-	←

17.6 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1L	F1M	F1H
WDTAnWDTE	<WDTAn_base> + 0000H	Same	Same	Same	Same	Same
WDTAnEVAC	<WDTAn_base> + 0004H	Same	Same	Same	Same	Same
WDTAnREF	<WDTAn_base> + 0008H	Same	Same	Same	Same	Same
WDTAnMD	<WDTAn_base> + 000CH	Same	Same	Same	Same	Same

18. OS Timer (OSTM)

18.1 Overview

The functional feature set of the OSTM between F1Kx and F1L/F1M/F1H/F1K is identical.

Applicable differences can result from the different number of available instances.

18.2 Register Base Address

Base Address Name	F1KH	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
< OSTM0_base>	FFD7 0000H	←	←	←	FFEC 0000H	FFD7 0000H	←
< OSTM1_base>	FFD7 0100H	←	-	FFD7 0100H	-	FFD7 0100H	←
< OSTM2_base>	FFD7 0200H	←	-	FFD7 0200H	-	FFD7 0200H	←
< OSTM3_base>	FFD7 0300H	←	-	FFD7 0300H	-	FFD7 0300H	←
< OSTM4_base>	FFD7 0400H	←	-	FFD7 0400H	-	FFD7 0400H	←
< OSTM5_base>	FFD7 1000H	-	-	-	-	-	FFD7 1000H
< OSTM6_base>	FFD7 1100H	-	-	-	-	-	FFD7 1100H
< OSTM7_base>	FFD7 1200H	-	-	-	-	-	FFD7 1200H
< OSTM8_base>	FFD7 1300H	-	-	-	-	-	FFD7 1300H
< OSTM9_base>	FFD7 1400H	-	-	-	-	-	FFD7 1400H

18.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
OSTMn	PCLK	CPUCLK_L	CPUCLK2	←	←	←
	Register access	CPUCLK_L	CPUCLK2	←	←	←

18.4 Interrupt Requests

Unit Interrupt Signal	Interrupt Number					
	F1KH	F1KM	F1K	F1L	F1M	F1H
OSTM0						
OSTMTINT	84	←	←	76	84	84
OSTM5						
OSTMTINT	314	-	-	-	-	314

Unit Interrupt Signal (FE Level Maskable Interrupt)	Interrupt Request						
	F1KH	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
OSTM0							
OSTMTINT	INTOSTM0_FE	←	←	←	←	←	←
OSTMn	(n=1..9)	(n=1..4)	-	(n=1..4)	-	(n=1..4)	(n=1..9)
OSTMTINT	INTOSTMn_FE	←	-	←	-	INTOSTMn_FE	INTOSTMn_FE

18.5 Reset Sources

Unit Name	F1Kx	F1K	F1L	F1M	F1H
OSTMn	All reset sources (ISORES)	←	←	←	←

18.6 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1KM	F1K	F1L	F1M	F1H
OSTMnCMP	<OSTMn_base> + 0000H	Same	Same	Same	Same	Same
OSTMnCNT	<OSTMn_base> + 0004H	Same	Same	Same	Same	Same
OSTMnTE	<OSTMn_base> + 0010H	Same	Same	Same	Same	Same
OSTMnTS	<OSTMn_base> + 0014H	Same	Same	Same	Same	Same
OSTMnTT	<OSTMn_base> + 0018H	Same	Same	Same	Same	Same
OSTMnCTL	<OSTMn_base> + 0020H	Same	Same	Same	Same	Same
OSTMnEMU	<OSTMn_base> + 0024H	Same	Same	Same	Same	Same

19. Timer Array Unit B (TAUB)

19.1 Overview

On the F1Kx input signal selection circuits are available on each timer input.
Besides this, the functional feature set of the TAUB between F1Kx and F1L/F1M/F1H is identical

19.2 Register Base Address

Base Address Name	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
<TAUB0_base>	FFE3 0000H	←	←	←	←	←
<TAUB1_base>	FFE3 1000H	-	FFE3 1000H	←	←	←

19.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
TAUBn	PCLK	CKSCLK_IPERI2	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_IPERI2	CPUCLK2 CKSCLK_IPERI2	CKSCLK_IPERI2	←	←

19.4 Interrupt Requests

Interrupt signal	Interrupt Number						DMA Trigger Number					
	F1KH F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
TAUB0												
INTTAUB0I0	142	142	142	134	142	142	33 to 38	33 to 38	33	33[1)]	33	33
INTTAUB0I1	143	143	143	135	143	143	33 to 38	33 to 38	92	28[2)]	92	92
INTTAUB0I2	144	144	144	136	144	144	33 to 38	33 to 38	34	34[1)]	34	34
INTTAUB0I3	145	145	145	137	145	145	33 to 38	33 to 38	93	29[2)]	93	93
INTTAUB0I4	146	146	146	138	146	146	33 to 38	33 to 38	35	35[1)]	35	35
INTTAUB0I5	147	147	147	139	147	147	33 to 38	33 to 38	94	30[2)]	94	94
INTTAUB0I6	148	148	148	140	148	148	33 to 38	33 to 38	36	36[1)]	36	36
INTTAUB0I7	149	149	149	141	149	149	33 to 38	33 to 38	95	31[2)]	95	95
INTTAUB0I8	150	150	150	142	150	150	33 to 38	33 to 38	96	32[2)]	96	96
INTTAUB0I9	151	151	151	143	151	151	33 to 38	33 to 38	37	37[1)]	37	37
INTTAUB0I10	152	152	152	144	152	152	33 to 38	33 to 38	97	33[2)]	97	97
INTTAUB0I11	153	153	153	145	153	153	33 to 38	33 to 38	38	38[1)]	38	38
INTTAUB0I12	154	154	154	146	154	154	33 to 38	33 to 38	98	34[2)]	98	98
INTTAUB0I13	155	155	155	147	155	155	33 to 38	33 to 38	39	39[1)]	39	39
INTTAUB0I14	156	156	156	148	156	156	33 to 38	33 to 38	99	35[2)]	99	99
INTTAUB0I15	157	157	157	149	157	157	33 to 38	33 to 38	40	40[1)]	40	40
TAUB1												
INTTAUB1I0	256	-	256	248	256	256	52 to 57	-	52	52[1)]	52	52
INTTAUB1I1	257	-	257	249	257	257	52 to 57	-	115	51[2)]	115	115

Interrupt signal	Interrupt Number						DMA Trigger Number					
	F1KH F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
INTTAUB1I2	258	-	258	250	258	258	52 to 57	-	53	53[1)]	53	53
INTTAUB1I3	259	-	259	251	259	259	52 to 57	-	116	52[2)]	116	116
INTTAUB1I4	260	-	260	252	260	260	52 to 57	-	54	54[1)]	54	54
INTTAUB1I5	261	-	261	253	261	261	52 to 57	-	117	53[2)]	117	117
INTTAUB1I6	262	-	262	254	262	262	52 to 57	-	55	55[1)]	55	55
INTTAUB1I7	263	-	263	255	263	263	52 to 57	-	118	54[2)]	118	118
INTTAUB1I8	264	-	264	256	264	264	52 to 57	-	119	55[2)]	119	119
INTTAUB1I9	265	-	265	257	265	265	52 to 57	-	56	56[1)]	56	56
INTTAUB1I10	266	-	266	258	266	266	52 to 57	-	120	56[2)]	120	120
INTTAUB1I11	267	-	267	259	267	267	52 to 57	-	57	57[1)]	57	57
INTTAUB1I12	268	-	268	260	268	268	52 to 57	-	121	57[2)]	121	121
INTTAUB1I13	269	-	269	261	269	269	52 to 57	-	58	58[1)]	58	58
INTTAUB1I14	270	-	270	262	270	270	52 to 57	-	122	58[2)]	122	122
INTTAUB1I15	271	-	271	263	271	271	52 to 57	-	59	59[1)]	59	59

1) Channels 0 to 7

2) Channels 8 to 15

19.5 Reset Sources

Unit Name	F1Kx	F1K	F1L	F1M	F1H
TAUBn	All reset sources (ISORES)	All reset sources (ISORES)	All reset sources (ISORES)	All reset sources (ISORES)	All reset sources (ISORES)

19.6 Registers overview

Name	Address	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
TAUBn prescaler registers							
TAUBnTPS	<TAUBn_base> + 240H	Same	Same	Same	Same	Same	Same
TAUBn control registers							
TAUBnCDRm	<TAUBn_base> + m × 4H	Same	Same	Same	Same	Same	Same
TAUBnCNTm	<TAUBn_base> + 80H + m × 4H	Same	Same	Same	Same	Same	Same
TAUBnCMORm	<TAUBn_base> + 200H + m × 4H	Same	Same	Same	Same	Same	Same
TAUBnCMURm	<TAUBn_base> + C0H + m × 4H	Same	Same	Same	Same	Same	Same
TAUBnCSRm	<TAUBn_base> + 140H + m × 4H	Same	Same	Same	Same	Same	Same
TAUBnCSCm	<TAUBn_base> + 180H + m × 4H	Same	Same	Same	Same	Same	Same
TAUBnTS	<TAUBn_base> + 1C4H	Same	Same	Same	Same	Same	Same
TAUBnTE	<TAUBn_base> + 1C0H	Same	Same	Same	Same	Same	Same
TAUBnTT	<TAUBn_base> + 1C8H	Same	Same	Same	Same	Same	Same
TAUBn input selection registers							

Name	Address	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
SELB_TAUB0I	<TAUB0_base> + 2000H	Yes	Yes	-	-	-	-
SELB_TAUB1I	<TAUB1_base> + 3000H	Yes	-		-	-	-
TAUBn output registers							
TAUBnTOE	<TAUBn_base> + 5CH	Same	Same	Same	Same	Same	Same
TAUBnTO	<TAUBn_base> + 58H	Same	Same	Same	Same	Same	Same
TAUBnTOM	<TAUBn_base> + 248H	Same	Same	Same	Same	Same	Same
TAUBnTOC	<TAUBn_base> + 24CH	Same	Same	Same	Same	Same	Same
TAUBnTOL	<TAUBn_base> + 040H	Same	Same	Same	Same	Same	Same
TAUBnTDE	<TAUBn_base> + 250H	Same	Same	Same	Same	Same	Same
TAUBnTDL	<TAUBn_base> + 54H	Same	Same	Same	Same	Same	Same
TAUBn reload data registers							
TAUBnRDE	<TAUBn_base> + 260H	Same	Same	Same	Same	Same	Same
TAUBnRDM	<TAUBn_base> + 264H	Same	Same	Same	Same	Same	Same
TAUBnRDS	<TAUBn_base> + 268H	Same	Same	Same	Same	Same	Same
TAUBnRDC	<TAUBn_base> + 26CH	Same	Same	Same	Same	Same	Same
TAUBnRDT	<TAUBn_base> + 44H	Same	Same	Same	Same	Same	Same
TAUBnRSF	<TAUBn_base> + 48H	Same	Same	Same	Same	Same	Same
TAUBn emulation register							
TAUBnEMU	<TAUBn_base> + 290H	Same	Same	Same	Same	Same	Same

20. Timer Array Unit D (TAUD)

20.1 Overview

On the F1Kx input signal selection circuits are available on each timer input.
Besides this, the functional feature set of the TAUD between F1Kx and F1L/F1M/F1H is identical.

20.2 Register Base Address

Base Address Name	F1Kx	F1K	F1L	F1M	F1H
<TAUD0_base>	FFE2 0000H	←	←	←	←

20.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
TAUD0	PCLK	CKSCLK_IPERI1	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_IPERI1	CPUCLK2 CKSCLK_IPERI1	CKSCLK_IPERI1	←	←

20.4 Interrupt Requests

Interrupt signal	Interrupt Number					DMA Trigger Number				
	F1Kx	F1K	F1L	F1M	F1H	F1Kx	F1K	F1L	F1M	F1H
TAUD0										
INTTAUD0I0	8, 132	←	0, 124	8, 132	8, 132	0 to 3, 17, 18	0	0[1)]	0	0
INTTAUD0I1	48	←	39	48	48	0 to 3, 17, 18	15	15[1)]	15	15
INTTAUD0I2	9, 158	←	1, 150	9, 158	9, 158	0 to 3, 17, 18	64	0[2)]	64	64
INTTAUD0I3	49	←	40	49	49	0 to 3, 17, 18	76	12[2)]	76	76
INTTAUD0I4	10, 133	←	2	10, 133	10, 133	0 to 3, 17, 18	1	1[1)]	1	1
INTTAUD0I5	50	←	41	50	50	0 to 3, 17, 18	16	16[1)]	16	16
INTTAUD0I6	11, 134	←	3	11, 134	11, 134	0 to 3, 17, 18	65	1[2)]	65	65
INTTAUD0I7	51	←	42	51	51	0 to 3, 17, 18	77	13[2)]	77	77
INTTAUD0I8	12, 135	←	4	12, 135	12, 135	0 to 3, 17, 18	2	2[1)]	2	2
INTTAUD0I9	52	←	43	52	52	0 to 3, 17, 18	17	17[1)]	17	17
INTTAUD0I10	13, 159	←	5, 151	13, 159	13, 159	0 to 3, 17, 18	66	2[2)]	66	66
INTTAUD0I11	53	←	44	53	53	0 to 3, 17, 18	78	14[2)]	78	78
INTTAUD0I12	14, 160	←	6, 152	14, 160	14, 160	0 to 3, 17, 18	3	3[1)]	3	3

Interrupt signal	Interrupt Number					DMA Trigger Number				
	F1Kx	F1K	F1L	F1M	F1H	F1Kx	F1K	F1L	F1M	F1H
INTTAUD0I13	54	←	45	54	54	0 to 3, 17, 18	18	18[1)]	18	18
INTTAUD0I14	15, 161	←	7, 153	15, 161	15, 161	0 to 3, 17, 18	67	3[2)]	67	67
INTTAUD0I15	55	←	46	55	55	0 to 3, 17, 18	79	15[2)]	79	79

3) Channels 0 to 7

4) Channels 8 to 15

20.5 Reset Sources

Unit Name	F1Kx	F1K	F1L	F1M	F1H
TAUDn	All reset sources (ISORES)	←	←	←	←

20.6 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1L	F1M	F1H
TAUDn prescaler registers						
TAUDnTPS	<TAUDn_base> + 240H	Same	Same	Same	Same	Same
TAUDnBRS	<TAUDn_base> + 244H	Same	Same	Same	Same	Same
TAUDn control registers						
TAUDnCDRm	<TAUDn_base> + m × 4H	Same	Same	Same	Same	Same
TAUDnCNTm	<TAUDn_base> + 80H + m × 4H	Same	Same	Same	Same	Same
TAUDnCMORm	<TAUDn_base> + 200H + m × 4H	Same	Same	Same	Same	Same
TAUDnCMURm	<TAUDn_base> + C0H + m × 4H	Same	Same	Same	Same	Same
TAUDnCSRm	<TAUDn_base> + 140H + m × 4H	Same	Same	Same	Same	Same
TAUDnCSCm	<TAUDn_base> + 180H + m × 4H	Same	Same	Same	Same	Same
TAUDnTS	<TAUDn_base> + 1C4H	Same	Same	Same	Same	Same
TAUDnTE	<TAUDn_base> + 1C0H	Same	Same	Same	Same	Same
TAUDnTT	<TAUDn_base> + 1C8H	Same	Same	Same	Same	Same
TAUDn input selection registers						
SELB_TAUD0I	<TAUD0_base> + 4000H	Yes	-	-	-	-
TAUDn output registers						
TAUDnTOE	<TAUDn_base> + 5CH	Same	Same	Same	Same	Same
TAUDnTO	<TAUDn_base> + 58H	Same	Same	Same	Same	Same
TAUDnTOM	<TAUDn_base> + 248H	Same	Same	Same	Same	Same
TAUDnTOC	<TAUDn_base> + 24CH	Same	Same	Same	Same	Same
TAUDnTOL	<TAUDn_base> + 040H	Same	Same	Same	Same	Same
TAUDnTDE	<TAUDn_base> + 250H	Same	Same	Same	Same	Same
TAUDnTDM	<TAUDn_base> + 254H	Same	Same	Same	Same	Same
TAUDnTDL	<TAUDn_base> + 54H	Same	Same	Same	Same	Same
TAUDnTRO	<TAUDn_base> + 4CH	Same	Same	Same	Same	Same
TAUDnTRE	<TAUDn_base> + 258H	Same	Same	Same	Same	Same
TAUDnTRC	<TAUDn_base> + 25CH	Same	Same	Same	Same	Same

Name	Address	F1Kx	F1K	F1L	F1M	F1H
TAUDnTME	<TAUDn_base> + 50H	Same	Same	Same	Same	Same
TAUDn reload data registers						
TAUDnRDE	<TAUDn_base> + 260H	Same	Same	Same	Same	Same
TAUDnRDM	<TAUDn_base> + 264H	Same	Same	Same	Same	Same
TAUDnRDS	<TAUDn_base> + 268H	Same	Same	Same	Same	Same
TAUDnRDC	<TAUDn_base> + 26CH	Same	Same	Same	Same	Same
TAUDnRDT	<TAUDn_base> + 44H	Same	Same	Same	Same	Same
TAUDnRSF	<TAUDn_base> + 48H	Same	Same	Same	Same	Same
TAUDn emulation register						
TAUDnEMU	<TAUDn_base> + 290H	Same	Same	Same	Same	Same

21. Timer Array Unit J (TAUJ)

21.1 Overview

The functional feature set of the TAUJ between F1Kx and F1K, F1L/F1M/F1H is identical.

21.2 Register Base Address

Base Address Name	F1Kx	F1K	F1L	F1M	F1H
<TAUJ0_base>	FFE5 0000H	FFE5 0000H	FFE5 0000H	FFE5 0000H	FFE5 0000H
<TAUJ1_base>	FFE5 1000H	FFE5 1000H	FFE5 1000H	FFE5 1000H	FFE5 1000H
<TAUJ2_base>	FFE5 0100H	-	-	-	-
<TAUJ3_base>	FFE5 1100H	-	-	-	-

21.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
TAUJ0	PCLK	CKSCLK_ATAUJ	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_ATAUJ	CPUCLK2, CKSCLK_ATAUJ	CPUCLK_ATAUJ	←	←
TAUJ1	PCLK	CKSCLK_IPERI1	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_IPERI1	CPUCLK2, CKSCLK_IPERI1	CKSCLK_IPERI1	←	←
TAUJ2	PCLK	CKSCLK_ATAUJ	-	-	-	-
	Register access	CPUCLK_L, CKSCLK_ATAUJ	-	-	-	-
TAUJ3	PCLK	CKSCLK_IPERI1	-	-	-	-
	Register access	CPUCLK_L, CKSCLK_IPERI1	-	-	-	-

21.4 Interrupt Requests

Interrupt signal	Interrupt Number					DMA Trigger Number				
	F1Kx	F1K	F1L	F1M	F1H	F1Kx	F1K	F1L	F1M	F1H
TAUJ0										
INTTAUJ0I0	80	80	72	80	80	21	21	21[1)]	21	21
INTTAUJ0I1	81	81	73	81	81	80	80	16[2)]	80	80
INTTAUJ0I2	82	82	74	82	82	81	81	17[2)]	81	81
INTTAUJ0I3	83	83	75	83	83	22	22	22[1)]	22	22
TAUJ1										
INTTAUJ1I0	168	168	160	168	168	46	46	46[1)]	46	46
INTTAUJ1I1	169	169	161	169	169	100	100	36[2)]	100	100
INTTAUJ1I2	170	170	162	170	170	47	47	47[1)]	47	47
INTTAUJ1I3	171	171	163	171	171	101	101	37[2)]	101	101
TAUJ2										

Interrupt signal	Interrupt Number					DMA Trigger Number				
	F1Kx	F1K	F1L	F1M	F1H	F1Kx	F1K	F1L	F1M	F1H
INTTAUJ2I0	277	-	-	-	-	103	-	-	-	-
INTTAUJ2I1	278	-	-	-	-	104	-	-	-	-
INTTAUJ2I2	279	-	-	-	-	105	-	-	-	-
INTTAUJ2I3	280	-	-	-	-	106	-	-	-	-
TAUJ3										
INTTAUJ3I0	281	-	-	-	-	107	-	-	-	-
INTTAUJ3I1	282	-	-	-	-	108	-	-	-	-
INTTAUJ3I2	283	-	-	-	-	109	-	-	-	-
INTTAUJ3I3	284	-	-	-	-	110	-	-	-	-

1) Channels 0 to 7

2) Channels 8 to 15

21.5 Reset Sources

Unit Name	F1Kx	F1K	F1L	F1M	F1H
TAUJ0	All reset sources except the transition to DeepSTOP mode (AWORES)				
TAUJ1	All reset sources (ISORES)				
TAUJ2	All reset sources except the transition to DeepSTOP mode (AWORES)	-	-	-	-
TAUJ3	All reset sources (ISORES)	-	-	-	-

21.6 Registers overview

Registers are identical between F1Kx and F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1L	F1M	F1H
TAUJn prescaler registers						
TAUJnTPS	<TAUJn_base> + 90H	Same	Same	Same	Same	Same
TAUJnBRS	<TAUJn_base> + 94H	Same	Same	Same	Same	Same
TAUJn control registers						
TAUJnCDRm	<TAUJn_base> + m × 4H	Same	Same	Same	Same	Same
TAUJnCNTm	<TAUJn_base> + 10H + m × 4H	Same	Same	Same	Same	Same
TAUJnCMORm	<TAUJn_base> + 80H + m × 4H	Same	Same	Same	Same	Same
TAUJnCMURm	<TAUJn_base> + 20H + m × 4H	Same	Same	Same	Same	Same
TAUJnCSRm	<TAUJn_base> + 30H + m × 4H	Same	Same	Same	Same	Same
TAUJnCSCm	<TAUJn_base> + 40H + m × 4H	Same	Same	Same	Same	Same
TAUJnTS	<TAUJn_base> + 54H	Same	Same	Same	Same	Same
TAUJnTE	<TAUJn_base> + 50H	Same	Same	Same	Same	Same
TAUJnTT	<TAUJn_base> + 58H	Same	Same	Same	Same	Same
TAUJn input selection registers						
SELB_TAUJ0I	<TAUJ0_base> + 4000H	Yes	Yes	Yes	Yes	Yes
SELB_TAUJ0I	<TAUJ0_base> + 4004H	Yes	-	-	-	-
TAUJn output registers						
TAUJnTOE	<TAUJn_base> + 60H	Same	Same	Same	Same	Same
TAUJnTO	<TAUJn_base> + 5CH	Same	Same	Same	Same	Same

Name	Address	F1Kx	F1K	F1L	F1M	F1H
TAUJnTOM	<TAUJn_base> + 98H	Same	Same	Same	Same	Same
TAUJnTOC	<TAUJn_base> + 9CH	Same	Same	Same	Same	Same
TAUJnTOL	<TAUJn_base> + 64H	Same	Same	Same	Same	Same
TAUJn reload data registers						
TAUJnRDE	<TAUJn_base> + A0H	Same	Same	Same	Same	Same
TAUJnRDM	<TAUJn_base> + A4H	Same	Same	Same	Same	Same
TAUJnRDT	<TAUJn_base> + 68H	Same	Same	Same	Same	Same
TAUJnRSF	<TAUJn_base> + 6CH	Same	Same	Same	Same	Same
TAUJn emulation register						
TAUJnEMU	<TAUJn_base> + A8H	Same	Same	Same	Same	Same

22. Real-Time Clock (RTCA)

22.1 Overview

The functional feature set of the RTCA between F1Kx and F1K, F1L/F1M/F1H is identical.

22.2 Register Base Address

Base Address Name	F1Kx	F1K	F1L	F1M	F1H
<RTCA0_base>	FFE7 8000H	←	←	←	←

22.3 Clock Supply

Base Address Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
RTCA0	RTCATCKI	CKSCLK_ARTCA	←	←	←	←
	PCLK	CPUCLK_L	CPUCLK2	←	←	←
	Register access	CPUCLK_L	CPUCLK2	←	←	←

22.4 Interrupt Requests

Unit Interrupt Signal	F1Kx	F1K	F1L	F1M	F1H
RTCA0					
INTRTCA01S	209	←	201	209	209
INTRTCA0AL	210	←	202	210	210
INTRTCA0R	211	←	203	211	211

22.5 Reset Sources

Unit Name	F1Kx	F1K	F1L	F1M	F1H
RTCA0	Power-up reset (PURES)	←	←	←	←

22.6 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1L	F1M	F1H
Control registers						
RTCAnCTL0	<RTCAn_base> + 00H	Same	Same	Same	Same	Same
RTCAnCTL1	<RTCAn_base> + 04H	Same	Same	Same	Same	Same
RTCAnCTL2	<RTCAn_base> + 08H	Same	Same	Same	Same	Same
Sub-counter registers						
RTCAnSUBC	<RTCAn_base> + 0CH	Same	Same	Same	Same	Same
RTCAnSRBU	<RTCAn_base> + 10H	Same	Same	Same	Same	Same
RTCAnSUBU	<RTCAn_base> + 38H	Same	Same	Same	Same	Same
RTCAnSCMP	<RTCAn_base> + 3CH	Same	Same	Same	Same	Same
Clock counter and buffer registers						
RTCAnSECC	<RTCAn_base> + 4CH	Same	Same	Same	Same	Same
RTCAnSEC	<RTCAn_base> + 14H	Same	Same	Same	Same	Same

Name	Address	F1Kx	F1K	F1L	F1M	F1H
RTCAnMINC	<RTCAn_base> + 50H	Same	Same	Same	Same	Same
RTCAnMIN	<RTCAn_base> + 18H	Same	Same	Same	Same	Same
RTCAnHOURC	<RTCAn_base> + 54H	Same	Same	Same	Same	Same
RTCAnHOUR	<RTCAn_base> + 1CH	Same	Same	Same	Same	Same
RTCAnWEEKC	<RTCAn_base> + 58H	Same	Same	Same	Same	Same
RTCAnWEEK	<RTCAn_base> + 20H	Same	Same	Same	Same	Same
RTCAnDAYC	<RTCAn_base> + 5CH	Same	Same	Same	Same	Same
RTCAnDAY	<RTCAn_base> + 24H	Same	Same	Same	Same	Same
RTCAnMONC	<RTCAn_base> + 60H	Same	Same	Same	Same	Same
RTCAnMONTH	<RTCAn_base> + 28H	Same	Same	Same	Same	Same
RTCAnYEARC	<RTCAn_base> + 64H	Same	Same	Same	Same	Same
RTCAnYEAR	<RTCAn_base> + 2CH	Same	Same	Same	Same	Same
Special counter and buffer registers						
RTCAnTIMEC	<RTCAn_base> + 68H	Same	Same	Same	Same	Same
RTCAnTIME	<RTCAn_base> + 30H	Same	Same	Same	Same	Same
RTCAnCALC	<RTCAn_base> + 6CH	Same	Same	Same	Same	Same
RTCAnCAL	<RTCAn_base> + 34H	Same	Same	Same	Same	Same
Alarm time setting registers						
RTCAnALM	<RTCAn_base> + 40H	Same	Same	Same	Same	Same
RTCAnALH	<RTCAn_base> + 44H	Same	Same	Same	Same	Same
RTCAnALW	<RTCAn_base> + 48H	Same	Same	Same	Same	Same
Emulation register						
RTCAnEMU	<RTCAn_base> + 74H	Same	Same	Same	Same	Same

23. Encoder Timer (ENCA)

23.1 Overview

The functional feature set of the ENCA between F1Kx and F1K, F1L/F1M/F1H is identical.

23.2 Register Base Address

Base Address Name	F1Kx	F1K	F1L	F1M	F1H
<ENCA0_base>	FFE8 0000H	←	←	←	←

23.3 Clock Supply

Unit Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
ENCA0	PCLK	CKSCLK_IPERI1	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_IPERI1	CPUCLK2 CKSCLK_IPERI1	CKSCLK_IPERI1	←	←

23.4 Interrupt Requests

Unit Interrupt Signal	F1Kx	F1K	F1L	F1M	F1H
ENCA0					
ENCATIOV	85	85	77	85	85
ENCATIUD	86	86	78	86	86
ENCATINT0	87	87	79	87	87
ENCATINT1	88	88	80	88	88
ENCATIEC	89	89	81	89	89

23.5 Reset Sources

Unit Name	F1Kx	F1K	F1L	F1M	F1H
ENCA0	All reset sources (ISORES)	←	←	←	←

23.6 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1L	F1M	F1H
ENCAnCCR0	<ENCAn_base>	Same	Same	Same	Same	Same
ENCAnCCR1	<ENCAn_base> + 04H	Same	Same	Same	Same	Same
ENCAnCNT	<ENCAn_base> + 08H	Same	Same	Same	Same	Same
ENCAnFLG	<ENCAn_base> + 0CH	Same	Same	Same	Same	Same
ENCAnFGC	<ENCAn_base> + 10H	Same	Same	Same	Same	Same
ENCAnTE	<ENCAn_base> + 14H	Same	Same	Same	Same	Same
ENCAnTS	<ENCAn_base> + 18H	Same	Same	Same	Same	Same
ENCAnTT	<ENCAn_base> + 1CH	Same	Same	Same	Same	Same
ENCAnIOC0	<ENCAn_base> + 20H	Same	Same	Same	Same	Same

Name	Address	F1Kx	F1K	F1L	F1M	F1H
ENCAnCTL	<ENCAn_base> + 40H	Same	Same	Same	Same	Same
ENCAnIOC1	<ENCAn_base> + 44H	Same	Same	Same	Same	Same
ENCAnEMU	<ENCAn_base> + 48H	Same	Same	Same	Same	Same

24. PWM Output/Diagnostic (PWM-Diag)

24.1 Overview

The PWM-Diag macro provides additional functionality on the F1Kx compared to the F1K/F1L/F1M/F1H devices.

24.2 Register Base Address

Base Address Name	F1Kx	F1K	F1L	F1M	F1H
<PWBAn_base>	FFE7 2800H	FFE7 2800H	Same	Same	Same
<PWGAn_base>	FFE7 1000H + 40H × n	FFE7 1000H + 40H × n	Same	Same	Same
<PWSAn_base>	FFE7 0000H	FFE7 0000H	Same	Same	Same
<SLPW_base>	FFE7 3000H	FFE7 3000H	FFBC 1000H	FFE7 3000H	FFE7 3000H
<PWGAINTF_base>	FFE7 3100 H	-	-	-	-

24.3 Clock Supply

Unit Name	Clock for the Unit	F1Kx	F1K	F1L	F1M	F1H
PWBAn	PCLK	CKSCLK_IPERI2	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_IPERI2	CPUCLK2 CKSCLK_IPERI2	-	-	-
PWGAn	PCLK	CKSCLK_IPERI2	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_IPERI2	CPUCLK2 CKSCLK_IPERI2	-	-	-
PWSAn	PCLK	CKSCLK_IPERI2	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_IPERI2	CPUCLK2 CKSCLK_IPERI2	-	-	-

24.4 Interrupt Requests

Unit Interrupt Signal	F1KH	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
INTQFULL	91	91	91	91	83	91	91
PWGA_INT0	92, 95	92	92	92	84	92	92
PWGA_INT1	92, 95	92	92	93	85	93	93
PWGA_INT2	92, 95	92	92	94	86	94	94
PWGA_INT3	92, 95	92	92	95	87	95	95
PWGA_INT4	92, 95	92	92	85	77	85	85
PWGA_INT5	92, 95	92	92	86	78	86	86
PWGA_INT6	92, 95	92	92	87	79	87	87
PWGA_INT7	92, 95	92	92	88	80	88	88
PWGA_INT8	92, 95	92	92	96	88	96	96
PWGA_INT9	92, 95	92	92	97	89	97	97
PWGA_INT10	92, 95	92	92	98	90	98	98
PWGA_INT11	92, 95	92	92	99	91	99	99
PWGA_INT12	92, 95	92	92	100	92	100	100
PWGA_INT13	92, 95	92	92	101	93	101	101
PWGA_INT14	92, 95	92	92	102	94	102	102
PWGA_INT15	92, 95	92	92	103	95	103	103
PWGA_INT16	92, 95	92	92	145	137	145	145
PWGA_INT17	92, 95	92	92	147	139	147	147

Unit Interrupt Signal	F1KH	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
PWGA_INT18	92, 95	92	92	149	141	149	149
PWGA_INT19	92, 95	92	92	151	143	151	151
PWGA_INT20	92, 95	92	92	124	116	124	124
PWGA_INT21	92, 95	92	92	125	117	125	125
PWGA_INT22	92, 95	92	92	126	118	126	126
PWGA_INT23	92, 95	92	92	127	119	127	127
PWGA_INT24	92, 95	92	92	184	176	184	184
PWGA_INT25	92, 95	92	92	185	177	185	185
PWGA_INT26	92, 95	92	92	153	145	153	153
PWGA_INT27	92, 95	92	92	186	178	186	186
PWGA_INT28	92, 95	92	92	187	179	187	187
PWGA_INT29	92, 95	92	92	188	180	188	188
PWGA_INT30	92, 95	92	92	155	147	155	155
PWGA_INT31	92, 95	92	92	157	149	157	157
PWGA_INT32	93, 96	93	93	189	181	189	189
PWGA_INT33	93, 96	93	93	190	182	190	190
PWGA_INT34	93, 96	93	93	191	183	191	191
PWGA_INT35	93, 96	93	93	192	184	192	192
PWGA_INT36	93, 96	93	93	193	185	193	193
PWGA_INT37	93, 96	93	93	194	186	194	194
PWGA_INT38	93, 96	93	93	195	187	195	195
PWGA_INT39	93, 96	93	93	196	188	196	196
PWGA_INT40	93, 96	93	93	197	189	197	197
PWGA_INT41	93, 96	93	93	198	190	198	198
PWGA_INT42	93, 96	93	93	199	191	199	199
PWGA_INT43	93, 96	93	93	200	192	200	200
PWGA_INT44	93, 96	93	93	201	193	201	201
PWGA_INT45	93, 96	93	93	202	194	202	202
PWGA_INT46	93, 96	93	93	203	195	203	203
PWGA_INT47	93, 96	93	93	204	196	204	204
PWGA_INT48	93, 96	93	-	240	232	240	240
PWGA_INT49	93, 96	93	-	241	233	241	241
PWGA_INT50	93, 96	93	-	242	234	242	242
PWGA_INT51	93, 96	93	-	243	235	243	243
PWGA_INT52	93, 96	93	-	244	236	244	244
PWGA_INT53	93, 96	93	-	245	237	245	245
PWGA_INT54	93, 96	93	-	246	238	246	246
PWGA_INT55	93, 96	93	-	247	239	247	247
PWGA_INT56	93, 96	93	-	248	240	248	248
PWGA_INT57	93, 96	93	-	249	241	249	249
PWGA_INT58	93, 96	93	-	250	242	250	250
PWGA_INT59	93, 96	93	-	251	243	251	251
PWGA_INT60	93, 96	93	-	252	244	252	252
PWGA_INT61	93, 96	93	-	253	245	253	253
PWGA_INT62	93, 96	93	-	254	246	254	254
PWGA_INT63	93, 96	93	-	255	247	255	255
PWGA_INT64	94, 97	94	-	277	269	277	277
PWGA_INT65	94, 97	94	-	278	270	278	278
PWGA_INT66	94, 97	94	-	279	271	279	279
PWGA_INT67	94, 97	94	-	280	272	280	280
PWGA_INT68	94, 97	94	-	281	273	281	281
PWGA_INT69	94, 97	94	-	282	274	282	282
PWGA_INT70	94, 97	94	-	283	275	283	283
PWGA_INT71	94, 97	94	-	284	276	284	284
PWGA_INT72	94, 97	94	-	-	-	290	290

Unit Interrupt Signal	F1KH	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
PWGA_INT73	94, 97	94	-	-	-	291	291
PWGA_INT74	94, 97	94	-	-	-	292	292
PWGA_INT75	94, 97	94	-	-	-	293	293
PWGA_INT76	94, 97	94	-	-	-	294	294
PWGA_INT77	94, 97	94	-	-	-	295	295
PWGA_INT78	94, 97	94	-	-	-	296	296
PWGA_INT79	94, 97	94	-	-	-	297	297
PWGA_INT80	94, 97	94	-	-	-	-	335
PWGA_INT81	94, 97	94	-	-	-	-	336
PWGA_INT82	94, 97	94	-	-	-	-	337
PWGA_INT83	94, 97	94	-	-	-	-	338
PWGA_INT84	94, 97	94	-	-	-	-	339
PWGA_INT85	94, 97	94	-	-	-	-	340
PWGA_INT86	94, 97	94	-	-	-	-	341
PWGA_INT87	94, 97	94	-	-	-	-	342
PWGA_INT88	94, 97	94	-	-	-	-	343
PWGA_INT89	94, 97	94	-	-	-	-	344
PWGA_INT90	94, 97	94	-	-	-	-	345
PWGA_INT91	94, 97	94	-	-	-	-	346
PWGA_INT92	94, 97	94	-	-	-	-	347
PWGA_INT93	94, 97	94	-	-	-	-	348
PWGA_INT94	94, 97	94	-	-	-	-	349
PWGA_INT95	94, 97	94	-	-	-	-	350

24.5 Reset Sources

Unit Name	F1Kx	F1K	F1L	F1M	F1H
PWBAn PWGAn PWSAn	All reset sources (ISORES)	←	←	←	←

24.6 Registers overview

Name	Address	F1Kx	F1K	F1L	F1M	F1H
PWBAnBRSm	<PWBAn_base> + 0004H × m	Same	Same	Same	Same	Same
PWBAnTE	<PWBAn_base> + 0010H	Same	Same	Same	Same	Same
PWBAnTS	<PWBAn_base> + 0014H	Same	Same	Same	Same	Same
PWBAnTT	<PWBAn_base> + 0018H	Same	Same	Same	Same	Same
PWBAnEMU	<PWBAn_base> + 001CH	Same	Same	Same	Same	Same
PWGAnCSDR	<PWGAn_base> + 0000H	Same	Same	Same	Same	Same
PWGAnCRDR	<PWGAn_base> + 0004H	Same	Same	Same	Same	Same
PWGAnCTDR	<PWGAn_base> + 0008H	Same	Same	Same	Same	Same
PWGAnRDT	<PWGAn_base> + 000CH	Yes	Yes	Yes	Yes	Yes
PWGAnRSF	<PWGAn_base> + 0010H	Yes	Yes	Yes	Yes	Yes
PWGAnCNT	<PWGAn_base> + 0014H	Same	Same	Same	Same	Same
PWGAnTCR	<PWGAn_base> + 0018H	Yes	-	-	-	-
PWGAnTCBR	<PWGAn_base> + 001CH	Yes	-	-	-	-
PWGAnCTL	<PWGAn_base> + 0020H	Yes	Yes	Yes	Yes	Yes
PWGAnCSBR	<PWGAn_base> + 0024H	Same	Same	Same	Same	Yes
PWGAnCRBR	<PWGAn_base> + 0028H	Same	Same	Same	Same	Same
PWGAnCTBR	<PWGAn_base> + 002CH	Same	Same	Same	Same	Same

Name	Address	F1Kx	F1K	F1L	F1M	F1H
SLPWGAk	<SLPW_base> + k × 4H	Same	Same	Same	Same	Same
PWGAPRD	<SLPW_base> + 000CH	Yes	-	-	-	-
PWGAPRDSLk	<SLPW_base> + 0010H + k × 4H	Yes	-	-	-	-
PWSAnCTL	<PWSAn_base> + 0000H	Yes	Yes	Yes	Yes	Yes
PWSAnSTR	<PWSAn_base> + 0004H	Same	Same	Same	Same	Same
PWSAnSTC	<PWSAn_base> + 0008H	Same	Same	Same	Same	Same
PWSAnQUEj	<PWSAn_base> + 0020H + j × 4H	Same	Same	Same	Same	Same
PWSAnPVCRx_y	<PWSAn_base> + 0040H + x × 2H	Yes	Yes	Yes	Yes	Yes
PWSAnPWDDIRz	<PWSAn_base> + 0200H + z × 4H	Yes	-	-	-	-
PWSAnEMU	<PWSAn_base> + 000CH	Same	Same	Same	Same	Same
PWGAINTFhk	<PWGAINTF_base> + h × 30H + k × 10H	Yes	-	-	-	-
PWGAINTMSKhk	<PWGAINTF_base> + h × 30H + k × 10H + 4H	Yes	-	-	-	-
PWGAINTFChk	<PWGAINTF_base> + h × 30H + k × 10H + 8H	Yes	-	-	-	-

25. A/D Converter (ADCA)

25.1 Overview

The F1Kx provides additional features compared to the F1K/F1L/F1M/F1H devices:

- Increased number of upper/lower limit pairs (from 3 pairs to 8 pairs).
- Individual synchronous stop trigger for each scan group.
- Stabilization time control for each AIn pin.

25.2 Register Base Address

Base Address Name	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
<ADCA0_base>	FFF2 0000H	FFF2 0000H	←	←	←	←
<ADCA1_base>	FFD6 D000H	-	FFD6 D000H	FFF2 1000H	FFD6 D000H	←

25.3 Clock Supply

Unit Name	Clock for the Unit	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
ADCA0	ADCLK	CKSCLK_AADCA	←	←	←	←	←
	Register access	CPUCLK_L, CKSCLK_AADCA	←	CPUCLK2 CKSCLK_AADCA	CKSCLK_AADCA	←	←
ADCA1	ADCLK	CKSCLK_IADCA	-	CKSCLK_IADCA	←	←	←
	Register access	CPUCLK_L	-	CPUCLK2	←	←	←

25.4 Interrupt Requests

Interrupt signal	Interrupt Number						DMA Trigger Number					
	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
ADCA0												
INT_ADE	56	56	56	47	56	56	—	—	—	—	—	—
INT_SG1	18	18	18	10	18	18	4	4	4	4[1)]	4	4
INT_SG2	19	19	19	11	19	19	5	5	5	5[1)]	5	5
INT_SG3	20, 32	20, 32	20, 32	12	20, 32	20, 32	6	6	6	6[1)]	6	6
ADC_CONV_END0	—	—	—	—	—	—	7	7	7	7[1)]	7	7
ADCA1												
INT_ADE	212	—	212	204	212	212	—	—	—	—	—	—
INT_SG1	213	—	213	205	213	213	115	—	103	39[2)]	103	103
INT_SG2	214	—	214	206	214	214	116	—	104	40[2)]	104	104
INT_SG3	215	—	215	207	215	215	117	—	105	41[2)]	105	105
ADC_CONV_END1	—	—	—	—	—	—	118	—	106	42[2)]	106	106

1) Channels 0 to 7
2) Channels 8 to 15

25.5 Reset Sources

Unit Name	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
ADCA0	Reset sources other than transition to DeepSTOP mode (AWORES)					
ADCA1	All reset sources (ISORES)	-	All reset sources (ISORES)			

25.6 Registers overview

Name	Address	F1Kx	F1K	F1L	F1M	F1H
ADCA Specific Registers (Virtual Channel)						
ADCAnVCRj	<ADCAn_base> + j × 4H	Yes	←	←	←	←
ADCAnPWDVCR	<ADCAn_base> + 0F4H	Yes	←	←	←	←
ADCAnDRj	<ADCAn_base> + 100H + j × 2H	Yes	←	←	←	←
ADCAnDIRj	<ADCAn_base> + 200H + j × 4H	Yes	←	←	←	←
ADCAnPWDTSNDR	<ADCAn_base> + 178H	Yes	←	←	←	←
ADCAnPWDDIR	<ADCAn_base> + 2F4H	Yes	←	←	←	←
ADCA Specific Registers (Control)						
ADCAnADHALTR	<ADCAn_base> + 300H	Yes	←	←	←	←
ADCAnADCR	<ADCAn_base> + 304H	Yes	←	←	←	←
ADCAnMPXCURR	<ADCAn_base> + 30CH	Yes	←	←	←	←
ADCAnTHSMPSTCR	<ADCAn_base> + 314H	Yes	←	←	←	←
ADCAnTHCR	<ADCAn_base> + 318H	Yes	←	←	←	←
ADCAnTHAHLDSTCR	<ADCAn_base> + 31CH	Yes	←	←	←	←
ADCAnTHBHLDSTCR	<ADCAn_base> + 320H	Yes	←	←	←	←
ADCAnTHACR	<ADCAn_base> + 324H	Yes	←	←	←	←
ADCAnTHBCR	<ADCAn_base> + 328H	Yes	←	←	←	←
ADCAnTHER	<ADCAn_base> + 32CH	Yes	←	←	←	←
ADCAnTHGSR	<ADCAn_base> + 330H	Yes	←	←	←	←
ADCAnSMPCR	<ADCAn_base> + 380H	Yes	←	←	←	←
ADCAnMPXSTBTSELR0	<ADCAn_base> + 5F0H	Yes	-	-	-	-
ADCAnMPXSTBTSELR1	<ADCAn_base> + 5F4H	Yes	-	-	-	-
ADCAnMPXSTBTSELR2	<ADCAn_base> + 5F8H	Yes	-	-	-	-
ADCAnMPXSTBTSELR3	<ADCAn_base> + 5FCH	Yes	-	-	-	-
ADCAnMPXSTBTSELR4	<ADCAn_base> + 600H	Yes	-	-	-	-
ADCAnMPXSTBTR0	<ADCAn_base> + 610H	Yes	-	-	-	-
ADCAnMPXSTBTR1	<ADCAn_base> + 614H	Yes	-	-	-	-
ADCAnMPXSTBTR2	<ADCAn_base> + 618H	Yes	-	-	-	-
ADCAnMPXSTBTR3	<ADCAn_base> + 61CH	Yes	-	-	-	-
ADCAnMPXSTBTR4	<ADCAn_base> + 620H	Yes	-	-	-	-
ADCAnMPXSTBTR5	<ADCAn_base> + 624H	Yes	-	-	-	-
ADCAnMPXSTBTR6	<ADCAn_base> + 628H	Yes	-	-	-	-
ADCAnMPXSTBTR7	<ADCAn_base> + 62CH	Yes	-	-	-	-
ADCA Specific Registers (Safety-related)						
ADCAnSFTCR	<ADCAn_base> + 334H	Yes	←	←	←	←
ADCAnULLMTBR0	<ADCAn_base> + 338H	Yes	←	←	←	←
ADCAnULLMTBR1	<ADCAn_base> + 33CH	Yes	←	←	←	←
ADCAnULLMTBR2	<ADCAn_base> + 340H	Yes	←	←	←	←
ADCAnECR	<ADCAn_base> + 344H	Yes	←	←	←	←
ADCAnULER	<ADCAn_base> + 348H	Yes	←	←	←	←

Name	Address	F1Kx	F1K	F1L	F1M	F1H
ADCAnOWER	<ADCAn_base> + 34CH	Yes	←	←	←	←
ADCAnULEVCFR0	<ADCAn_base> + 540H	Yes	-	-	-	-
ADCAnULEVCFR1	<ADCAn_base> + 544H	Yes	-	-	-	-
ADCAnULLMTBR3	<ADCAn_base> + 564H	Yes	-	-	-	-
ADCAnULLMTBR4	<ADCAn_base> + 568H	Yes	-	-	-	-
ADCAnULLMTBR5	<ADCAn_base> + 56CH	Yes	-	-	-	-
ADCAnULLMTBR6	<ADCAn_base> + 570H	Yes	-	-	-	-
ADCAnULLMTBR7	<ADCAn_base> + 574H	Yes	-	-	-	-
Scan Group Unique Registers						
ADCAnSGSTCRx	<ADCAn_base> + x × 40H + 400H	Yes	←	←	←	←
ADCAnPWDSGSTPCR	<ADCAn_base> + 504H	Yes	-	-	-	-
ADCAnPWDSGCR	<ADCAn_base> + 508H	Yes	←	←	←	←
ADCAnSGCRx	<ADCAn_base> + x × 40H + 408H	Yes	←	←	←	←
ADCAnSGVCSPx	<ADCAn_base> + x × 40H + 40CH	Yes	←	←	←	←
ADCAnSGVCEPx	<ADCAn_base> + x × 40H + 410H	Yes	←	←	←	←
ADCAnSGMCYCRx	<ADCAn_base> + x × 40H + 414H	Yes	←	←	←	←
ADCAnPWDSGSEFCR	<ADCAn_base> + 518H	Yes	←	←	←	←
ADCAnSGSEFCRx	<ADCAn_base> + x × 40H + 418H	Yes	←	←	←	←
ADCAnSGSTR	<ADCAn_base> + 308H	Yes	←	←	←	←
ADCAnSGSTPCRx	<ADCAn_base> + x × 40H + 404H	Yes	-	-	-	-
H/W Trigger Specific Register						
ADCAnSGTSELx	<ADCAn_base> + x × 40H + 41CH	Yes	←	←	←	←
Self-Diagnosis Specific Registers						
ADCAnDGCTL0	<ADCAn_base> + 350H	Yes	←	←	←	←
ADCAnDGCTL1	<ADCAn_base> + 354H	Yes	←	←	←	←
ADCAnPDCTL1	<ADCAn_base> + 358H	Yes	←	←	←	←
ADCAnPDCTL2	<ADCAn_base> + 35CH	Yes	←	←	←	←
Emulation Specific Register						
ADCAnEMU	<ADCAn_base> + 388H	Yes	←	←	←	←

26. Key Return (KR)

26.1 Overview

The functional feature set of the KR between F1Kx and F1K/F1L/F1M/F1H is identical.

26.2 Register Base Address

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
<KR0_base>	FFF7 8000H	←	←	←	←

26.3 Clock Supply

Unit Name	Clock for the Unit	F1Kx	F1K	F1H	F1M	F1L
KR0	PCLK	CPUCLK_UL	CPUCLK4	←	←	CPUCLK2
	Register access	CPUCLK_UL	CPUCLK2, CPUCLK4	CPUCLK4	←	CPUCLK2

26.4 Interrupt Requests

Unit Interrupt Signal	F1Kx	F1K	F1H	F1M	F1L
KR0					
INTKRn	90	←	←	←	82

26.5 Reset Sources

Unit Name	F1Kx	F1K	F1H	F1M	F1L
KR0	All reset sources (ISORES)				

26.6 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1H	F1M	F1L
KRnKRM	<KRn_base>	Yes	←	←	←	←

27. Functional Safety

27.1 Overview

The implementation details of ECC and resulting interrupts/exceptions differs between device series and memory type.

27.2 Code Flash ECC

27.2.1 Interrupt Requests

Code Flash ECC Interrupt Requests (During CPU Fetching)

Unit Interrupt Signal	F1Kx	F1K	F1L	F1M	F1H
ECC 1-bit error interrupt	SYSERR, INTECCFLI0	INTECCSCFLI0	INTECCSDFLI0	INTECCSCFLI0	←
ECC 2-bit error interrupt	SYSERR	←	←	←	←

Code Flash ECC Interrupt Requests (During Read Access except CPU Fetching)

Unit Interrupt Signal	F1Kx	F1K	F1L	F1M	F1H
ECC 1-bit error interrupt	SYSERR, INTECCFLI0	INTECCSCFLI0	INTECCSDFLI0	INTECCSCFLI0	←
ECC 2-bit error interrupt	SYSERR, INTECCFLI0	SYSERR, INTECCSCFLI0	SYSERR -	← -	← -

27.2.2 Registers overview

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
CFAPCTL	FFC6 2000H	-	-	-	-	Yes	Yes
CFECCCTL_VCI	FFC6 2200H	Yes	Yes	Yes	-	Yes	Yes
CFERRINT_VCI	FFC6 2204H	Yes	Yes	Yes	-	Yes	Yes
CFSTCLR_VCI	FFC6 2208H	Yes	Yes	Yes	-	Yes	Yes
CFOVFSTR_VCI	FFC6 220CH	Yes	Yes	Yes	-	Yes	Yes
CF1STERSTR_VCI	FFC6 2210H	Yes	Yes	Yes	-	Yes	Yes
CF1STEADR0_VCI	FFC6 2250H	Yes	Yes	Yes	-	Yes	Yes
CFECCCTL_PE1	FFC6 2400H	Yes	Yes	Yes	-	Yes	Yes
CFECCCTL	FFC6 2000H	-	-	-	Yes	-	-
CFERRINT_PE1	FFC6 2404H	Yes	Yes	Yes	-	Yes	Yes
CFERRINT	FFC6 2030H	-	-	-	Yes	-	-
CFSTCLR_PE1	FFC6 2408H	Yes	Yes	Yes	-	Yes	Yes
CFOVFSTR_PE1	FFC6 240CH	Yes	Yes	Yes	-	Yes	Yes
CFOVFSTR	FFC6 2028H	-	-	-	Yes	-	-
CFOVFSTC	FFC6 202CH	-	-	-	Yes	-	-
CF1STERSTR_PE1	FFC6 2410H	Yes	Yes	Yes	-	Yes	Yes
CFFSTERSTR	FFC6 2004H	-	-	-	Yes	-	-
CF1STEADR0_PE1	FFC6 2450H	Yes	Yes	Yes	-	Yes	Yes
CFFSTEADR	FFC6 2034H	-	-	-	Yes	-	-
CFECCCTL_PE2	FFC6 2600H	Yes	-	-	-	-	Yes
CFERRINT_PE2	FFC6 2604H	Yes	-	-	-	-	Yes
CFSTCLR_PE2	FFC6 2608H	Yes	-	-	-	-	Yes
CFOVFSTR_PE2	FFC6 260CH	Yes	-	-	-	-	Yes

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
CF1STERSTR_PE2	FFC6 2610H	Yes	-	-	-	-	Yes
CF1STEADR0_PE2	FFC6 2650H	Yes	-	-	-	-	Yes
CFFSTSTC	FFC6 2024H	-	-	-	Yes	-	-
CFSTSTCTL_VCI	FFC6 2350H	Yes	Yes	Yes	-	Yes	Yes
CFSTSTCTL_PE1	FFC6 2550H	-	-	Yes	-	Yes	Yes
CFTSTCTL	FFC6 2054H	-	-	-	Yes	-	-
CFSTSTCTL_PE2	FFC6 2750H	-	-	-	-	-	Yes

27.3 Data Flash ECC

27.3.1 Interrupt Requests

Data Flash ECC Interrupt Requests (During read access)

Unit Interrupt Signal	F1Kx	F1K	F1H	F1M	F1L
ECC 1-bit error interrupt	INTECCEEP0	INTECCDEEP0	-	-	-
ECC 2-bit error interrupt	INTECCEEP0	INTECCDEEP0	←	←	←

27.3.2 Register Base Address

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
<DFECC_base>	FFC6 2A00H	←	←	←	FFC6 6000H

27.3.3 Registers overview

Name	Address	F1Kx	F1K	F1H	F1M	F1L
DFECCCTL	<DFECC_base> + 00H	Yes	Yes	Yes	Yes	Yes
DFERSTR	<DFECC_base> + 04H	Yes	Yes	Yes	Yes	Yes
DFERSTC	<DFECC_base> + 08H	Yes	Yes	Yes	Yes	Yes
DFOVFSTR	<DFECC_base> + 0CH	Yes	Yes	-	-	-
DFOVFSTC	<DFECC_base> + 10H	Yes	Yes	-	-	-
DFERRINT	<DFECC_base> + 14H	Yes	Yes	Yes	Yes	Yes
DFEADR	<DFECC_base> + 18H	Yes	Yes	-	-	-
DFTSTCTL	<DFECC_base> + 1CH	Yes	Yes	Yes	Yes	Yes

27.4 Local RAM ECC

On the F1Kx/F1K the retention RAM is a part of the local RAM (same as on the F1L). The ECC for the retention RAM is shared with the local RAM's. Therefore, the same register as the local RAM's are used in case of the retention RAM.

27.4.1 Interrupt Requests

Local RAM ECC Interrupt Requests (During CPU Fetching)

Unit Interrupt Signal	F1Kx	F1K	F1H	F1M	F1L
ECC 1-bit error interrupt	SYSERR, INTECCRAM	←	←	←	←
ECC 2-bit error interrupt	SYSERR, INTECCRAM	←	SYSERR	←	←

Local RAM ECC Interrupt Requests (During CPU access)

Unit Interrupt Signal	F1Kx	F1K	F1H	F1M	F1L
ECC 1-bit error interrupt	SYSERR, INTECCRAM	INTECCRAM	←	←	←
ECC 2-bit error interrupt	INTECCRAM, SYSERR	←	SYSERR	←	←

Local RAM ECC Interrupt Requests (During Read Access except CPU access)

Unit Interrupt Signal	F1Kx	F1K	F1H	F1M	F1L
ECC 1-bit error interrupt	INTECCRAM	←	←	←	←
ECC 2-bit error interrupt	INTECCRAM	←	SYSERR	←	←

27.4.2 Registers overview

Name	Address	F1KH	F1KM	F1K	F1H	F1M	F1L
LRTSTCTL_PE1	FFC6 5004H	Yes	Yes	Yes	Yes	Yes	-
LRTSTCTL	FFC6 30B4H	-	-	-	-	-	Yes
LRTDATBF0_PE1	FFC6 5008H	Yes	Yes	Yes	Yes	Yes	-
LRTDATBF0	FFC6 30B8H	-	-	-	-	-	Yes
LRTDATBF1_PE1	FFC6 500CH	-	-	-	Yes	Yes	-
LRECCCTL_PE1	FFC6 5400H	Yes	Yes	Yes	Yes	Yes	-
LRECCCTL	FFC6 3000H	-	-	-	-	-	Yes
LRERRINT_PE1	FFC6 5404H	Yes	Yes	Yes	Yes	Yes	-
LRERRINT	FFC6 30B0H	-	-	-	-	-	Yes
LRSTCLR_PE1	FFC6 5408H	Yes	Yes	Yes	Yes	Yes	-
LRSTCLR	FFC6 3024H	-	-	-	-	-	Yes
LROVFSTR_PE1	FFC6 540CH	Yes	Yes	Yes	-	-	-
LROVFSTR	FFC6 3028H	-	-	-	-	-	Yes
LROVFSTC	FFC6 302CH	-	-	-	-	-	Yes
LR1STERSTR_PE1	FFC6 5410H	Yes	Yes	Yes	Yes	Yes	-
LRFSTERSTR	FFC6 3004H	-	-	-	-	-	Yes
LR1STEADR0_PE1	FFC6 5450H	Yes	Yes	Yes	-	-	-
LRFSTEADR0	FFC6 3030H	-	-	-	-	-	Yes
LRTSTCTL_PE2	FFC6 5024H	Yes	-	-	Yes	-	-
LRTDATBF0_PE2	FFC6 5028H	Yes	-	-	Yes	-	-
LRTDATBF1_PE2	FFC6 502CH	-	-	-	Yes	-	-

Name	Address	F1KH	F1KM	F1K	F1H	F1M	F1L
LRECCCTL_PE2	FFC6 5600H	Yes	-	-	Yes	-	-
LRERRINT_PE2	FFC6 5604H	Yes	-	-	Yes	-	-
LRSTCLR_PE2	FFC6 5608H	Yes	-	-	Yes	-	-
LROVFSTR_PE2	FFC6 560CH	Yes	-	-	-	-	-
LR1STERSTR_PE2	FFC6 5610H	Yes	-	-	Yes	-	-
LR1STEADR0_PE2	FFC6 5650H	Yes	-	-	-	-	-

27.5 Global RAM

For F1M read ‘Global RAM’ as ‘Retention RAM’.

27.5.1 Interrupt Requests

Global RAM ECC Interrupt Requests (During CPU Fetching)

Unit Interrupt Signal	F1KH, F1KM-S4	F1K	F1H	F1M	F1L
ECC 1-bit error interrupt	SYSERR, INTECCRAM	-	SYSERR, INTECCRAM	SYSERR, INTECCRAM	-
ECC 2-bit error interrupt	SYSERR, INTECCRAM	-	SYSERR	SYSERR	-

Global RAM ECC Interrupt Requests (During CPU Access)

Unit Interrupt Signal	F1KH, F1KM-S4	F1K	F1H	F1M	F1L
ECC 1-bit error interrupt	SYSERR, INTECCRAM	-	INTECCRAM	←	-
ECC 2-bit error interrupt	SYSERR, INTECCRAM	-	SYSERR	←	-

Global RAM ECC Interrupt Requests (During Read Access except CPU Access)

Unit Interrupt Signal	F1KH, F1KM-S4	F1K	F1H	F1M	F1L
ECC 1-bit error interrupt	INTECCRAM	-	INTECCRAM	←	-
ECC 2-bit error interrupt	INTECCRAM	-	SYSERR	←	-

27.5.1 Register Base Address

Base Address Name	F1KH, F1KM-S4	F1K	F1H	F1M	F1L
<GRAMECC_base>	FFC6 4000H	-	FFC6 4000H	←	-

27.5.1 Registers overview

Name	Address	F1KH, F1KM-S4	F1K	F1L	F1M	F1H
GRECCCTL_GRAMC	<GRAMECC_base> + 000H	-	-	-	Yes	Yes
GRTSTCTL	<GRAMECC_base> + 004H	-	-	-	Yes	Yes
GRTDATBF0	<GRAMECC_base> + 008H	-	-	-	-	Yes
GRTDATBF1	<GRAMECC_base> + 00CH	-	-	-	-	Yes
GRTDATBF2	<GRAMECC_base> + 010H	-	-	-	Yes	Yes
GRTDATBF3	<GRAMECC_base> + 014H	-	-	-	Yes	Yes
GRDECINBF0	<GRAMECC_base> + 018H	-	-	-	Yes	Yes
GRDECINBF1	<GRAMECC_base> + 01CH	-	-	-	Yes	Yes
GRECCCTL_VCI	<GRAMECC_base> + 200H	-	-	-	Yes	Yes
GRERRINT_VCI	<GRAMECC_base> + 204H	-	-	-	Yes	Yes

Name	Address	F1KH, F1KM-S4	F1K	F1L	F1M	F1H
GRSTCLR_VCI	<GRAMECC_base> + 208H	-	-	-	Yes	Yes
GROVFSTR_VCI	<GRAMECC_base> + 20CH	-	-	-	Yes	Yes
GR1STERSTR_VCI	<GRAMECC_base> + 210H	-	-	-	Yes	Yes
GR1STEADR0_VCI	<GRAMECC_base> + 250H	-	-	-	Yes	Yes
GR1STEADR1_VCI	<GRAMECC_base> + 254H	-	-	-	Yes	Yes
GRECCCTL_PE1	<GRAMECC_base> + 400H	-	-	-	Yes	Yes
GRERRINT_PE1	<GRAMECC_base> + 404H	-	-	-	Yes	Yes
GRSTCLR_PE1	<GRAMECC_base> + 408H	-	-	-	Yes	Yes
GROVFSTR_PE1	<GRAMECC_base> + 40CH	-	-	-	Yes	Yes
GR1STERSTR_PE1	<GRAMECC_base> + 410H	-	-	-	Yes	Yes
GR1STEADR0_PE1	<GRAMECC_base> + 450H	-	-	-	Yes	Yes
GR1STEADR1_PE1	<GRAMECC_base> + 454H	-	-	-	Yes	Yes
GRECCCTL_PE2	<GRAMECC_base> + 600H	-	-	-	-	Yes
GRERRINT_PE2	<GRAMECC_base> + 604H	-	-	-	-	Yes
GRSTCLR_PE2	<GRAMECC_base> + 608H	-	-	-	-	Yes
GROVFSTR_PE2	<GRAMECC_base> + 60CH	-	-	-	-	Yes
GR1STERSTR_PE2	<GRAMECC_base> + 610H	-	-	-	-	Yes
GR1STEADR0_PE2	<GRAMECC_base> + 650H	-	-	-	-	Yes
GR1STEADR1_PE2	<GRAMECC_base> + 654H	-	-	-	-	Yes
GRECCCTL_BKA	<GRAMECC_base> + 000H	Yes	-	-	-	-
GRERRINT_BKA	<GRAMECC_base> + 004H	Yes	-	-	-	-
GRSTCLR_BKA	<GRAMECC_base> + 010H	Yes	-	-	-	-
GROVFSTR_BKA	<GRAMECC_base> + 014H	Yes	-	-	-	-
GR1STERSTR_BKA	<GRAMECC_base> + 018H	Yes	-	-	-	-
GR1STEADR_BKA	<GRAMECC_base> + 01CH	Yes	-	-	-	-
GRTSTCTL_BKA	<GRAMECC_base> + 020H	Yes	-	-	-	-
GRDECINBF1_BKA	<GRAMECC_base> + 024H	Yes	-	-	-	-
GRECCCTL_BKB	<GRAMECC_base> + 200H	Yes	-	-	-	-
GRERRINT_BKB	<GRAMECC_base> + 204H	Yes	-	-	-	-
GRSTCLR_BKB	<GRAMECC_base> + 210H	Yes	-	-	-	-
GROVFSTR_BKB	<GRAMECC_base> + 214H	Yes	-	-	-	-
GR1STERSTR_BKB	<GRAMECC_base> + 218H	Yes	-	-	-	-
GR1STEADR_BKB	<GRAMECC_base> + 21CH	Yes	-	-	-	-
GRTSTCTL_BKB	<GRAMECC_base> + 220H	Yes	-	-	-	-
GRDECINBF1_BKB	<GRAMECC_base> + 224H	Yes	-	-	-	-

27.6 Instruction Cache ECC

The F1Kx/F1K does not have an instruction cache. Therefore no registers for this functionality are available on F1Kx/F1K.

27.7 CSIHn RAM ECC

27.7.1 Interrupt Requests

Unit Interrupt Signal	F1Kx	F1K	F1H	F1M	F1L
ECC 1-bit error interrupt	INTECCCSIHn	INTECCDCSIHn	-	-	-
ECC 2-bit error interrupt	INTECCCSIHn	INTECCDCSIHn	←	←	←

27.7.2 Register Base Address

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
<ECCCSIHn_base>	FFC7 0100H + n x100H	←	FFC7 00n0H	←	←

27.7.3 Registers overview

Name	Address	F1Kx	F1K	F1L	F1M	F1H
ECCCSIHnCTL	<ECCCSIHn_base> + 00H	Yes	←	←	←	←
ECCCSIHnTMC	<ECCCSIHn_base> + 04H	Yes	←	←	←	←
ECCCSIHnTED	<ECCCSIHn_base> + 0CH	Yes	←	←	←	←
ECCCSIHnTRC	<ECCCSIHn_base> + 08H	Yes	←	←	←	←
ECCCSIHnAD0	<ECCCSIHn_base> + 10H	Yes	←	-	-	-
ECCCSIHnSYND	<ECCCSIHn_base> + 0BH	Yes	←	←	←	←
ECCCSIHnHORD	<ECCCSIHn_base> + 0AH	Yes	←	←	←	←
ECCCSIHnECRD	<ECCCSIHn_base> + 09H	Yes	←	←	←	←
ECCCSIHnERDB	<ECCCSIHn_base> + 08H	Yes	←	←	←	←
SELB_READTEST	FFC7 8000H FFBC 0600H	Yes -	← -	- ←	← -	← -

27.8 RS-CAN / RS-CANFD RAM ECC

27.8.1 Interrupt Requests

RS-CAN / RS-CANFD ECC Interrupt Requests

<INT> = INTECCDCN for F1L, F1M, F1H, F1K
<INT> = INTECCCNFD for F1KH, F1KM

Unit Interrupt Signal	F1KH	F1KM	F1K	F1L	F1M	F1H
ECC 1-bit error interrupt	<INT>RAM0 <INT>RAM1	<INT>RAM	<INT>RAM0 <INT>RAM1[1]	-	-	-
ECC 2-bit error interrupt	<INT>RAM0 <INT>RAM1	<INT>RAM	<INT>RAM0 <INT>RAM1[1]	<INT>RAM	<INT>RAM0	<INT>RAM0 <INT>RAM1[1]

[1] RS-CAN only

27.8.2 Register Base Address

Base Address Name	F1KH	F1KM	F1K	F1L	F1M	F1H
<ECCCAN0_base>	-	-	FFC7 1300H	FFC7 1000H	FFC7 1000H	FFC7 1000H
<ECCCAN1_base>	-	-	FFC7 1020H	-	-	FFC7 1020H
<ECCCANFD0_base>	-	-	FFC7 1400H	-	-	-
ECCCFD0MB_base	FFC7 1300H	←	-	-	-	-
ECCCFD0AFL0_base	FFC7 1400H	←	-	-	-	-
ECCCFD0AFL1_base	FFC7 1500H	←	-	-	-	-
ECCCFD1MB_base	FFC7 1A00H	-	-	-	-	-
ECCCFD1AFL0_base	FFC7 1B00H	-	-	-	-	-
ECCCFD1AFL1_base	FFC7 1C00H	-	-	-	-	-

27.8.3 Registers overview

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
ECCRCAN0CTL	<ECCCAN0_base> + 00H	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0CTL	<ECCCANFD0_base> + 00H	-	-	Yes	-	-	-
ECCRCAN1CTL	<ECCCAN1_base> + 00H	-	-	Yes	-	-	Yes
ECCRCAN0TMC	<ECCCAN0_base> + 04H	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0TMC	<ECCCANFD0_base> + 04H	-	-	Yes	-	-	-
ECCRCAN1TMC	<ECCCAN1_base> + 04H	-	-	Yes	-	-	Yes
ECCRCAN0TED	<ECCCAN0_base> + 0CH	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0TED	<ECCCANFD0_base> + 0CH	-	-	Yes	-	-	-
ECCRCAN1TED	<ECCCAN1_base> + 0CH	-	-	Yes	-	-	Yes
ECCRCAN0TRC	<ECCCAN0_base> + 08H	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0TRC	<ECCCANFD0_base> + 08H	-	-	Yes	-	-	-
ECCRCAN1TRC	<ECCCAN1_base> + 08H	-	-	Yes	-	-	Yes
ECCRCAN0SYND	<ECCCAN0_base> + 0BH	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0SYND	<ECCCANFD0_base> + 0BH	-	-	Yes	-	-	-
ECCRCAN1SYND	<ECCCAN1_base> + 0BH	-	-	Yes	-	-	Yes
ECCRCAN0HORD	<ECCCAN0_base> + 0AH	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0HORD	<ECCCANFD0_base> + 0AH	-	-	Yes	-	-	-
ECCRCAN1HORD	<ECCCAN1_base> + 0AH	-	-	Yes	-	-	Yes
ECCRCAN0ECRD	<ECCCAN0_base> + 09H	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0ECRD	<ECCCANFD0_base> + 09H	-	-	Yes	-	-	-
ECCRCAN1ECRD	<ECCCAN1_base> + 09H	-	-	Yes	-	-	Yes

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
ECCRCAN0ERDB	<ECCCAN0_base> + 08H	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0ERDB	<ECCCANFD0_base> + 08H	-	-	Yes	-	-	-
ECCRCAN1ERDB	<ECCCAN1_base> + 08H	-	-	Yes	-	-	Yes
ECCRCAN0AD0ECC	<ECCCAN0_base> + 10H	-	-	Yes	Yes	Yes	Yes
ECCRCANFD0AD0	<ECCCANFD0_base> + 10H	-	-	Yes	-	-	-
RCAN1AD0	<ECCCAN1_base> + 10H	-	-	Yes	-	-	Yes
ECCRCAN00CTL	<ECCCAN0_base> + 40H	-	-	-	-	Yes	Yes
ECCRCAN00TMC	<ECCCAN0_base> + 44H	-	-	-	-	Yes	Yes
ECCRCAN00TED	<ECCCAN0_base> + 4CH	-	-	-	-	Yes	Yes
ECCRCAN00TRC	<ECCCAN0_base> + 48H	-	-	-	-	Yes	Yes
ECCRCAN00ERDB	<ECCCAN0_base> + 48H	-	-	-	-	Yes	Yes
ECCRCAN00ECRD	<ECCCAN0_base> + 49H	-	-	-	-	Yes	Yes
ECCRCAN00HORD	<ECCCAN0_base> + 4AH	-	-	-	-	Yes	Yes
ECCRCAN00SYND	<ECCCAN0_base> + 4BH	-	-	-	-	Yes	Yes
ECCRCAN01CTL	<ECCCAN0_base> + 50H	-	-	-	-	Yes	Yes
ECCRCAN01TMC	<ECCCAN0_base> + 54H	-	-	-	-	Yes	Yes
ECCRCAN01TED	<ECCCAN0_base> + 5CH	-	-	-	-	Yes	Yes
ECCRCAN01TRC	<ECCCAN0_base> + 58H	-	-	-	-	Yes	Yes
ECCRCAN01ERDB	<ECCCAN0_base> + 58H	-	-	-	-	Yes	Yes
ECCRCAN01ECRD	<ECCCAN0_base> + 59H	-	-	-	-	Yes	Yes
ECCRCAN01HORD	<ECCCAN0_base> + 5AH	-	-	-	-	Yes	Yes
ECCRCAN01SYND	<ECCCAN0_base> + 5BH	-	-	-	-	Yes	Yes
RCFDC0 ECC Register (for MB RAM)							
ECCCFD0MBCTL	<ECCCFD0MB_base> + 00H	Yes	Yes	-	-	-	-
ECCCFD0MBTMC	<ECCCFD0MB_base> + 04H	Yes	Yes	-	-	-	-
ECCCFD0MBTED	<ECCCFD0MB_base> + 0CH	Yes	Yes	-	-	-	-
ECCCFD0MBTRC	<ECCCFD0MB_base> + 08H	Yes	Yes	-	-	-	-
ECCCFD0MBSYND	<ECCCFD0MB_base> + 0BH	Yes	Yes	-	-	-	-
ECCCFD0MBHORD	<ECCCFD0MB_base> + 0AH	Yes	Yes	-	-	-	-
ECCCFD0MBECRD	<ECCCFD0MB_base> + 09H	Yes	Yes	-	-	-	-
ECCCFD0MBERDB	<ECCCFD0MB_base> + 08H	Yes	Yes	-	-	-	-
ECCCFD0MBAD0	<ECCCFD0MB_base> + 10H	Yes	Yes	-	-	-	-
RCFDC0 ECC Register (for AFL0 RAM)							
ECCCFD0AFL0CTL	<ECCCFD0AFL0_base> + 00H	Yes	Yes	-	-	-	-
ECCCFD0AFL0TMC	<ECCCFD0AFL0_base> + 04H	Yes	Yes	-	-	-	-
ECCCFD0AFL0TED	<ECCCFD0AFL0_base> + 0CH	Yes	Yes	-	-	-	-
ECCCFD0AFL0TRC	<ECCCFD0AFL0_base> + 08H	Yes	Yes	-	-	-	-
ECCCFD0AFL0SYND	<ECCCFD0AFL0_base> + 0BH	Yes	Yes	-	-	-	-
ECCCFD0AFL0HORD	<ECCCFD0AFL0_base> + 0AH	Yes	Yes	-	-	-	-
ECCCFD0AFL0ECRD	<ECCCFD0AFL0_base> + 09H	Yes	Yes	-	-	-	-
ECCCFD0AFL0ERDB	<ECCCFD0AFL0_base> + 08H	Yes	Yes	-	-	-	-
ECCCFD0AFL0AD0	<ECCCFD0AFL0_base> + 10H	Yes	Yes	-	-	-	-
RCFDC0 ECC Register (for AFL1 RAM)							
ECCCFD0AFL1CTL	<ECCCFD0AFL1_base> + 00H	Yes	Yes	-	-	-	-
ECCCFD0AFL1TMC	<ECCCFD0AFL1_base> + 04H	Yes	Yes	-	-	-	-
ECCCFD0AFL1TED	<ECCCFD0AFL1_base> + 0CH	Yes	Yes	-	-	-	-
ECCCFD0AFL1TRC	<ECCCFD0AFL1_base> + 08H	Yes	Yes	-	-	-	-
ECCCFD0AFL1SYND	<ECCCFD0AFL1_base> + 0BH	Yes	Yes	-	-	-	-

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
ECCCFD0AFL1HORD	<ECCCFD0AFL1_base> + 0AH	Yes	Yes	-	-	-	-
ECCCFD0AFL1ECRD	<ECCCFD0AFL1_base> + 09H	Yes	Yes	-	-	-	-
ECCCFD0AFL1ERDB	<ECCCFD0AFL1_base> + 08H	Yes	Yes	-	-	-	-
ECCCFD0AFL1AD0	<ECCCFD0AFL1_base> + 10H	Yes	Yes	-	-	-	-
RCFDC1 ECC Register (for MB RAM)							
ECCCFD1MBCTL	<ECCCFD1MB_base> + 00H	Yes	-	-	-	-	-
ECCCFD1MBTMC	<ECCCFD1MB_base> + 04H	Yes	-	-	-	-	-
ECCCFD1MBTED	<ECCCFD1MB_base> + 0CH	Yes	-	-	-	-	-
ECCCFD1MBTRC	<ECCCFD1MB_base> + 08H	Yes	-	-	-	-	-
ECCCFD1MBSYND	<ECCCFD1MB_base> + 0BH	Yes	-	-	-	-	-
ECCCFD1MBHORD	<ECCCFD1MB_base> + 0AH	Yes	-	-	-	-	-
ECCCFD1MBECRD	<ECCCFD1MB_base> + 09H	Yes	-	-	-	-	-
ECCCFD1MBERDB	<ECCCFD1MB_base> + 08H	Yes	-	-	-	-	-
ECCCFD1MBAD0	<ECCCFD1MB_base> + 10H	Yes	-	-	-	-	-
RCFDC1 ECC Register (for AFL0 RAM)							
ECCCFD1AFL0CTL	<ECCCFD1AFL0_base> + 00H	Yes	-	-	-	-	-
ECCCFD1AFL0TMC	<ECCCFD1AFL0_base> + 04H	Yes	-	-	-	-	-
ECCCFD1AFL0TED	<ECCCFD1AFL0_base> + 0CH	Yes	-	-	-	-	-
ECCCFD1AFL0TRC	<ECCCFD1AFL0_base> + 08H	Yes	-	-	-	-	-
ECCCFD1AFL0SYND	<ECCCFD1AFL0_base> + 0BH	Yes	-	-	-	-	-
ECCCFD1AFL0HORD	<ECCCFD1AFL0_base> + 0AH	Yes	-	-	-	-	-
ECCCFD1AFL0ECRD	<ECCCFD1AFL0_base> + 09H	Yes	-	-	-	-	-
ECCCFD1AFL0ERDB	<ECCCFD1AFL0_base> + 08H	Yes	-	-	-	-	-
ECCCFD1AFL0AD0	<ECCCFD1AFL0_base> + 10H	Yes	-	-	-	-	-
RCFDC1 ECC Register (for AFL1 RAM)							
ECCCFD1AFL1CTL	<ECCCFD1AFL1_base> + 00H	Yes	-	-	-	-	-
ECCCFD1AFL1TMC	<ECCCFD1AFL1_base> + 04H	Yes	-	-	-	-	-
ECCCFD1AFL1TED	<ECCCFD1AFL1_base> + 0CH	Yes	-	-	-	-	-
ECCCFD1AFL1TRC	<ECCCFD1AFL1_base> + 08H	Yes	-	-	-	-	-
ECCCFD1AFL1SYND	<ECCCFD1AFL1_base> + 0BH	Yes	-	-	-	-	-
ECCCFD1AFL1HORD	<ECCCFD1AFL1_base> + 0AH	Yes	-	-	-	-	-
ECCCFD1AFL1ECRD	<ECCCFD1AFL1_base> + 09H	Yes	-	-	-	-	-
ECCCFD1AFL1ERDB	<ECCCFD1AFL1_base> + 08H	Yes	-	-	-	-	-
ECCCFD1AFL1AD0	<ECCCFD1AFL1_base> + 10H	Yes	-	-	-	-	-

27.9 FlexRay RAM ECC

27.9.1 Interrupt Requests

Unit Interrupt Signal	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
ECC 1-bit error interrupt	INTECCFLRAM	-	-	-	-	-
ECC 2-bit error interrupt	INTECCFLRAM	-	-	-	INTECCDFLRAM	←

27.9.2 Register Base Address

Base Address Name <modulename_base>	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
<ECCFLXA0_base>	FFC7 3100H	-	-	-	FFC7 2000H	FFC7 2000H
<ECCFLXA0T0_base>	FFC7 3200H	-	-	-	FFC7 3000H	FFC7 3000H
<ECCFLXA0T1_base>	FFC7 3300H	-	-	-	FFC7 3010H	FFC7 3010H

27.9.3 Registers overview

Name	Address	F1KH, F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
<modulename>CTL	<module_base> + 00H	Yes	-	-	-	Yes	Yes
<modulename>TMC	<module_base> + 04H	Yes	-	-	-	Yes	Yes
<modulename>TRC	<module_base> + 08H	Yes	-	-	-	Yes	Yes
<modulename>ERDB	<module_base> + 08H	Yes	-	-	-	Yes	Yes
<modulename>ECRD	<module_base> + 09H	Yes	-	-	-	Yes	Yes
<modulename>HORD	<module_base> + 0AH	Yes	-	-	-	Yes	Yes
<modulename>ASYND	<module_base> + 0BH	Yes	-	-	-	Yes	Yes
<modulename>TED	<module_base> + 0CH	Yes	-	-	-	Yes	Yes

27.10 MMCA RAM ECC

27.10.1 Interrupt Requests

Unit Interrupt Signal	F1KH	F1KM	F1K	F1L	F1M	F1H
ECC 1-bit error interrupt	INTECCMMCA0RAM	-	-	-	-	-
ECC 2-bit error interrupt	INTECCMMCA0RAM	-	-	-	-	-

27.10.2 Register Base Address

Base Address Name <modulename_base>	F1KH	F1KM	F1K	F1L	F1M	F1H
<ECCMMCA0A_base>	FFED A000H	-	-	-	-	-
<ECCMMCA0B_base>	FFED A100H	-	-	-	-	-

27.10.3 Registers overview

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
<modulename>CTL	<module_base> + 00H	Yes	-	-	-	-	-
<modulename>TMC	<module_base> + 04H	Yes	-	-	-	-	-
<modulename>TRC	<module_base> + 08H	Yes	-	-	-	-	-
<modulename>ERDB	<module_base> + 08H	Yes	-	-	-	-	-
<modulename>ECRD	<module_base> + 09H	Yes	-	-	-	-	-
<modulename>HORD	<module_base> + 0AH	Yes	-	-	-	-	-
<modulename>ASYND	<module_base> + 0BH	Yes	-	-	-	-	-
<modulename>TED	<module_base> + 0CH	Yes	-	-	-	-	-
<modulename>AD0	<module_base> + 10H	Yes	-	-	-	-	-

27.11 EthernetAVB ECC RAM

27.11.1 Interrupt Requests

Unit Interrupt Signal	F1KH	F1KM-S4	F1KM-S1	F1K	F1L	F1M	F1H
ECC 1-bit error interrupt	INTECCETH0 INTECCETH1	INTECCETH	-	-	-	-	-
ECC 2-bit error interrupt	INTECCETH0 INTECCETH1	INTECCETH	-	-	-	-	INTECCDETH

27.11.2 Register Base Address

Base Address Name <modulename_base>	F1KH	F1M-S4	F1KM-S1	F1K	F1L	F1M	F1H
<ECCETNB0TX_base>	FFC7 4100H	FFC7 4100H	-	-	-	-	FFC7 3040H
<ECCETNB0RX_base>	FFC7 4200H	FFC7 4200H	-	-	-	-	FFC7 3050H
<ECCETNB1TX_base>	FFC7 4300H	-	-	-	-	-	-
<ECCETNB1TX_base>	FFC7 4400H	-	-	-	-	-	-

27.11.3 Registers overview

Name	Address	F1KH	F1KM	F1K	F1L	F1M	F1H
<modulename>CTL	<module_base> + 00H	Yes	-	-	-	-	Yes
<modulename>TMC	<module_base> + 04H	Yes	-	-	-	-	Yes
<modulename>ERDB	<module_base> + 08H	Yes	-	-	-	-	Yes
<modulename>TRC	<module_base> + 08H	Yes	-	-	-	-	Yes
<modulename>ECRD	<module_base> + 09H	Yes	-	-	-	-	Yes
<modulename>HORD	<module_base> + 0AH	Yes	-	-	-	-	Yes
<modulename>ASYND	<module_base> + 0BH	Yes	-	-	-	-	Yes
<modulename>TED	<module_base> + 0CH	Yes	-	-	-	-	Yes
<modulename>AD0	<module_base> + 10H	Yes	-	-	-	-	-

28. Data CRC (DCRA)

28.1 Overview

The functional feature set of the DCRA between F1Kx/F1K and F1L/F1M/F1H is identical.

28.2 Register Base Address

Base Address Name	F1Kx	F1K	F1H	F1M	F1L
<DCRA0_base>	FFF7 0000H	←	←	←	←
<DCRA1_base>	FFF7 1000H	←	←	←	←
<DCRA2_base>	FFF7 2000H	←	←	←	←
<DCRA3_base>	FFF7 3000H	←	←	←	←

28.3 Clock Supply

Unit Name	Clock for the Unit	F1Kx	F1K	F1H	F1M	F1L
DCRAn	PCLK	CPUCLK_UL	CPUCLK4	←	←	CPUCLK2
	Register access	CPUCLK_UL	CPUCLK2, CPUCLK4	CPUCLK4	←	CPUCLK2

28.4 Reset Sources

Unit Name	F1Kx	F1K	F1H	F1M	F1L
DCRAn	All reset sources (ISORES)				

28.5 Registers overview

Registers are identical between F1Kx, F1K, F1L, F1M and F1H.

Name	Address	F1Kx	F1K	F1H	F1M	F1L
DCRAnCIN	<DCRAn_base> + 00H	Same	←	←	←	←
DCRAnCOUT	<DCRAn_base> + 04H	Same	←	←	←	←
DCRAnCTL	<DCRAn_base> + 20H	Same	←	←	←	←

29. Memory Protection

The basic functionality and operation of the memory protection functions is very similar between the F1Kx series and the F1K/F1H/F1M devices. Still, the in-detail assignment may be different.

29.1 Register Base Address

Base Address Name	F1KH	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
<MGDGR_base>	FFC4 9000H	←	←	-	-	FFC4 9000H	←	-
<PBG1x_base>	FFC4 0000H	←	←	←	←	←	-	-
<PBG2x_base>	FFDD D000H	←	←	←	←	←	-	-
<PBG3x_base>	FFF9 4000H	←	←	←	←	←	-	-
<PBG4x_base>	FFC5 9C00H	←	←	-	-	-	-	-
<PBG5x_base>	FFF9 0000H	←	←	←	←	←	-	-
<PBG6x_base>	FFC7 1800H	←	←	-	-	-	-	-
<HBG0x_base>	FFF9 C000H	←	←	-	-	FFF9 C000H	-	-
<PBGCx_base>	FFC4 C000H	←	←	←	←	-	-	-

29.2 Registers overview

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
Global RAM Guard								
MGDGRPROT0(_BKA)	<MGDGR_base> + 000H	Yes	←	-	-	Yes	Yes	-
MGDGRBAD0(_BKA)	<MGDGR_base> + 004H	Yes	←	-	-	Yes	Yes	-
MGDGRADV0(_BKA)	<MGDGR_base> + 008H	Yes	←	-	-	Yes	Yes	-
MGDGRPROT1(_BKA)	<MGDGR_base> + 010H	Yes	←	-	-	Yes	Yes	-
MGDGRBAD1(_BKA)	<MGDGR_base> + 014H	Yes	←	-	-	Yes	Yes	-
MGDGRADV1(_BKA)	<MGDGR_base> + 018H	Yes	←	-	-	Yes	Yes	-
MGDGRPROT2(_BKA)	<MGDGR_base> + 020H	Yes	←	-	-	Yes	Yes	-
MGDGRBAD2(_BKA)	<MGDGR_base> + 024H	Yes	←	-	-	Yes	Yes	-
MGDGRADV2(_BKA)	<MGDGR_base> + 028H	Yes	←	-	-	Yes	Yes	-
MGDGRPROT3(_BKA)	<MGDGR_base> + 030H	Yes	←	-	-	Yes	Yes	-
MGDGRBAD3(_BKA)	<MGDGR_base> + 034H	Yes	←	-	-	Yes	Yes	-
MGDGRADV3(_BKA)	<MGDGR_base> + 038H	Yes	←	-	-	Yes	Yes	-
MGDGRSCTL_BKA	<MGDGR_base> + 040H	Yes	←	-	-	-	-	-
MGDGRSSTAT_BKA	<MGDGR_base> + 044H	Yes	←	-	-	-	-	-
MGDGRSTYPE_BKA	<MGDGR_base> + 048H	Yes	←	-	-	-	-	-
MGDGRSAD_BKA	<MGDGR_base> + 04CH	Yes	←	-	-	-	-	-
MGDGRSCTL_VCI	<MGDGR_base> + 100H	-	-	-	-	Yes	Yes	-
MGDGRSSTAT_VCI	<MGDGR_base> + 104H	-	-	-	-	Yes	Yes	-
MGDGRSTYPE_VCI	<MGDGR_base> + 10CH	-	-	-	-	Yes	Yes	-
MGDGRPROT0_BKB MGDGRSCTL_PE1	<MGDGR_base> + 200H	Yes -	← -	- -	- -	- Yes	- Yes	- -
MGDGRBAD0_BKB MGDGRSSTAT_PE1	<MGDGR_base> + 204H	Yes -	← -	- -	- -	- Yes	- Yes	- -
MGDGRADV0_BKB	<MGDGR_base> + 208H	Yes	←	-	-	-	-	-
MGDGRSTYPE_PE1	<MGDGR_base> + 20CH	-	-	-	-	Yes	Yes	-
MGDGRPROT1_BKB	<MGDGR_base> + 210H	Yes	←	-	-	-	-	-
MGDGRBAD1_BKB	<MGDGR_base> + 214H	Yes	←	-	-	-	-	-
MGDGRADV1_BKB	<MGDGR_base> + 218H	Yes	←	-	-	-	-	-
MGDGRPROT2_BKB	<MGDGR_base> + 220H	Yes	←	-	-	-	-	-
MGDGRBAD2_BKB	<MGDGR_base> + 224H	Yes	←	-	-	-	-	-

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
MGDGRADV2_BKB	<MGDGR_base> + 228H	Yes	←	-	-	-	-	-
MGDGRPROT3_BKB	<MGDGR_base> + 230H	Yes	←	-	-	-	-	-
MGDGRBAD3_BKB	<MGDGR_base> + 234H	Yes	←	-	-	-	-	-
MGDGRADV3_BKB	<MGDGR_base> + 238H	Yes	←	-	-	-	-	-
MGDGRSCTL_BKB	<MGDGR_base> + 240H	Yes	←	-	-	-	-	-
MGDGRSSTAT_BKB	<MGDGR_base> + 244H	Yes	←	-	-	-	-	-
MGDGRSTYPE_BKB	<MGDGR_base> + 248H	Yes	←	-	-	-	-	-
MGDGRSAD_BKB	<MGDGR_base> + 24CH	Yes	←	-	-	-	-	-
MGDGRSCTL_PE2	<MGDGR_base> + 300H	-	-	-	-	Yes	-	-
MGDGRSSTAT_PE2	<MGDGR_base> + 304H	-	-	-	-	Yes	-	-
MGDGRSTYPE_PE2	<MGDGR_base> + 30CH	-	-	-	-	Yes	-	-
Periphereal Bus Guard (PBG) / HBus Guard (HBG)								
FSGD00PROT0	<PBG1x_base> + 000H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT1	<PBG1x_base> + 004H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT2	<PBG1x_base> + 008H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT3	<PBG1x_base> + 00CH	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT4	<PBG1x_base> + 010H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT5	<PBG1x_base> + 014H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT6	<PBG1x_base> + 018H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT7	<PBG1x_base> + 01CH	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT8	<PBG1x_base> + 020H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT9	<PBG1x_base> + 024H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT10	<PBG1x_base> + 028H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT11	<PBG1x_base> + 02CH	Yes	Yes	Yes	Yes	Yes	-	-
FSGD00PROT12	<PBG1x_base> + 030H	Yes	Yes	-	Yes	Yes	-	-
FSGD00PROT13	<PBG1x_base> + 034H	Yes	Yes	-	Yes	Yes	-	-
FSGD00PROT14	<PBG1x_base> + 038H	Yes	Yes	-	-	-	-	-
FSGD00PROT15	<PBG1x_base> + 03CH	Yes	Yes	-	-	-	-	-
FSGD01PROT0	<PBG1x_base> + 100H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD01PROT1	<PBG1x_base> + 104H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD01PROT2	<PBG1x_base> + 108H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD01PROT3	<PBG1x_base> + 10CH	Yes	Yes	Yes	Yes	Yes	-	-
FSGD01PROT4	<PBG1x_base> + 110H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD01PROT5	<PBG1x_base> + 114H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD01PROT6	<PBG1x_base> + 118H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD01PROT7	<PBG1x_base> + 11CH	Yes	Yes	-	Yes	Yes	-	-
FSGD01PROT8	<PBG1x_base> + 120H	Yes	Yes	-	Yes	Yes	-	-
FSGD01PROT9	<PBG1x_base> + 124H	Yes	Yes	Yes	Yes	-	-	-
FSGD01PROT10	<PBG1x_base> + 128H	Yes	Yes	-	Yes	-	-	-
—	—							
FSGD01PROT12	<PBG1x_base> + 130H	Yes	Yes	Yes	Yes	-	-	-
FSGD01PROT13	<PBG1x_base> + 134H	Yes	Yes	Yes	Yes	-	-	-
FSGD01PROT14	<PBG1x_base> + 138H	Yes	Yes	Yes	Yes	-	-	-
FSGD01PROT15	<PBG1x_base> + 13CH	Yes	Yes	-	-	-	-	-
FSGD07PROT0	<PBG1x_base> + 400H	Yes	Yes	Yes	Yes	-	-	-
FSGD07PROT1	<PBG1x_base> + 404H	Yes	Yes	Yes	Yes	-	-	-
FSGD07PROT2	<PBG1x_base> + 408H	Yes	Yes	Yes	Yes	-	-	-
FSGD07PROT3	<PBG1x_base> + 40CH	Yes	Yes	Yes	Yes	-	-	-
FSGD07PROT4	<PBG1x_base> + 410H	Yes	Yes	-	Yes	-	-	-
FSGD07PROT5	<PBG1x_base> + 414H	Yes	Yes	-	Yes	-	-	-
FSGD07PROT6	<PBG1x_base> + 418H	Yes	Yes	-	Yes	-	-	-
FSGD07PROT7	<PBG1x_base> + 41CH	Yes	Yes	-	Yes	-	-	-
FSGD07PROT8	<PBG1x_base> + 420H	Yes	Yes	-	Yes	-	-	-
FSGD07PROT9	<PBG1x_base> + 424H	Yes	Yes	-	Yes	-	-	-

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
FSGD07PROT10	<PBG1x_base> + 428H	Yes	Yes	-	Yes	-	-	-
FSGD07PROT11	<PBG1x_base> + 42CH	Yes	Yes	-	Yes	-	-	-
FSGD07PROT12	<PBG1x_base> + 430H	Yes	Yes	-	Yes	-	-	-
FSGD07PROT13	<PBG1x_base> + 434H	Yes	Yes	-	-	-	-	-
FSGD07PROT14	<PBG1x_base> + 438H	Yes	Yes	-	-	-	-	-
FSGD07PROT15	<PBG1x_base> + 43CH	Yes	Yes	Yes	-	-	-	-
FSGD08PROT0	<PBG1x_base> + 500H	Yes	Yes	Yes	Yes	-	-	-
FSGD08PROT1	<PBG1x_base> + 504H	Yes	Yes	Yes	Yes	-	-	-
FSGD08PROT2	<PBG1x_base> + 508H	Yes	Yes	Yes	Yes	-	-	-
FSGD08PROT3	<PBG1x_base> + 50CH	Yes	Yes	Yes	Yes	-	-	-
FSGD08PROT4	<PBG1x_base> + 510H	Yes	Yes	Yes	Yes	-	-	-
FSGD08PROT5	<PBG1x_base> + 514H	Yes	Yes	Yes	Yes	-	-	-
FSGD08PROT6	<PBG1x_base> + 518H	Yes	Yes	Yes	-	-	-	-
FSGD08PROT7	<PBG1x_base> + 51CH	Yes	Yes	-	-	-	-	-
FSGD08PROT8	<PBG1x_base> + 520H	Yes	Yes	Yes	-	-	-	-
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FSGD08PROT13	<PBG1x_base> + 534H	Yes	Yes	Yes	-	-	-	-
FSGD08PROT14	<PBG1x_base> + 538H	Yes	Yes	Yes	-	-	-	-
FSGD12PROT0	<PBG1x_base> + 600H	Yes	-	-	-	-	-	-
FSGD12PROT1	<PBG1x_base> + 604H	Yes	-	-	-	-	-	-
FSGD12PROT2	<PBG1x_base> + 608H	Yes	-	-	-	-	-	-
FSGD12PROT3	<PBG1x_base> + 60CH	Yes	-	-	-	-	-	-
FSGD12PROT4	<PBG1x_base> + 610H	Yes	-	-	-	-	-	-
FSGD02PROT0	<PBG2x_base> + 000H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT1	<PBG2x_base> + 004H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT2	<PBG2x_base> + 008H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT3	<PBG2x_base> + 00CH	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT4	<PBG2x_base> + 010H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT5	<PBG2x_base> + 014H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT6	<PBG2x_base> + 018H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT7	<PBG2x_base> + 01CH	Yes	-	-	-	Yes	-	-
FSGD02PROT8	<PBG2x_base> + 020H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT9	<PBG2x_base> + 024H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT10	<PBG2x_base> + 028H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD02PROT11	<PBG2x_base> + 02CH	Yes	Yes	Yes	Yes	-	-	-
FSGD02PROT12	<PBG2x_base> + 030H	Yes	Yes	Yes	Yes	-	-	-
FSGD02PROT13	<PBG2x_base> + 034H	Yes	Yes	-	Yes	-	-	-
FSGD02PROT14	<PBG2x_base> + 038H	Yes	Yes	Yes	Yes	-	-	-
FSGD02PROT15	<PBG2x_base> + 03CH	Yes	Yes	Yes	-	-	-	-
FSGD09PROT0	<PBG2x_base> + 100H	-	-	Yes	Yes	-	-	-
FSGD09PROT1	<PBG2x_base> + 104H	-	-	Yes	Yes	-	-	-
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FSGD09PROT5	<PBG2x_base> + 114H	Yes	Yes	Yes	-	-	-	-
FSGD09PROT6	<PBG2x_base> + 118H	Yes	Yes	-	-	-	-	-
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FSGD09PROT8	<PBG2x_base> + 120H	Yes	Yes	Yes	-	-	-	-
FSGD09PROT9	<PBG2x_base> + 124H	Yes	Yes	Yes	-	-	-	-
FSGD09PROT10	<PBG2x_base> + 128H	Yes	-	-	-	-	-	-
FSGD09PROT11	<PBG2x_base> + 12CH	Yes	-	-	-	-	-	-

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
FSGD09PROT12	<PBG2x_base> + 130H	Yes	-	-	-	-	-	-
FSGD03PROT0	<PBG3x_base> + 000H	-	-	Yes	Yes	Yes	-	-
FSGD03PROT1	<PBG3x_base> + 004H	-	-	Yes	Yes	Yes	-	-
FSGD03PROT2	<PBG3x_base> + 008H	-	-	Yes	Yes	Yes	-	-
FSGD03PROT3	<PBG3x_base> + 00CH	-	-	Yes	Yes	Yes	-	-
FSGD03PROT4	<PBG3x_base> + 010H	-	-	Yes	Yes	Yes	-	-
FSGD03PROT5	<PBG3x_base> + 014H	-	-	Yes	Yes	Yes	-	-
FSGD03PROT6	<PBG3x_base> + 018H	-	-	-	Yes	Yes	-	-
FSGD03PROT7	<PBG3x_base> + 01CH	-	-	-	Yes	Yes	-	-
FSGD03PROT8	<PBG3x_base> + 020H	-	-	Yes	-	Yes	-	-
FSGD03PROT9	<PBG3x_base> + 024H	-	-	-	Yes	Yes	-	-
FSGD03PROT10	<PBG3x_base> + 028H	Yes	Yes	-	-	Yes	-	-
FSGD03PROT11	<PBG3x_base> + 02CH	-	-	-	-	Yes	-	-
FSGD03PROT12	<PBG3x_base> + 030H	Yes	Yes	-	Yes	Yes	-	-
FSGD03PROT13	<PBG3x_base> + 034H	Yes	Yes	-	-	-	-	-
FSGD03PROT14	<PBG3x_base> + 038H	Yes	Yes	-	-	-	-	-
FSGD04PROT0	<PBG3x_base> + 100H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD04PROT1	<PBG3x_base> + 104H	Yes	Yes	-	Yes	Yes	-	-
FSGD04PROT2	<PBG3x_base> + 108H	Yes	-	-	-	Yes	-	-
FSGD04PROT3	<PBG3x_base> + 10CH	Yes	-	-	-	Yes	-	-
FSGD04PROT4	<PBG3x_base> + 110H	Yes	Yes	Yes	Yes	-	-	-
FSGD04PROT5	<PBG3x_base> + 114H	Yes	Yes	Yes	Yes	-	-	-
FSGD04PROT6	<PBG3x_base> + 118H	Yes	Yes	Yes	Yes	-	-	-
FSGD04PROT7	<PBG3x_base> + 11CH	Yes	Yes	Yes	Yes	-	-	-
FSGD04PROT8	<PBG3x_base> + 120H	-	-	Yes	-	-	-	-
FSGD04PROT9	<PBG3x_base> + 124H	-	-	Yes	Yes	-	-	-
FSGD04PROT10	<PBG3x_base> + 128H	-	-	Yes	Yes	-	-	-
FSGD04PROT11	<PBG3x_base> + 12CH	-	-	-	Yes	-	-	-
FSGD04PROT12	<PBG3x_base> + 130H	Yes	Yes	-	-	-	-	-
FSGD04PROT13	<PBG3x_base> + 134H	Yes	Yes	-	-	-	-	-
FSGD04PROT14	<PBG3x_base> + 138H	Yes	Yes	-	-	-	-	-
FSGD05PROT0	<PBG3x_base> + 200H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT1	<PBG3x_base> + 204H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT2	<PBG3x_base> + 208H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT3	<PBG3x_base> + 20CH	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT4	<PBG3x_base> + 210H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT5	<PBG3x_base> + 214H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT6	<PBG3x_base> + 218H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT7	<PBG3x_base> + 21CH	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT8	<PBG3x_base> + 220H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT9	<PBG3x_base> + 224H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD05PROT10	<PBG3x_base> + 228H	Yes	Yes	-	Yes	Yes	-	-
FSGD05PROT11	<PBG3x_base> + 22CH	Yes	Yes	-	Yes	Yes	-	-
FSGD05PROT12	<PBG3x_base> + 230H	Yes	Yes	-	-	Yes	-	-
FSGD05PROT13	<PBG3x_base> + 234H	Yes	Yes	-	-	Yes	-	-
FSGD05PROT14	<PBG3x_base> + 238H	Yes	Yes	-	-	Yes	-	-
FSGD05PROT15	<PBG3x_base> + 23CH	Yes	Yes	-	-	Yes	-	-
FSGD13PROT0	<PBG3x_base> + 300H	Yes	-	-	-	-	-	-
FSGD13PROT1	<PBG3x_base> + 304H	Yes	-	-	-	-	-	-
FSGD13PROT2	<PBG3x_base> + 308H	Yes	-	-	-	-	-	-
FSGD13PROT3	<PBG3x_base> + 30CH	Yes	-	-	-	-	-	-
FSGD13PROT4	<PBG3x_base> + 310H	Yes	-	-	-	-	-	-
FSGD13PROT5	<PBG3x_base> + 314H	Yes	-	-	-	-	-	-
FSGD13PROT6	<PBG3x_base> + 318H	Yes	-	-	-	-	-	-

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
FSGD13PROT7	<PBG3x_base> + 31CH	Yes	-	-	-	-	-	-
FSGD10PROT0	<PBG4x_base> + C00H	Yes	Yes	-	-	-	-	-
FSGD10PROT1	<PBG4x_base> + C04H	Yes	Yes	-	-	-	-	-
FSGD06PROT0	<PBG5x_base> + 000H	Yes	Yes	Yes	Yes	Yes	-	-
FSGD06PROT1	<PBG5x_base> + 004H	Yes	Yes	Yes	Yes	Yes	-	-
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FSGD06PROT4	<PBG5x_base> + 010H	Yes	Yes	Yes	Yes	-	-	-
FSGD06PROT5	<PBG5x_base> + 014H	Yes	Yes	Yes	Yes	-	-	-
—								
FSGD06PROT7	<PBG5x_base> + 01CH	Yes	Yes	Yes	Yes	-	-	-
FSGD06PROT8	<PBG5x_base> + 020H	Yes	Yes	Yes	Yes	-	-	-
FSGD11PROT0	<PBG6x_base> + 800H	Yes	Yes	-	-	-	-	-
FSGD11PROT1	<PBG6x_base> + 804H	Yes	Yes	-	-	-	-	-
FSGD11PROT2	<PBG6x_base> + 808H	Yes	Yes	-	-	-	-	-
FSGD11PROT3	<PBG6x_base> + 80CH	Yes	Yes	-	-	-	-	-
FSGD11PROT4	<PBG6x_base> + 810H	Yes	Yes	-	-	-	-	-
FSGD11PROT5	<PBG6x_base> + 814H	Yes	Yes	-	-	-	-	-
FSGD11PROT6	<PBG6x_base> + 818H	Yes	Yes	-	-	-	-	-
FSGD11PROT7	<PBG6x_base> + 81CH	Yes	Yes	-	-	-	-	-
FSGD11PROT8	<PBG6x_base> + 820H	Yes	Yes	-	-	-	-	-
FSGD11PROT9	<PBG6x_base> + 824H	Yes	Yes	-	-	-	-	-
FSGD11PROT10	<PBG6x_base> + 828H	Yes	Yes	-	-	-	-	-
FSGD11PROT11	<PBG6x_base> + 82CH	Yes	Yes	-	-	-	-	-
FSGD14PROT0	<PBG6x_base> + 900H	Yes	-	-	-	-	-	-
FSGD14PROT1	<PBG6x_base> + 904H	Yes	-	-	-	-	-	-
FSGD14PROT2	<PBG6x_base> + 908H	Yes	-	-	-	-	-	-
FSGD14PROT3	<PBG6x_base> + 90CH	Yes	-	-	-	-	-	-
FSGD14PROT4	<PBG6x_base> + 910H	Yes	-	-	-	-	-	-
FSGD14PROT5	<PBG6x_base> + 914H	Yes	-	-	-	-	-	-
FSGD14PROT6	<PBG6x_base> + 918H	Yes	-	-	-	-	-	-
FSGD14PROT7	<PBG6x_base> + 91CH	Yes	-	-	-	-	-	-
HFSGD00PROT0	<HBG0x_base> + 000H	Yes	Yes	-	-	Yes	-	-
HFSGD00PROT1	<HBG0x_base> + 004H	Yes	Yes	-	-	-	-	-
HFSGD00PROT2	<HBG0x_base> + 008H	Yes	Yes	-	-	-	-	-
HFSGD00PROT3	<HBG0x_base> + 00CH	Yes	Yes	-	-	-	-	-
HFSGD00PROT4	<HBG0x_base> + 010H	Yes	Yes	-	-	-	-	-
HFSGD01PROT0	<HBG0x_base> + 100H	Yes	Yes	-	-	-	-	-
HFSGD01PROT1	<HBG0x_base> + 104H	Yes	Yes	-	-	-	-	-
HFSGD02PROT0	<HBG0x_base> + 108H	Yes	Yes	-	-	-	-	-
PBG for CPU System								
FSGDC0PROT0	<PBGCx_base> + 000H	Yes	Yes	Yes	Yes	-	-	-
FSGDC0PROT1	<PBGCx_base> + 004H	Yes	Yes	Yes	Yes	-	-	-
FSGDC0PROT2	<PBGCx_base> + 008H	Yes	-	-	-	-	-	-
FSGDC1PROT0	<PBGCx_base> + 120H	Yes	Yes	Yes	Yes	-	-	-
FSGDC1PROT1	<PBGCx_base> + 124H	Yes	Yes	Yes	Yes	-	-	-
FSGDC1PROT2	<PBGCx_base> + 128H	Yes	Yes	Yes	Yes	-	-	-
FSGDC1PROT3	<PBGCx_base> + 12CH	Yes	Yes	Yes	Yes	-	-	-
FSGDC1PROT4	<PBGCx_base> + 130H	Yes	Yes	Yes	Yes	-	-	-
FSGDC1PROT5	<PBGCx_base> + 134H	Yes	Yes	Yes	Yes	-	-	-
FSGDC1PROT6	<PBGCx_base> + 118H	Yes	Yes	-	-	-	-	-
FSGDC1PROT7	<PBGCx_base> + 11CH	Yes	Yes	-	-	-	-	-
FSGDC1PROT8	<PBGCx_base> + 138H	Yes	-	-	-	-	-	-
FSGDC1PROT9	<PBGCx_base> + 13CH	Yes	-	-	-	-	-	-

Name	Address	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
ERRSLVC0CTL	<PBGCx_base> + 800H	Yes	Yes	Yes	Yes	-	-	-
ERRSLVC0STAT	<PBGCx_base> + 804H	Yes	Yes	Yes	Yes	-	-	-
ERRSLVC0ADDR	<PBGCx_base> + 808H	Yes	Yes	Yes	Yes	-	-	-
ERRSLVC0TYPE	<PBGCx_base> + 80CH	Yes	Yes	Yes	Yes	-	-	-
ERRSLVC1CTL	<PBGCx_base> + 900H	Yes	Yes	Yes	Yes	-	-	-
ERRSLVC1STAT	<PBGCx_base> + 904H	Yes	Yes	Yes	Yes	-	-	-
ERRSLVC1ADDR	<PBGCx_base> + 908H	Yes	Yes	Yes	Yes	-	-	-
ERRSLVC1TYPE	<PBGCx_base> + 90CH	Yes	Yes	Yes	Yes	-	-	-

29.3 Guard group assignments

The table below shows the functional assignment of each guard group:

PBG/HBG Group	Group No. (Register Name index)	PBG/HBG Channel Number	Protection Target Module	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
PBG10	00	0	ECON_NMI FENMI	Yes -	Yes -	Yes -	- Yes	- Yes	- -	- -
		1	ECON_FEINT FEINT	Yes -	Yes -	Yes -	- Yes	- Yes	- -	- -
		2	SL_INTC INTC1/INTC2	Yes -	Yes -	Yes -	- Yes	- Yes	- -	- -
		3	ADCA0	Yes	←	←	←	←	-	-
		4	KR0	Yes	←	←	←	←	-	-
		5	PORT (Group A_ISO)	Yes	←	←	←	←	-	-
		6	PORT (Group A_AWO)	Yes	←	←	←	←	-	-
		7	JTAG (Group A)	Yes	←	←	←	←	-	-
		8	RLN30	Yes	←	←	←	←	-	-
		9	RLN31	Yes	←	←	←	←	-	-
		10	RLN32	Yes	←	←	←	←	-	-
		11	RLN33	Yes	←	←	←	←	-	-
		12	RLN34	Yes	←	-	←	←	-	-
		13	RLN35	Yes	←	-	←	←	-	-
		14	RLN36	Yes	←	-	-	-	-	-
		15	RLN37	Yes	←	-	-	-	-	-
PBG11	01	0	DNF (TAUD0)	Yes	←	←	←	←	-	-
		1	DNF (ADCA0)	Yes	←	←	←	←	-	-
		2	FCLA0 (ADCA0)	Yes	←	←	←	←	-	-
		3	FCLA0 (NMI)	Yes	←	←	←	←	-	-
		4	FCLA0 (INTPn)	Yes	←	←	←	←	-	-
		5	FCLA0 (INTPn)	Yes	←	←	←	←	-	-
		6	DNF (ENCA0)	Yes	←	←	←	←	-	-
		7	DNF (ADCA1)	Yes	←	-	←	←	-	-
		8	FCLA0 (ADCA1)	Yes	←	-	←	←	-	-
		9	DNF (TAUB0)	Yes	←	←	←	-	-	-
		10	DNF (TAUB1)	Yes	←	-	←	-	-	-
		11	Reserved area	-	-	-	-	-	-	-
		12	PORT (Group B_ISO)	Yes	←	←	←	-	-	-
		13	PORT (Group B_AWO)	Yes	←	←	←	-	-	-
		14	JTAG (Group B)	Yes	←	←	←	-	-	-
		15	FCLA0 (INTPn)	Yes	←	-	-	-	-	-
PBG12	07	0	RLN240 (Global)	Yes	←	←	←	-	-	-
		1	RLN2400	Yes	←	←	←	-	-	-

PBG/HBG Group	Group No. (Register Name index)	PBG/HBG Channel Number	Protection Target Module	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
		2	RLN2401	Yes	←	←	←	-	-	-
		3	RLN2402	Yes	←	←	←	-	-	-
		4	RLN2403	Yes	←	-	←	-	-	-
		5	RLN241 (Global)	Yes	←	-	←	-	-	-
		6	RLN2414	Yes	←	-	←	-	-	-
		7	RLN2415	Yes	←	-	←	-	-	-
		8	RLN2416	Yes	←	-	←	-	-	-
		9	RLN2417	Yes	←	-	←	-	-	-
		10	RLN242 (Global)	Yes	←	-	←	-	-	-
		11	RLN2428	Yes	←	-	←	-	-	-
		12	RLN2429	Yes	←	-	←	-	-	-
		13	RLN24210	Yes	←	-	-	-	-	-
		14	RLN24211	Yes	←	-	-	-	-	-
		15	DNF (RSENTn)	Yes	←	←	-	-	-	-
PBG13	08	0	DCRA0	Yes	←	←	←	-	-	-
		1	DCRA1	Yes	←	←	←	-	-	-
		2	DCRA2	Yes	←	←	←	-	-	-
		3	DCRA3	Yes	←	←	←	-	-	-
		4	RIIC0	Yes	←	←	←	-	-	-
		5	SL_READTEST	Yes	←	←	-	-	-	-
			ECC test	-	-	-	←	-	-	-
		6	SL_DMAC	Yes	←	←	-	-	-	-
		7	GRZF	Yes	←	←	-	-	-	-
		8	RIIC1	Yes	←	←	-	-	-	-
		9	Reserved area	-	-	-	-	-	-	-
		10	Reserved area	-	-	-	-	-	-	-
		11	Reserved area	-	-	-	-	-	-	-
		12	Reserved area	-	-	-	-	-	-	-
		13	RSENT0	Yes	←	←	-	-	-	-
		14	RSENT1	Yes	←	←	-	-	-	-
PBG14	12	0	RLN243 (Global)	Yes	-	-	-	-	-	-
		1	RLN24312	Yes	-	-	-	-	-	-
		2	RLN24313	Yes	-	-	-	-	-	-
		3	RLN24314	Yes	-	-	-	-	-	-
		4	RLN24315	Yes	-	-	-	-	-	-
PBG20	02	0	TAUD0	Yes	←	←	←	←	-	-
		1	SL_TAUD0	Yes	←	←	←	←	-	-
		2	TAUJ0	Yes	←	←	←	←	-	-
		3	SL_TAUJ0	Yes	←	←	←	←	-	-
		4	RTCA0	Yes	←	←	←	←	-	-
		5	WDTA0	Yes	←	←	←	←	-	-
		6	WDTA1	Yes	←	←	←	←	-	-
		7	WDTA2	Yes	-	-	-	Yes	-	-
		8	PIC0	Yes	←	←	←	←	-	-
		9	TAPA0	Yes	←	←	←	←	-	-
		10	ENCA0	Yes	←	←	←	←	-	-
		11	TAUJ1	Yes	←	←	←	-	-	-
		12	TAUB0	Yes	←	←	←	-	-	-
		13	TAUB1	Yes	←	-	←	-	-	-
		14	PWBAn, PWGAn, PWSAn, SLPWG, PWGA_INTF	Yes	←	←	←	-	-	-

PBG/HBG Group	Group No. (Register Name index)	PBG/HBG Channel Number	Protection Target Module	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
		15	SL_TAUJ2	Yes	←	←	-	-	-	-
PBG21	09	0	Flash memory (DCIB)	-	-	Yes	←	-	-	-
		1	DFECC	-	-	Yes	←	-	-	-
		2	Reserved area	-	-	-	-	-	-	-
		3	Reserved area	-	-	-	-	-	-	-
		4	Reserved area	-	-	-	-	-	-	-
		5	SL_TAUB0	Yes	←	←	-	-	-	-
		6	SL_TAUB1	Yes	←	-	-	-	-	-
		7	Reserved area	-	-	-	-	-	-	-
		8	TAUJ2	Yes	←	←	-	-	-	-
		9	TAUJ3	Yes	←	←	-	-	-	-
		10	MMCA0	Yes	-	-	-	-	-	-
		11	ECCMMC0A	Yes	-	-	-	-	-	-
		12	ECCMMC0B	Yes	-	-	-	-	-	-
PBG30	03	0	RCFDC0 (channel 0)	-	-	Yes	←	←	-	-
		1	RCFDC0 (channel 1)	-	-	Yes	←	←	-	-
		2	RCFDC0 (channel 2)	-	-	Yes	←	←	-	-
		3	RCFDC0 (channel 3)	-	-	Yes	←	←	-	-
		4	RCFDC0 (channel 4)	-	-	Yes	←	←	-	-
		5	RCFDC0 (channel 5)	-	-	Yes	←	←	-	-
		6	RSCAN0_Global	-	-	-	Yes	←	-	-
		7	RSCAN1_CAN6	-	-	-	Yes	←	-	-
		8	RCFDC0 (Global)	-	-	Yes	-	-	-	-
			RSCAN1_CAN7	-	-	-	-	←	-	-
		9	RSCAN1_Global	-	-	-	Yes	←	-	-
		10	ETNB0	Yes	←	-	-	Yes	-	-
		11	ETHER0 (Group B)	-	-	-	-	Yes	-	-
		12	ADCA1	Yes	←	-	Yes	←	-	-
		13	ECCETNB0TX	Yes	←	-	-	-	-	-
		14	ECCETNB0RX	Yes	←	-	-	-	-	-
PBG31	04	0	OSTM0	Yes	←	←	←	←	-	-
		1	OSTM1-4	Yes	←	-	←	←	-	-
		2	OSTM5	Yes	-	-	-	←	-	-
		3	OSTM6-9	Yes	-	-	-	←	-	-
		4	ECCCSIH0	Yes	←	←	←	-	-	-
		5	ECCCSIH1	Yes	←	←	←	-	-	-
		6	ECCCSIH2	Yes	←	←	←	-	-	-
		7	ECCCSIH3	Yes	←	←	←	-	-	-
		8	ECCCFD0MB	-	-	Yes	-	-	-	-
		9	ECCCFD0AFL0	-	-	Yes	-	-	-	-
			ECCCAN1	-	-	-	Yes		-	-
		10	ECCCFD0AFL1	-	-	Yes	-	-	-	-
			ECCCAN0 PHY1	-	-	-	Yes		-	-
		11	ECCCAN0 PHY2	-	-	-	Yes	-	-	-
		12	ECCFLXA0	Yes	←	-	-	-	-	-
		13	ECCFLXA0T0	Yes	←	-	-	-	-	-
		14	ECCFLXA0T1	Yes	←	-	-	-	-	-
PBG32	05	0	CSIH0 (Group A)	Yes	←	←	←	←	-	-
		1	CSIH0 (Group B)	Yes	←	←	←	←	-	-
		2	CSIH1 (Group A)	Yes	←	←	←	←	-	-
		3	CSIH1 (Group B)	Yes	←	←	←	←	-	-
		4	CSIH2 (Group A)	Yes	←	←	←	←	-	-

PBG/HBG Group	Group No. (Register Name index)	PBG/HBG Channel Number	Protection Target Module	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
		5	CSIH2 (Group B)	Yes	←	←	←	←	-	-
		6	CSIH3 (Group A)	Yes	←	←	←	←	-	-
		7	CSIH3 (Group B)	Yes	←	←	←	←	-	-
		8	CSIG0 (Group A)	Yes	←	←	←	←	-	-
		9	CSIG0 (Group B)	Yes	←	←	←	←	-	-
		10	CSIG1 (Group A)	Yes	←	-	←	←	-	-
		11	CSIG1 (Group B)	Yes	←	-	←	←	-	-
		12	CSIG2 (Group A)	Yes	←	-	-	Yes	-	-
		13	CSIG2 (Group B)	Yes	←	-	-	Yes	-	-
		14	CSIG3 (Group A)	Yes	←	-	-	Yes	-	-
		15	CSIG3 (Group B)	Yes	←	-	-	Yes	-	-
PBG33	13	0	CSIH4 (Group A)	Yes	-	-	-	-	-	-
		1	CSIH4 (Group B)	Yes	-	-	-	-	-	-
		2	ECCCSIH4	Yes	-	-	-	-	-	-
		3	CSIG4 (Group A)	Yes	-	-	-	-	-	-
		4	CSIG4 (Group B)	Yes	-	-	-	-	-	-
		5	ETNB1	Yes	-	-	-	-	-	-
		6	ECCETNB1TX	Yes	-	-	-	-	-	-
		7	ECCETNB1RX	Yes	-	-	-	-	-	-
PBG40	10	0	Flash memory (DCIB)	Yes	←	-	-	-	-	-
		1	DFECC	Yes	←	-	-	-	-	-
PBG50	06	0	System control	Yes	←	←	←	←	-	-
		1	STBC0	Yes	←	←	←	←	-	-
		2	Reserved area	-	-	-	-	-	-	-
		3	Reserved area	-	-	-	-	-	-	-
		4	RESCTL SWRESET	Yes -	← -	← -	- ←	-	-	-
		5	Flash memory (Self Programming)	Yes	←	←	←	-	-	-
		6	Flash memory (Control)	Yes	←	←	←	-	-	-
		7	Flash memory (SCDS)	Yes	←	←	←	-	-	-
		8	WPROTR	Yes	←	←	←	-	-	-
PBG60	11	0	RCFDC0 (channel 0)	Yes	←	-	-	-	-	-
		1	RCFDC0 (channel 1)	Yes	←	-	-	-	-	-
		2	RCFDC0 (channel 2)	Yes	←	-	-	-	-	-
		3	RCFDC0 (channel 3)	Yes	←	-	-	-	-	-
		4	RCFDC0 (channel 4)	Yes	←	-	-	-	-	-
		5	RCFDC0 (channel 5)	Yes	←	-	-	-	-	-
		6	RCFDC0 (channel 6)	Yes	←	-	-	-	-	-
		7	RCFDC0 (channel 7)	Yes	←	-	-	-	-	-
		8	RCFDC0 (Global)	Yes	←	-	-	-	-	-
		9	ECCCFD0MB	Yes	←	-	-	-	-	-
		10	ECCCFD0AFL0	Yes	←	-	-	-	-	-
		11	ECCCFD0AFL1	Yes	←	-	-	-	-	-
PBG61	14	0	RCFDC1_CAN0	Yes	-	-	-	-	-	-
		1	RCFDC1_CAN1	Yes	-	-	-	-	-	-
		2	RCFDC1_CAN2	Yes	-	-	-	-	-	-
		3	RCFDC1_CAN3	Yes	-	-	-	-	-	-
		4	RCFDC1_Global	Yes	-	-	-	-	-	-
		5	ECCCFD1MB	Yes	-	-	-	-	-	-
		6	ECCCFD1AFL0	Yes	-	-	-	-	-	-

PBG/HBG Group	Group No. (Register Name index)	PBG/HBG Channel Number	Protection Target Module	F1KH-D8	F1KM-S4	F1KM-S1	F1K	F1H	F1M	F1L
		7	ECCCFD1AFL1	Yes	-	-	-	-	-	-
HBG00	00	0	MEMC0	Yes	←	-	-	Yes	-	-
		1	MEMC0_CS0	Yes	←	-	-	-	-	-
		2	MEMC0_CS1	Yes	←	-	-	-	-	-
		3	MEMC0_CS2	Yes	←	-	-	-	-	-
		4	MEMC0_CS3	Yes	←	-	-	-	-	-
HBG01	01	0	SFMA0	Yes	←	-	-	-	-	-
		1	SFMA0_MEM	Yes	←	-	-	-	-	-
HBG02	02	0	FLXA0	Yes	←	-	-	-	-	-
PBGC0	C0	0	INTC2	Yes	←	←	←	-	-	-
		1	PDMA0	Yes	←	←	←	-	-	-
		2	PDMA1	Yes	-	-	-	-	-	-
PBGC1	C1	0	Flash memory (Programing function)	Yes	←	←	←	-	-	-
		1	Code flash ECC control register (VCI)	Yes	←	←	←	-	-	-
		2	Code flash ECC control register (PE1)	Yes	←	←	←	-	-	-
		3	Local RAM ECC control register (PE1)	Yes	←	←	←	-	-	-
		4	System control module On-Chip Debug module	Yes -	- Yes	- ←	- ←	- -	- -	- -
		5	Buffer controller	Yes	←	←	←	-	-	-
		6	Global RAM ECC Control register (bank A)	Yes	←	-	-	-	-	-
		7	Global RAM ECC Control register (bank B)	Yes	←	-	-	-	-	-
		8	Code flash ECC control register (PE2)	Yes	-	-	-	-	-	-
		9	Local RAM ECC control register (PE2)	Yes	-	-	-	-	-	-

30. Intelligent Cryptographic Unit (ICU)

Details of the ICU are not described in this document.

31. On-Chip Debug Unit (OCD)

Details of the OCD are not described in this document.

Still, due to the highly identical implementation on F1Kx/F1K to the previous device series no immediate impact to the application is foreseen.

32. Flash Memory

Information about ECC related functions of the Flash can be found in the chapter ‘Functional Safety’.

33. RAM

Information about ECC related functions of the RAM can be found in the chapter ‘Functional Safety’.

34. Boundary Scan

The description of boundary scan is not part of this document.

35. Power Supply and Power Domains

The description of the power supply and power domains is not part of this document.

Revision History

This table shows the major changes compared to the previous document version:

Revision	Date	Description
1.00	2015-Apr-30	• Initial version
2.00	2017-Jan-31	• Added F1KM-S4 and F1KM-S1 as key comparison devices of this document.
2.10	2017-Mar-01	• Aligned content with updated F1KM UM v0.5 • Added pinning differences in chapter 2
2.20	2017-12-12	• Added F1KH device • Corrected pinning chapter 2 • Added F1KM-S4 100pin in chapter 2 (pinning differences) • Corrected P0_2 comparison of F1KM-S4 vs. F1K 144pin devices
2.30	2018-07-26	• Corrected F1KM-S4 vs F1H 233pin pad difference table • Corrected F1KM-S4 vs F1M 233pin pad difference table • Reflect changes of pinning related to the F1Kx UM update • Added chapter ’15 FlexRay Interface (FLXA)’ • Added chapter ‘28 Memory Protection’
2.40	2018-08-14	• Corrected CSIG Register Base Address Table for F1L
3.00	2018-12-19	• Various corrections in each chapter.
3.10	2019-09-27	• Update of document references and update of related content. • Removal of references to F1KH-D8 272pin • Added chapter ‘6. Reset Controller’

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.3.0-1 November 2016)

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