Summary

This document describes notes on implementation of crystal resonators and matching evaluation methods of oscillation circuits.

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1. Implementation Notes of Crystal Resonator

When you implement a crystal resonator into a PCB, follow the instructions in this document to prevent a decrease in an oscillation margin and to suppress the EMI level.

1.1 Recommended Crystal Oscillation Circuit

Figure 1 shows a recommended example of a crystal oscillation circuit.

When you use an internal capacitor (Set MOSC_CAP_SEL[3:0] to the value except for 0000b), implementation of a damping resistor (Rd) and load capacitors (Cx1 and Cx2) is basically not required. However, some resonators or parasitic capacitance may require their implementation. Consult with a crystal resonator manufacturer and decide the details.

When you do not use an internal capacitor (Set MOSC_CAP_SEL[3:0] = 0000b), a damping resistor (Rd) and load capacitors (Cx1 and Cx2) should be implemented. Consult with a crystal resonator manufacturer and decide the details. You do not have to implement a feedback resistor on your board, since it is incorporated in the MCU.

Use an AT-cut crystal resonator in fundamental mode.

![Figure 1 Example of Crystal Oscillation Circuit](image)
1.2 Board Pattern Example for Stable Oscillation

- Design traces on the top layer of the board (the GND shield is required).
- Place the GND shield on the bottom layer of the board.
- Do not use middle layers of the board.
- The trace length from the MCU pin to the crystal resonator should be 10 mm maximum.
- Make the signal trace width between 0.1 and 0.3 mm.
- Leave a 0.3 mm space or more between the signal traces and other traces (also leave a 0.3 mm space or more between the X1 and X2 trace).
- X1 and X2 trace resistance < 2 Ω
- X1 and X2 trace capacitance < 2 pF
- Connect an approximately 0.1 μF capacitor between VCC and VSS.

Figure 2  Board Pattern Example for Stable Oscillation (BGA373)
1.3 Unfavorable Crystal Oscillation Circuit

Figure 3 and Figure 4 show examples of an unfavorable crystal oscillation circuit.

(a) Traces of oscillation circuit are long
(b) Signal traces are crossed
(c) X1 & X2 signal traces are crossed
(d) Middle layers under X1 & X2 traces have power or GND patterns / Space between GND shield and oscillation circuit is narrow

**Note 1.** Avoid signal crossing so that the pin-to-pin capacitance between X1 and X2 may not degrade the oscillation characteristics. In addition, when the traces are placed parallely, pay attention to the trace space and the parallel length of the trace not to increase the pin-to-pin capacitance.

**Note 2.** When you use a multi-layered board, do not place power or GND patterns under the trace of the X1 and X2 pins and the crystal resonator area, the dotted area in the figure (d). Secure at least a 0.5 mm space between the GND shield and the oscillation circuit.
circuit. Otherwise, the increase in the parasitic capacitance may affect the oscillation characteristics.

Figure 3  Unfavorable Crystal Oscillation Circuit (1/2)

(e) Changing high current is placed near signal traces

(f) Currents flow on GND line in oscillation circuit
(Potentials at A, B, and C vary)

(g) Trace is branched

Figure 4  Unfavorable Crystal Oscillation Circuit (2/2)
1.4 Verified Crystal Resonator and Reference Oscillation Circuit Parameter

Figure 5 and Table 1 show verified crystal resonators and reference oscillation circuit parameters. Crystal oscillator manufacturers measured these parameters under specific conditions with our evaluation board. To confirm the oscillation characteristics in actual applications, consult with an oscillator resonator manufacturer to perform an evaluation on the actual PCB.

![Figure 5 External Circuit Example](image)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product name</th>
<th>CL (pF)</th>
<th>SMD/lead</th>
<th>Frequency (MHz)</th>
<th>Cx1 (pF)</th>
<th>Cx2 (pF)</th>
<th>Rd (kΩ)</th>
<th>External oscillation circuit parameter (reference)</th>
<th>OPBT setting (reference)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NIHON DEMPA KOGYO CO., LTD.</td>
<td>NX2016GC</td>
<td>8</td>
<td>SMD</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>SMD</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td>NX3225GB</td>
<td>8</td>
<td>SMD</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1 0 0111 1 0 011 100 000 000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>SMD</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>1 1</td>
<td>1 0 0001 1 0 100 110 000 000</td>
<td>TBD</td>
</tr>
<tr>
<td>Kyocera Corp.</td>
<td>CX2016GR</td>
<td>8</td>
<td>SMD</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1 0 0010 1 0 100 001 010 000</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td>SMD</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>1 1</td>
<td>1 0 0010 1 0 011 100 000 000</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td>CX3225GA</td>
<td>8</td>
<td>SMD</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1 0 0100 1 0 000 010 001 000</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td>SMD</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>1 1</td>
<td>1 0 0101 1 0 100 101 000 000</td>
<td>TBD</td>
</tr>
<tr>
<td>Daishinku Corp.</td>
<td>DSX210GE</td>
<td>8</td>
<td>SMD</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1 0 0000 1 0 111 111 001 000</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8</td>
<td>SMD</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>1 1</td>
<td>1 0 0000 1 0 100 111 000 000</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td>DSX320GE</td>
<td>8</td>
<td>SMD</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1 0 0000 1 0 111 111 001 000</td>
<td>TBD</td>
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<tr>
<td></td>
<td></td>
<td>8</td>
<td>SMD</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>1 1</td>
<td>1 0 0000 1 0 100 111 000 000</td>
<td>TBD</td>
</tr>
</tbody>
</table>
Note 1. The verified crystal resonators, reference oscillation circuit parameters, and OPBT settings listed here are only reference values based on information from crystal resonator manufacturers and are not guaranteed. The reference oscillation circuit parameters are measured by crystal resonator manufacturers under specific conditions using our evaluation board. Since crystal oscillation depends on a crystal resonator or board design, consult with a crystal resonator manufacturer to perform an evaluation on the actual PCB. In addition, the conditions above are applied for oscillating the resonator connected to the MCU, and do not indicate MCU operating conditions. Use the MCU within the DC and AC characteristics.

Note 2. You do not have to implement a feedback resistor on your board, since it is incorporated in the MCU.
2. Matching Evaluation Methods of Oscillation Circuit

2.1 Oscillation Circuit

Figure 6 shows a block diagram of an oscillation circuit. The MCU in the oscillation circuit incorporates an internal capacitor and a damping resistor to reduce the number of external components. Also, to be compatible with a wide range of crystal resonators, each parameter of the oscillation circuit can be set in Option Byte (OPBT) individually depending on whether the oscillation is unstable or stable.

Figure 6  Block Diagram of Oscillation Circuit

Figure 7 shows a block diagram of OSC monitor mode. In OSC monitor mode, inputting the same parameter to be set in OPBT with external pins reduces the time and effort to rewrite OPBT so many times to evaluate circuit matching.

Figure 7  Block Diagram of OSC Monitor Mode

2.2 How to Decide Matching

This section describes how to decide matching with the following two procedures:

1. Provisional OPBT Settings by Theoretical Study (Section 2.3)

   Before matching evaluation on the actual PCB, provisionally configure OPBT settings based on a crystal resonator to be used or parasitic capacitance which depends on board patterns.

2. Oscillation Characterization on Actual System (Section 2.4)

   Due to differences between estimated values and values extracted or measured by the actual PCB, provisional values may not match desired electrical characteristics of a crystal oscillation circuit. To see if you can obtain the desired electrical characteristics of the crystal oscillation circuit when these values are applied on actual applications, perform a matching
evaluation or request a crystal resonator manufacturer to make the evaluation.

### 2.2.1 Oscillation Circuit Model and Parameters to Be Used

![Oscillation Circuit Model](image)

Figure 8 shows the oscillation circuit model and Table 2 the parameters to be used.

#### Table 2 Parameters to Be Used

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Data source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillation frequency</td>
<td>$f_L$</td>
<td>Crystal resonator data sheet</td>
</tr>
<tr>
<td>Crystal resonator load capacitance</td>
<td>$C_L$</td>
<td>Crystal resonator data sheet</td>
</tr>
<tr>
<td>Crystal resonator series resistance (max)</td>
<td>$R_1$(max)</td>
<td>Crystal resonator data sheet</td>
</tr>
<tr>
<td>Crystal resonator drive level (max)</td>
<td>$D_L$(max)</td>
<td>Crystal resonator data sheet</td>
</tr>
<tr>
<td>Parallel capacitance in crystal resonator</td>
<td>$C_0$</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td>equivalent circuit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Series resistance in crystal resonator</td>
<td>$R_1$</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td>equivalent circuit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Series inductance in crystal resonator</td>
<td>$L_1$</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td>equivalent circuit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Series capacitance in crystal resonator</td>
<td>$C_1$</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td>equivalent circuit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Target gain margin Note 1 (unstable/stable)</td>
<td>$\text{Gain margin}$</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td>Target negative resistance Note 1</td>
<td>$-R$</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td>(unstable/stable)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trans conductance in internal oscillation</td>
<td>$g_m$</td>
<td>See RH850/E2x-FCC2 Electrical Characteristics, User’s Manual: Hardware</td>
</tr>
<tr>
<td>amplifier</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X1/X2 trace capacitance in MCU</td>
<td>$C_{s_MCU}$</td>
<td>See RH850/E2x-FCC2 Electrical Characteristics, User’s Manual: Hardware</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>-------------</td>
<td>--------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>X1/X2 trace capacitance in board</td>
<td>$C_{s_board}$</td>
<td>Make an estimation based on the actual board design. When it is difficult to perform the estimation, provisionally set 2 pF under the conditions that you follow the board pattern examples in 1.2.</td>
</tr>
</tbody>
</table>

Note 1. If a crystal resonator manufacturer provides you with both max and min target values, ignore the max target value at first and only satisfy the min target value of the negative resistance. Check the max target value of the negative resistance by an evaluation on the actual PCB in which the risk of 3rd overtones should also be checked.
2.3 Provisional OPBT Settings by Theoretical Study

2.3.1 Provisional Settings of Internal Capacitance (Configured by CAPSEL[3:0])

CAPSEL[3:0], a parameter specifying the internal capacitance $C_{x1}$ and $C_{x2}$, needs settings to obtain the target frequency of a crystal resonator. By using the formula (1), provisionally set the value which can match $C_L$ in the crystal resonator data sheet as much as possible.

$$C_L = \frac{(C_{x1} + C_{s, MCU} + C_{s, board}) \times (C_{x2} + C_{s, MCU} + C_{s, board})}{(C_{x1} + C_{s, MCU} + C_{s, board}) + (C_{x2} + C_{s, MCU} + C_{s, board})} \cdots (1)$$

Refer to RH850/E2x-FCC2 Electrical Characteristics, User’s Manual: Hardware, 1.3.4.1, Main Oscillator Characteristics to see how CAPSEL[3:0] corresponds to $C_{X1}$, $C_{X2}$, and $C_{s, MCU}$.

2.3.1.1 Calculation Example

When $C_L = 8$ pF and $C_{s, board} = 2$ pF, provisionally set CAPSEL[3:0] = 0110b based on the following formula.

$$C_L = \frac{(10.5 + 2.5 + 2) \times (12.1 + 2.5 + 2)}{(10.5 + 2.5 + 2) + (12.1 + 2.5 + 2)} = 8 \text{ [pF]} \cdots (2)$$
2.3.2  Provisional Settings of Internal Damping Resistance (Configured by RDSEL[2:0])

RDSEL[2:0], a parameter specifying internal damping resistance, can be used for satisfying both of drive level and gain margin of a crystal resonator. However, it is difficult in theoretical study to adjust drive level, so provisionally set the minimum value (TYP) 338Ω (RDSEL[2:0] = 000b) based on RDSEL[2:0] settings in RH850/E2x-FCC2 Electrical Characteristics, User’s Manual: Hardware, 1.3.4.1, Main Oscillator Characteristics. Also, adjust RDSEL[2:0] when too much gain is obtained with the calculation in 2.3.3.

2.3.3  Provisional Settings of Oscillation Amplifier Gain (Configured by SHTSTBY, AMPSEL[2:0])

SHTSTBY and AMPSEL[2:0], parameters specifying the oscillation margin of the amplifier gain, require settings for stable oscillation start-up. Conduct a theoretical examination by using trans conductance of an internal oscillation amplifier (g_m) or equivalent circuit parameters of a crystal resonator.

The minimum required trans conductance for an oscillation circuit, g_m (min), can be calculated by the formula (3) based on the equivalent circuit parameter, frequency, and load capacitance of a crystal resonator.

\[
g_m (\text{min}) = R_L (\text{max}) \times (2\pi f)^2 \times 4 \times (C_L)^2 \quad \cdots \quad (3)
\]

CL can be calculated by the formula (1) and R_L (max) by the formula (4).

\[
R_L (\text{max}) \cong R_1 (\text{max}) \times \left( 1 + \frac{C_0}{C_L} \right)^2 \quad \cdots \quad (4)
\]

Gain margin can be calculated by the formula (5).

\[
\text{gain margin} > \frac{g_m}{g_m (\text{min})} \quad \cdots \quad (5)
\]

Refer to RH850/E2x-FCC2 Electrical Characteristics, User’s Manual: Hardware, 1.3.4.1, Main Oscillator Characteristics to see how SHTSTBY and AMPSEL[2:0] correspond to g_m.
2.3.3.1 Calculation Example

The following formulas show the calculation results when \( f = 20 \text{ MHz} \), \( C_L = 8 \text{ pF} \), \( C_0 = 1.72 \text{ pF} \), \( R_1 \text{ (max)} = 100 \text{ Ω} \), \( VCC = 3.0 \text{ to 3.6 V} \), gain margin (Main OSC: Unstable) > 10 times compared to \( g_m \) (min), and gain margin (Main OSC: Stable) > 5 times compared to \( g_m \) (min).

(1) When the state of Main OSC is unstable

\[
R_L(\text{max}) = 100 \times \left( 1 + \frac{1.72}{8} \right)^2 = 148 [Ω] \quad \text{(6)}
\]

\[
g_m(\text{min}) = 148 \times (2π \times 20 \times 10^6)^2 \times 4 \times (8 \times 10^{-12})^2 \\
= 0.60 [mS] \quad \text{(7)}
\]

gain margin > \( \frac{6.53}{0.60} = 11 \text{ times compared to } g_m \text{ (min)} \) \quad \text{(8)}

Provisionally set \( \{ \text{SHTSTBY}_A, \text{AMPSEL}_A[2:0] \} = 1100b \) when gain margin (Main OSC: Unstable) > 10 times compared to gain margin (min).

(2) When the state of Main OSC is stable

When the same parameter for \( R_d \) as the state of Main OSC is unstable is used, the calculation result of the formula (7) can also be used.

gain margin > \( \frac{3.87}{0.60} = 6.5 \text{ times compared to } g_m \text{ (min)} \) \quad \text{(9)}

Provisionally set \( \{ \text{SHTSTBY}_B, \text{AMPSEL}_B[2:0] \} = 0100b \) when gain margin (Main OSC: Stable) > 5 times compared to gain margin (min).

Increase \( \text{RDSEL}_B[2:0] \) when too much gain seems to be obtained.

2.3.3.2 Calculation Example (When \( R_d \) Needs Adjustment)

When \( R_d \) needs adjustment to optimize drive level, use \( g_m', \) the converted value of \( g_m \) by the formula (10). When this adjustment is not required, skip this section and go on to Section 2.4.

\[
g_m' = \frac{g_m}{1 + g_{ds} \times R_d} \quad \text{(10)}
\]
2.4 Oscillation Characterization on Actual System

Since crystal oscillation depends on a crystal resonator or board design, perform a matching evaluation on the actual system or request a crystal resonator manufacturer to make the evaluation.

2.4.1 OPBT Settings for Matching Evaluation

It is recommended to configure OPBT settings in OSC monitor mode for matching evaluation. For mode transition, evaluation flowchart, and the correspondence between OPBT and external pins, see RH850/E2x-FCC2 User’s Manual: Hardware, 15.4.4, OSC Monitor Mode.

2.4.2 Major Matching Evaluation Parameters

Table 3 shows the major matching evaluation parameters. Inquire with a crystal resonator manufacturer about parameters, measurement methods, and target characteristics required for a crystal resonator.

<table>
<thead>
<tr>
<th>Category</th>
<th>Parameter</th>
<th>State of Main OSC</th>
<th>Target characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required characteristics for a crystal resonator</td>
<td>Oscillation frequency</td>
<td>Stable</td>
<td>Crystal resonator data sheet</td>
</tr>
<tr>
<td></td>
<td>Gain margin (oscillation margin)/Negative resistance</td>
<td>Unstable</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Stable</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td></td>
<td>3rd overtone risk check</td>
<td>Unstable</td>
<td>Check if the negative resistance of the resonator at the approximately three-times frequency is small enough for that of the resonator at the target frequency</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Stable</td>
<td></td>
</tr>
<tr>
<td>Drive level</td>
<td></td>
<td>Unstable</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Stable</td>
<td>Inquire with a crystal resonator manufacturer</td>
</tr>
<tr>
<td>Required characteristics for the MCU</td>
<td>Oscillation amplitude</td>
<td>Unstable</td>
<td>Main Osc oscillation amplitude ($V_{MOSAMP}$) *^1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Stable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Oscillation stabilization time</td>
<td>Unstable</td>
<td>Main Osc oscillation stabilization time ($t_{MSTB}$)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Stable</td>
<td></td>
</tr>
</tbody>
</table>

Note 1. See RH850/E2x-FCC2 Electrical Characteristics, User’s Manual: Hardware, 1.3.4.1, Main Oscillator Characteristics.

2.4.3 Evaluation and Adjustment of OPBT Settings

Adjust internal capacitance (configured by CAPSEL[3:0]), internal damping resistance (configured by RDSEL[2:0]), and oscillation amplifier gain (configured by SHTSTBY, AMPSEL[2:0]) to satisfy the following target characteristics of each evaluation parameter.
2.4.3.1 Oscillation Frequency

Measure the frequency \( f_L \) at which Main OSC is operating by using a frequency counter. The pin to be measured is the P20_3 pin (in OSC monitor mode).

When the oscillation frequency is different from the target frequency, adjust CAPSEL[3:0], since \( C_L \) is also different from the target value due to parasitic capacitance being different.

The formula (11) shows the correspondence between the frequency \( f_L \) and \( C_L \). Increase \( C_L \) to lower the frequency, or decrease \( C_L \) to make it higher.

\[
f_L = f_r \times \left( \frac{C_1}{2 \times (C_0 + C_L)} + 1 \right) \quad \ldots \ldots \ldots (11)
\]

\( f_r \) is defined in the formula (12).

\[
f_r = \frac{1}{2\pi \sqrt{L_1 C_1}} \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (12)
\]

2.4.3.2 Negative Resistance, Oscillation Amplitude, and 3rd Overtone Risk Check

Perform a measurement in OSC monitor mode. Insert a resistor (Rsup) in series with a crystal resonator. Obtain Rsup which can surely output the clock by turning the Main OSC OFF and ON with the P14_2 pin (STOP) and gradually increasing Rsup until the P20_3 clock output is disabled. Perform an evaluation by using both parameters when Main OSC is unstable and stable. By using the same above-mentioned procedure, measure and check if the negative resistance of the resonator at the three-times frequency is small enough for that of the resonator at the target frequency, and see if there is no risk of 3rd overtones.

![Figure 9 Schematic of Negative Resistance Measurement Circuit](image)

The negative resistance can be calculated by the formula (13).

\[-R = Rsup + R_L \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (13)\]

To decrease the negative resistance, increase RDSEL[2:0] or decrease SHTSTBY, AMPSEL[2:0]. To increase the negative resistance, decrease RDSEL[2:0] or increase SHTSTBY, AMPSEL[2:0].
This evaluation in which the clock signal is output from the P20_3 pin simultaneously enables confirmation that at this oscillation amplitude the oscillation output clock can be propagated to various circuits in the MCU.
2.4.3.3 Drive Level

Perform a measurement in OSC monitor mode. Measure the peak-to-peak voltage amplitude in the X2 pin ($V_{X2pp}$) with a low-leakage, low-capacitance probe, or measure the peak-to-peak current in a crystal resonator ($I_{pp}$) with a current probe (e.g. the P6022 by Tektronics). Perform an evaluation by using both parameters when Main OSC is unstable and stable.

![Schematic of Drive Level Measurement Circuit](image)

Drive level can be calculated by the formula (14).

$$DL = R_L \times \left(\frac{I_{pp}}{2\sqrt{2}}\right)^2 \quad \text{……………….. (14)}$$

$I_{pp}/2\sqrt{2}$ is defined in the formula (15).

$$I_{pp}/2\sqrt{2} = 2\pi f \times 2CL \times \frac{V_{X2pp}}{2\sqrt{2}} \quad \text{……………….. (15)}$$

To decrease the drive level, increase RDSEL[2:0]. To increase the drive level, decrease RDSEL[2:0].
2.4.3.4 Oscillation Stabilization Time

Perform a measurement in OSC monitor mode. When you measure the oscillation stabilization time with the P20_3 pin, the stabilization time is defined as the time from when the P14_2 (Stop) pin is turned OFF to ON to the time the clock waveforms at the target frequency are output 1,000 times. When you measure the oscillation stabilization time with the X2 pin, the stabilization time is defined as the time from when the P14_2 (Stop) pin is turned OFF to ON to the time the oscillation amplitude reaches 90%, as compared to that of the stable state. Perform an evaluation only when Main OSC is unstable.

To shorten oscillation stabilization time, increase SHTSTBY and AMPSEL[2:0] or decrease CAPSEL[3:0].
3. APPENDIX

3.1 Measurement Conditions of Trans Conductance (gm)

Trans conductance (gm) can be calculated by the measurement of trans conductance (gm) + output conductance (gds) and output conductance (gds).

3.1.1 Measurement Conditions of Trans Conductance \( (g_m) + \) Output Conductance \( (g_{ds}) \)

Figure 12 shows the measurement conditions of trance conductance (gm) + output conductance (gds).

The measurement result shows that trans conductance (gm) + output conductance (gds) can be calculated by the following formula.

\[
g_m + g_{ds} = \frac{v_g}{V_{in}} \left( 1 + \frac{R_{terminal}}{R_i} \right) \quad (16)
\]
3.1.2 Measurement Conditions of Output Conductance ($g_{ds}$)

Figure 13 shows the measurement conditions of output conductance ($g_{ds}$).

![Figure 13 Measurement Conditions of Output Conductance ($g_{ds}$)](image)

The measurement result shows that output conductance ($g_{ds}$) can be calculated by the following formula.

$$g_{ds} = \frac{v_{g} - v_{in}}{R_{i}} \quad \text{......(17)}$$
Website and Contact Information

- Renesas Electronics Website
  http://japan.renesas.com/

- Contact
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   - Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   
   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   - The state of the product is undefined at the moment when power is supplied.
   
   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   - Access to reserved addresses is prohibited.
   
   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   - After applying a reset, only release the reset line after the operating clock signal has become stable.

   When switching the clock signal during program execution, wait until the target clock signal has stabilized. When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   - Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to products of different type numbers, implement a system-evaluation test for each of the products.
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