

RH850 Series

Gateway Procedure (CAN FD Mode)

 R01AN6030EJ0100
 Rev.1.0

Summary

This document describes an example of the procedure for performing a CAN gateway using the RH850 series. For the setting of each register, refer to the notes described in the latest user's manual hardware edition.

Operation Confirmed Devices

This document applies to the RH850 series.

Please refer to Table 1-1 for the variables described in the text.

Table 1-1 Target Device and Variable

	Variable	Target MCU		
		RH850/E2x	RH850/E1M-S2	RH850/P1M-E
RS-CAN FD channel number	m	0~4	0~3	0~2
GAFLIDj, GAFLMj, GAFLP0j, GAFLP1j register numbers	j	0~15	0~15	0~15
Transmit/receive FIFO buffer number	k	0~14	0~11	0~8
Receive FIFO buffer number	x	0~7	0~7	0~7
Receive buffer number	q	0~79	0~63	0~47
Transmit buffer number	p	0~79	0~63	0~47
RAM test number	r	0~63	0~63	0~63
GAFLCFGi, GTINTSTSi register numbers	i	0	0	0
Number of each status register	y	0~2	0,1	0,1

The functions marked with ★ in the text are applicable when 2 channels or more are installed. CFD is omitted from the register names in the text.

Contents

1. Gateway Function	3
2. Gateway Operation	4
3. CAN-CAN FD Gateway (Only in CAN FD Mode)	12
4. CAN-related Interrupt Processing	13
5. Precautions for Processing Flow	14

1. Gateway Function

The functions available when using CAN gateway are shown below. For details of each processing, refer to the following chapters.

- Gateway operation
- Transmit abort function
- Interval transmission function gateway operation
- Interrupt processing of transmit/receive FIFO buffer (gateway mode)

2. Gateway Operation

When the transmit/receive FIFO buffer is set to gateway mode, the received message can be sent from any channel without going through the CPU.

When the transmit/receive FIFO buffer with the CFM [1: 0] bit of the CFCCk register set to "10_B" (gateway mode) is selected with the GAFLP1j register, the messages that have passed the receive rule filter processing are stored in the specified transmit/receive FIFO buffer and are automatically transmitted from the buffer..

The transmit/receive FIFO buffer is transmitted in order from the first stored message. In addition, priority determination is performed only for the next message to be transmitted in the transmit/receive FIFO buffer.

In gateway mode, you cannot read or write to the transmit/receive FIFO buffer, but you can check the message transmitted from the transmit/receive FIFO buffer in gateway mode by using the mirror function.

For the configuration settings for using the transmit/receive FIFO buffer in gateway mode, refer to "CAN Configuration Application Note".

Figure 2-1 shows an example of the operation of the transmit/receive FIFO buffer in gateway mode.

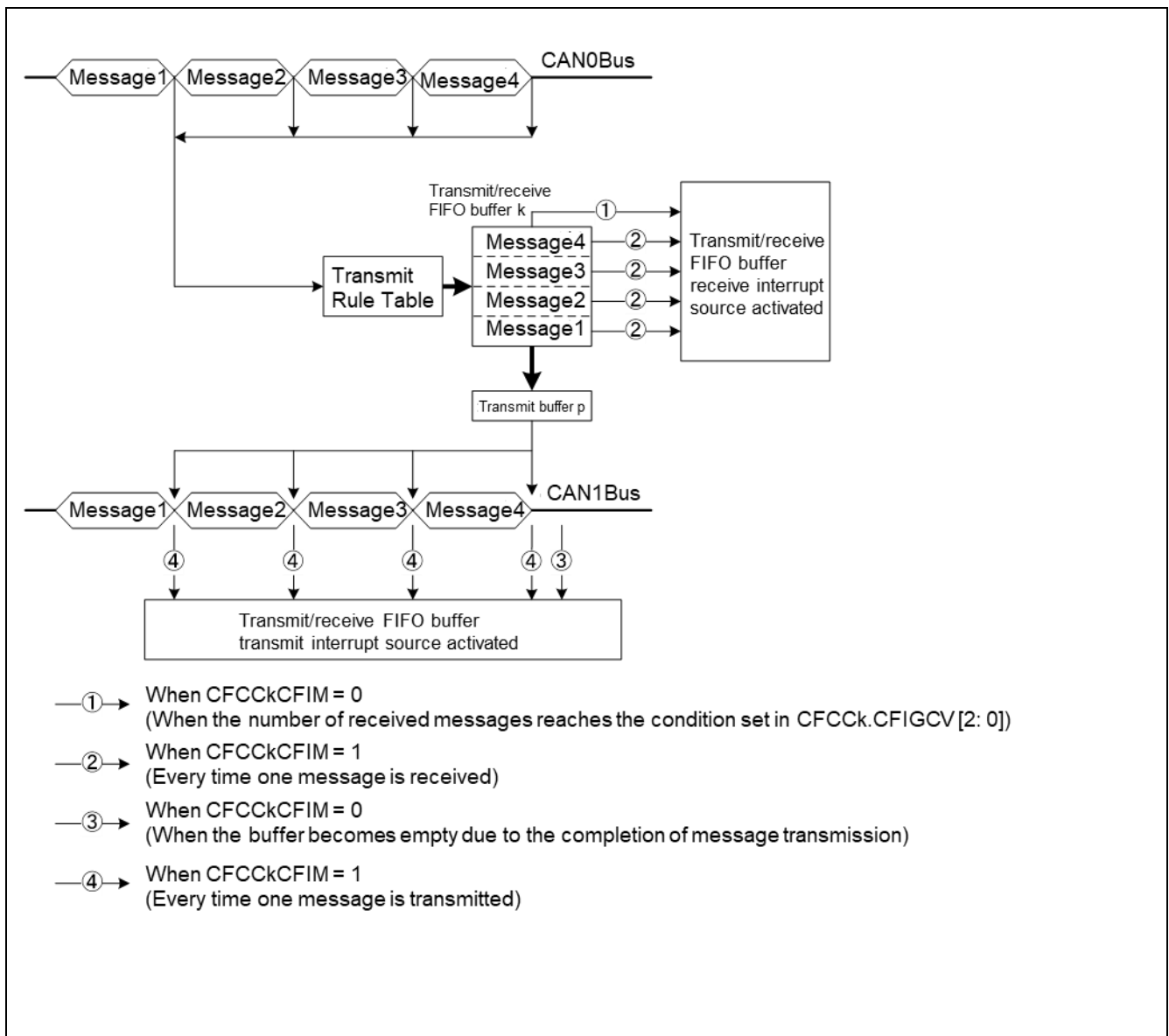


Figure 2-1 Operation Example of Transmit/Receive FIFO Buffer (Gateway Mode)

2.1 Gateway Procedure in Transmit/Receive FIFO Buffer

In gateway mode, messages are transmitted and received automatically within the RS-CANFD module, so there is no need to perform the transmit/receive processing with the program.

Figures 2-2 and 2-3 show the procedure for enabling and prohibiting the transmit/receive FIFO buffer.

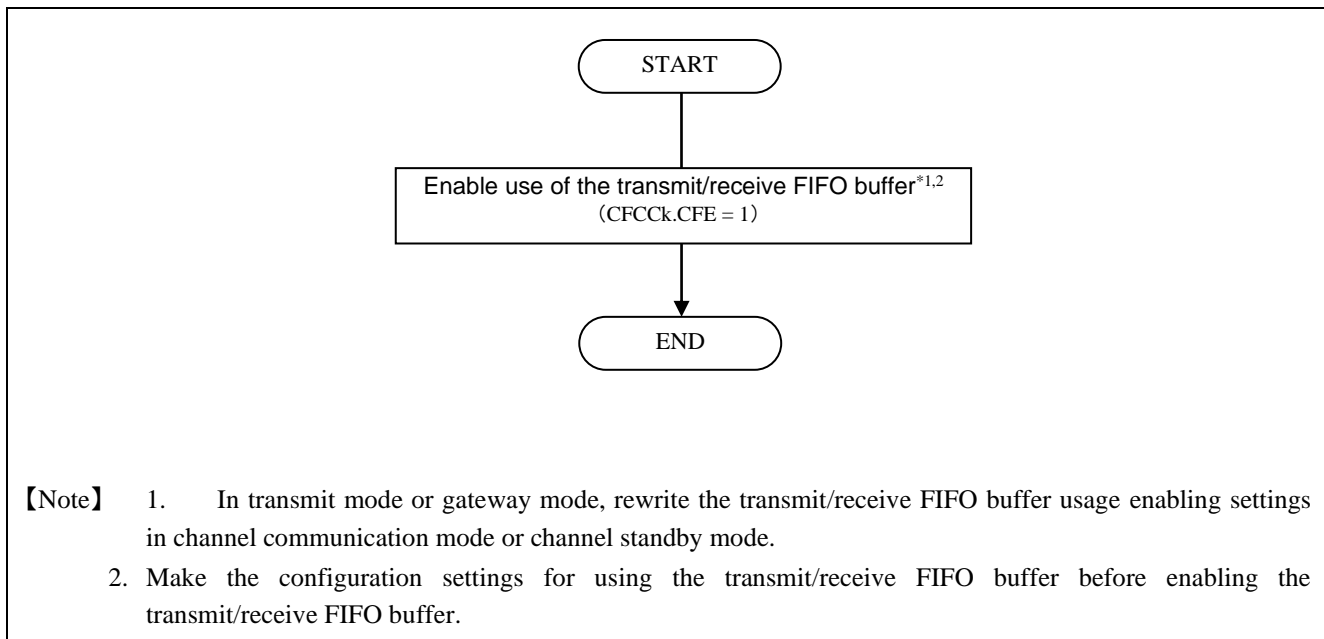


Figure 2-2 Procedure for Enabling Transmit/Receive FIFO Buffer

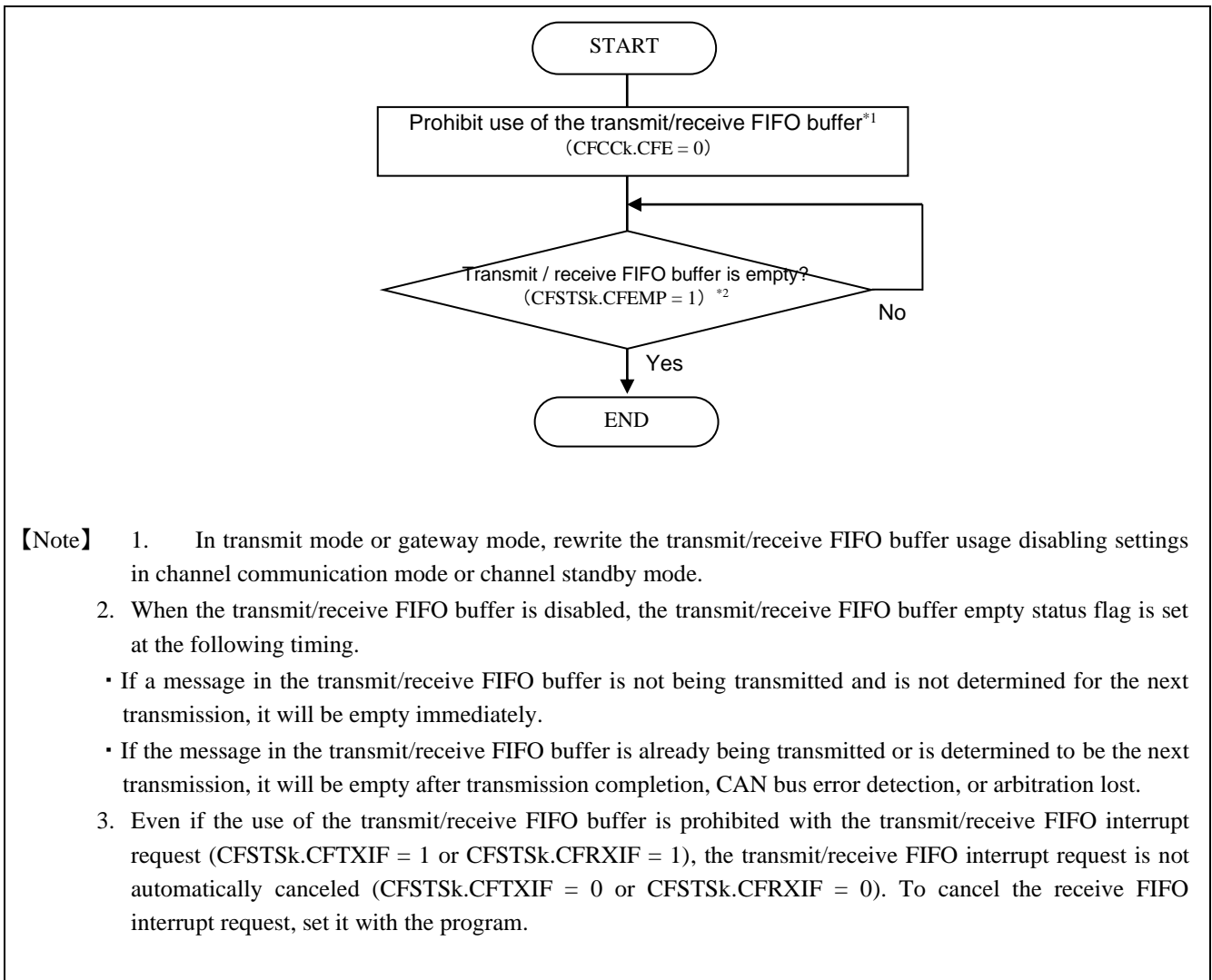


Figure 2-3 Procedure for Prohibiting Transmit/Receive FIFO Buffer

2.2 Transmit Abort Function

By disabling the transmit/receive FIFO buffer (CFCCk.CFE = 0), all messages in the transmit/receive FIFO buffer are lost, and the transmit/receive FIFO buffer empty status flag in the transmit/receive FIFO buffer status register is set to "1" (CFSTSk.CFEMP = 1). "1" is set in the transmit/receive FIFO buffer empty status flag at the following timing. Note that no message is stored in the transmit/receive FIFO buffer when the use of the transmit/receive FIFO buffer is prohibited.

- If a message in the transmit/receive FIFO buffer is not being transmitted and is not determined for the next transmission, it will be empty immediately.
- If the message in the transmit/receive FIFO buffer is already being transmitted or is determined to be the next transmission, it will be empty after transmission completion, CAN bus error detection, or arbitration lost.

No interrupt is generated when the transmit abort of the transmit/receive FIFO buffer is completed. However, if aborted during transmission, a CANm transmit/receive FIFO transmission completion interrupt may occur due to transmission completion. For details, refer to "CAN Transmission Procedure Application Note".

For the transmit abort procedure of the transmit/receive FIFO buffer, refer to "Figure 2-3 Procedure for Prohibiting Transmit/Receive FIFO Buffer".

2.3 Interval Transmission Function

To transmit messages continuously from the same transmit/receive FIFO buffer that is set to transmit mode or gateway mode, message transmission interval time can be set.

After the transmit/receive FIFO buffer is enabled (CFCCk.CFE = 1) and the first message is successfully sent from the transmit/receive FIFO buffer, the interval timer starts counting (after the 7th bit of the CAN protocol EOF). After that, when the interval time elapses, the following message is sent and the interval timer is reset. The timing at which the interval timer stops is shown below.

- When the use of the transmit/receive FIFO buffer is prohibited (CFCCk.CFE = 0)
- When transitioning to channel reset mode

Table 2-1 shows the count source of the interval timer and the calculation formula of the interval timer, Figure 2-4 shows the block diagram of the interval timer, and Figure 2-5 shows the operation example of the interval timer.

Table 2-1 Interval Timer Count Source and Calculation Formula

CFCCk		Count Source	Interval Timer Calculation Formula*
CFITR	CFITSS		
0	0	Clock obtained by dividing pclk/2 by the value of the ITRCP [15: 0] bit of the GCFG register	$1/f_{PBA} \times 2 \times M \times N$
1	0	Clock obtained by dividing pclk/2 by the value of the ITRCP [15: 0] bits of the GCFG register x 10.	$1/f_{PBA} \times 2 \times M \times 10 \times N$
-	1	Normal CANm bit time clock	$1/f_{CANBIT} \times N$

【Note】 M: Divided value of the clock source of the interval timer for FIFO (set value of GCFG.ITRCP [15: 0])
 N: Message transmission interval (set value of CFCCk.CFITTT [7: 0])
 f_{PBA} : pclk frequency
 f_{CANBIT} : Normal CANm bit time clock frequency

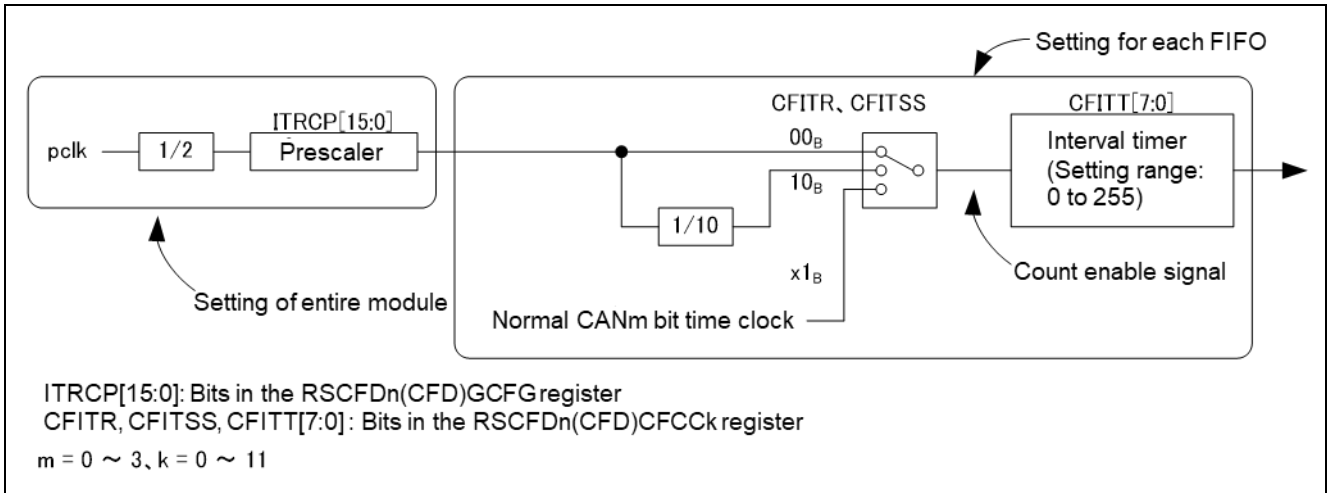


Figure 2-4 Block Diagram of the Interval Timer

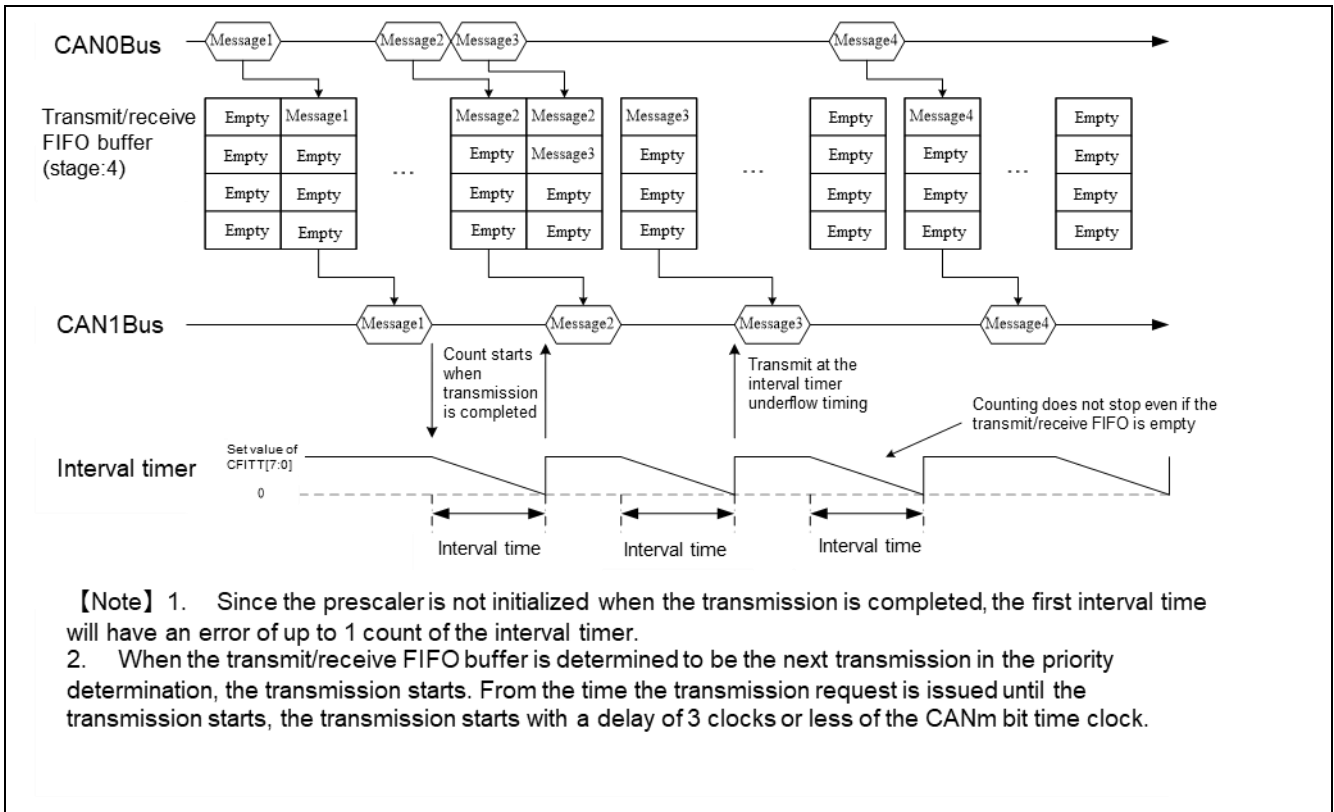


Figure 2-5 Interval Transmission Operation Example (Gateway Mode)

2.4 Transmit/Receive FIFO Buffer Interrupt Processing (Gateway Mode)

2.4.1 Transmit/Receive FIFO Receive Interrupt Processing

If the transmit/receive FIFO receive interrupt is enabled, the transmit/receive FIFO receive interrupt occurs when the condition selected by the CFIM bit of the CFCCk register is satisfied.

Even if the use of the transmit/receive FIFO buffer is set to be prohibited (CFCCk.CFE=0) while the transmit/receive FIFO receive interrupt request is being generated (CFSTSk.CFRXIF=1), the transmit / receive FIFO receive interrupt request is not automatically canceled (CFSTSk.CFRXIF=0). When canceling the transmit/receive FIFO receive interrupt request, please set it with the program.

Whether to enable or disable the transmit/receive FIFO receive interrupt can be set for each transmit/receive FIFO buffer by the CFRXIE bit of the CFCCk register.

The transmit/receive FIFO receive interrupt request generation condition can be selected for each transmit/receive FIFO buffer by the CFIM bit and CFIGCV bit of the CFCCk register.

Table 2-2 summarizes the sources of transmit/receive FIFO receive interrupt in gateway mode.

Table 2-2 Transmit/Receive FIFO Receive Interrupt Source

CFCCk		FIFO receive interrupt request generation condition	How to clear the interrupt request
CFIM	CFIGCV		
1	-	Every time one message is received	Write "0" to the CFRXIF bit of the CFSTSk register
0	000*	When a message is stored up to 1/8 in the FIFO buffer	
	001	When a message is stored up to 2/8 in the FIFO buffer	
	010*	When a message is stored up to 3/8 in the FIFO buffer	
	011	When a message is stored up to 4/8 in the FIFO buffer	
	100*	When a message is stored up to 5/8 in the FIFO buffer	
	101	When a message is stored up to 6/8 in the FIFO buffer	
	110*	When a message is stored up to 7/8 in the FIFO buffer	
	111	When the FIFO buffer is full	

* Set the number of transmit/receive FIFO buffers to 4 messages

If set to (CFCCk.CFDC [2: 0] = 001), selection is prohibited.

2.4.2 Transmit/Receive FIFO Transmit Interrupt Processing

If the transmit/receive FIFO transmit interrupt is enabled, the transmit/receive FIFO transmit interrupt occurs when the condition selected by the CFIM bit of the CFCCk register is satisfied.

Even if the use of the transmit/receive FIFO buffer is set to be prohibited (CFCCk.CFE=0) while the transmit/receive FIFO receive interrupt request is being generated (CFSTSk.CFRXIF=1), the transmit/receive FIFO transmit interrupt request is not automatically canceled (CFSTSk.CFRXIF=0). When canceling the transmit/receive FIFO transmit interrupt request, please set it with the program.

Whether to enable or disable the transmit/receive FIFO transmit interrupt can be set for each transmit/receive FIFO buffer by the CFRXIE bit of the CFCCk register.

The transmit/receive FIFO transmit interrupt request generation condition can be selected for each transmit/receive FIFO buffer by the CFIM bit and FIGCV bit of the CFCCk register.

Table 2-3 summarizes the sources of transmit/receive FIFO transmit interrupt in gateway mode.

Table 2-3 Transmit/Receive FIFO Transmit Interrupt Source

CFIM	FIFO transmit interrupt request generation condition	How to clear the interrupt request
1	Every time one message is transmitted	Write "0" to the CFTXI bit of the CFSTSk register
0	When the buffer becomes empty due to the completion of message transmission	

2.4.3 Global Error Interrupt Processing

By enabling the FIFO message lost interrupt, a global error interrupt is generated when the message lost in the transmit/receive FIFO buffer is detected. Whether to enable or disable the FIFO message lost interrupt can be set in common for the entire module with the MEIE bit of the GCTR register.

Table 2-4 summarizes the sources of global error interrupt.

Table 2-4 Global Error Interrupt Source

Global error interrupt request generation condition	How to clear the interrupt request
When a message lost in the transmit/receive FIFO buffer is detected	Write "0" to the CFMLT bit of the CFSTSk register*1

*1 Multiple interrupt factors can be selected for global error interrupts.

Clear the following flags to "0" according to the interrupt factor that occurred.

- Transmit history buffer overflow:

GERFL register THLES bit (THLSTSm register THLELT bit of all channels)

- DLC error: GCTR register DEIE bit

3. CAN-CAN FD Gateway (Only in CAN FD Mode)

When using the gateway function in CAN FD mode, the frame to be transmitted can be replaced with a classical CAN frame or a CAN FD frame.

Setting the GWEN bit of the FDCFG register to “1” enables the CAN-CAN FD gateway. You can select the FDF bit and BRS bit of the transmit frame with the GWFDF bit and GWBRS bit of the FDCFG register. If the DLC value of the received CAN frame is “1001B” or higher and the GWFDF bit is “1” (CAN FD frame), the DLC is replaced with “1000B”.

Do not route the following frames when the CAN-CAN FD gateway is enabled.

- CAN FD frame with payload length greater than 8 bytes
- Remote frame

Also, when the CAN-CAN FD gateway is enabled, transmit only the following frames from the corresponding channel according to the GWFDF settings.

- GWFDF = 0 : Transmit the received frame as a classical CAN frame
- GWFDF = 1 : Transmit the received frame as a CAN FD frame

4. CAN-related Interrupt Processing

When using interrupts, the interrupt source flag must be cleared to "0".

Figure 4-1 shows how to clear the interrupt source flag to "0" in interrupt processing.

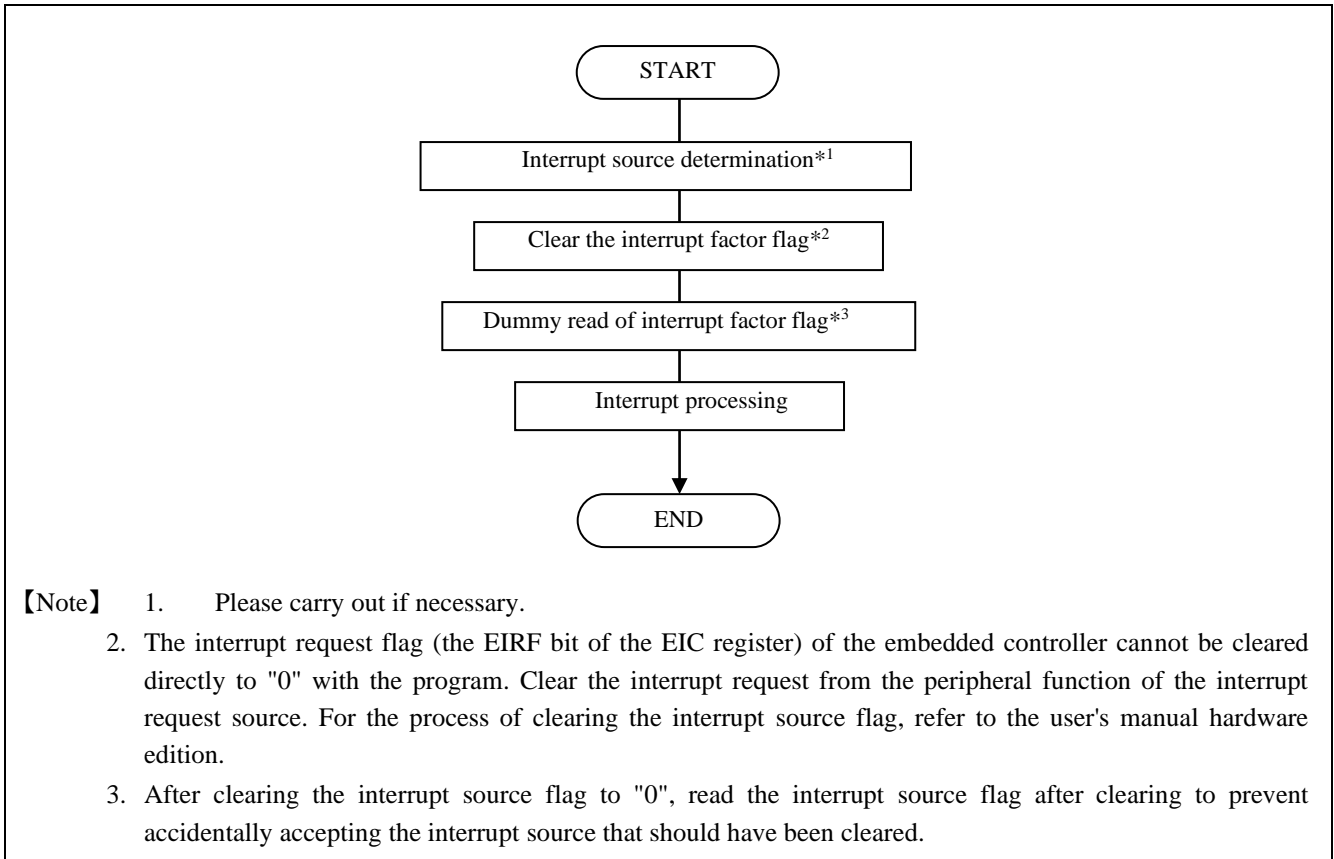


Figure 4-1 CAN-related Interrupt Processing Procedure

5. Precautions for Processing Flow

5.1 About Functions

In this application note, there is a part that is functionalized even in the processing of single line, but this is only described as a function to clarify the processing for each function. When you actually create a program, you don't necessarily have to make it functional.

5.2 Settings for Each Channel, FIFO, and Buffer

In this application note, even if processing is required for each channel, FIFO, or buffer, only one processing is described. When actually creating a program, perform multiple processes as necessary.

5.3 Infinite Loop

To simplify the notation, there are some infinite loops in the processing flow. When actually creating a program, give each loop a time limit so that it can be exited during overtime. Figure 5-1 shows an example of processing with a loop time limit.

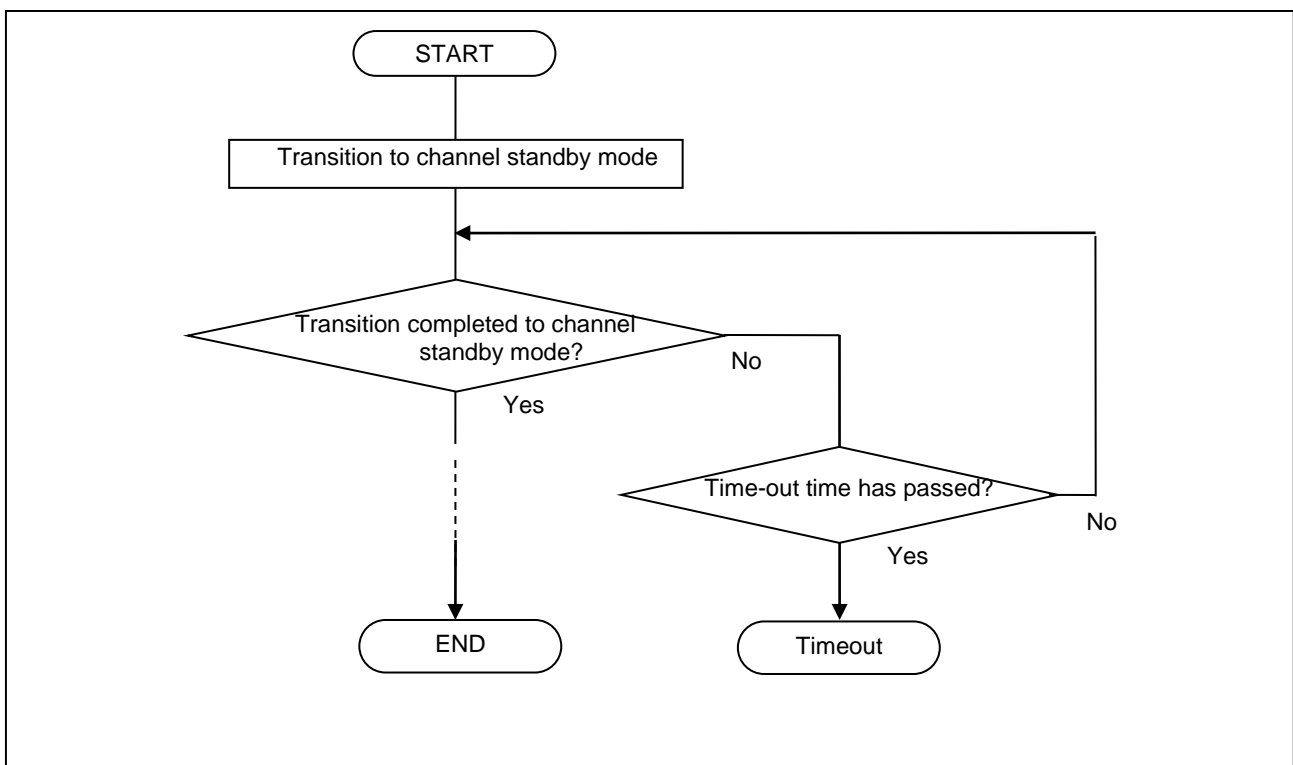


Figure 5-1 Example of Processing with Loop Time Limit

Our Company's Website and Inquiry

Website

<http://japan.renesas.com/>

Inquiry

<http://japan.renesas.com/contact/>

All trademarks and registered trademarks are the property of their respective owners.

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	2017.5.10	—	Initial edition

Precautions for use of the product

This section describes the "Precautions" that apply to all microcontroller products. Please refer to this document and the Technical Update for precautions on individual products.

1. Treatment of unused pins

[Caution] Please dispose of unused pins according to "Handling of unused pins" in the text.

The impedance of the input pins of CMOS products is generally high impedance. If the unused pins are operated in an open state, noise around the LSI may be applied due to the induction phenomenon, a through current may flow inside the LSI, or it may be recognized as an input signal and malfunction may occur. Dispose of unused pins according to the instructions given in "Disposal of unused pins" in the text.

2. Treatment at power-on

[Caution] The state of the product is undefined when the power is turned on.

When the power is turned on, the state of the internal circuits of the LSI is indeterminate and the state of register settings and pins is undefined.

For products that are reset using the external reset pin, the pin state cannot be guaranteed from the time the power is supplied until the reset becomes valid.

Similarly, in the case of products that are reset using the built-in power-on reset function, the pin states cannot be guaranteed from the time the power is turned on until the voltage reaches a certain level.

3. Prohibition of Access to Reserved Addresses

[Caution] Access to reserved addresses is prohibited.

The address area has a reserved address allocated for future function expansion. The operation when these addresses are accessed cannot be guaranteed, so do not access them.

4. About clock

[Caution] When resetting, release the reset after the clock has stabilized.

When switching the clock during program execution, switch the clock after the switching destination clock is stable.

In a system that starts operating with a clock that uses an external oscillator (or external oscillator circuit) at reset, release the reset after the clock is sufficiently stable. Also, when switching to a clock that uses an external oscillator (or external oscillator circuit) in the middle of a program, make sure that the clock to be switched to is sufficiently stable before switching.

5. Differences between products

[Caution] When changing to a product with a different model name, perform a system evaluation test for each product model name.

Even if the MCUs in the same group have different model numbers, the characteristic values, operating margins, noise immunity, noise radiation, etc. may differ within the range of electrical characteristics due to differences in internal ROM and layout patterns. When changing to a product with a different model name, perform a system evaluation test for each individual product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
 2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
 4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
 5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.), traffic control (traffic lights), large-scale communication equipment, key financial terminal systems, safety control equipment, etc.
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations, etc.), or may cause serious property damage (space system, undersea repeaters, nuclear power control systems, aircraft control systems, key plant systems, military equipment, etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
 6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
 7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
 8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
 9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
 10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
 11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
 12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note 2) "Renesas Electronics products" means any product developed or manufactured by or for Renesas Electronics.

(Rev. 4.0-1, November 2017)



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com>" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No. 27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya 4, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No. 777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAM CO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338