RH850 Series

R01AN6028EJ0100
Rev.1.0

CAN Receive Procedure (CAN FD Mode)

Summary

This document describes an example of a procedure for receiving CAN using the RH850 series. Please refer to the notes in the latest user's manual hardware edition for the settings of each register.

Operation Confirmed Devices

This document applies to the RH850 series.

The variables described in the text are as follows.

Table 1-1 Target Devices and Variables

	Variable	Target MCU		
		RH850/E2x	RH850/E1M-S2	RH850/P1M-E
RS-CAN FD channel number	m	0~4	0~3	0~2
GAFLIDj, GAFLMj, GAFLP0j, GAFLP1j Register numbers	j	0~15	0~15	0~15
Transmit/Receive FIFO buffer number	k	0~14	0~11	0~8
Receive FIFO buffer number	x	0~7	0~7	0~7
Receive buffer number	q	0~79	0~63	0~47
Transmit buffer number	p	0~79	0~63	0~47
RAM test number	r	0~63	0~63	0~63
GAFLCFGi、GTINTSTSi register number	i	0	0	0
Number of each status register	y	0~2	0,1	0,1

The functions marked with "★" in the text are applicable to cases where 2 or more channels are installed.

In the text, CFD is omitted from the register names.

Contents

1. Receive Function

The functions that can be used when receiving CAN messages are shown below. For details on each process, refer to the following chapters.

- ・Receive using the receive buffer
- ・Receive using the receive FIFO buffer
- ・Receive using the transmit / receive FIFO buffer

2. Receive Using Receive Buffers

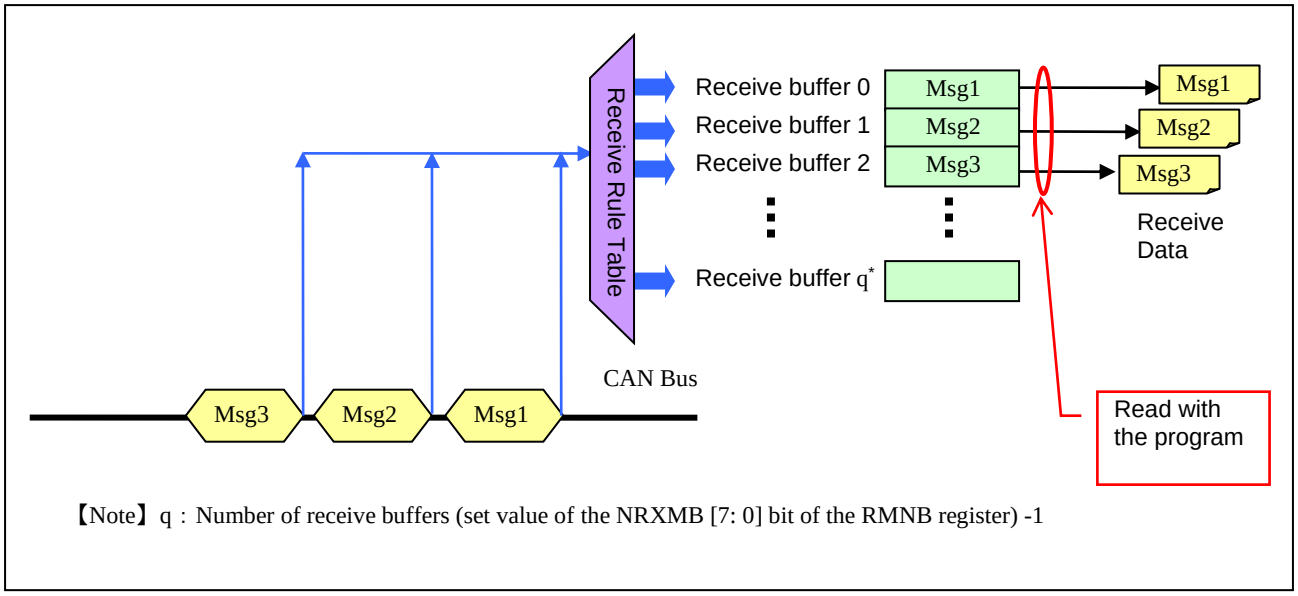
Receive buffer q shared by all channels is available. Since the message stored in the receive buffer with the same number is overwritten, the latest received data can be read.

If it is received in the receive buffer, no interrupt is generated.

When the process of storing the received message in the receive buffer starts, the receive buffer q becomes "new message" (the RMNSq flag in the RMNDy register becomes "1"). Received data information can be read from the RMIDq register, RMPTRq register, and RMDFb_q register (b = 0 to 4). The payload size that can be received by the receive buffer is up to 20 bytes. You must use the receive or transmit / receive FIFO to receive messages exceeding 20 bytes.

For the configuration settings for using the receive buffer, refer to "CAN Configuration Application Note".

Figure 2-1 shows the operation of the receive buffer.

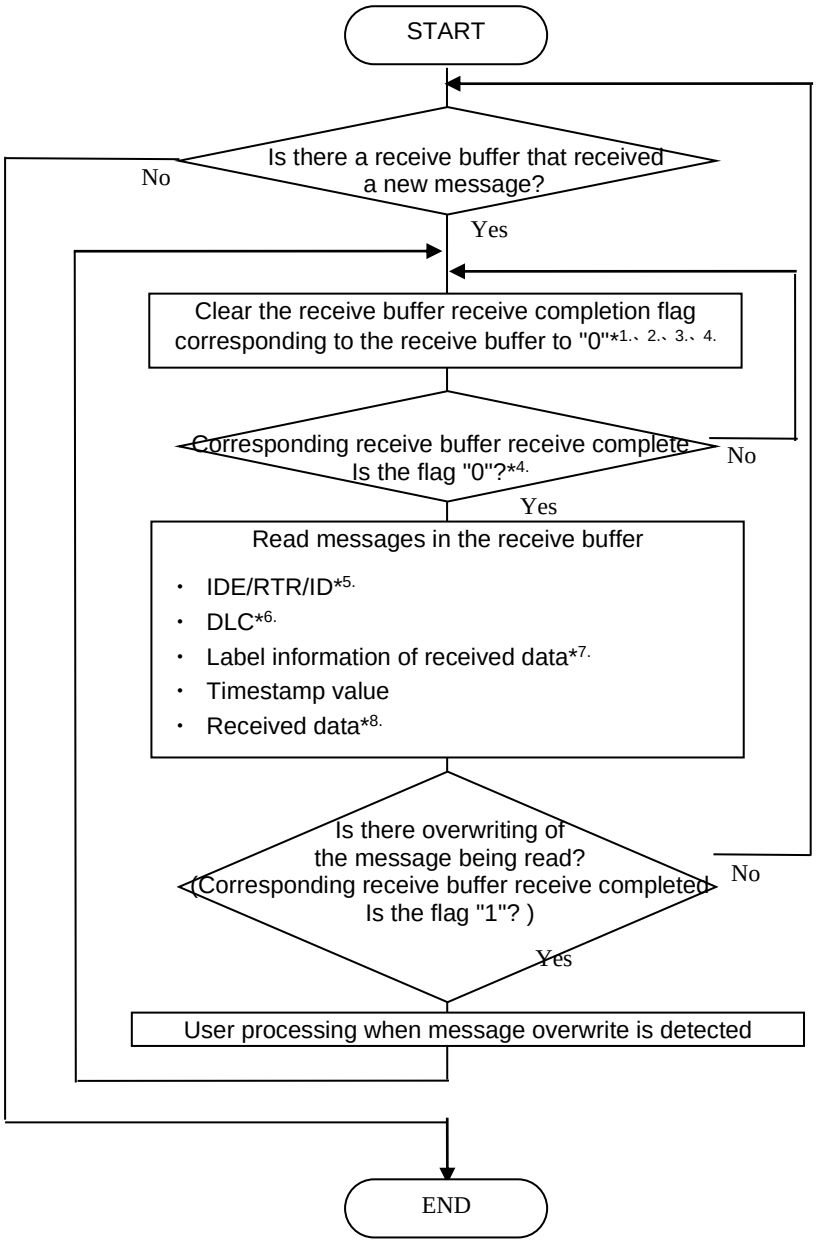


【Note】q：Number of receive buffers (set value of the NRXMB [7: 0] bit of the RMNB register) -1

Figure 2-1 Receive Buffer Operation

2.1 Receive Buffer Read Procedure

Figure 2-2 shows the procedure for reading the receive buffer.



【Note】 1. Write “0” for the RMNSq flag in the RMNDy register in global operation mode or global test mode.

2. To set the RMNSq flag to “0”, write “0” with the program.
3. To write "0" in the RMNSq flag, use the store instruction to write "0" in the bit you want to set to "0" and "1" in the other bits.
4. The RMNSq flag cannot be set to “0” while the message is being stored. The time to store a message depends on the size of the payload stored in the receive buffer.
5. For a standard ID, read b10 to b0 of the ID (the RMID [28: 0] bit of the RMIDq register). “0” can be read for b28 to b11.

6. If DLC replacement is enabled after filtering by the reception rule (the DCE bit of the GCFG register is “1”, DRE bit is “1”), the received message matches the DLC set value in the reception rule table (the GAFLDLC[3:0] bit of the GAFLP0_j register) that matches the received message is stored. Otherwise, the DLC value of the received message is stored.
7. After filtering by the receive rule, the set value of the label of the receive rule table (the GAFLPTR [11: 0] bit of the GAFLP0_j register) that matches the received message is stored.
8. If the DLC of the received message (the value of the RMPLC [3: 0] bit of the RMPTRq register) is less than the payload storage size of the receive buffer, “H'00” can be read for the data byte (RMDFb_q register) for which no data is set.

Figure 2-2 Receive Buffer Read Procedure

3. Receive Using Receive FIFO Buffers

There are 8 receive FIFO buffers shared by all channels. Messages can be stored in each receive FIFO buffer for the number of buffers.

When a received message is stored in the receive FIFO buffer, the value of the corresponding message count display counter (the RFMC [7: 0] bit of the RFSTSx register) is incremented.

Received messages can be read from the RFIDx register, RFPTRx register, RFFDSTSx register, and RFDFd_x register (d = 0 to 15). The receive FIFO buffer can be read from the oldest message.

When the value of the message count display counter matches the buffer value of the FIFO buffer (the value set by the RFCCx register RFDC [2: 0] bit), the receive FIFO buffer becomes full (the RFFLL flag in the RFSTSx register is “1”). When all messages are read from the receive FIFO buffer, the receive FIFO buffer becomes empty (the RFEMP flag in the RFSTSx register is “1”).

Refer to the CAN Configuration Application Note for configuration settings to use the receive FIFO buffer.

Figure 3-1 shows the operation of the receive FIFO buffer.

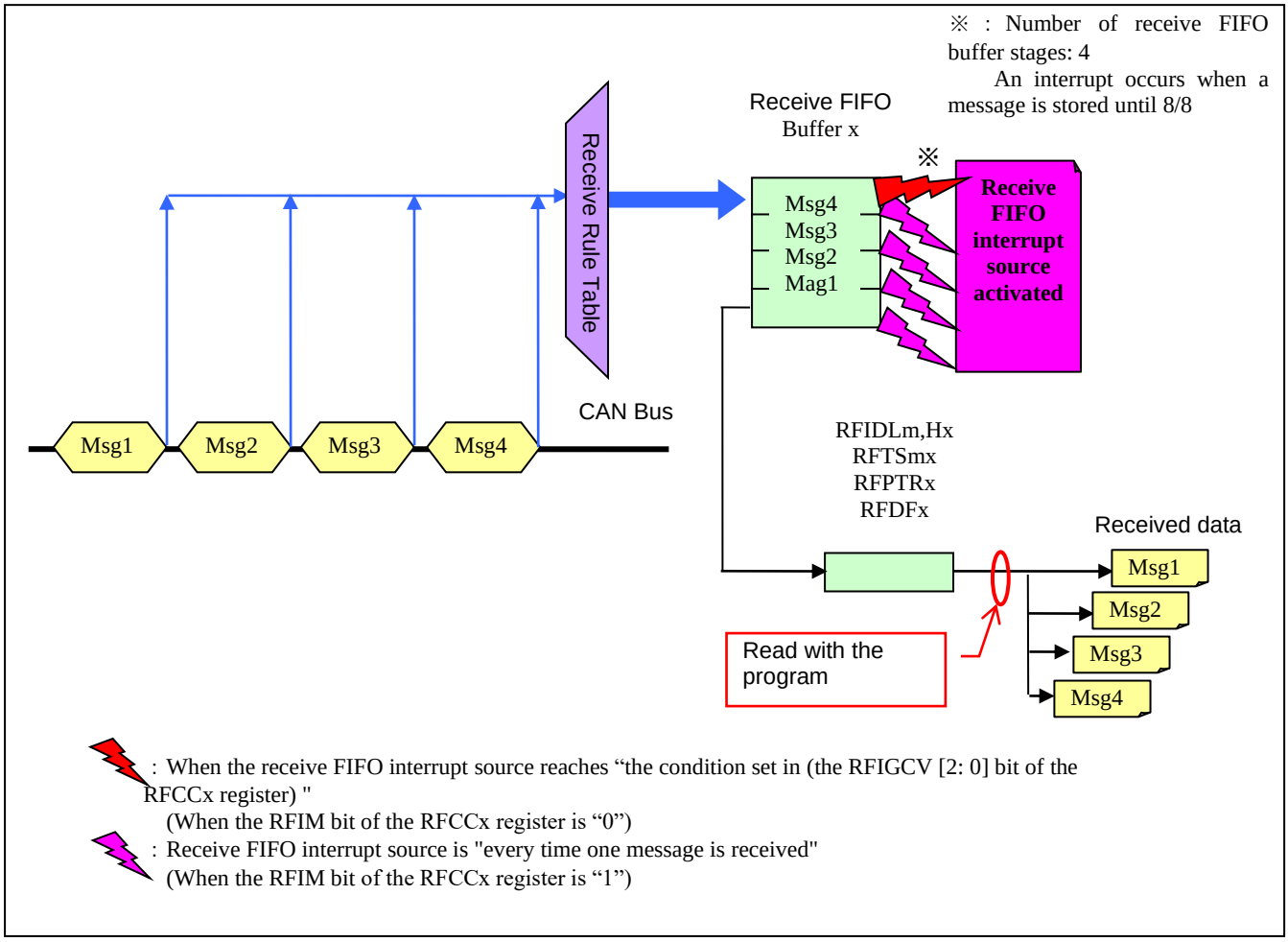
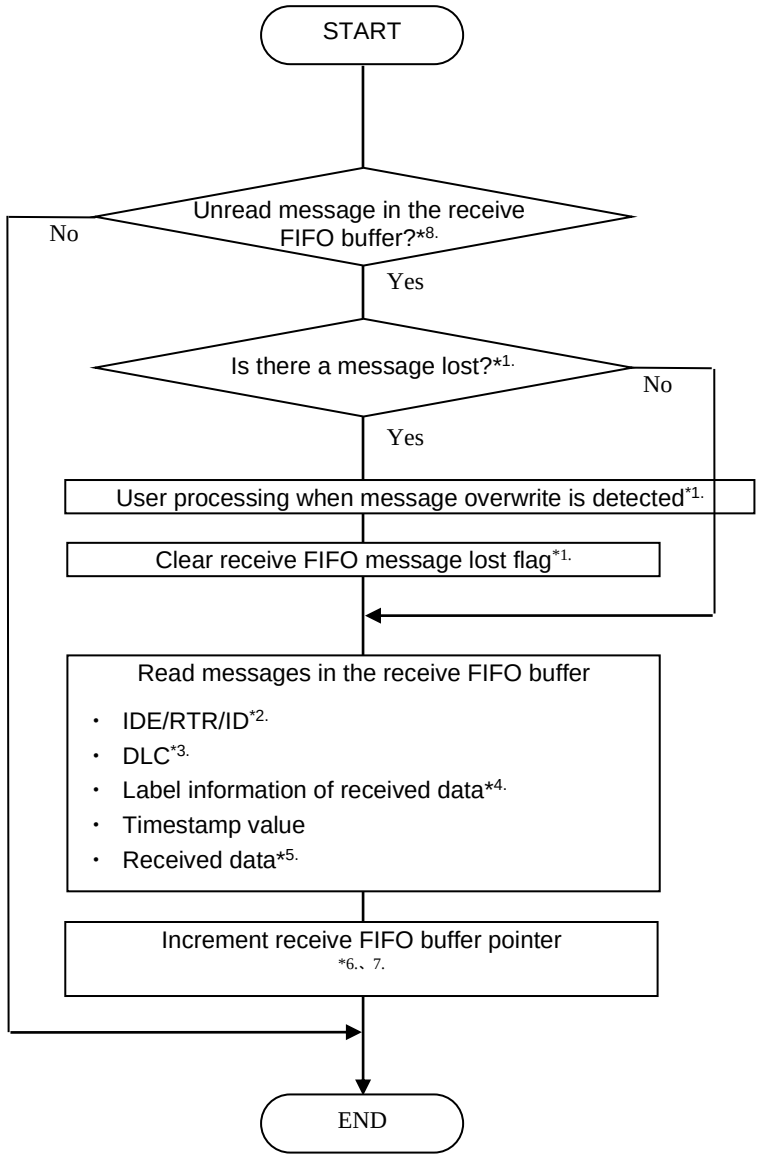


Figure 3-1 Receive FIFO Buffer Operation

3.1 Receive FIFO Buffer Read Procedure

Figure 3-2 shows the procedure for reading the receive FIFO buffer, and Figure 3-3 and Figure 3-4 show the procedure for enabling and prohibiting the use of the receive FIFO buffer.

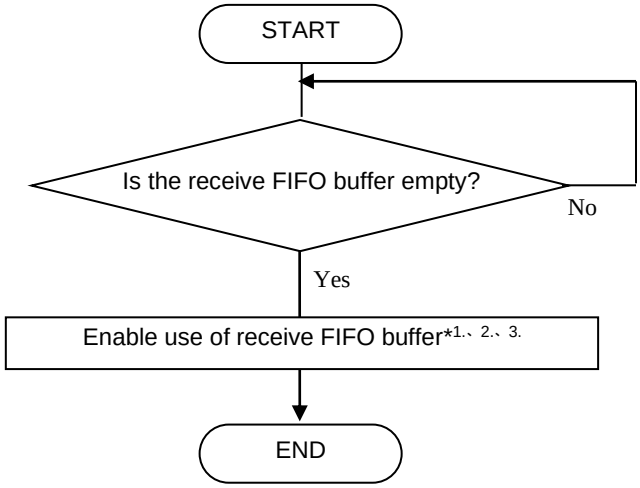


【Note】 1. If the FIFO message lost interrupt is enabled, execute it in the global error interrupt processing.

2. For standard ID, read b10-b0 of ID (the RFID [28: 0] bit of the RFIDx register). “0” can be read for b28-b11.
3. If DLC replacement is enabled after filtering by the reception rule (the DCE bit of the GCFG register is “1”, DRE bit is “1”), the DLC set value in the reception rule table (the GAFLDLC[3:0] bit of the GAFLP0_j register) that matches the received message is stored. Otherwise, the DLC value of the received message is stored.
4. After filtering by the reception rule, the set value of the receive rule table label (the GAFLPTR [11: 0] bit of GAFLP0_j) that matches the received message is stored.

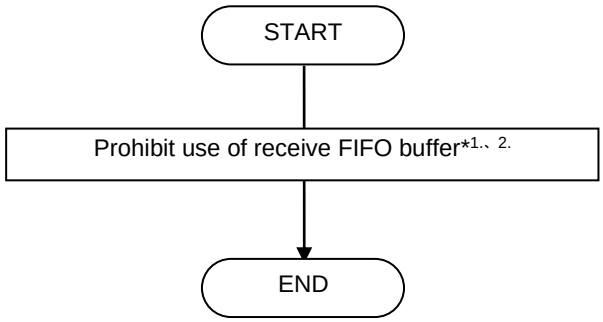
5. If the DLC of the received message (value of the RFDLC [3: 0] bit of the RFPTRx register) is less than the payload storage size of the receive FIFO buffer, "H'00" can be read for the data byte (RFDFb_x register) for which no data is set.
6. After reading the messages in the receive FIFO buffer (RFIDx register, RFPTRx register, RFDFb_x register), increment the pointer (write "H'FF" to the RFCC [7: 0] bit of the RFIDCTRx register).
7. Increment the pointer when the receive FIFO buffer is used (the RFE bit of the RFCCx register is “1”) and there are unread messages in the receive FIFO buffer (the RFEMP flag in the RFSTSx register is “0”).
8. When reading all the unread messages in the receive FIFO buffer, use a loop statement or the like to read until the buffer is empty.

Figure 3-2 Receive FIFO Buffer Read Procedure (no interrupt used)



【Note】 1. Rewrite to enable/disable the receive FIFO buffer (the RFE bit of the RFCCx register) in the global operation mode or global test mode.
2. Make the configuration settings for using the receive FIFO buffer, and then enable the use of the receive FIFO buffer (the RFE bit is "1").
3. If the number of receive FIFO buffers is set to “0” (“B’000” in the RFDC [2: 0] bit of the RFCCx register), do not allow the receive FIFO buffer to be used.

Figure 3-3 Procedure to Enable Receive FIFO Buffer Use



【Note】 1. Rewrite to enable/disable the receive FIFO buffer (the RFE bit of the RFCCx register) in the global operation mode or global test mode.
2. Even if the use of the receive FIFO buffer is prohibited (the RFE bit is “0”) while an interrupt request is generated (the RFIF flag in the RFSTSx register is “1”), the interrupt request flag (RFIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Figure 3-4 Procedure to Prohibit Receive FIFO Buffer Use

3.2 Receive FIFO Interrupt Processing

3.2.1 Receive FIFO Interrupt Processing

If the receive FIFO interrupt is enabled, the receive FIFO interrupt is generated when the condition selected in the RFIM bit setting of the RFCCx register is satisfied.

Even if the use of the receive FIFO buffer is prohibited (RFE bit is “0”) while an interrupt request is generated (the RFIF flag in the RFSTSx register is “1”), the interrupt request flag (RFIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Whether to enable or disable receive FIFO interrupts can be set for each receive FIFO buffer using the RFIE bit of the RFCCx register. The sources of receive FIFO interrupts are shown below.

A receive FIFO interrupt request is generated when the condition set by the RFIGCV [2: 0] bit of the RFCCx register is reached (the RFIM bit of the RFCCx register is "0").

RFIGCV[2:0] bit settings

- When a message is stored up to 1/8 in the receive FIFO buffer*1
- When a message is stored up to 2/8 in the receive FIFO buffer
- When a message is stored up to 3/8 in the receive FIFO buffer*1
- When a message is stored up to 4/8 in the receive FIFO buffer
- When a message is stored up to 5/8 in the receive FIFO buffer*1
- When a message is stored up to 6/8 in the receive FIFO buffer
- When a message is stored up to 7/8 in the receive FIFO buffer*1
- When the receive FIFO buffer is full

— Receive FIFO interrupt request occurs every time message reception is completed (the RFIM bit of RFCCx register is “1”)

【Note】 1. Do not set if the number of receive FIFO buffers is set to 4 messages (the RFDC [2: 0] bit of the RFCCx register is set to "B'001").

3.2.2 Global Error Interrupt Processing

If the FIFO message lost interrupt is enabled, a global error interrupt is generated when a message lost in the receive FIFO buffer is detected. Whether to enable or disable the FIFO message lost interrupt can be set in common for the entire module with the MEIE bit of the GCTR register.

4. Receive Using Transmit/Receive FIFO Buffers

The transmit/receive FIFO buffer can be used in receive mode, transmit mode, or gateway mode (only receive mode is described in this chapter).

There are 3 transmit/receive FIFO buffers per channel dedicated to each channel. The transmit/receive FIFO buffer set to receive mode can store as many messages as the number of buffers, just like the receive FIFO buffer.

When a received message is stored in the transmit/receive FIFO buffer set to receive mode, the value of the corresponding message count display counter (the CFMC [7: 0] bit of the CFSTSk register) is incremented.

Received messages can be read from the CFIDk register, CFPTRk register, and CFDFd_k register (d = 0 to 15). The transmit/receive FIFO buffer can be read from the oldest message.

When the value of the message count display counter matches the buffer value of the transmit/receive FIFO buffer (the value set by the CFDC [2: 0] bit of the CFCCk register), the transmit/receive FIFO buffer becomes full (the CFFLL flag in the CFSTsk register is “1”).

When all messages are read from the transmit/receive FIFO buffer, the transmit/receive FIFO buffer becomes empty (the CFEMP flag in the CFSTSk register is “1”).

For the configuration settings for using the transmit/receive FIFO buffer, refer to "CAN Configuration Application Note".

Figure 4-1 shows the receive operation of the transmit/receive FIFO buffer.

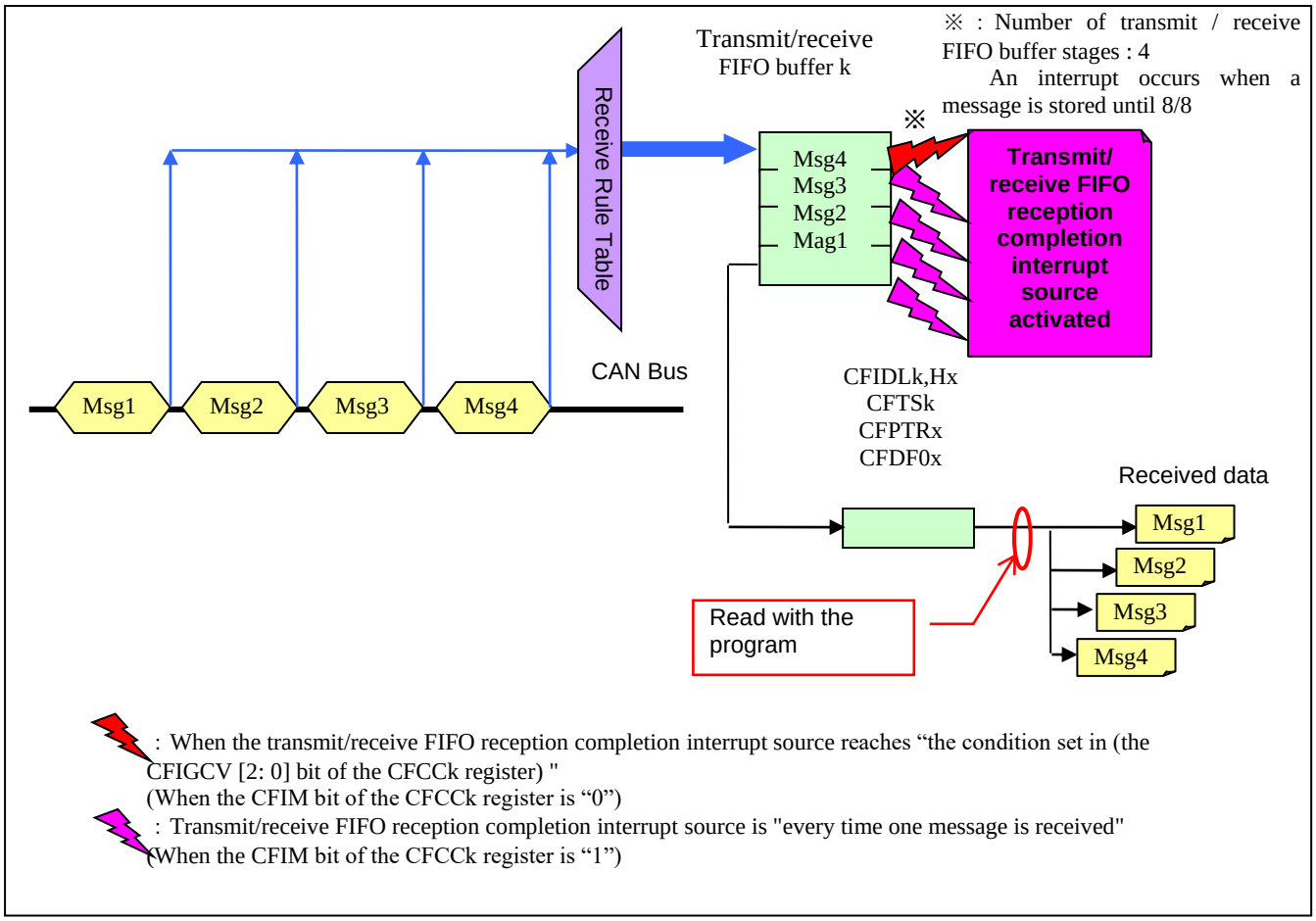
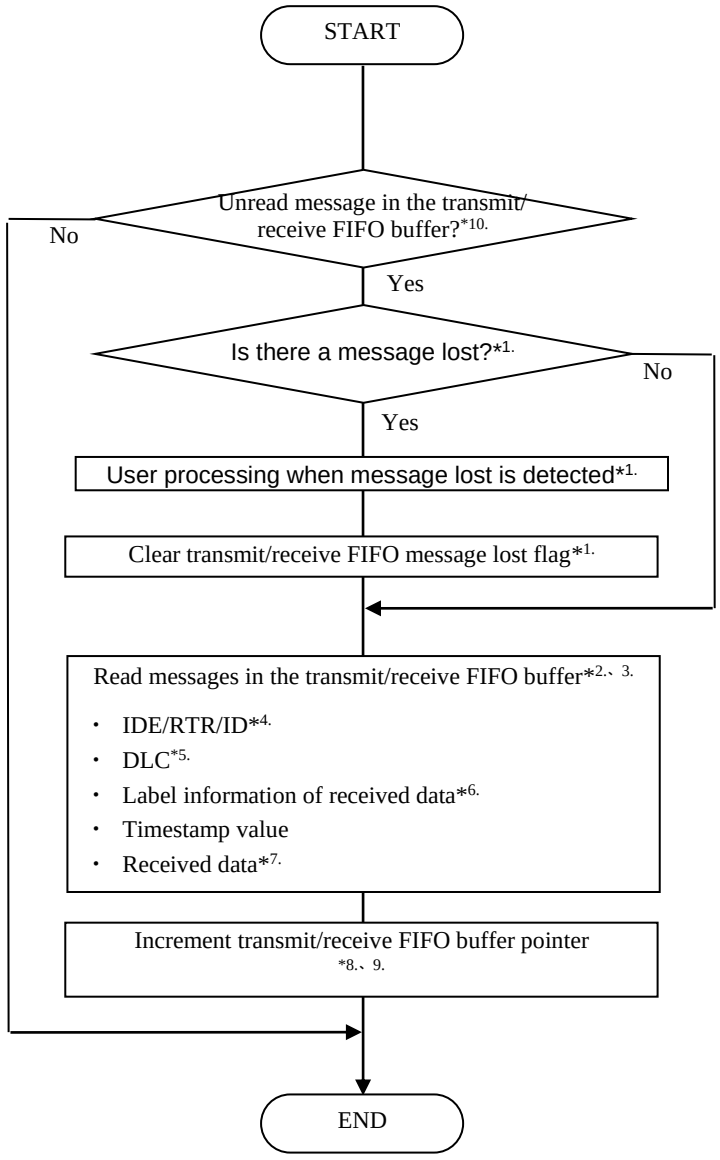


Figure 4-1 Transmit/receive FIFO Buffer Operation (Receive mode)

4.1 Transmit/receive FIFO Buffer Read Procedure

Figure 4-2 shows the procedure for reading the transmit/receive FIFO buffer, and Figure 4-3 and Figure 4-4 show the procedure for enabling and prohibiting the use of the transmit/receive FIFO buffer.

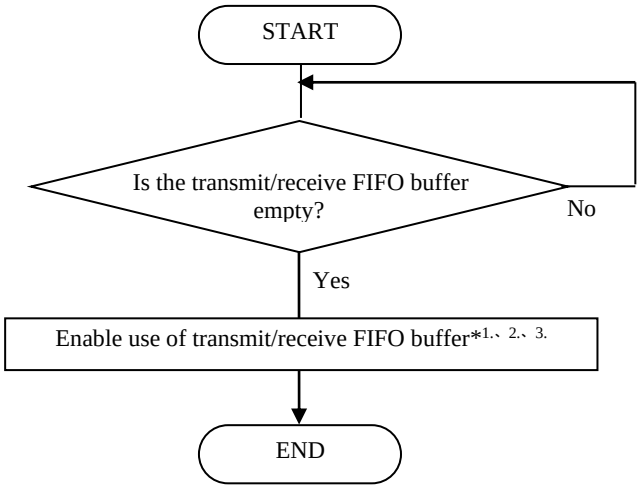


【Note】 1. If the FIFO message lost interrupt is enabled, execute it in the global error interrupt processing.

2. The transmit/receive FIFO buffer (CFIDk register, CFPTRk register, CFDF0_k register, CFDF1k register) can be read only in the receive mode (CFM [1: 0] bis of the CFCCk register is “B’00”).
3. In the receive mode, enabling or prohibiting the storage of transmission history data (the THLEN bit of CFIDk register) is invalid.
4. For standard ID, read b10 to b0 of ID (the CFID [28: 0] bit of the CFIDk register). “0” can be read for b28 to b11.

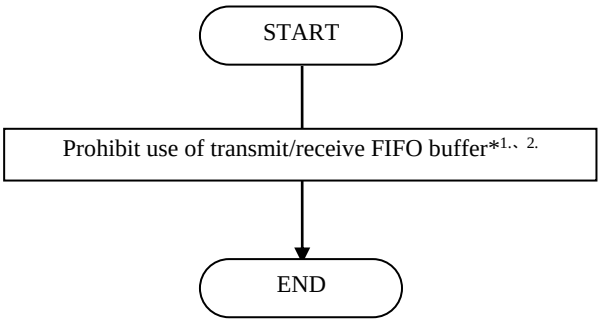
5. If DLC replacement is enabled after filtering by the reception rule (the DCE bit of the GCFG register is “1”, DRE bit is “1”), the DLC set value in the reception rule table (the GAFLDLC bit of the GAFLP0_j register) that matches the received message is stored. Otherwise, the DLC value of the received message is stored.
6. After filtering by the reception rule, the set value of the reception rule table label (GAFLPTR [11: 0] bit of GAFLP0_j) that matches the received message is stored.
7. If the DLC of the received message (value of the CFDLC [3: 0] bit of the FPTRk register) is less than the payload storage size of the transmit/receive FIFO buffer, "H'00" can be read for the data byte (the CFDFd_k register) for which no data is set.
8. After reading the messages in the transmit/receive FIFO buffer (the CFIDk register, CFPTRk register, CFDFd_k register), increment the pointer (write "H'FF" to the CFPC [7: 0] bit of the CFPCTRk register).
9. Increment the pointer when the transmit/receive FIFO buffer is used (the CFE bit of the CFCCk register is “1”) and there are unread messages in the transmit/receive FIFO buffer (the CFEMP flag in the CFSTSk register is “0”).
10. When reading all the unread messages in the transmit/receive FIFO buffer, use a loop statement or the like to read until the buffer is empty.

Figure 4-2 Transmit/receive FIFO Buffer Read Procedure (Receive mode) (no interrupt used)



【Note】 1. Rewrite to enable/disable the transmit/receive FIFO buffer (the CFE bit of the CFCCk register) in the global operation mode or global test mode.
2. Make the configuration settings for using the transmit/receive FIFO buffer, and then enable the use of the transmit/receive FIFO buffer (CFE bit is "1").
3. If the number of transmit/receive FIFO buffers is set to “0” (“B’000” in the CFDC [2: 0] bit of the CFCCk register), do not allow the transmit/receive FIFO buffer to be used.

Figure 4-3 Procedure to Enable Transmit/receive FIFO Buffer Use



【Note】 1. Rewrite to enable/disable the transmit/receive FIFO buffer (the CFE bit of the CFCCk register) in the global operation mode or global test mode.
2. Even if the use of the transmit/receive FIFO buffer is prohibited (the CFE bit is “0”) while an interrupt request is generated (the CFRXIF flag in the CFSTSk register is “1”), the interrupt request flag (CFRXIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Figure 4-4 Procedure to Prohibit Transmit/receive FIFO Buffer Use

4.2 Transmit/Receive FIFO Buffer (Receive Mode) Interrupt Processing

4.2.1 Transmit/receive FIFO Reception Completion Interrupt Processing

If the transmit/receive FIFO interrupt is enabled, the transmit/receive FIFO interrupt is generated when the condition selected in the CFIM bit setting of the CFCCk register is satisfied.

Even if the use of the transmit/receive FIFO buffer is prohibited (CFE bit is “0”) while an interrupt request is generated (the CFRXIF flag in the CFSTSk register is “1”), the interrupt request flag (CFRXIF flag) is not automatically set to “0”. Set the interrupt request flag to "0" with the program.

Whether to enable or disable transmit/receive FIFO interrupts can be set for each transmit/receive FIFO buffer using the CFRXIE bit of the CFCCk register.

The sources of transmit/receive FIFO interrupts in receive mode are shown below.

A transmit/receive FIFO interrupt request is generated when the condition set by the CFIGCV [2: 0] bit of the CFCCk register is reached (the CFIM bit of the CFCCk register is "0").

RFIGCV[2:0] bit settings

- When a message is stored up to 1/8 in the transmit/receive FIFO buffer*1
- When a message is stored up to 2/8 in the transmit/receive FIFO buffer
- When a message is stored up to 3/8 in the transmit/receive FIFO buffer*1
- When a message is stored up to 4/8 in the transmit/receive FIFO buffer
- When a message is stored up to 5/8 in the transmit/receive FIFO buffer*1
- When a message is stored up to 6/8 in the transmit/receive FIFO buffer
- When a message is stored up to 7/8 in the transmit/receive FIFO buffer*1
- When the transmit/receive FIFO buffer is full

— Transmit/receive FIFO interrupt request occurs every time message reception is completed (the CFIM bit of CFCCk register is “1”)

【Note】 1. Do not set if the number of transmit/receive FIFO buffers is set to 4 messages (the CFDC [2: 0] bit of the CFCCk register is set to "B'001").

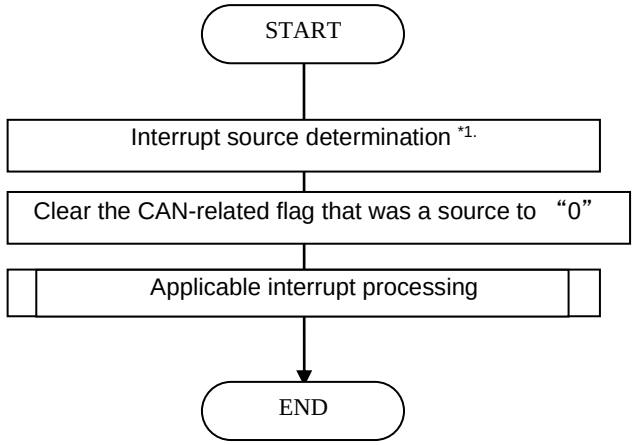
4.2.2 Global Error Interrupt Processing

If the FIFO message lost interrupt is enabled, a global error interrupt is generated when a message lost in the transmit/receive FIFO buffer is detected. Whether to enable or disable the FIFO message lost interrupt can be set in common for the entire module with the MEIE bit of the GCTR register.

5. CAN-related Interrupt Processing

When using interrupts, the interrupt source flag must be cleared to “0”. For CAN-related flags related to each interrupt source flag on the interrupt control side, refer to "7.1 CAN-related interrupt sources".

Figure 5-1 shows how to clear the interrupt source flag in interrupt processing.



【Note】 1. Please carry out if necessary.

Figure 5-1 CAN-related Interrupt Processing Procedure

6. Precautions for Processing Flow

6.1 About Functions

In this application note, there is a part that is functionalized even in the processing of single line, but this is only described as a function to clarify the processing for each function. When you actually create a program, it is not necessary to make it functional.

6.2 Settings for Each Channel, FIFO, and Buffer

In this application note, even if processing is required for each channel, FIFO, or buffer, only one processing is described. When actually creating a program, perform multiple processes as necessary.

6.3 Infinite Loop

To simplify the notation, there are some infinite loops in the processing flow. When actually creating a program, give each loop a time limit so that it can be exited during overtime. Figure 6-1 shows an example of processing with a loop time limit.

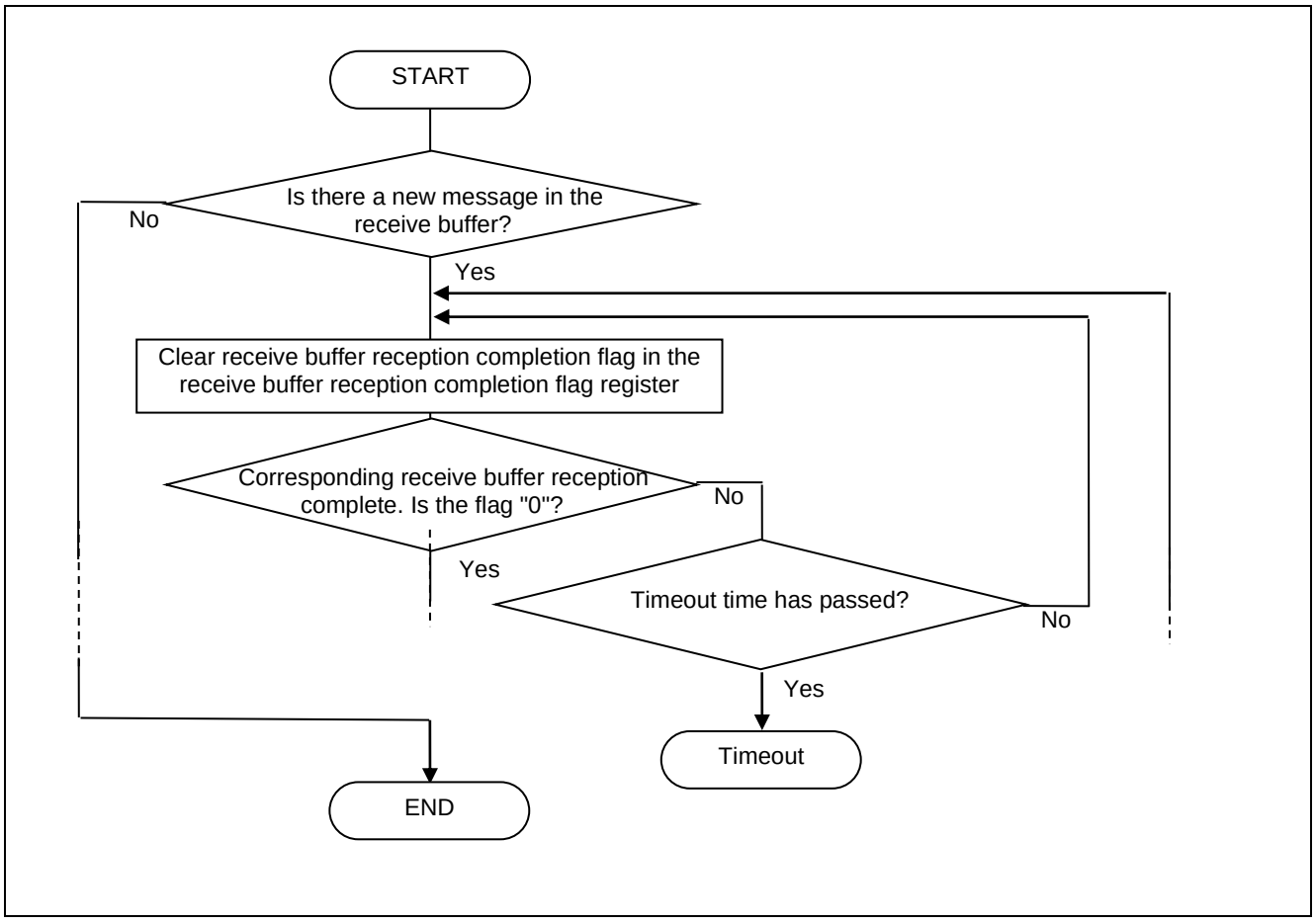


Figure 6-1 Example of Processing with Loop Time Limit

7. Appendix

7.1 CAN-related Interrupt Sources

Table 7-1 shows the CAN-related interrupt sources.

Interrupt	Occurrence Source	Configuration (Enable) Unit *1	Interrupt Source	Request Clear Method *1
Global receive FIFO interrupt	Receive FIFOx interrupt request	RFIE bit of the RFCCx register	When the condition set by the RFIGCV[2:0] bit of the RFCCx register is met*2	RFIF flag in the RFSTSx register = "0"
			Every time one message is received	
Global error interrupt	DLC check error	DEF flag in the GERFL register	When the DLC check detects an error	DEF flag in the GERFL register = "0"
	FIFO message lost	MES bit of the GERFL register	When a message lost in the transmit/receive FIFO buffer is detected	・ CFMLT flag in the CFSTSk register of all channels = "0". ' ・ RFMLT flag in the CRFSRx register of all channels = "0"
			When a message lost in the receive FIFO buffer is detected	
	Transmit history buffer overflow	THLES flag in the GERFL register	When the transmission history buffer is full and you try to store more new transmission history data	THLMLT flag in the THLSTSm register of all channels = "0"
CANm transmit interrupt	CANm transmist complete interrupt request	TMIIEp bit of the TMIECy register	When the buffer becomes empty due to the completion of message transmission	TMTRF[1:0] flag in the TMSTSp register = "B'00".
	CANm transmit abort interrupt request	TAIE bit of the CmCTR register	When the buffer becomes empty due to the completion of sending a message abort	
	CANm transmit queue interrupt request	TQIE bit of the TXQCCm register	When the send queue becomes empty due to the completion of transmission	TQIF bit of the TXQSTSm register = "0"
			Every time one message is sent	
	CANm transmit /receive FIFO transmission complete interrupt request	CFTXIE bit of the CFCCk register	When the buffer becomes empty due to the completion of message transmission	CFTXIF flag in the CFSTSk register = "0"
			Every time one message is sent	
	CANm transmist history interrupt request	THIE bit of the THLCCm register	When 12 data are stored in the transmission history buffer	THIF flag in the THLSTSm register = "0"
			Every time the transmission history data is stored	
CANm transmit/receive FIFO reception completion interrupt	Channel m transmit/ receive FIFO reception complete interrupt request	CFRXIE bit of the CFCCk register	When the condition set by the TRFRIT bit of the CFCCk register is met*3	CFRXIF flag in the CFSTSk register = "0"
			Every time one message is received	
CANm error interrupt	Bus error	BEIE bit of the CmCTR register	When any one of the ADERR, B0ERR, B1ERR, CERR, AERR, FERR, and SERR flags of the CmERFL register becomes "1".*4	BEF flag in the CmERFL register = "0"
	Error warning	EWIE bit of the CmCTR register	When the value of the REC [7: 0] or TEC [7: 0] bit of the CmERFL register exceeds 95	EWF flag in the CmERFL register = "0"
	Error passive	EPIE bit of the CmCTR register	In case of the error passive state (REC [7: 0] or TEC [7: 0] bits> 127).	EPF flag in the CmERFL register = "0"
	Bus off start	BOEIE bit of the CmCTR register	When the bus is off (TEC [7: 0] bits> 255)	BOEF flag in the CmERFL register = "0"
	Bus off return	BORIE bit of the CmCTR register	When 11-bit consecutive recessive is detected 128 times and the bus is restored from the off state.*5	BORF flag in the CmERFL register = "0"
	Overload frame transmission	OLEE bit of the CmCTR register	When the transmission condition of the overloaded frame is detected when receiving or transmitting	OVLF flag in the CmERFL register = "'0'"
	Bus lock	BLIE bit of the CmCTR register	When a 32-bit consecutive dominant is detected on the CAN bus in channel communication mode	BLF flag in the CmERFL register = "0"
	Arbitration lost	ALIE bit of the CmCTR register	When arbitration lost is detected	ALF flag in the CmERFL register = "0"
CANm wakeup interrupt	CAN bus falling edge detection	--	When a falling edge is detected at the CRXmD pin	--

Table 7-1 CAN-related Interrupt Sources

【Note】 1. The interrupt request flag and interrupt enable bit in the interrupt function are not described. For details, refer to the interrupt chapter in the hardware chapter of each user's manual.

2. Settings of the RFIGCV[2:0] bit of the RFCCx register
   - ・When a message is stored up to 1/8 in the receive FIFO buffer*
   - ・When a message is stored up to 2/8 in the receive FIFO buffer
   - ・When a message is stored up to 3/8 in the receive FIFO buffer*
   - ・When a message is stored up to 4/8 in the receive FIFO buffer
   - ・When a message is stored up to 5/8 in the receive FIFO buffer*
   - ・When a message is stored up to 6/8 in the receive FIFO buffer
   - ・When a message is stored up to 7/8 in the receive FIFO buffer*
   - ・When the receive FIFO buffer is full

   * Do not set if the number of buffers in the receive FIFO buffer is set to 4 messages (the RFDC [2:0] bit of the RFCCx register is "B'001").
3. Settings of the RFIGCV[2:0] bit of the CFCCk register
   - ・When a message is stored up to 1/8 in the transmit/receive FIFO buffer*
   - ・When a message is stored up to 2/8 in the transmit/receive FIFO buffer
   - ・When a message is stored up to 3/8 in the transmit/receive FIFO buffer*
   - ・When a message is stored up to 4/8 in the transmit/receive FIFO buffer
   - ・When a message is stored up to 5/8 in the transmit/receive FIFO buffer*
   - ・When a message is stored up to 6/8 in the transmit/receive FIFO buffer
   - ・When a message is stored up to 7/8 in the transmit/receive FIFO buffer*
   - ・When the transmit/receive FIFO buffer is full

   ※Do not set if the number of buffers in the transmit/receive FIFO buffer is set to 4 messages (the CFDC [2: 0] bit of the CFCCk register is “B’001”).
4. An interrupt is generated when any one of the following is detected.
   - ・The ADERR flag in the CmERFL register is “1”, and a form error is detected by ACK delimiter.
   - ・The B0ERR flag in the CmERFL register is “1”, and a recessive is detected despite sending a dominant.
   - ・The B1DRR flag in the CmERFL register is “1”, and a dominant is detected despite sending a recessive.
   - ・The CERR flag in the CmERFL register is “1”, and a CRC error is detected.
   - ・The AERR flag in the CmERFLL register is “1”, and an ACK error is detected.
   - ・The FERR flag in the CmERFL register is “1”, and a form error is detected.
   - ・The SERR flag in the CmERFL register is “1”, and a stuff error is detected.
5. If you return from the bus-off state by the following methods before 11 consecutive recessive bits 128 times are detected, no interrupt will be generated (the BORF flag will not be "1").
   - ・When the CHMDC [1: 0] bit of the CmCTR register is set to "B'01" (channel reset mode)
   - ・When the RTBO bit of the CmCTR register is set to "1" (forced recovery from bus off)
   - ・When the BOM [1: 0] bit of the CmCTR register is set to "B'01" (transition to channel standby mode when bus off starts)
   - ・When the BOM [1: 0] bit is “B'11” (transition to channel standby mode at the request of the program during bus off) and the CHMDC [1: 0] bit is set to “B'10” (channel standby mode) before detecting 11 consecutive recessive bits 128 times.

7.2 Operation when Receive Buffer is Completed and Receive (Transmit/receive) FIFO Buffer is Full

Table 7-2 shows the operation when a message to be stored is received when the reception buffer reception is completed, and the reception FIFO buffer, the transmit/receive FIFO buffer (reception mode) are full.

Table 7-1 Operation when Receive Buffer is Completed and Receive (Transmit/receive) FIFO Buffer is Full

FIFO/Buffer	When the next message is received*1	Interrupt request that occurs
Receive buffer	Overwrite	None
Receive FIFO buffer	Discard	Global error interrupt (Message lost in receive FIFO buffer)
Transmit/receive FIFO buffer (receive mode)	Discard	Global error interrupt (Message lost in transmit/receive FIFO buffer)

【Note】 1. Overwrite : The next message is overwritten in the receive buffer
Discard : The next message is discarded (not stored in FIFO) and the message is lost.

7.3 About Receive Rule Table

The receive rule table is a table with rules for filtering received messages.

The selected messages are stored in the specified buffer by data processing using the receive rule table. Data processing includes acceptance filter processing, DLC filter processing, routing processing, label addition processing, and mirror function. For details on how to set the receive rule table, refer to "CAN Configuration Application Note".

The functions performed during data processing of received message according to the receive rule are shown below.

・Comparison of IDE / RTR / ID by IDE mask / RTR mask / ID mask

・Determination of receive rule target message (message sent by other node / own node) (when mirror function is enabled)

・DLC check (when DLC check is enabled)

・DLC replacement (when DLC check and DCL replacement are enabled)

・Storage FIFO / buffer selection

・Addition of receive rule label

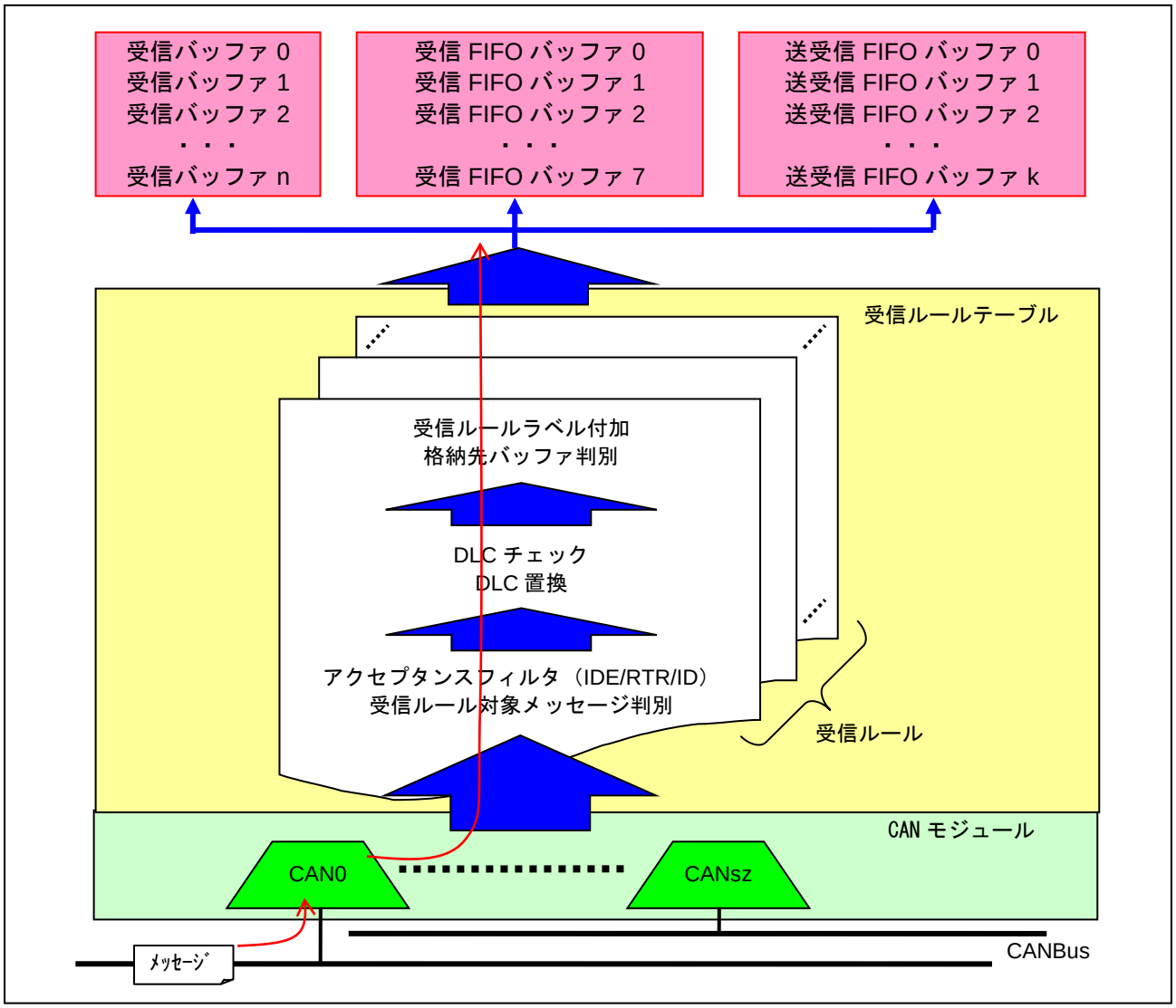


Figure 7-1 Filtering Image by Receive Rule Table

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Website
http://japan.renesas.com/

Inquiry
http://japan.renesas.com/contact/

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	2017.5.10	—	Initial edition

Precautions for use of the product

This section describes the "Precautions" that apply to all microcontroller products. Please refer to this document and the Technical Update for precautions on individual products.

1. Treatment of unused pins

[Caution] Please dispose of unused pins according to "Handling of unused pins" in the text.

The impedance of the input pins of CMOS products is generally high impedance. If the unused pins are operated in an open state, noise around the LSI may be applied due to the induction phenomenon, a through current may flow inside the LSI, or it may be recognized as an input signal and malfunction may occur. Dispose of unused pins according to the instructions given in "Disposal of unused pins" in the text.

2. Treatment at power-on

[Caution] The state of the product is undefined when the power is turned on.

When the power is turned on, the state of the internal circuits of the LSI is indeterminate and the state of register settings and pins is undefined.

For products that are reset using the external reset pin, the pin state cannot be guaranteed from the time the power is supplied until the reset becomes valid.

Similarly, in the case of products that are reset using the built-in power-on reset function, the pin states cannot be guaranteed from the time the power is turned on until the voltage reaches a certain level.

3. Prohibition of Access to Reserved Addresses

[Caution] Access to reserved addresses is prohibited.

The address area has a reserved address allocated for future function expansion. The operation when these addresses are accessed cannot be guaranteed, so do not access them.

4. About clock

[Caution] When resetting, release the reset after the clock has stabilized.

When switching the clock during program execution, switch the clock after the switching destination clock is stable.

In a system that starts operating with a clock that uses an external oscillator (or external oscillator circuit) at reset, release the reset after the clock is sufficiently stable. Also, when switching to a clock that uses an external oscillator (or external oscillator circuit) in the middle of a program, make sure that the clock to be switched to is sufficiently stable before switching.

5. Differences between products

[Caution] When changing to a product with a different model name, perform a system evaluation test for each product model name.

Even if the MCUs in the same group have different model numbers, the characteristic values, operating margins, noise immunity, noise radiation, etc. may differ within the range of electrical characteristics due to differences in internal ROM and layout patterns. When changing to a product with a different model name, perform a system evaluation test for each individual product.

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