

RX72T Group

Renesas Starter Kit for RX72T Boot Loader Application Note

RENESAS 32-Bit MCU
RX Family / RX700 Series

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1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

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4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This application note is designed to provide the user with an understanding of how the System_Bootloader sample works, in order to provide a guide on how such systems may be developed on a RX72T based system. It is intended for users working with a RSKRX72T platform.

Further details regarding operating the RX72T microcontroller may be found in the Hardware Manual and within the sample code.

The following documents applying to the RSKRX72T may provide assistance. Refer to the device specific versions located on the installation of the RSK software or check the Renesas Electronics Web site for the latest versions.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the CPU Board hardware.	Renesas Starter Kit for RX72T User's Manual	R20UT4272EG
Tutorial Manual	Provides a guide to setting up RSK environment, running sample code and debugging programs.	Renesas Starter Kit for RX72T Tutorial Manual	CS+: R20UT4273EG e ² studio: R20UT4276EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample, on a single A4 sheet.	Renesas Starter Kit for RX72T Quick Start Guide	CS+: R20UT4274EG e ² studio: R20UT4277EG
Smart Configurator Tutorial Manual	Provides a guide to code generation and importing into the e ² studio/CS+ IDE.	Renesas Starter Kit for RX72T Smart Configurator Tutorial Manual	CS+: R20UT4275EG e ² studio: R20UT4278EG
Schematics	Full detail circuit schematics of the RSK.	Renesas Starter Kit for RX72T Schematics	R20UT4271EG
Hardware Manual	Provides technical details of the RX72T microcontroller.	RX72T Group Hardware Manual	R01UH0803EJ
Application Note	Application note for the Renesas Flash Module Using Firmware Integration Technology.	RX Family Flash Module Using Firmware Integration Technology	R01AN2184EU
Application Note	Application note detailing the operation of the RSKRX72T Bootloader Sample Program.	Renesas Starter Kit for RX72T Bootloader Application note	R20AN0491EG

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
API	Application Program Interface
Bootloader	Program designed to update firmware on a device while it is running in application
bps	Bits Per Second
CGC	Clock Generation Circuit
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
E1/E2 Lite	Renesas On-chip Debugging Emulator
FSL	Flash Self-programming Library
GUI	Graphical User Interface
I ² C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
ISR	Interrupt Service Routine
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
MCU	Micro-controller Unit
NAK (NACK)	Negative Acknowledgement
RSK	Renesas Starter Kit

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1. Overview

1.1 Purpose

This application note describes the operation of the System Bootloader sample code on the RSK platform with a view to aiding development of similar applications. In addition, this application note uses “RX Family Flash Module Using Firmware Integration Technology (FIT)”.

1.2 Features

The System Bootloader sample code demonstrates the ability to update application code in the internal flash memory of RX72T via SCI while the system is running, using a standard S-Record or hex programmer file format. It incorporates system integrity checking facilities such as CRC Flash memory verification and a watchdog.

The RSK board contains all the circuitry required for microcontroller operation.

2. Introduction

This application note is designed to illustrate how the System Sample: System_Bootloader provides the ability to update application code located in on-board Flash memory on the MCU whilst running, via a serial connection from a PC or equivalent device.

3. System Bootloader

3.1 Memory Map - Flash

In order to understand the operation of the Bootloader and Application system it is important to have an appreciation of the memory space in which they are operating. This is shown in Figure 3-1 Flash Memory Map.

Block36, 37 (Address 0xFFFF0000-0xFFFF0FFF) of the flash memory is the Bootloader code, including the Flash Self-Programming Library. This includes an exception vector table (Address 0xFFFFF80-0xFFFFF8FB). Reset vector was located Address 0xFFFFF8FC.

Block35 (Address 0xFFFF10000-0xFFFFFEEF3) of the flash memory is the user application code. This includes an exception vector table (Address 0xFFFFFEE4-0xFFFFFEE6F). Reset vector was located Address 0xFFFFFEE70.

In the addresses immediately above is the user application area checksum byte. This checksum is calculated and verified by the Bootloader to determine if the application area contains a valid application.

3.2 Memory Map - RAM

The RX72T fitted to the RSK has 128K bytes of RAM.

Because Application code and Bootloader code run entirely separately, there is no shared RAM between them and no restrictions placed on application RAM use.

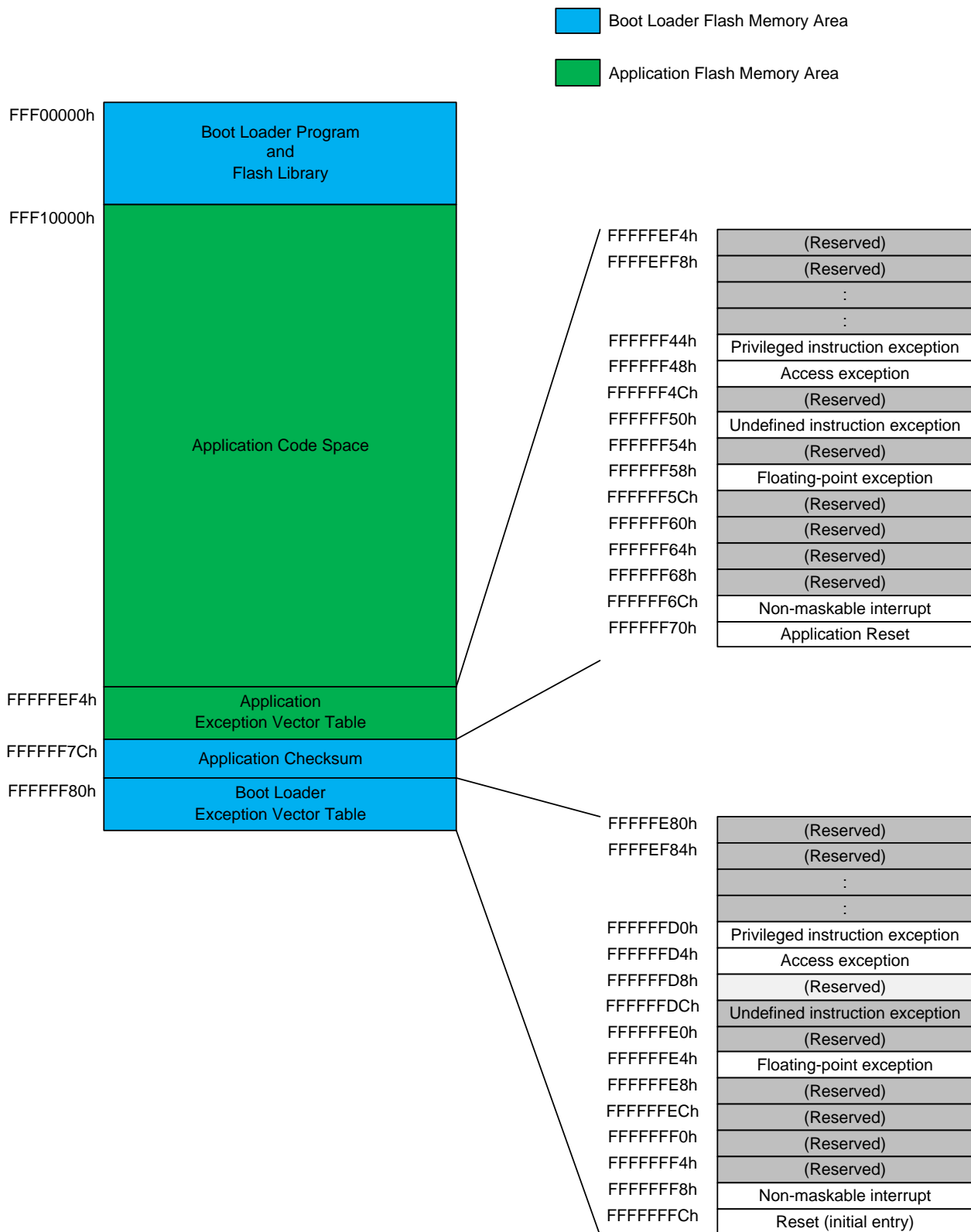


Figure 3-1 Flash Memory Map

3.3 Operation

Figure 3-2 Bootloader Flow Chart shows the workflow for the Bootloader.

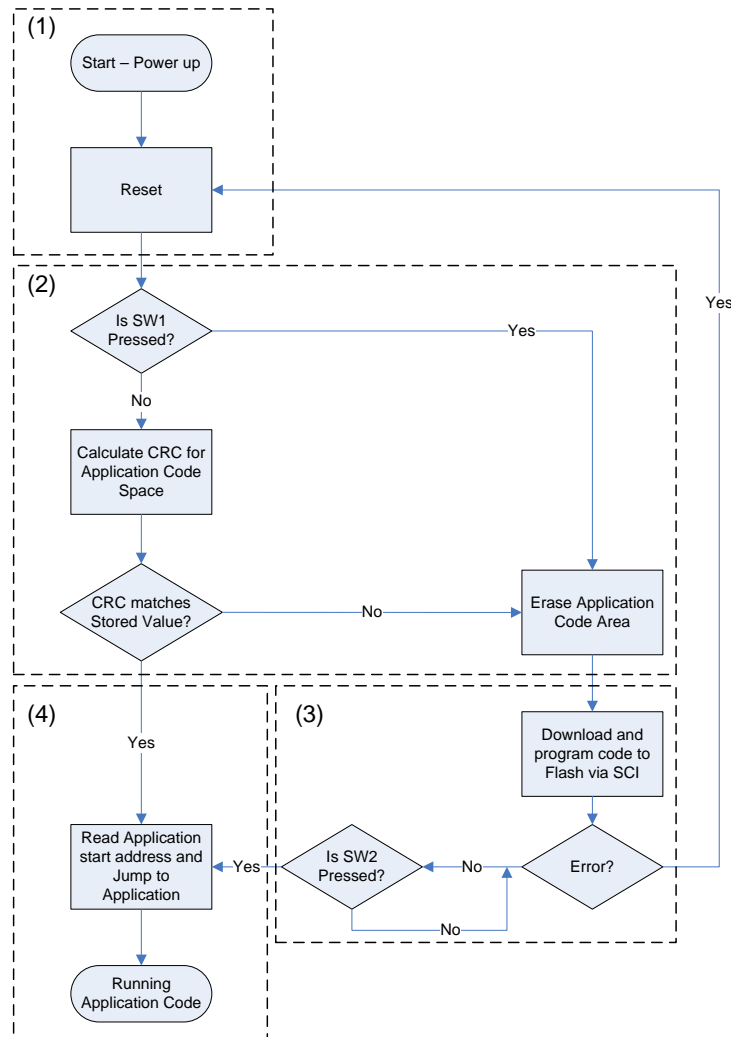


Figure 3-2 Bootloader Flow Chart

- (1) The MCU starts operation always by jumping to the location pointed to by the Bootloader fixed reset vector.
- (2) The Bootloader decides to erase the Application following two conditions.
 1. SW1 is pressed when the RSK starts.
 2. A CRC check of the Application code space determines that the code is invalid.
- (3) The Bootloader is responsible for deciding whether to run code located within the Application area, or to download new code via SCI and reprogram the flash area with this code. Once Application flash programming is complete, the Bootloader then calculates a CRC value for the Application space and programs it to a fixed location in Flash. When an error and hang-up occur, push reset SW on the CPU board, and try again.
- (4) The Bootloader will run Application following two conditions.
 1. Once the Application update process is complete and SW2 pressed.
 2. The application checksum is validated at start-up

The Bootloader will jump to the start address of the Application by reading the Reset vector entry in the Application's exception vector.

4. Vector Handling

The RX72T processor has two vector tables: Interrupt Vector table & Exception Vector table.

4.1 Interrupt Vector Table

As the name suggests this vector table can be located anywhere in the RX72T flash area and stores addresses for the majority of standard interrupt vectors.

The user application is responsible for setting the INTB register to the location of the application's interrupt table.

4.2 Exception Vector Table

This table contains a number of reserved vectors and vectors for:

- Reset,
- Non-maskable interrupt,
- Single-precision floating-point exception,
- Undefined instruction exception,
- Access exception &
- Privileged instruction exception.

The RX72T uses the fixed locations of 0xFFFFF80 through 0xFFFFFFFF for this vector table. This is within the bootloader address space and is not modifiable by the user's application.

Exception Vector Table (EXTB) sets the 0xFFFFF80 after a reset.

The user application must have an exception vector table located at addresses 0xFFFFFEF4 through 0xFFFFF73. This table is in the same format as a standard exception vector table.

Exception Vector Table (EXTB) sets the 0xFFFFFEF4 after jumping to the user application.

If the exception has occurred by except for reset, exception handling by the user application is invoked.

4.3 Code Description

The System_Bootloader project has been based on code generated by the Smart Configurator. Many configuration options can be quickly modified to suit the application using a GUI, for example, changing the baud rate of the SCI connection etc. Smart Configurator files prefixed by "Config_" are files controlled by the Smart Configurator and within such files it is important to make modifications only in areas between the comments such as shown.

```
/* Start user code for adding. Do not edit comment generated here */  
/* End user code. Do not edit comment generated here */
```

Any code additions or modifications performed outside of these comments will be overwritten if the code re-generated by Smart Configurator.

For a more detailed guide to using Smart Configurator, refer to Smart Configurator Tutorial manual.

main.c is the file of the project containing the main function. The function main.c provides a high level guide of the process, following Figure 3-2 Bootloader Flow Chart.

Function update_from_data_source guides the update procedure of reading data from the SCI and programming the Flash with this data. It handles the incoming data byte by byte, determining the format of the file being sent (Intel Hex or S-Record) automatically, and assigning function pointers to handle the data reception appropriately. When complete lines of records from the file are received, it determines what to do with the information; whether it is code and needs to be programmed to Flash or otherwise.

The SCI code is in Config_SCI11.c. By default the SCI is set to use 38400 Baud, 8 Data Bits, No Parity, 1 Stop Bit. These parameters may be changed using Smart Configurator.

To control the flow of data from the host PC, XModem transfer protocol has been employed. This is a 128-byte packet based protocol and allows the System_Bootloader to hold off further transfers from the PC while decoding and programming operations are in progress.

XModem packets are fed into a buffer, which is controlled in buffer.c. The buffer is circular, i.e. when the end of the buffer is reached it loops back to the start. The buffer handling code has been deliberately constructed so as to make it easy to replace the data reception functions with those from a different communications medium.

Programming or erasing Flash via the FIT flash API is achieved via the file code_flash.c. This employs functions to write to the Flash independently of block size or location, encapsulating the FSL library functions. Furthermore repetitive calls to the Flash_Write function will just append the data to a buffer held in RAM and only write the data to the Flash if new data is passed to it that lies outside of the Flash block, in order to reduce the number of Flash writes. Any remaining data held in the Flash Write buffer can be written to the Flash by calling the flash_flush_buffer function.

Decoding of S-Record formatted files is handled in srec.c. Further information on the S-Record file format can be obtained at the following link: [http://en.wikipedia.org/wiki/SREC_\(file_format\)](http://en.wikipedia.org/wiki/SREC_(file_format))

Decoding of Intel hex formatted files is handled in hex.c. Further information on the hex file format can be obtained at the following link: http://en.wikipedia.org/wiki/Intel_HEX

The Bootloader activates the watchdog timer, as a system integrity function. This is achieved in the Config_IWDT.c file. The function R_Config_IWDT_Restart in the Bootloader code resets the watchdog to prevent timeout and reset.

4.3.1 XModem transfer implementation

Details of the XModem protocol may be found at the following link: <http://en.wikipedia.org/wiki/XMODEM>.

The Bootloader implements the standard XModem protocol and not any variant such as XModem-1K or XModem-CRC.

In line with the standard protocol implementation, NAKs are sent by the RSK every 10 seconds before the first packet is received. As such there may be up to ten seconds delay between initialising the transfer on the terminal and the first packet being sent. ^{*1}

A <CAN> flag is sent to the terminal if the Bootloader detects a problem during the XModem transfer. This will cancel the transfer from the PC and allow the error message to be displayed to the user. <CAN> aborts are not supported by all PC terminal programs.

*1: Select S-Record formatted file within 10 seconds after running boot loader.

4.3.2 Flash API and FIT

The Renesas Flash API is used to perform the flash erase and programming. Please refer to 'RX Family Flash Module Firmware Integration Technology' Application Note for the details.

4.4 Bootloader Section Link Addresses

To implement the memory map detailed in section 3.1 Memory Map, **Table 4-1** settings are used for the Bootloader linker sections.

Table 4-1. Section setting of the boot loader

Address	Section Name	Comment
0x00001000	SU	Bootloader work RAM start
	SI	
	B_1	
	R_1	
	B_2	
	R_2	
	B	
	R	
	RPFRAM	
0xFFFF0000	C_1	Start of Bootloader code
	C_2	
	C	
	C\$*	
	D*	
	W*	
	L	
	P*	
0xFFFFFFFF80	EXCEPTVECT	Bootloader Interrupt Vector Table
0xFFFFFFFFFC	RESETVECT	Bootloader Exception Vector Table

4.5 Considerations for Bootloader Application Code

4.5.1 Section Link Addresses

The Bootloader application code and vector tables must be linked within the section shown in **Figure 3-1 Flash Memory Map**, summarised below.

Table 4-2. Section setting of the boot loader application

Address	Section Name	Comment
0x00008000	SU	Application work RAM start
	SI	
	B_1	
	R_1	
	B_2	
	R_2	
	B	
	R	
0xFFFF10000	C_1	Start of Application code
	C_2	
	C	
	C\$*	
	D*	
	W*	
	L	
	P*	
0xFFFFFEF4	EXCEPTVECT	Application Exception Vector Table
0xFFFFF70	RESETVECT	Application Reset

During download the image will be rejected if the Bootloader Application has code placed outside of the Application area shown in Figure 3-1 Flash Memory Map. If this occurs, analysis of the Bootloader Application linker map output file should indicate what has been set incorrectly.

Please note that Smart Configurator in e² studio adjusts Linker Section addresses each time code generated. If using Smart Configurator in e² studio the user needs to manually change the sections to the addresses required.

4.5.2 Fixed Register Configuration

The RX72T has a number of registers that store non-volatile configuration information in the code flash. These include:

- a) Endian Select Register (MDE)
 - b) Option Function Select (OFS0 & OFS1)
 - c) ID Code.
- etc.

These registers are configured by, and located within, the Bootloader area of flash.

Smart Configurator creates the file 'vecttbl.c' which has configuration for these registers. However, these registers are not used in Bootloader Application.

4.5.3 Microcontroller Defaults

Before the user application is launched the Bootloader runs, this sets up various peripherals including the CGC, SCI and WDT. The Bootloader Application should be such that it is can accommodate peripherals not being in their default power-on state.

5. Additional Information

Technical Support

For information about the RX72T group microcontroller refer to the RX72T Group Hardware Manual.

For information about the RX assembly language, refer to the RX Series Software Manual.

Technical Contact Details

Please refer to the contact details listed in section 8 of the “Quick Start Guide”

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