

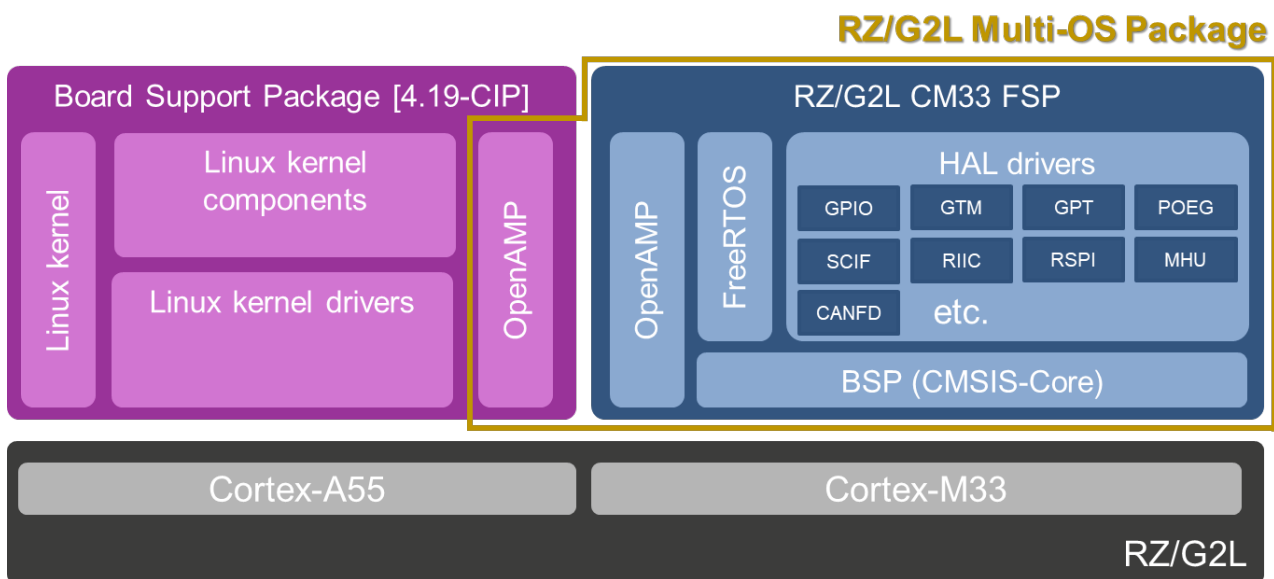
# RZ/G2L, G2LC, G2UL

## Release Note for RZ/G2L Multi-OS Package V1.11

### Introduction

This software package provides user with easy way to establish multi-OS (i.e., CIP Linux running on Cortex®-A55 and FreeRTOS running on Cortex-M33) environment and sample program showing how to implement Inter-Processor Communication between those CPU cores.

This package consists of RZ/G2L Cortex-M33 Flexible Software Package (hereinafter referred to as RZ/G2L CM33 FSP) and Inter-Processor Communication Feature Package for RZ/G2L Board Support Package (hereinafter referred to as RZ/G2L BSP).



Here are brief descriptions of each component of RZ/G2 Multi-OS Package:

- **RZ/G2L CM33 FSP**  
The software package consisting of production ready peripheral drivers, FreeRTOS and portable middleware stacks and the best in-case HAL drivers with low memory footprint.
- **OpenAMP**  
The framework including the software components needed for Asymmetric Multiprocessing (AMP) systems such as Inter-Processor Communication.

### Target Device

RZ/G2L, RZ/G2LC, RZ/G2UL

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## 1. Specifications

Table 1-1 lists the on-chip peripheral modules to be used in this application.

**Table 1-1. Peripheral module used**

Peripheral module	Usage
Message Handling Unit (MHU)	Configures Inter-Processor Interrupt.
Serial Communications Interface with FIFO (SCIFA)	Performs standard serial communications sending and receiving console messages.
Interrupt controller (INTC)	Configures interrupt settings; the processor will receive interrupts during buffered serial communications, and in the MHU module when Inter-Processor Interrupt is fired.
General Purpose Input Output (GPIO)	Configures I/O lines used by serial communications.
General Timer (GTM)	Configures the tick for FreeRTOS.

### 1.1 RZ/G2L reference boards setup

Please refer to [RZ/G2L Group, RZ/V2L, and RZ/Five SMARC EVK Start-up Guide](#).

## 2. Verified Operation Conditions

**Table 2-1. Verified Operating Conditions**

Item	Contents
Microprocessor used	RZ/G2L, RZ/G2LC, RZ/G2UL
Integrated Development Environment	e <sup>2</sup> studio 2022-04 or later
C compiler	GNU Arm Embedded 9.2.1 2019q4 Compiler Options (except directory path): <ul style="list-style-type: none"> <li>• Release               <ul style="list-style-type: none"> <li>-D_RENESAS_RZG_ -mthumb</li> <li>-mcpu=cortex-m33+nodsp+nofp</li> <li>-fdiagnostics-parseable-fixits -O2</li> <li>-fmessage-length=0 -fsigned-char</li> <li>-ffunction-sections -fdata-sections</li> <li>-Wunused -Wuninitialized -Wall</li> <li>-Wextra -Wmissing-declarations -Wconversion</li> <li>-Wpointer-arith -Wshadow -Wlogical-op</li> <li>-Waggregate-return -Wfloat-equal</li> <li>-Wnull-dereference -g -std=c99 -mcmse</li> </ul> </li> <li>• Hardware Debug               <ul style="list-style-type: none"> <li>-D_RENESAS_RZG_ -mthumb</li> <li>-mcpu=cortex-m33+nodsp+nofp</li> <li>-fdiagnostics-parseable-fixits -Og</li> <li>-fmessage-length=0 -fsigned-char</li> <li>-ffunction-sections -fdata-sections</li> <li>-Wunused -Wuninitialized -Wall -Wextra</li> <li>-Wmissing-declarations -Wconversion</li> <li>-Wpointer-arith -Wshadow -Wlogical-op</li> <li>-Waggregate-return -Wfloat-equal</li> <li>-Wnull-dereference -g -std=c99 -mcmse</li> </ul> </li> </ul>

### 3. Sample Program Setup

#### 3.1 RZ/G2L Flexible Software Package Setup

Please refer to [RZ/G2L Getting Started with Flexible Software Package](#).

#### 3.2 OpenAMP related stuff Integration to RZ/G2L Group Board Support Package

This section describes how to integrate OpenAMP related stuff to RZ/G Verified Linux Package [5.10-CIP] for RZ/G2L, RZ/G2LC and RZ/G2UL (hereinafter referred to as VLP). For details on how to build the VLP, please refer to its Release Note which can be downloaded from the link below:

- <https://www.renesas.com/jp/ja/document/mas/release-note-rzg-verified-linux-package-v300>

1. Install the package needed for building BSP.

```
$ sudo apt-get update
$ sudo apt-get install gawk wget git-core diffstat unzip texinfo \
gcc-multilib build-essential chrpath socat cpio python3 python3-pip \
python3-pexpect xz-utils debianutils iputils-ping python3-git \
python3-jinja2 libegl1-mesa libsdl1.2-dev pylint3 xterm p7zip-full
```

2. Configure your Git.

```
$ git config --global user.email "you@example.com"
$ git config --global user.name "Your Name"
```

3. Create a working directory (rzg\_bsp\_v3.0.0) at your home directory, and extract BSP there.

```
$ mkdir ~/rzg_bsp_v3.0.0
$ cd ~/rzg_bsp_v3.0.0
$ tar zxvf ~/rzg_bsp_v3.0.0.tar.gz
```

Please note that rzg\_bsp\_v3.0.0.tar.gz is included in the downloaded package.

4. (Optional) Enable GPU on RZ/G2L and RZ/G2LC with **core-image-weston**, you need to copy the Graphics package (RTK0EF0045Z13001ZJ-v1.0\_EN.zip or RTK0EF0045Z13001ZJ-v1.0\_JP.zip) to working directory and run the commands stated blow:

```
$ cd ~/rzg_bsp_v3.0.0
$ unzip RTK0EF0045Z13001ZJ-v1.0_EN.zip
$ tar zxvf RTK0EF0045Z13001ZJ-v1.0_EN/meta-rz-features.tar.gz
```

5. (Optional) Enable Video Codec on RZ/G2L with **core-image-weston** or **core-image-bsp**, you need to copy the Video Codec package (RTK0EF0045Z15001ZJ-v1.0\_EN.zip or RTK0EF0045Z15001ZJ-v1.0\_JP.zip) to working directory and run the commands stated blow:

```
$ cd ~/rzg_bsp_v3.0.0
$ unzip RTK0EF0045Z15001ZJ-v0.56_EN.zip
$ tar zxvf RTK0EF0045Z15001ZJ-v0.56_EN/meta-rz-features.tar.gz
```

6. Download Multi-OS Package () to working directory and run the commands stated below:

```
$ cd ~/rzg_bsp_v3.0.0
$ unzip r01an5869ej0111-rzg2l-cm33-multi-os-pkg.zip
$ tar zxvf r01an5869ej0111-rzg2l-cm33-multi-os-pkg/meta-rz-features.tar.gz
```

Be sure that you extract Multi-OS Package after Graphics and/or Video Codec package are extracted if you would like to enable either of package.

7. In case of not enabling Graphic and/or Video Codec package, please apply the red-colored modification described below:

- In case of not enabling Graphic package:

File: meta-rz-feature/include/graphic/feature.inc

```
#We want to enable all as default
USE_RENESAS_GLES ?= "0"
USE_RENESAS_OPENCL_rzg2l ?= "0"
```

File: meta-rz-feature/include/demos/demos.inc

```
INSTALL_RZG2_DEMOS ?= "0"
```

- In case of not enabling Video Codec package:

File: meta-rz-feature/include/demos/codecs/plugin.inc

```
USE_CODEC_DEC ?= "0"
USE_CODEC_ENC ?= "0"
```

8. Set up a build environment

```
$ cd ~/rzg_bsp_v3.0.0
$ source poky/oe-init-build-env
```

9. Prepare the default configuration files for the target board by invoking the commands listed below:

```
$ cd ~/rzg_bsp_v3.0.0/build
$ cp ../meta-renesas/docs/template/conf/board/*.conf ./conf/
```

Please replace "**board**" in the above command as follows in accordance with the board you use:

- RZ/G2L Evaluation Board Kit PMIC version      smarc-rzg2l
- RZ/G2LC Evaluation Board Kit                      smarc-rzg2lc
- RZ/G2UL Evaluation Board Kit                      smarc-rzg2ul

10. Start a build by invoking the commands for building VLP. Building an image might take up to a few hours depending on the user's host system performance.

```
$ bitbake core-image-weston
```

### 3.3 Note for integration to VLP

On VLP, the peripherals which is NOT used enters Module Standby Mode. That means the peripherals used on CM33 side might NOT become work implicitly. To avoid this situation, we prepare for the patch shown below:

- 0006-clk-renesas-r9a07g044-Set-SCIF2-OSTM2.patch

This patch prevent SCIF and GTM(OSTM) used in the rmsg sample program from entering Module Standby Mode. If you have any other peripherals which should NOT enter Module Standby Mode, please apply the following modification in red to the patch.

```

drivers/clk/renesas/r9a07g044-cpg.c | 2 ++
1 file changed, 2 insertions(+)

diff --git a/drivers/clk/renesas/r9a07g044-cpg.c
b/drivers/clk/renesas/r9a07g044-cpg.c
index e27caa075af7..9e904d2e8180 100644
--- a/drivers/clk/renesas/r9a07g044-cpg.c
+++ b/drivers/clk/renesas/r9a07g044-cpg.c
@@ -449,6 +449,9 @@ static const unsigned int r9a07g044_crit_mod_clks[]
__initconst = {
    MOD_CLK_BASE + R9A07G044_IA55_PCLK,
    MOD_CLK_BASE + R9A07G044_IA55_CLK,
    MOD_CLK_BASE + R9A07G044_DMACH_ACLK,
+   MOD_CLK_BASE + R9A07G044_SCIF2_CLK_PCK,
+   MOD_CLK_BASE + R9A07G044_OSTM2_PCLK,
+   MOD_CLK_BASE + R9A07G044_XXXX,
};

```

The line number should be revised in accordance with the number of lines you added.

With respect to the allowable value for xxxx above, please refer to the source code below:

[https://github.com/renesas-rz/rz\\_linux-cip/blob/e52825e45b036b8885502182fb83fc8bcd37a00a/drivers/clk/renesas/r9a07g044-cpg.c#L199-L374](https://github.com/renesas-rz/rz_linux-cip/blob/e52825e45b036b8885502182fb83fc8bcd37a00a/drivers/clk/renesas/r9a07g044-cpg.c#L199-L374)

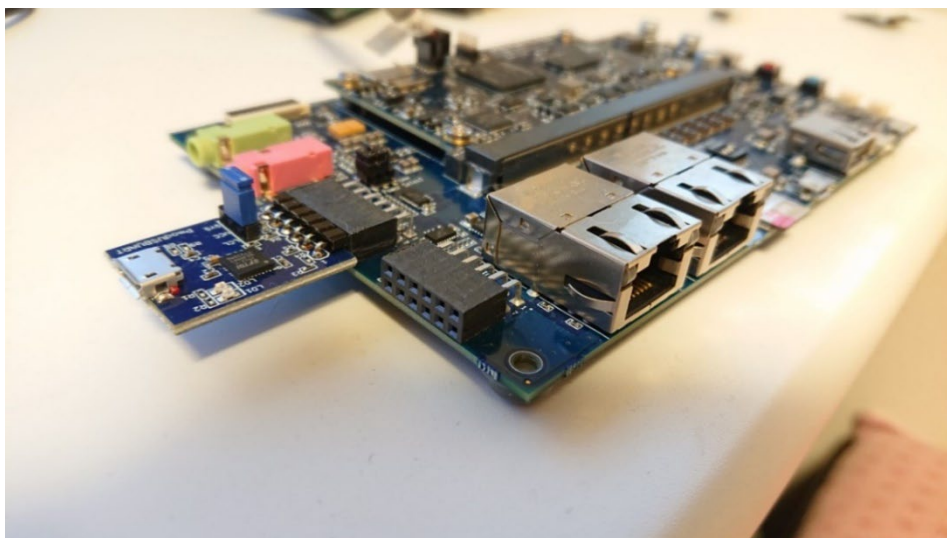
### 3.4 Deployment of RZ/G2L BSP

First, you need to deploy Linux kernel, device tree and root filesystem referring to the section 3 of [Linux Interface Specification Yocto recipe Start-Up Guide](#) or [RZ/G2L Group, RZ/V2L, and RZ/Five SMARC EVK Start-up Guide](#).

## 4. Sample Program Invocation

### 4.1 Hardware setup

1. Connect J-Link to RZ/G2L SMARC EVK. For details, please refer to [RZ/G2L Getting Started with Flexible Software Package](#).
2. Connect [Pmod USBUART](#) to the Pmod 1 of SMARC Carrier Board as shown below for securing the console for the program running on CM33 (note)



**Figure 4-1. Connection between RZ/G2L SMARC EVK and Pmod USBUART**

(note) There is no valid SCIF channel connected to Pmod 0 or Pmod 1 on RZ/G2UL Smarc EVK.

## 4.2 CM33 Sample Program Setup

Please carry out the following procedures for setting up demo program running on CM33.

1. Extract 01an5869ej0050-rzg2l-cm33-multi-os-pkg.zip on your development PC.
2. Extract rzg2l\_cm33\_rpmg\_demo.zip there.
3. Open e<sup>2</sup> studio 2021-07 and click File > Import.
4. Double-click General and select Existing Projects into Workspace as shown in Figure 4-2:

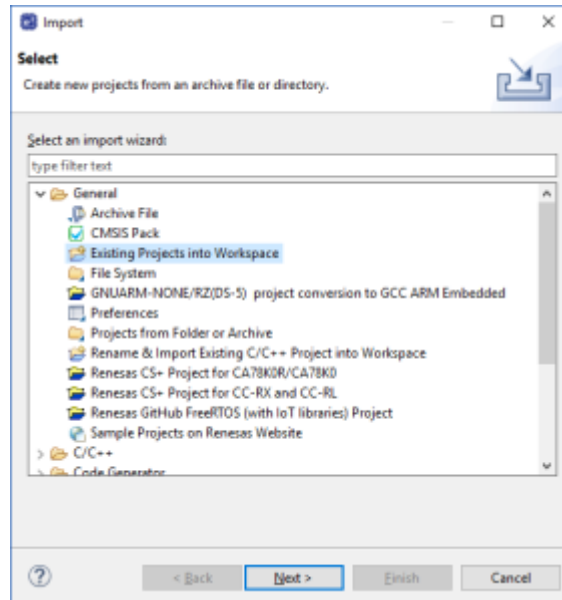


Figure 4-2. Import sample project (1)

5. Input the path to the folder rzg2l\_cm33\_rpmg\_demo, press Enter key and click Finish button.

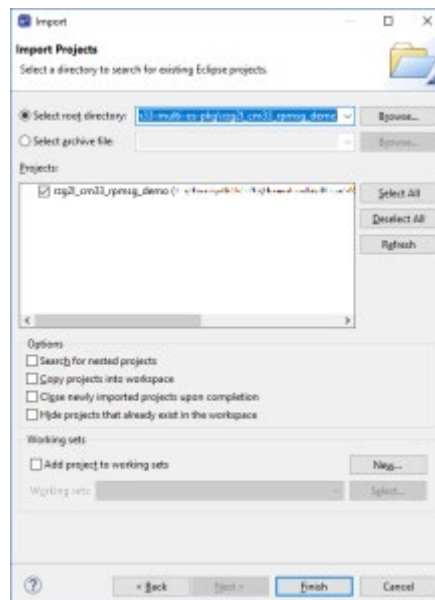


Figure 4-3. Import sample project (2)

- Build the project from Choose Project > Build Project.
- If the build is successfully completed, the following files should be generated in Debug and/or Release folder in accordance with the active Build Configuration.
  - rzg2l\_cm33\_rpmsg\_demo.elf
  - rzg2l\_cm33\_rpmsg\_demo\_non\_secure\_code.bin
  - rzg2l\_cm33\_rpmsg\_demo\_non\_secure\_vector.bin
  - rzg2l\_cm33\_rpmsg\_demo\_secure\_code.bin
  - rzg2l\_cm33\_rpmsg\_demo\_secure\_vector.bin

## 4.3 CM33 Sample Program Invocation

### 4.3.1 CM33 Sample Program Invocation with Segger J-Link

You need to follow the following steps to invoke CM33 sample program with Segger J-Link.

- Choose rzg2l\_cm33\_rpmsg\_demo Debug\_Flat or rzg2l\_cm33\_rpmsg\_demo Release\_Flat from the drop-down list indicated by a red arrow in Figure 4-4.

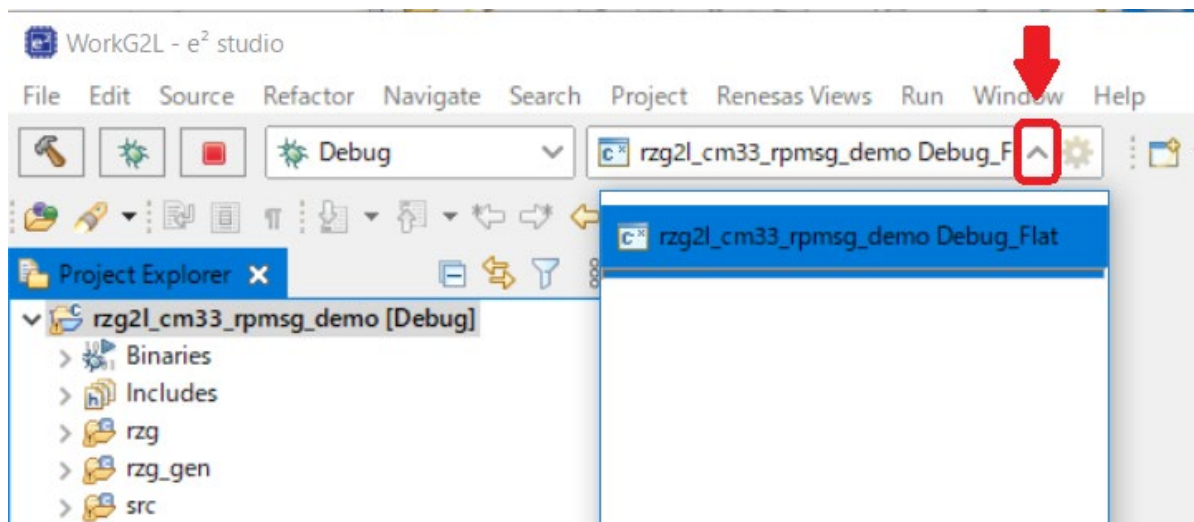


Figure 4-4. Select of Debug Configuration

- Click the debug button indicated by a red arrow in Figure 4-5.

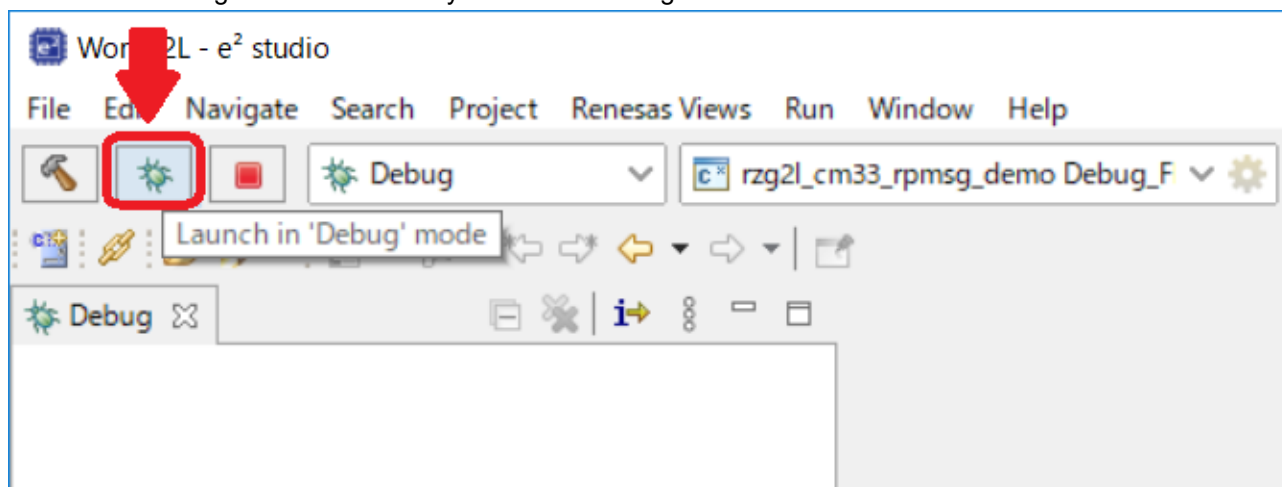


Figure 4-5. Debug Function Launch



If “Confirmation Perspective Switch” window below appears, please press “Switch” to go ahead.

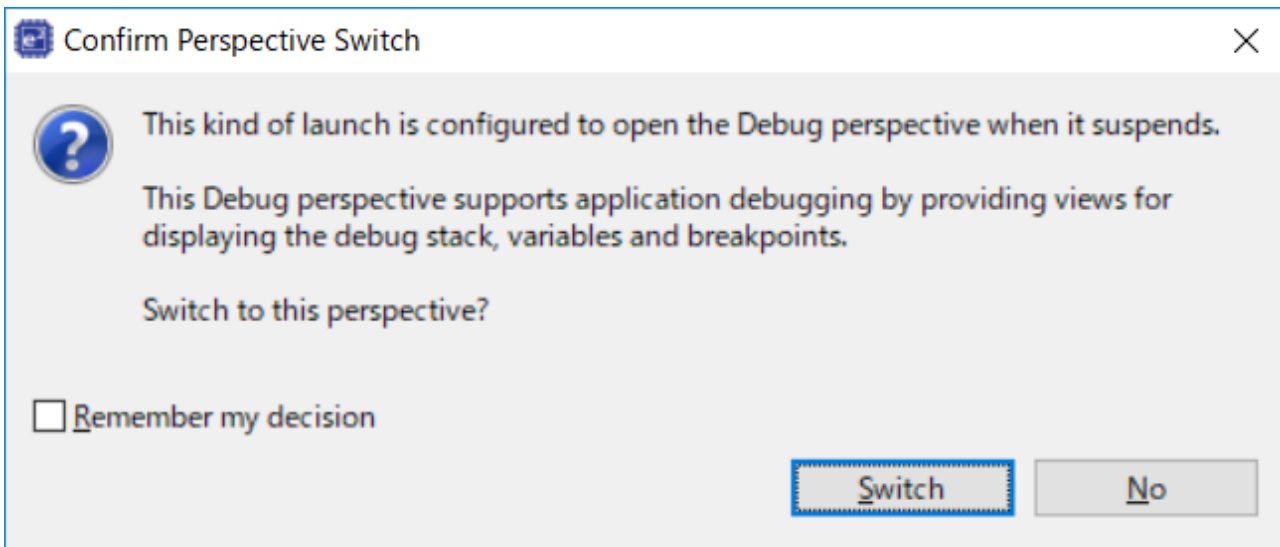


Figure 4-6. Confirmation window to open the Debug perspective

- When the debug perspective is opened, Program Counter (PC) should be located at the top of Warm\_Reset\_S function. Then, you need to press the button indicated by a red arrow in Figure 4-7.

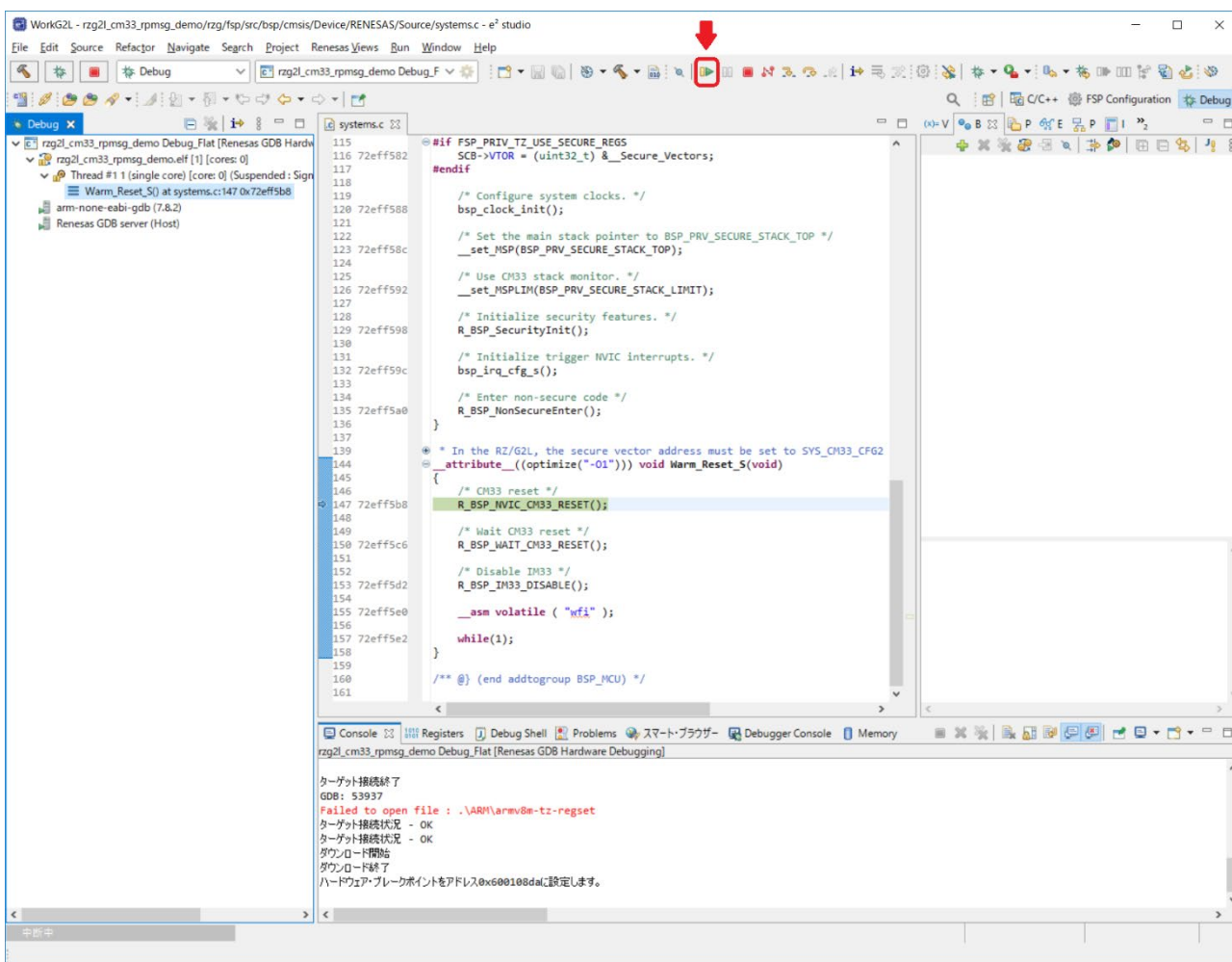


Figure 4-7. How to start to debug sample program (1)

4. The program should stop at the top of main function. Thus, please click the same button as the previous step.

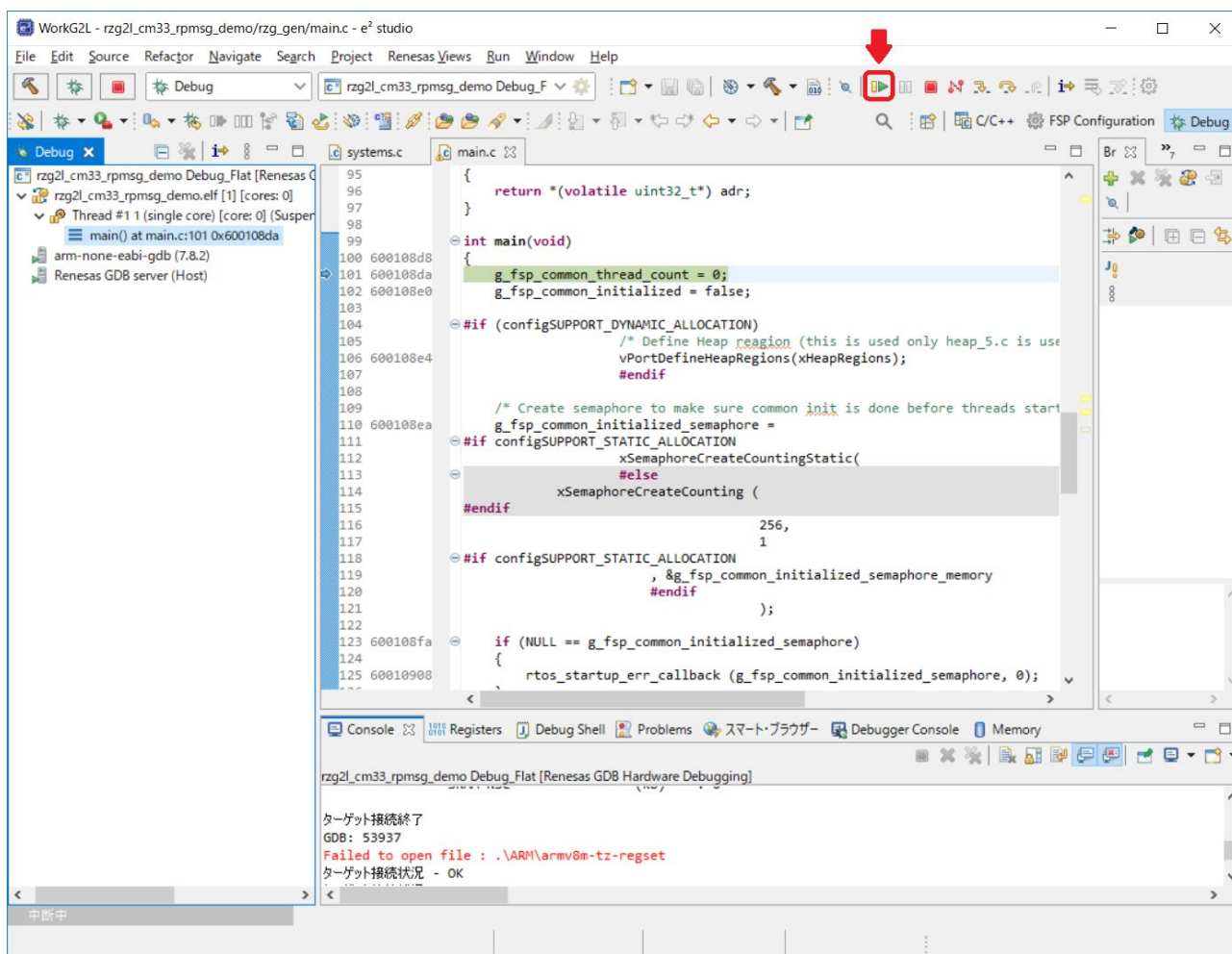


Figure 4-8. How to start to debug sample program (2)

5. Now that CM33 sample program has been started, the following message is shown on the console connected to Pmod USBUART: (note)

```

Successfully probed IPI device
Successfully open uio device: 42F00000.rsctbl.
Successfully added memory device 42F00000.rsctbl.
Successfully open uio device: 43000000.vring-ctl0.
Successfully added memory device 43000000.vring-ctl0.
Successfully open uio device: 43200000.vring-shm0.
Successfully added memory device 43200000.vring-shm0.
Initialize remoteproc successfully.
creating remoteproc virtio
initializing rpmsg vdev

```

At this point of time, CM33 program is waiting for the establishment of rpmsg channel between CM33 and CA55.

- (note) There is no valid SCIF channel connected to Pmod 0 or Pmod 1 on RZ/G2UL Smarc EVK and so, any message won't be shown with RG/G2UL.

### 4.3.2 CM33 Sample Program Invocation with u-boot

You can invoke CM33 sample program from u-boot by following the procedure described below:

1. Copy rzg2l\_cm33\_rpmsg\_demo\_secure\_code.bin, rzg2l\_cm33\_rpmsg\_demo\_secure\_vector.bin, rzg2l\_cm33\_rpmsg\_demo\_non\_secure\_code.bin and rzg2l\_cm33\_rpmsg\_demo\_non\_secure\_vector.bin generated at 7 of section 4.2 to microSD card.
2. Insert the microSD card into CN10 of SMARC carrier board.
3. Turn on SMARC EVK by pressing reset button (i.e., SW14)
4. You should now see the following message in the console connected to CN14 of SMARC carrier board:

```
U-boot 2020.10 (Mar 25 2021 - 08:20:26 +0000)
```

```
CPU: Renesas Electronics E rev 9.7
Model: smarc-rzg2l
DRAM: 1.9GiB
MMC: sh-sdhi: 0, sh-sdhi: 1
Loading Environment from MMC... OK
In: serial@1004b800
Out: serial@1004b800
Err: serial@1004b800
Net: No ethernet found.
Hit any key to stop autoboot: 0
=>
```

Then, you need to hit any key to stop autoboot within 3 sec.

5. Load the binary files listed in 1. from microSD card to RAM by executing the commands below on the console. Here, N denotes the partition number in which you stored those binaries.

```
dcache off
mmc dev 1
fatload mmc 1:N 0x0001FF80 rzg2l_cm33_rpmsg_demo_secure_vector.bin
fatload mmc 1:N 0x42EFF440 rzg2l_cm33_rpmsg_demo_secure_code.bin
fatload mmc 1:N 0x00010000 rzg2l_cm33_rpmsg_demo_non_secure_vector.bin
fatload mmc 1:N 0x40010000 rzg2l_cm33_rpmsg_demo_non_secure_code.bin
cm33 start_debug 0x1001FF80 0x00010000
dcache on
```

6. Now that CM33 program has been started to run. With respect to the behavior of sample program, please see 4.5.

## 4.4 CA55 Sample Program Invocation

You need to follow the procedure shown below to invoke CA55 sample program running on Linux.

1. Boot up Linux by executing the following command on u-boot:

```
run bootcmd
```

2. Login as "root"

```
smarc-rzg2l login: root
```

3. Run CA55 sample program by executing the following command on Linux.

```
root@smarc-rzg2l:~# rpmsg_sample_client 0
```

4. Then, you can see the following message on the console relative to CN14 of SMARC carrier board. Be sure that you invoke CM33 program in advance.

```
Successfully probed IPI device
metal: info:      metal_uio_dev_open: No IRQ for device 42f00000.rsctbl.
Successfully open uio device: 42f00000.rsctbl.
Successfully added memory device 42f00000.rsctbl.
metal: info:      metal_uio_dev_open: No IRQ for device 43000000.vring-ctl0.
Successfully open uio device: 43000000.vring-ctl0.
Successfully added memory device 43000000.vring-ctl0.
metal: info:      metal_uio_dev_open: No IRQ for device 43200000.vring-shm0.
Successfully open uio device: 43200000.vring-shm0.
Successfully added memory device 43200000.vring-shm0.
metal: info:      metal_uio_dev_open: No IRQ for device 42f01000.mhu-shm.
Successfully open uio device: 42f01000.mhu-shm.
Successfully added memory device 42f01000.mhu-shm.
Initialize remoteproc successfully.
creating remoteproc virtio
initializing rpmsg shared buffer pool
initializing rpmsg vdev
```

For details, please refer to section 4.5.

## 4.5 Overview of Sample Program Behavior

The behavior of sample program is as follows:

1. Wait until a communication channel between CA55 and CM33 is established.
2. Once the communication channel is established, CA55 sample program starts to send the message to CM33 with incrementing its size from the minimum value 17 to the maximum value 488. At that time, the message like the following should be shown in the console connected to CN14 of SMARC carrier board:

```
Sending payload number 148 of size 165
```

3. When CM33 receives the message sent from CA55, the echo reply is sent back to CA55.
4. When CA55 receives the echo reply, the message below should be displayed in the console connected to CN14 of SMARC carrier board:

```
echo test: sent : 165
received payload number 148 of size 165
```

5. After the message which has 488 bytes sized payload is sent from CA55 to CM33 and CM33 sends back the echo reply, the message for terminating the communication channel is sent from CA55 to CM33. Then, CA55 and CM33 sample programs output the following log messages to the corresponding consoles respectively when receiving the termination message.

- Termination message on CA55 side

```
*****
Test Results: Error count = 0
*****
Quitting application .. Echo test end
Stopping application...
```

- Termination message on CM33 side

```
De-initializing remoteproc
```

Then, CM33 side re-waits for the establishment of connection channel. You can see the following log on the console a short time later:

```
creating remoteproc virtio
initializing rpmsg vdev
```

## 5. Reference Documents

- R01AN5924: RZ/G2L Getting Started with Flexible Software Package  
The latest version can be downloaded from Renesas Electronics website.
- R01US0553: RZ/G Verified Linux Package Version 3.0.0 Release Note  
The latest version can be downloaded from Renesas Electronics website.
- R01US0554: RZ/G Verified Linux Package Version 3.0.0 Component list  
The latest version can be downloaded from Renesas Electronics website.
- R01US0556: RZ/G2L Group, RZ/V2L, and RZ/Five SMARC EVK Start-up Guide  
The latest version can be downloaded from Renesas Electronics website.
- R01US0398: Linux Interface Specification Yocto recipe Start-Up Guide  
The latest version can be downloaded from Renesas Electronics website.

## Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul.30.21	-	First edition issued.
1.01	Nov.30.21	-	Updated in align with RZ/G2L BSP V1.3.
1.02	Jan.21.21	-	Updated in align with RZ/G2L BSP V1.3 update2.
1.10	Apr.27.22	-	Updated in align with RZ/G2L BSP V1.4.
1.11	May.30.22	-	Updated in align with RZ/G2 Verified Linux Package Version 3.0.0

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

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(Rev.5.0-1 October 2020)

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