REIN_Inverter_V2
Hardware Design Document

Introduction
This Hardware Design Document serves as a technical blueprint for the Traction Motor Controller Board project. This document is intended to describe the hardware system architecture and the design details.

Target Device
RH850/C1M-A1
RAA270000KFT
ISL78434
uPC1251AGR

Figure 1-1 Renesas RH850/C1M-A1 Inverter Board
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1. Architecture

Traction Motor Controller mainly intends to drive motor control for HEV/EV based applications and these consist of two boards – Controller board which controls motor driver, digital, analog sections and Power board includes Power MOSFETs for motor drive. The Controller board controls and drives each phase of the motor windings in Power Board through MOSFET Pre-Driver Stage -ISL78434.

Traction Motor controller includes the RH850/C1M-A1 Microcontroller (R7F701278EAFP QFP), which is equipped with an RH850 Family G3MH CPU core operating at a frequency of 240MHz, providing high processing power. Along with the ROM, RAM, and DMA, it includes various timers such as a motor control timer, various serial interfaces including CAN (CAN FD compatible), a 12-bit A/D converter (ADC), an R/D converter (RDC3A) that converts the resolver output signal to digital angle data, and a CPU and parallel motor control unit (EMU3), etc., providing peripheral functions that are ideal for motor control in HEVs/EVs.

The Controller board has three ISL78434 MOSFET Pre-Driver Stage & uPC1251A Op-Amps for Analog & fault generation circuits, PMIC, LDO, and Power MOSFET Board with RBAZ25N10CHPF. The Power will be 5KW Continuous Power and 8KW peak Power. The number of MOSFET per phase shall be defined accordingly with necessary load dump protection.

The MCU in Controller board interacts with external peripherals through System I/O connectors (COM, ANA and DIO), which carries several communication interfaces, analog, and digital I/O signals. It does also include Intelligent Power Devices (IPD) for additional loads.

Protection for Over-Current, Over-Voltage, Under-Voltage, Over Temperature (Controller and Motor) and its relevant status and precaution are implemented. Interfaces such as CAN-FD, LIN, SENT, Isolated UART such as are also integrated in the design.

![Inverter Block Diagram](image)

**Figure 1-1 - Inverter Block Diagram**
2. Hardware Design

The Hardware is categorized based on the function:

1. Power Supply section
2. IPD section
3. System I/O connections
4. Microcontroller Function Mapping
5. Analog Functions
3. Power Supply Section

The DC power supply input range is limited by the specifications of Step-down DC/DC on-board. The DC/DC output is regulated at 15.6V and is used to derive other supplies required by the controller and logic on board.

The DC Supply input is provided via 20.5mm Brass Studs that directly connect to the Power Board inverter bridge and smaller 6mm studs used for coupling the Power board to control board provide mechanical strength and connect power from the DC Bus to the DC Link capacitors and Step-down DC/DC converter. The current requirement for control board is not very high and is easily managed by the M3 screws. Therefore, note that these screws are active power points on the board when assembled.

The input DC Supply current is monitored by high side current sensor, this current sensor is assembled on the control board. The DC Bus current sensor is bi-directional and therefore can be used to measure currents when motoring and when generating.

![Figure 3-1 System Power Tree](image)
3.1 DC/DC Converter Module

The PDQE20-Q48-S15-D is a DC-DC Isolated converter that provides (15.6V) 15V6 supply to the controller board. The module has isolation up to 1.5KV (if required) and provides maximum 20W output. The output voltage of 15V is nominal, which is trimmed to 15V6 by varying the resistor at the trim pin. The module provides constant output current of 1.333A.

Features:

- Ultra-wide input voltage range (18V~75V).
- 20 W isolated output.
- Single/dual regulated outputs.
- 1500 Vdc isolation.
- Extended temperature range (-40~105°C).
- Input under-voltage protection.
- Output short circuit, over-current and over-voltage protection.
- DIP package.
- Ripple of 100mV.
- Efficiency of 91%.

![DC-DC Module Schematics](image)

**Figure 3-2 Schematics of PDQE20-Q48-S15-D**

**Design Consideration for DC/DC Supply Module:**

**VIN (3)** Input supply pin: Followed by reverse voltage protection (D47) and current limiting PTC fuse (F5)-750mA, input supply **DC_PWR** is applied to this pin through filter section comprised of capacitors of 330 µF/50 V, 4.7 µF/50 V and inductor of value 2.2uH. As per datasheet recommendation, in design electrolytic capacitor and ceramic capacitor are used.

**CTRL (1):** Remote ON/OFF: Used to enabled and disabled. In design, during emergency conditions logic low from MCU will turn off the module through transistor-based switch circuit, which avoids fault operation and disconnect supply power to rest circuitry.

**TRIM (5):** The Output voltage is trimmed through this pin. In design, the voltage is trimmed to 15.6V, which is the power source for the system.
The voltage is set as per the following calculation suggested in the datasheet. Figure 6 shows the calculation formula for Trim Pin.

\[ RT = \left( \frac{aR_2}{R_2-a} \right) - R_3 \]
\[ \text{Where } a = \left( \frac{V_{\text{ref}}}{V_O - V_{\text{ref}}} \right) \times R_1 \]

As per Table 5 in Datasheet

For \( V_O = 15V, V_{\text{ref}} = 2.5V \)
\( R_1 = 14.494\, k\Omega, R_2 = 2.87\, k\Omega, R_3 = 17.4\, k\Omega \)

\( a = \frac{2.5}{(15.6-2.5)} \times 14.494\, k\Omega \)
\( a = 2.766\, k\Omega \)

\[ RT = \left( \frac{2.766\, k\Omega \times 2.87\, k\Omega}{2.87\, k\Omega - 2.766\, k\Omega} \right) - 17.4\, k\Omega \]
\( RT = 58.9\, k\Omega \)

In design as per application circuit and calculations resistor RT of 58.3kΩ is used to trim voltage to 15.6V.

### Table 5

<table>
<thead>
<tr>
<th>( V_O ) (Vdc)</th>
<th>( R_1 ) (kΩ)</th>
<th>( R_2 ) (kΩ)</th>
<th>( R_3 ) (kΩ)</th>
<th>( V_{\text{ref}} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>4.829</td>
<td>2.87</td>
<td>15</td>
<td>1.24</td>
</tr>
<tr>
<td>5</td>
<td>2.894</td>
<td>2.87</td>
<td>10</td>
<td>2.5</td>
</tr>
<tr>
<td>12</td>
<td>11,000</td>
<td>2.87</td>
<td>17.4</td>
<td>2.5</td>
</tr>
<tr>
<td><strong>15</strong></td>
<td><strong>14.494</strong></td>
<td><strong>2.87</strong></td>
<td><strong>17.4</strong></td>
<td><strong>2.5</strong></td>
</tr>
<tr>
<td>24</td>
<td>24.872</td>
<td>2.87</td>
<td>20</td>
<td>2.5</td>
</tr>
</tbody>
</table>

+\( V_O \) (4): Output Voltage: A nominal output voltage of 15V is observed at this pin which is set to 15.6V using resistor (RT). In design as per datasheet recommendation output voltage is noise filtered using a tantalum capacitor of 100µF / 50V. Power LED (D53) is provided in design to indicate the generated voltage 15.6V o/p.

The Power Supply is indicated by 2 LED’s on-board, LED D53 indicates 15V6 Supply output and D54 indicates EVCC5V output as shown below:

The other voltage levels can be checked by tapping into the on-board test points provided and as per schematics.
### 3.2 Power Management IC: RAA270000KFT (U1)

The RAA270000KFT is a Power Management IC (PMIC) for automotive RH850 microcontroller series. The RAA270000KFT contains two integrated current mode DC-DC converters, four low dropout linear regulators (LDOs) and two linear trackers. The switching frequency of the DC-DC converters is typically 2.1MHz. Also, several monitor functions and diagnostic functions such as over-voltage and under-voltage detection of the regulators and watchdog for monitoring external microcontroller are implemented.

The input voltage of the RAA270000KFT, the output of all regulators, and internal analog voltage corresponding to temperature can be monitored through ADCs in external microcontroller. Since the RAA270000KFT includes a power-up/down sequence controller, users can reduce external components for controlling the target microcontroller power-up/down sequence.

#### Features

- **Input range**: 6.0V to 18.5V to perform specified characteristics.
  - 5.4V`: Power rails, 5V/3.3V/1.25V and trackers functional (Not detect low voltage)
  - 3.9V`: Not issues reset.
- **2 switching regulators**,
  - For point of load: 5.7V/1000mA
  - For MCU core: 1.25V/700mA
- **4 linear regulators**
  - For MCU: 3.3V/10mA, 5.0V/300mA, 3.3V/160mA, 5.0V/60mA
- **2 linear trackers**,
  - 150mA ability with short protection to battery
- **Automatic power sequence**
- **Watchdog timer**
- **Analog multiplexer** – Used for monitoring the PMIC voltage levels from MCU ADC
- **Interrupt request to MCU**
- **CSI(SPI) Communication with Main MCU.**
- **Thermal shut down.**
- **Reset generator.**

#### Design Consideration for PMIC Supply:

For further details on the PMIC please refer the datasheet or contact Renesas Engineer for any clarification.

**CAUTION**: Care must be taken that excess input voltage is not applied to J1 to avoid damage to the PMIC IC.
3.3 LDO: BD00C0AWFP-CE2 (U3)

The BDxxC0A-C series and the BDxxC0AW-C series are low-saturation regulators. This series feature variable and fixed voltage output with selectable Shutdown switch (referred to as SW). This series has a built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits and a thermal Shutdown circuit that protects the IC from thermal damage due to overloading.

Features

- Output current capability: 1A.
- Output voltage: Variable, 3.3V, 5.0V, 8.0V and 9.0V
- High output voltage accuracy (Ta=25°C, TO252-3/5, HRP5): ±1%
- Low saturation with PDMOS output
- Built-in over-current protection circuit that prevents the destruction of the IC due to O/P short circuits.
- Built-in thermal Shutdown circuit for protecting the IC from thermal damage due to overloading.

In Design, the BD00C0AWFP-CE2 is an independent Power source which is dedicated to generating 5V6VCC – general 5V supply for most of the circuits in the design. In addition to 5V6VCC optional power supply for CAN Sections and Current sensor are provided in case of shortage of current through diodes. The output value is set to 5V6 to counter the drop across the series diode used for distributing this supply across various on-board and off-board supplies requiring typ. 5V0 DC supply.

![Figure 3-4 LDO Power Supply On-Board](image)

**Design considerations for the LDO supply:**

CTL (Pin 1) – Output Control Pin: This pin controls the output voltage and enabled by MCU pin and optional enable is provided by tying to 3V3 supply with jumper. By default, this pin is pulled low through 33kΩ resistor. Based on requirement MCU may enable and disable this LDO output.

VCC (Pin 2) Input supply. A capacitor greater than 1-µF or larger capacitor with excellent voltage and temperature characteristics must be connected between VCC and GND for stability. Larger value capacitors result in better transient and noise performance. Although an input capacitor is not required for stability, when a 0.1-µF or larger capacitor is placed between VCC and GND, it counteracts reactive input sources and improves transient and noise performance. Higher value capacitors are necessary if large, fast rise time load transients are anticipated. In design 10-µF, 25V, X5R and 0.1-µF, 50V, X7R.

In design current is limited with PTC resettable fuse of maximum current of 20A, hold current of 500mA and trip current of 2.5A with maximum 16V. Reverse voltage protection is provided with 100V schottky diode.
ADJ (Pin 5) Adjustable Pin: The Output of LDO is set using voltage divider. The reference voltage is 0.75V and R1 is 10kΩ as recommended by datasheet.

\[ V_O = ADJ \times \frac{(R_1+R_2)}{R_1} \]

Where \( V_O = 5.7 \text{V}, \ ADJ = 0.75 \)

\[ R_2 = (\frac{5.7}{0.75} - 1) \times 10K \]

\[ R_2 = 66.5kΩ \]

VO (4) Output Pin: To prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. A tantalum capacitor with a capacitance 47μF, 10V is used followed by Ceramic capacitor of 0.1μF, 50V.

**CAUTION:** As shown in the schematic R38 is mounted connecting the PMIC 5V7 output to 5V6VCC therefore, this LDO default state on-board is “INACTIVE” by applying “Low” on CTL (Pin 1) of LDO. If user wish to enable the LDO, it can be done only after unmounting R38, then applying “High” on CTL via MCU through ADJ_VCC_EN Signal.
4. IPD Section

In this reference design there are three µPD166033T1U and one µPD166023T1J IPD devices which drive 12V load connected through J10 connector. These devices are controlled by MCU.

µPD166033T1U is part of 2nd Generation Intelligent Power Devices (IPD). They are N-channel high-side switches with charge pump, voltage-controlled input, diagnostic feedback with proportional load current sense and embedded protection function. Family includes up to 14 devices depending on on-state resistance, package and channel number combination.

µPD166023T1J is part of 2nd Generation Intelligent Power Devices (IPD). This is N-channel high-side switch with charge pump, voltage-controlled input, diagnostic feedback with proportional load current sense and embedded protection function. Family includes up to 14 devices depending on on-state resistance, package and channel number combination.

**IPD feature summary:**

- Built-in charge pump.
- 3.3V compatible logic interface.
- Low standby current.
- Short circuit protection.
  - Shutdown by over current detection.
  - Power limitation protection by overload detection (Power limitation: current limitation with delta Tch control).
  - Absolute Tch over temperature protection.
- Built-in diagnostic function.
  - Proportional load current sensing.
  - Defined fault signal in case of abnormal load condition.
- Loss of ground protection.
- Under voltage lock out.
- Active clamp operation at inductive load switches off.
- Cross current protection in case of H-bridge high side usage.
- Reverse battery protection by turn on the output.
Design consideration for IPD Functions:

IPD devices are powered by external connector (J10) through VBUS_EXT_PIN & optional internal supply ORING between 12VDC VBUS External and on-board 15V6 (15.6V) through series diode is possible via mounting of the diode as shown in figure below.

![Figure 4-1](image1)

IN (Input signal): MCU (U2) enables these devices through control signals EN_IPD_OUT1, EN_IPD_OUT2, EN_IPD_OUT3 & EN_IPD_OUT4.

IS (Current sense and Diagnosis output signal): These pins are pulled low by connecting to GND, which generates voltage drop proportional to load current. MCU (U2) monitors voltage drop through ADC and analyses current consumption of the load through IPD connector (J10).

Zener diodes are provided at the IS pin, to protect MCU from over voltage, when voltage drop between IS pin and ground is greater than VCC.

SEN (Sense enable input): VSEN is set to 5V (EVCC) in design. RSEN is set to 4.7kΩ.

OUT (Protected high-side power output): The output of IPD devices, OUT1, OUT2, OUT3 & OUT4 are connected to the IPD connector (J10).

A capacitor of 0.1uF/50V and 12kΩ resistor is provided across output pin and connector (J10). TVS diode (D30) is provided across the output pin, for ESD protection of the device.

![Figure 4-2](image2)
5. **System I/O Connector Details**

Controller board has 1 Nos of 12-Pin and 3 Nos. of 34 pin System I/O connectors, which deals with 12V External Load Drive, Control, Communication & I/O signals respectively across controller board to external system. Since these connectors carry all system related signals in and out of the board, these are classified based on type of signals.

These connectors are named as ANA, COM and DIO in the design, where ANA connector deals with analog signals such as RDC, temperature sensor, pedal, brake status. COM connector deals with communication related signals such as classical CAN, CAN-FD, LIN interfaced and UART. DIO connector deals digital I/O, Frequency Capture, and interrupts.

**12-pin connector details:**
- Manufacturer: Molex
- Part Number: 0367831201
- 12 Pin header Connector
- 3.20mm Pitch
- 10.5A maximum current per contact
- 28V DC maximum voltage
- Temperature Range - Operating -40° to +105°C

**34-Pin header Connector details:**
- Manufacturer: JAE Electronics
- Part Number: MX23A34NF1
- 2.50mm Pitch
- Board Guide
- Low profiled type with board mounting height of 18.3mm and socket connector height of 22.2mm.
- 3A rated current.
- Temperature Range - Operating -40° to +125°C

Following are the system I/O Connectors
2. ANA Connector – Analog input signal/s interfacing.
3. COM Connector – Communication signal/s interfacing.
5.1 IPD Connector

A 12-pin connector is dedicated for IPD (Intelligent Power Devices), the 4 outputs on the connector are driven by protected High-side switches working from the 12V Bus Net Power. IPD’s also provide diagnostic function to monitor the fault conditions occurring on the output or load side.

Note:
Mating Connector MX23A34SF1
Includes in BOM

Caution: VBUS_EXT_PIN must be supplied from external 12V DC supply connection only, IPD’s will not source from Primary Supply of the Inverter Board. The J10 connector outputs can only be used with the presence of the 12V DC Supply.

Table 5-1 IPD Connector electrical details

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Signal Name</th>
<th>5V</th>
<th>12V</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT3</td>
<td>x</td>
<td>✓</td>
<td>Output</td>
<td>Output signal 3 from the IPD Device (U30) to external system</td>
</tr>
<tr>
<td>2</td>
<td>OUT2</td>
<td>x</td>
<td>✓</td>
<td>Output</td>
<td>Output signal 2 from the IPD Device (U29) to external system</td>
</tr>
<tr>
<td>3</td>
<td>OUT1</td>
<td>x</td>
<td>✓</td>
<td>Output</td>
<td>Output signal 1 from the IPD Device (U26) to external system</td>
</tr>
<tr>
<td>4</td>
<td>OUT4</td>
<td>x</td>
<td>✓</td>
<td>Output</td>
<td>Output signal 4 from the IPD Device (U27) to external system</td>
</tr>
<tr>
<td>5</td>
<td>VBUS_EXT_PIN</td>
<td>x</td>
<td>✓</td>
<td>Power</td>
<td>VBUS_EXT_PIN, 12V supply to IPD devices in the board</td>
</tr>
<tr>
<td>6</td>
<td>VBUS_EXT_PIN</td>
<td>-</td>
<td>✓</td>
<td>Power</td>
<td>VBUS_EXT_PIN, 12V supply to IPD devices in the board</td>
</tr>
<tr>
<td>7</td>
<td>VBUS_EXT_GND_PIN</td>
<td>-</td>
<td>-</td>
<td>Ground</td>
<td>VBUS_EXT_GND_PIN, connected to IPD device</td>
</tr>
<tr>
<td>8</td>
<td>VBUS_EXT_GND_PIN</td>
<td>-</td>
<td>-</td>
<td>Ground</td>
<td>VBUS_EXT_GND_PIN, connected to IPD device</td>
</tr>
<tr>
<td>9</td>
<td>VBUS_EXT_GND_PIN</td>
<td>-</td>
<td>-</td>
<td>Ground</td>
<td>VBUS_EXT_GND_PIN, connected to IPD device</td>
</tr>
<tr>
<td>10</td>
<td>VBUS_EXT_GND_PIN</td>
<td>-</td>
<td>-</td>
<td>Ground</td>
<td>VBUS_EXT_GND_PIN, connected to IPD device</td>
</tr>
<tr>
<td>11</td>
<td>VBUS_EXT_PIN</td>
<td>x</td>
<td>✓</td>
<td>Power</td>
<td>VBUS_EXT_PIN, 12V supply to IPD devices in the board</td>
</tr>
<tr>
<td>12</td>
<td>VBUS_EXT_PIN</td>
<td>x</td>
<td>✓</td>
<td>Power</td>
<td>VBUS_EXT_PIN, 12V supply to IPD devices in the board</td>
</tr>
</tbody>
</table>
5.2 ANA Connector

ANA Connector provides the analog input interfaces such as Resolver sin/ cos signals, Pedal, Brake and Temperature sensor inputs. Up to 6 analog inputs are available additionally for the user specific analog signal interfacing. The connector also provides uni-directional 5V DC Power Supply for sensor interfacing.

**Caution:** The ANA connector signals can be used as Analog inputs only and no digital input can be interfaced.

![Figure 5-2 ANA Connector details](image)

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Signal Name</th>
<th>5V</th>
<th>12V</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DC_RES_SIN_PIN</td>
<td>✓</td>
<td>✗</td>
<td>Input Analog signal related to RDC sine from ext. system to ADC of MCU (U2)</td>
</tr>
<tr>
<td>2</td>
<td>DC_RES_COS_PIN</td>
<td>✓</td>
<td>✗</td>
<td>Input Analog signal related to RDC cosine from ext. system to ADC of MCU (U2)</td>
</tr>
<tr>
<td>3</td>
<td>RES_S3_PIN</td>
<td>✗</td>
<td>✗</td>
<td>Input RDC S3 input signal from the external system to RDC of MCU (U2)</td>
</tr>
<tr>
<td>4</td>
<td>RES_S1_PIN</td>
<td>✗</td>
<td>✗</td>
<td>Input RDC S1 input signal from the external system to RDC of MCU (U2)</td>
</tr>
<tr>
<td>5</td>
<td>RES_S4_PIN</td>
<td>✗</td>
<td>✗</td>
<td>Input RDC S4 input signal from the external system to RDC of MCU (U2)</td>
</tr>
<tr>
<td>6</td>
<td>RES_S2_PIN</td>
<td>✗</td>
<td>✗</td>
<td>Input RDC S2 input signal from the external system to RDC of MCU (U2)</td>
</tr>
<tr>
<td>7</td>
<td>RES_R1_PIN</td>
<td>✗</td>
<td>✓</td>
<td>Output RDC Output R1 from RDC of MCU (U2) to external system.</td>
</tr>
<tr>
<td>8</td>
<td>RES_R2_PIN</td>
<td>✗</td>
<td>✓</td>
<td>Output RDC Output R2 from RDC of MCU (U2) to external system.</td>
</tr>
<tr>
<td>9</td>
<td>ANALOG_IN6</td>
<td>✓</td>
<td>✓</td>
<td>Input Analog input 6 signal from ext. system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>10</td>
<td>ANALOG_IN5</td>
<td>✓</td>
<td>✓</td>
<td>Input Analog input 5 signal from ext. system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>11</td>
<td>ANALOG_IN4</td>
<td>✓</td>
<td>✓</td>
<td>Input Analog input 4 signal from ext. system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>12</td>
<td>ANALOG_IN3</td>
<td>✓</td>
<td>✓</td>
<td>Input Analog input 3 signal from ext. system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>13</td>
<td>PEDAL_SENS_IN</td>
<td>✓</td>
<td>✓</td>
<td>Input Pedal sense input signal from ext. system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>14</td>
<td>BRAKE_SENS_IN</td>
<td>✓</td>
<td>✓</td>
<td>Input Brake sense input signal from ext. system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>15</td>
<td>TEMP_SENS2_IN</td>
<td>✓</td>
<td>✓</td>
<td>Input Temperature sense 2 input signal from ext. system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>16</td>
<td>TEMP_SENS1_IN</td>
<td>✓</td>
<td>✓</td>
<td>Input Temperature sense 1 input signal from ext. system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>17</td>
<td>ANALOG_IN1</td>
<td>✓</td>
<td>✓</td>
<td>Input Analog input 1 signal from external system to ADC of MCU (U2).</td>
</tr>
<tr>
<td>18</td>
<td>DC_RES_VS+</td>
<td>✓</td>
<td>✓</td>
<td>Power DC_RES_VS+, Power supply from board to connector.</td>
</tr>
<tr>
<td>19</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>20</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>21</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>22</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>23</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>24</td>
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<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
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<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
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<tr>
<td>26</td>
<td>SGND</td>
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<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
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<tr>
<td>27</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>28</td>
<td>ANALOG_SENS+</td>
<td>✓</td>
<td>✓</td>
<td>Power ANALOG_SENS+, Power supply from board to connector.</td>
</tr>
<tr>
<td>29</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND Connected to signal ground</td>
</tr>
<tr>
<td>30</td>
<td>PEDAL_VS+</td>
<td>✓</td>
<td>✓</td>
<td>Power PEDAL_VS+, Power supply from board to connector.</td>
</tr>
<tr>
<td>31</td>
<td>BRAKE_VS+</td>
<td>✓</td>
<td>✓</td>
<td>Power BRAKE_VS+, Power supply from board to connector.</td>
</tr>
<tr>
<td>32</td>
<td>TEMP_VS2+</td>
<td>✓</td>
<td>✓</td>
<td>Power TEMP_VS2+, Power supply from board to connector.</td>
</tr>
<tr>
<td>33</td>
<td>TEMP_VS1+</td>
<td>✓</td>
<td>✓</td>
<td>Power TEMP_VS1+, Power supply from board to connector.</td>
</tr>
<tr>
<td>34</td>
<td>ANALOG_IN2</td>
<td>✓</td>
<td>✓</td>
<td>Input Analog input 2 signal from external system to ADC of MCU (U2).</td>
</tr>
</tbody>
</table>
5.3 COM Connector

COM Connector provides communication interfaces from C1M-A1 for interfacing other ECU, Sensors and external diagnostic tools. Communication interfaces are available with and without isolation, please see the details for the isolated interfaces.

- 3 Nos Non-isolated CAN / CAN-FD
- 3 Nos LIN
- 2 Nos SENT
- 2 Nos “Isolated” UART
- 1 Nos “Isolated” CAN / CAN-FD

Figure 5-3 COM Connector details

Caution: “Isolated” interfaces UART & CAN require Power to be provided on the isolated side of the interface. CAN_ISO_5V, UART0_ISO_PWR_PIN & UART1_ISO_PWR_PIN must be supplied with 5V DC externally and respective CAN_ISO_GND, UART0_ISO_GND_PIN & UART1_ISO_GND_PIN must be connected to GND separately.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Signal Name</th>
<th>5V</th>
<th>12V</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CAN2 P</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>CAN2 P differential pair signal from isolated CAN-FD (U8)</td>
</tr>
<tr>
<td>2</td>
<td>CAN2 N</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>CAN2 N differential pair signal from isolated CAN-FD (U8)</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>No Connection</td>
</tr>
<tr>
<td>4</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>5</td>
<td>CAN3 P</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>CAN3 P differential pair signal from non-isolated CAN (U7)</td>
</tr>
<tr>
<td>6</td>
<td>CAN3 N</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>CAN3 N differential pair signal from non-isolated CAN (U7)</td>
</tr>
<tr>
<td>7</td>
<td>CAN1 P</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>CAN1 P differential pair signal from non-isolated CAN (U6)</td>
</tr>
<tr>
<td>8</td>
<td>CAN1 N</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>CAN1 N differential pair signal from non-isolated CAN (U6)</td>
</tr>
<tr>
<td>9</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>10</td>
<td>CAN0 P</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>CAN0 P differential pair signal from non-isolated CAN (U6)</td>
</tr>
<tr>
<td>11</td>
<td>CAN0 N</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>CAN0 N differential pair signal from non-isolated CAN (U6)</td>
</tr>
<tr>
<td>12</td>
<td>RXD1PIN</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>UART(U11) receiver signal</td>
</tr>
<tr>
<td>13</td>
<td>TXD1PIN</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>UART(U11) transmit signal</td>
</tr>
<tr>
<td>14</td>
<td>RLIN2</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>LIN Transceiver (U9) I/O</td>
</tr>
<tr>
<td>15</td>
<td>RLIN1</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>LIN Transceiver (U9) I/O</td>
</tr>
<tr>
<td>16</td>
<td>UART0_ISO_GND_PIN</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Isolated ground for U10</td>
</tr>
<tr>
<td>17</td>
<td>RXD0PIN</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>UART(U10) receiver signal</td>
</tr>
<tr>
<td>18</td>
<td>CAN_ISO_5V</td>
<td>✓</td>
<td>✓</td>
<td>Power</td>
<td>Power supply to isolated CAN-FD (U8)</td>
</tr>
<tr>
<td>19</td>
<td>CAN_ISO_GND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Isolated ground to CAN-FD (U8)</td>
</tr>
<tr>
<td>20</td>
<td>NC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>No Connection</td>
</tr>
<tr>
<td>21</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>22</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>23</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>24</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>25</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>26</td>
<td>SGND</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>27</td>
<td>SENTIF1PIN</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>RSENT1 data input from the external system to MCU (U2)</td>
</tr>
<tr>
<td>28</td>
<td>SENTIF2PIN</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>RSENT2 data input from the external system to MCU (U2)</td>
</tr>
<tr>
<td>29</td>
<td>UART1_ISO_PWR_PIN</td>
<td>✓</td>
<td>✓</td>
<td>Power</td>
<td>Power supply to isolated UART(U11)</td>
</tr>
<tr>
<td>30</td>
<td>UART1_ISO_GND_PIN</td>
<td>-</td>
<td>-</td>
<td>GND</td>
<td>Isolated ground to UART (U11)</td>
</tr>
<tr>
<td>31</td>
<td>RLIN_VS</td>
<td>✓</td>
<td>✓</td>
<td>Power</td>
<td>RLIN_VS, power supply to the COM</td>
</tr>
<tr>
<td>32</td>
<td>RLIN0</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>LIN Transceiver (U9) I/O</td>
</tr>
<tr>
<td>33</td>
<td>UART0_ISO_PWR_PIN</td>
<td>✓</td>
<td>✓</td>
<td>Power</td>
<td>Power supply to isolated UART(U10)</td>
</tr>
<tr>
<td>34</td>
<td>TXD0PIN</td>
<td>✓</td>
<td>✓</td>
<td>I/O</td>
<td>UART(U10) transmit signal</td>
</tr>
</tbody>
</table>
5.4 DIO Connector

DIO Connector provides digital input and output signal interfaces. For details refer the schematics to understand the Active low or Active High input support. Additionally, this connector also provides input for Hall sensor and Encoder interface for Motor control. The digital inputs are available as logic inputs, interrupts and frequency capture by selecting right function of the MCU port. The digital outputs can be configured as logic output or PWM output subject to the port configuration of the MCU.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Signal Name</th>
<th>5V</th>
<th>12V</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT4PIN</td>
<td>✓</td>
<td>✓</td>
<td>Output</td>
</tr>
<tr>
<td>2</td>
<td>_IN1PIN</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>3</td>
<td>ENC_IN1</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>4</td>
<td>ENC_IN0</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>5</td>
<td>FREQ_IN0PIN</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>6</td>
<td>FREQ_IN1PIN</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>7</td>
<td>HAL_W_PIN</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>8</td>
<td>HAL_V_PIN</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
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<td>9</td>
<td>HALL_U_PIN</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>10</td>
<td>CON_IN2PIN</td>
<td>✓</td>
<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>11</td>
<td>IN5PIN</td>
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<td>✓</td>
<td>Input</td>
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<td>Input</td>
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<td>✓</td>
<td>Input</td>
</tr>
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<td>✓</td>
<td>Input</td>
</tr>
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<td>17</td>
<td>IN1PIN</td>
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<td>✓</td>
<td>Input</td>
</tr>
<tr>
<td>18</td>
<td>OUT3PIN</td>
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<td>✓</td>
<td>Output</td>
</tr>
<tr>
<td>19</td>
<td>SGND</td>
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<td>✓</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>20</td>
<td>OUT2PIN</td>
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<td>Output</td>
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<td>22</td>
<td>IN8PIN</td>
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<td>Input</td>
</tr>
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<td>✓</td>
<td>Power</td>
</tr>
<tr>
<td>24</td>
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<td>✓</td>
<td>✓</td>
<td>Power</td>
</tr>
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<td>25</td>
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<td>✓</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>26</td>
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<td>✓</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
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<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>28</td>
<td>SGND</td>
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<td>✓</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>29</td>
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<td>✓</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>30</td>
<td>SGND</td>
<td>✓</td>
<td>✓</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
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<td>31</td>
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<td>32</td>
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<td>✓</td>
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</tr>
<tr>
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<td>SGND</td>
<td>✓</td>
<td>✓</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
<tr>
<td>34</td>
<td>SGND</td>
<td>✓</td>
<td>✓</td>
<td>Connected to Signal Ground (SGND)</td>
</tr>
</tbody>
</table>

Figure 5-4 DIO Connector details
6. Microcontroller functional Mapping

The Microcontroller used in the reference design is RH850/C1M-A1, part # R7F701278EAFP is 176-pin plastic QFP (0.5-mm pin pitch). The CPU is supporting Lock-Step Dual Core (Main Core + Checker Core) and consists of G3MH core operating at 240MHz and supports FPU (Floating Point Unit) and MPU (Memory Protection Unit). Additionally, there is support for Internal Peripheral Guard (IPG) and System Error notification control function (SEG).

Some important safety and security H/W IP provided on-chip are as follows:
- Clock Monitor (CLMA)
- Error Control Module (ECM)
- Error Correcting Coding (ECC)
- Data CRC (DCRA)
- Intelligent Cryptographic Unit E (ICUSE)
- Secure Watchdog Timer A (SWDTA)

For reference design of inverter, we have mapped the relevant peripherals allowing options to evaluate almost all the peripheral features of the device relevant for this application. From Top Level, we have mapped inverter application based on the I/O requirements, such as Analog Interfaces, PWM for Motor Drive, Communication Interfaces (UART, SPI, CAN, LIN and SENT).

For Motor Control Specific H/W IP on-chip include Embedded Motor Unit (EMU3) and resolver to digital converter (RDC3), these peripherals in conjunction with on-chip ADC and TSG (Timer Module) enable inverter function for Motor control. For details refer to the User’s Manual of RH850/C1M-Ax.
6.1 Device Functional Mapping Summary:

The RH850/C1M-A1 device functions are mapped based on the following categories:


Note: Please contact Renesas Support for Pin Mapping Excel for RH850/C1M-A1 for your use.
### 6.1.1 System Functions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>A2VREFH</td>
<td>A2VREFH</td>
<td>-0.3 to A2VCC + 0.3</td>
</tr>
<tr>
<td>5</td>
<td>A2VCC</td>
<td>A2VCC</td>
<td>4.5 V to 5.5 V Power for SAR AD</td>
</tr>
<tr>
<td>6</td>
<td>A2VSS</td>
<td>A2VSS</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>7</td>
<td>A1VCC</td>
<td>A1VCC</td>
<td>4.5 V to 5.5 V Power for SAR AD</td>
</tr>
<tr>
<td>8</td>
<td>A1VREFH</td>
<td>A1VREFH</td>
<td>-0.3 to A1VCC + 0.3</td>
</tr>
<tr>
<td>9</td>
<td>A1VSS</td>
<td>A1VSS</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>24</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>25</td>
<td>VDD</td>
<td>VDD</td>
<td>1.25V (Typ.) Power for the core (direct power supply) and connection of the stabilizing capacitor for core power</td>
</tr>
<tr>
<td>32</td>
<td>RVCC</td>
<td>RVCC</td>
<td>4.5 V to 5.5 V Power for RDC</td>
</tr>
<tr>
<td>33</td>
<td>RVSS</td>
<td>RVSS</td>
<td>Resolver Ground</td>
</tr>
<tr>
<td>44</td>
<td>A0VREFH</td>
<td>A0VREFH</td>
<td>-0.3 to A0VCC + 0.3</td>
</tr>
<tr>
<td>45</td>
<td>A0VSS</td>
<td>A0VSS</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>47</td>
<td>A0VCC</td>
<td>A0VCC</td>
<td>4.5 V to 5.5 V Power for SAR AD</td>
</tr>
<tr>
<td>50</td>
<td>VDD</td>
<td>VDD</td>
<td>1.25V (Typ.) Power for the core (direct power supply) and connection of the stabilizing capacitor for core power</td>
</tr>
<tr>
<td>52</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>66</td>
<td>VCC</td>
<td>VCC</td>
<td>4.5 V to 5.5 V Power for oscillator, flash programming, and ports</td>
</tr>
<tr>
<td>68</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>70</td>
<td>VDD</td>
<td>VDD</td>
<td>1.25V (Typ.) Power for the core (direct power supply) and connection of the stabilizing capacitor for core power</td>
</tr>
<tr>
<td>82</td>
<td>VDD</td>
<td>VDD</td>
<td>1.25V (Typ.) Power for the core (direct power supply) and connection of the stabilizing capacitor for core power</td>
</tr>
<tr>
<td>84</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>95</td>
<td>VDD</td>
<td>VDD</td>
<td>1.25V (Typ.) Power for the core (direct power supply) and connection of the stabilizing capacitor for core power</td>
</tr>
<tr>
<td>97</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>99</td>
<td>VCC</td>
<td>VCC</td>
<td>4.5 V to 5.5 V Power for oscillator, flash programming, and ports</td>
</tr>
<tr>
<td>110</td>
<td>VDD</td>
<td>VDD</td>
<td>1.25V (Typ.) Power for the core (direct power supply) and connection of the stabilizing capacitor for core power</td>
</tr>
<tr>
<td>112</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>117</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>119</td>
<td>VCC</td>
<td>VCC</td>
<td>4.5 V to 5.5 V Power for oscillator, flash programming, and ports</td>
</tr>
<tr>
<td>120</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>121</td>
<td>SYSVCC</td>
<td>SYSVCC</td>
<td>4.5 V to 5.5 V Power for system logic</td>
</tr>
<tr>
<td>126</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>128</td>
<td>SYSVCC</td>
<td>SYSVCC</td>
<td>4.5 V to 5.5 V Power for system logic</td>
</tr>
<tr>
<td>129</td>
<td>VCC</td>
<td>VCC</td>
<td>4.5 V to 5.5 V Power for oscillator, flash programming, and ports</td>
</tr>
<tr>
<td>130</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>144</td>
<td>VDD</td>
<td>VDD</td>
<td>1.25V (Typ.) Power for the core (direct power supply) and connection of the stabilizing capacitor for core power</td>
</tr>
<tr>
<td>146</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>147</td>
<td>VCC</td>
<td>VCC</td>
<td>4.5 V to 5.5 V Power for oscillator, flash programming, and ports</td>
</tr>
<tr>
<td>166</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>172</td>
<td>VDD</td>
<td>VDD</td>
<td>1.25V (Typ.) Power for the core (direct power supply) and connection of the stabilizing capacitor for core power</td>
</tr>
<tr>
<td>174</td>
<td>VSS</td>
<td>VSS</td>
<td>Ground</td>
</tr>
</tbody>
</table>

**Figure 6-2 Power Supply Pins**

AS PER SECTION: 39.2.19 OF REV1.10 USERS MANUAL

UNDER RESET:
- VDD SUPPLY CURRENT = 335mA [MAX]
- VCC SUPPLY CURRENT = 15mA [MAX]
- SYSVCC SUPPLY CURRENT = 3mA [MAX]

NORMAL OPERATION:
- VDD SUPPLY CURRENT = 540mA [MAX]
- VCC SUPPLY CURRENT = 60mA [MAX]
- SYSVCC SUPPLY CURRENT = 7mA [MAX]
- A0VCC, A1VCC, A2VCC SUPPLY CURRENT = 30mA [MAX]
- A0VREF, A1VREF, A2VREF SUPPLY CURRENT = 0.5mA [MAX]

CURRENT MEASUREMENT SUPPORT:
- R-IDD is for measurement of Core current
- RAVCC is for measurement of analog supply current
- R-ICC is for measurement of system logic current (will include I/O port and not match 39.2.19)
## Figure 6-3 System Pins

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>116</td>
<td>X2</td>
<td>X2</td>
<td>Crystal oscillator connections</td>
</tr>
<tr>
<td>118</td>
<td>X1</td>
<td>X1</td>
<td>Crystal oscillator connections</td>
</tr>
<tr>
<td>122</td>
<td>MD1</td>
<td>MD1</td>
<td>Operating mode select pin</td>
</tr>
<tr>
<td>124</td>
<td>RESET</td>
<td>RESET</td>
<td>External reset input</td>
</tr>
<tr>
<td>125</td>
<td>FLMODE</td>
<td>FLMODE</td>
<td>Operating mode select pin</td>
</tr>
<tr>
<td>127</td>
<td>MD0</td>
<td>MD0</td>
<td>Operating mode select pin</td>
</tr>
</tbody>
</table>

**CAUTION:** DO NOT PRESS SW1 when DEBUGGER (E1/ E2) is connected to the system.

## Figure 6-4 Debug Pins

**CAUTION:** DO NOT PRESS SW1 when DEBUGGER (E1/ E2) is connected to the system.

## Figure 6-5 Debugger Connectors
6.1.2 Reset Function

The Reset Circuit is a logical implementation with waterfall priority triggering interrupt or system reset. C1M_RESET is prioritized based on the critical signals on-board that can potentially damage the system if it continues to function under fault.

<table>
<thead>
<tr>
<th>Priority</th>
<th>C1M-RESET CAUSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>PMIC_RESET</td>
</tr>
<tr>
<td>2</td>
<td>E1_RESET</td>
</tr>
<tr>
<td>1</td>
<td>EMERGENCY_STOP</td>
</tr>
<tr>
<td>1</td>
<td>CKT_FAULT</td>
</tr>
</tbody>
</table>

Design Consideration for Fault Monitoring:

The design implements Over Current and Voltage Monitoring by window comparator functions, therefore, if the signal falls out of bound of their respective upper / lower limits then trigger is generated notifying the controller of the fault. OCP_FAULTx are current monitoring for DC Bus and Motor Phase currents. DC_FAULT is DC BUS monitoring and GDU_FAULT is Gate-driver Supply monitoring output. The CKT_FAULT is combined fault signal. The Priority of CKT_FAULT is same as EMERGENCY_STOP signal and is lower than the priority of E1_RESET and PMIC_RESET. C1M_RESET is direct Push-button hard reset for MCU.

Priority C1M_RESET > PMIC_RESET > E1_RESET > EMERGENCY_STOP == CKT_FAULT.

Unmount R386 to disable the CKT_FAULT reset generation capability, R228 Pull-up will take care of keeping the EMERGENCY_STOP, E1_RESET and PMIC_RESET functionality in-tact.
6.2 Motor control
Design Consideration for Motor control functions:

Motor control signaling includes Input (Sensor input / triggers) and output (PWM Signal). Using the on-chip peripherals there is combination of peripherals that can be deployed for implementing Inverter Motor control. The ADC, RDC3A & ENCA peripherals are used for sensor and analog interfaces, while TSG and TAUD timer modules are used for PWM generation.

6.2.1 Encoder Input

Rotor Position Sensor Interface is achieved using digital and analog signals from the sensor in use. The on-chip peripheral like ENCA provides the functionality to utilize the Encoder input pins to connect incremental encoder (A, B & Z) as well as Hall sensor signals (HA, HB, HC), the selection is possible depending on the mode of operation. However, same pins are used from MCU side, therefore, user can either connect incremental encoder or Hall Sensor.

As you can see below, for ease of use, we have listed Encoder input pins as HALL_U_PIN, HALL_V_PIN and HALL_W_PIN connecting them to Encoder inputs ENCA0E0, ENCA0E1 and ENCA0EC pins of MCU, respectively.

**Figure 6-7 Encoder / Hall sensor Interface**

**IMPORTANT**: When no sensor is connected to these connector pins, then, the pins will show ‘High’ due to pull-up to EVCC. Logic ‘HIGH’ indicates no motion when using encoder function and invalid pattern when using Hall-sensors, therefore, this is the safe state. The series diode ensure that only Active ‘Low’ signal is captured and any voltage above EVCC when applied to these input pins is blocked preventing damage to the MCU pins.
6.2.2 RDC Input

The R/D (resolver-to-digital) converter 3A converts the analog value (angle information) indicating the rotor angle of the resolver into a 16-bit (at maximum) digital value. RDC3A allows interfacing VR resolver (e.g. Tamagawa Seiki), the RDC3A provides option to interface DC resolver with Sin/Cosine signal output for absolute rotor position sensing. Selection of VR resolver or DC resolver is matter of configuration and tweaking the Hardware Input circuit to support the DC signaling with correct offset.

**SENS**

Required Sensor Selection Function

Selects the required sensor.

0: Use the DC resolver

1: Use the VR resolver (default)

![Figure 6-8 Selection of DC or VR Resolver](image)

**Figure 6-8 Selection of DC or VR Resolver**

Note: The input resistance (RIN) tolerance (%) can affect the conversion accuracy (LSB). Approximately 0.3% corresponds with 1 LSB.

VCOSMNT, VSINMNT: Resolver signal monitor voltage

VCOM: IC internal reference voltage (= RVCC/2)

RF: 21 kΩ (typ). Subject to register setting and automatic adjustment function.

![Figure 6-9 VR Resolver Signal Input Circuit](image)

**Figure 6-9 VR Resolver Signal Input Circuit**

RIN: Resolver signal level

Adjust the signal level so that,

\[
\text{VCOSMNT or VSINMNT} = (\text{VIN}) \times (\text{RF} / (\text{RIN} + 600 \, \Omega)) \text{ falls within the range from } 0.36 \times \text{RVCC} \text{ to } 0.64 \times \text{RVCC} \, \text{[Vpp]},
\]

(\text{where VIN} \text{ denotes the signal output voltage between resolver pins [Vpp], } \text{RIN} \geq 2[k\Omega])

RH and RL: Determine a resistance value in an 89% to 100% range from the following calculated values:

1. \[\text{RH} = ((\text{RVCC} - \text{VCOM}) / (22.0 \times 10^{-6})) - \text{RIN}, \text{ where } \text{VCOM} = \text{RVCC}/2[V]\]
2. \[\text{RL} = (\text{VCOM}/(22.0 \times 10^{-6})) - \text{RIN}, \text{ where } \text{VCOM} = \text{RVCC}/2[V]\]
Note: The input resistance (RIN) tolerance (%) can affect the conversion accuracy (LSB). Approximately 0.3% corresponds with 1 LSB. Differences in input signal conditions and peripheral circuits can affect the RD conversion accuracy and the error detection function.

**Figure 6-10 DC Resolver Input Circuit**

**CAUTION:** The reference design implements the Excitation Voltage Booster Amplifier Circuit (Single Power Supply) on-board, allowing to interface VR resolver. If the DC resolver must be interfaced via RDC3A pins RDC3AnS1 (RDC3AnS2) and RDC3AnS3 (RDC3AnS4) then please consult Renesas technical support.

**Figure 6-11 RDC Input Circuit**

**IMPORTANT:** DC Resolver interface, Unmount the following: R96, R107, R114 and R127. The Applied DC Resolver SIN/COSINE signal must be applied with 2.5V DC offset for the RDC to compute angle correctly.
6.2.3 Output: TSG3 for 3 Phase Motor Control

The TSG3n is an 18-bit timer counter with various motor control functions, the counter clock of 80MHz offers minimum resolution of 12.5nsec. Independent dead-time can be set for positive to inverse phase change and vice-versa. Forced output stop function allows the Hi-z control of the TSG output pins TSG3nO1~O6. Additionally, ADC Trigger signal generation from the TSG compare match is possible without any software intervention.

Figure 6-12 TSG30 PWM Output with TAPA3ESO Hi-z Control
The HT-PWM mode is commonly used for Inverter control. In this mode, the 18-bit counter (up/down count by ±2 bits, practically 17 bits) and the 18-bit compare registers (LSB is used to control additional pulse) are used to generate a 6-phase PWM signal.

1. Set the carrier wave period to TSG3nCMP0E.

2. Set the duty cycle of the voltage data signals of the U phase, V phase, and W phase with TSG3nCMPUE, TSG3nCMPVE, and TSG3nCMPWE. (The values set to TSG3nCMPUE, TSG3nCMPVE, and TSG3nCMPWE are reflected immediately to the corresponding TSG3nCMPmE (m = 1, 2, 5, 6, 9, 10)).

3. The INTTSG3nIPEK interrupt (Peak Intr.) is generated only when TSG3nCTL4.TSG3nPRE = 1.

4. The INTTSG3nIVLY interrupt (Trough Intr.) is generated only when TSG3nCTL4.TSG3nVRE = 1.

5. The ADC conversion trigger can be enabled from TSG in HT-PWM mode, please refer User’s Manual for details.

Figure 6-13 HT-PWM Mode Block Diagram
The 120-DC Mode: In this mode, PWM output period set to TSG3nCMP0E and timer output (TSG3nO1 to TSG3nO6) according to the duty cycle set to TSG3nCMP1E to TSG3nCMP12E are controlled with three types of pattern inputs (software output control method, pattern switch method, and trigger switch method) to perform 120-DC control.

1. Set the PWM period to TSG3nCMP0E.
2. Set the PWM duty to TSG3nCMP1E to TSG3nCMP12E and set the output pattern to TSG3nPAT0W and TSG3nPAT1W.
3. INTTSG3nIPEK Peak interrupt (generated at the same timing as INTTSG3nI0)
4. INTTSG3nIWN Warning interrupt → when illegal pattern is detected.
5. The ADC conversion trigger can be enabled from TSG in HT-PWM mode, please refer User’s Manual for details.

![120-DC Mode Block Diagram](image)

**Figure 6-14 120-DC Mode Block Diagram**

**Figure 6-15 ENCAnEx to TSG3nPTS\textsubscript{Ix} signal via PIC1B**

**IMPORTANT**: The TSG3nPTS\textsubscript{Ix} pin signal shown in Fig 6-13 is connected to ENCAnEx pin of the MCU. There is no TSG3nPTS\textsubscript{Ix} pin on the MCU.
6.2.4 Output: TAUD for 3 Phase Motor Control

The high accuracy triangle wave PWM output function with the dead time is realized by using the triangle wave PWM output function/one-shot pulse output function of TAUD0 and PIC1B in combination. The following figure shows the block diagram of the high accuracy triangle wave PWM output function with the dead time.
### 6.2.5 Output: Hi-z Control

Abnormal operation in timer motor-control under CPU control leads to rotation of the externally connected motor also becoming abnormal. In such a case, this function forcibly sets the motor control output to the Hi-Z state, independently of control by the CPU.

TAPA3 connects ESO3 to enable Hi-z control of TSG30 6-phase PWM outputs.

TAPA0 connects ESO0 to enable Hi-z control of TAUD0 PWM Outputs.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 0</th>
<th>Register to be Controlled</th>
<th>TAPA to be Connected</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC1BHIZCEN00</td>
<td>ERROROUTZ</td>
<td>—</td>
<td>—</td>
<td>ESO0</td>
<td>TAUD0</td>
<td>TAPA0</td>
</tr>
<tr>
<td>PIC1BHIZCEN01</td>
<td>ERROROUTZ</td>
<td>—</td>
<td>—</td>
<td>ESO1</td>
<td>TAUD1</td>
<td>TAPA1</td>
</tr>
<tr>
<td>PIC1BHIZCEN02</td>
<td>ERROROUTZ</td>
<td>—</td>
<td>INTTSG3IER</td>
<td>ESO3</td>
<td>TSG30</td>
<td>TAPA3</td>
</tr>
<tr>
<td>PIC1BHIZCEN03</td>
<td>ERROROUTZ</td>
<td>INTTSG31IER</td>
<td>—</td>
<td>ESO4</td>
<td>TSG31</td>
<td>TAPA4</td>
</tr>
<tr>
<td>PIC1BHIZCEN10+1</td>
<td>ERROROUTZ</td>
<td>—</td>
<td>—</td>
<td>ESO2</td>
<td>TAUD2</td>
<td>TAPA2</td>
</tr>
<tr>
<td>PIC1BHIZCEN12+1</td>
<td>ERROROUTZ</td>
<td>—</td>
<td>INTTSG32IER</td>
<td>ESO5</td>
<td>TSG32</td>
<td>TAPA5</td>
</tr>
</tbody>
</table>

Figure 6-18 Circuit Fault Signal Connects to PWM Hi-z Control.
6.2.6 Motor Control with RDC3A and EMU3

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>RDC3A0COSMNT</td>
<td>RDC3A0COSMNT</td>
<td>COS-side monitoring signal output</td>
</tr>
<tr>
<td>23</td>
<td>RDC3A0SINMNT</td>
<td>RDC3A0SINMNT</td>
<td>SIN-side monitoring signal output</td>
</tr>
<tr>
<td>26</td>
<td>RDC3A0S4</td>
<td>RDC3A0S4</td>
<td>Resolver signal input</td>
</tr>
<tr>
<td>27</td>
<td>RDC3A0S3</td>
<td>RDC3A0S3</td>
<td>Resolver signal input</td>
</tr>
<tr>
<td>28</td>
<td>RDC3A0S1</td>
<td>RDC3A0S1</td>
<td>Resolver signal input</td>
</tr>
<tr>
<td>29</td>
<td>RDC3A0S2</td>
<td>RDC3A0S2</td>
<td>Resolver signal input</td>
</tr>
<tr>
<td>30</td>
<td>RDC3A0RSO</td>
<td>RDC3A0RSO</td>
<td>Excitation signal input/output</td>
</tr>
<tr>
<td>31</td>
<td>RDC3A0CDM</td>
<td>RDC3A0CDM</td>
<td>Excitation common signal input/output</td>
</tr>
<tr>
<td>91</td>
<td>RDC3A0_OUT_W</td>
<td>RDC3A0_OUT_W</td>
<td>RDC0_OUT_W Encoder pulse output *-optional</td>
</tr>
<tr>
<td>92</td>
<td>RDC3A0_OUT_V</td>
<td>RDC3A0_OUT_V</td>
<td>RDC0_OUT_V Encoder pulse output *-optional</td>
</tr>
<tr>
<td>93</td>
<td>RDC3A0_OUT_U</td>
<td>RDC3A0_OUT_U</td>
<td>RDC0_OUT_U Encoder pulse output *-optional</td>
</tr>
<tr>
<td>139</td>
<td>TSG30O1</td>
<td>TSG30O1</td>
<td>Uphase +</td>
</tr>
<tr>
<td>140</td>
<td>TSG30O3</td>
<td>TSG30O3</td>
<td>Vphase +</td>
</tr>
<tr>
<td>141</td>
<td>TSG30O5</td>
<td>TSG30O5</td>
<td>Wphase +</td>
</tr>
<tr>
<td>142</td>
<td>TSG30O2</td>
<td>TSG30O2</td>
<td>Uphase -</td>
</tr>
<tr>
<td>143</td>
<td>TSG30O4</td>
<td>TSG30O4</td>
<td>Vphase -</td>
</tr>
<tr>
<td>145</td>
<td>TSG30O6</td>
<td>TSG30O6</td>
<td>Wphase -</td>
</tr>
<tr>
<td>169</td>
<td>TAPA3E5D</td>
<td>TAPA3E5D</td>
<td>Emergency Hi-Z request input (for TSG30 PWM) H/W Cut-off Trigger Input for PWM Output by TSG30</td>
</tr>
</tbody>
</table>

Figure 6-19 EMU30 Block Diagram

Figure 6-20 RDC3A Block Diagram
6.2.7 Motor Control with ENCA and EMU3

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>96</td>
<td>ENCA0E0</td>
<td>ENCA0E0 encoder input 0 (count pulse 0) - TSG30PTS0</td>
<td></td>
</tr>
<tr>
<td>98</td>
<td>ENCA0E1</td>
<td>ENCA0E1 encoder input 1 (count pulse 1) - TSG30PTS1</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>ENCA0EC</td>
<td>ENCA0EC encoder input (clear Pulse) - TSG30PTS2</td>
<td></td>
</tr>
<tr>
<td>102</td>
<td>TSG3003</td>
<td>Uphase +</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>104</td>
<td>TSG3005</td>
<td>Uphase +</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>106</td>
<td>TSG3002</td>
<td>Uphase -</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>108</td>
<td>TSG3004</td>
<td>Vphase -</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>110</td>
<td>TSG3006</td>
<td>Vphase -</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>112</td>
<td>TAPA3ESO</td>
<td>TAPA3ESO Emergency Hi-Z request input (for TSG30 PWM) H/W Cut-off Trigger Input for PWM Output by TSG30</td>
<td></td>
</tr>
</tbody>
</table>

6.2.8 Motor Control with ENCA and TAUD0 – 120 Deg Trapezoidal S/W Control

The ENCA0Ex pins can be used as Hall Sensor Input pins when using 120 Trapezoidal function using Software control implementation.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>96</td>
<td>ENCA0E0</td>
<td>ENCA0E0 encoder input 0 (count pulse 0) - TSG30PTS0</td>
<td>TSG30PTS0 is used as HALL SENSOR inputs in 120 deg Commutation mode.</td>
</tr>
<tr>
<td>98</td>
<td>ENCA0E1</td>
<td>ENCA0E1 encoder input 1 (count pulse 1) - TSG30PTS1</td>
<td>TSG30PTS1 is used as HALL SENSOR inputs in 120 deg Commutation mode.</td>
</tr>
<tr>
<td>100</td>
<td>ENCA0EC</td>
<td>ENCA0EC encoder input (clear Pulse) - TSG30PTS2</td>
<td>TSG30PTS2 is used as HALL SENSOR inputs in 120 deg Commutation mode.</td>
</tr>
<tr>
<td>103</td>
<td>TAPA0UP</td>
<td>TAPA0UP Motor control output U phase (positive)</td>
<td>TAUD Output</td>
</tr>
<tr>
<td>105</td>
<td>TAPA0VN</td>
<td>TAPA0VN Motor control output V phase (negative)</td>
<td>TAUD Output</td>
</tr>
<tr>
<td>107</td>
<td>TAPA0WU</td>
<td>TAPA0WU Motor control output W phase (positive)</td>
<td>TAUD Output</td>
</tr>
<tr>
<td>109</td>
<td>TAPA0WN</td>
<td>TAPA0WN Motor control output W phase (negative)</td>
<td>TAUD Output</td>
</tr>
<tr>
<td>112</td>
<td>TAPA0ESO</td>
<td>TAPA0ESO Emergency Hi-Z request input (for TAUD0 PWM) H/W Cut-off Trigger Input for PWM Output by TAUD0</td>
<td></td>
</tr>
</tbody>
</table>
### 6.2.9 Motor Control with ENCA and TSG30 – 120DC Mode H/W Control

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>96</td>
<td>ENCA0E0</td>
<td>ENCA0E0 encoder input 0 (count pulse 0) - TSG30PTSI0</td>
<td>TSG3nPTSI0 is used as HALL SENSOR inputs in 120 deg Commutation mode.</td>
</tr>
<tr>
<td>98</td>
<td>ENCA0E1</td>
<td>ENCA0E1 encoder input 1 (count pulse 1) - TSG30PTSI1</td>
<td>TSG3nPTSI1 is used as HALL SENSOR inputs in 120 deg Commutation mode.</td>
</tr>
<tr>
<td>100</td>
<td>ENCA0EC</td>
<td>ENCA0EC encoder input (clear Pulse) - TSG30PTSI2</td>
<td>TSG3nPTSI2 is used as HALL SENSOR inputs in 120 deg Commutation mode.</td>
</tr>
<tr>
<td>139</td>
<td>TSG3001</td>
<td>TSG3001 Uphase +</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>140</td>
<td>TSG3003</td>
<td>TSG3003 Vphase +</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>141</td>
<td>TSG3005</td>
<td>TSG3005 Wphase +</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>142</td>
<td>TSG3002</td>
<td>TSG3002 Uphase -</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>143</td>
<td>TSG3004</td>
<td>TSG3004 Vphase -</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>145</td>
<td>TSG3006</td>
<td>TSG3006 Wphase -</td>
<td>TSG PWM Output</td>
</tr>
<tr>
<td>169</td>
<td>TAPA3E50</td>
<td>TAPA3E50 Emergency Hi-Z request input (for TSG30 PWM)</td>
<td>H/W Cut-off Trigger Input for PWM Output by TSG30</td>
</tr>
</tbody>
</table>

![Figure 6-21 Example of 120DC Mode Operation](image-url)
6.3 Communication Functions

6.3.1 SPI Interface

SPI Communication is mapped to control PMIC and additional CS is provided to the user via on-board connector as shown below:

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>73</td>
<td>CSIHO5I</td>
<td>CSIHO5I</td>
<td>Serial data input signals</td>
</tr>
<tr>
<td>74</td>
<td>CSIHO5O</td>
<td>CSIHO5O</td>
<td>Serial data output signals</td>
</tr>
<tr>
<td>75</td>
<td>CSIHO5C</td>
<td>CSIHO5C</td>
<td>Serial clock input signal</td>
</tr>
<tr>
<td>76</td>
<td>CSIHOCSS0</td>
<td>CSIHOCSS0</td>
<td>Chip select signals</td>
</tr>
<tr>
<td>77</td>
<td>CSIHOCSS1</td>
<td>CSIHOCSS1</td>
<td>Chip select signals</td>
</tr>
</tbody>
</table>

**CAUTION:** EVCC = 5V is mapped to EXT_SPI, therefore, do not connect module operating at lower voltage such as 3.0V / 3.3V / 3.6V / 4.2V. If the EVCC is used for powering the external module, then due care to be taken by user, so that, it does not cause any harm to external module or Inverter control board power supply.
6.3.2 UART Interface

The 2 Nos of UART Channels are provided to the user for communicating externally. The Signals are isolated and therefore, require external power to be provided on the isolated side. E.g., if UART to USB module is connected to the Inverter via port then UARTx_ISO_PWR_PIN needs to be powered by 3.0V ~ 5V from the module side and on the Microcontroller side the isolator is powered by EVCC = 5V as shown in schematic. Refer COM Connector Detail for UARTx_ISO_PWR_PIN.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>49</td>
<td>SCI0RXD</td>
<td>SCI receive data</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>SCI0TXD</td>
<td>SCI transmit data</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>SCI2RXD</td>
<td>SCI receive data</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>SCI2TXD</td>
<td>SCI transmit data</td>
<td></td>
</tr>
</tbody>
</table>

**CAUTION:** Without Powering the Isolated side of the ADUM1286CRZ, communication cannot be established.
### 6.3.3 CAN Interface

The On-chip RS-CANFD Module support 2 interface modes:

1. **Classical CAN mode**: Handles only classical CAN frames.
2. **CAN FD mode**: Handles classical CAN frames and CAN FD frames.

This product supports ISO 11898-1:2015 compatible CAN FD with a new CRC field containing a stuff counter. It can also support the CRC field that conforms to ISO/CD 11898-1 (2014-08-12 version) when the NIE bit of the RSCFDnCFDGCRCCFG register is set to 1.

The RS-CANFD module support 320 Buffers in total for details refer User’s Manual & ECC is supported.

The reference design provides 4 CAN Channels to the user allowing to fully utilize the RS-CANFD.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>67</td>
<td>CAN0RX</td>
<td>CAN0RX</td>
<td>CANm receive data input</td>
</tr>
<tr>
<td>69</td>
<td>CAN0TX</td>
<td>CAN0TX</td>
<td>CANm transmit data output</td>
</tr>
<tr>
<td>71</td>
<td>CAN1RX</td>
<td>CAN1RX</td>
<td>CANm receive data input</td>
</tr>
<tr>
<td>72</td>
<td>CAN1TX</td>
<td>CAN1TX</td>
<td>CANm transmit data output</td>
</tr>
<tr>
<td>80</td>
<td>CAN3RX</td>
<td>CAN3RX</td>
<td>CANm receive data input</td>
</tr>
<tr>
<td>81</td>
<td>CAN3TX</td>
<td>CAN3TX</td>
<td>CANm transmit data output</td>
</tr>
<tr>
<td>134</td>
<td>CAN2RX</td>
<td>CAN2RX</td>
<td>CANm receive data input</td>
</tr>
<tr>
<td>135</td>
<td>CAN2TX</td>
<td>CAN2TX</td>
<td>CANm transmit data output</td>
</tr>
</tbody>
</table>

CAN0,1 and 3 provide Non-isolated Classic CAN interface via NCV7351D1ER2G transceiver. **EN Pin** on NCV7351D1E Version Allowing Switching the Transceiver to a **Very Low Current OFF Mode**.

![Figure 6-24 Non-Isolated CAN Interfaces](image)
CAN2 provides CANFD isolated interface via ADM3050EBRWZ. The transceiver features support for the following:

- 1.7 V to 5.5 V supply and logic side levels
- 4.5 V to 5.5 V supply on bus side
- ISO 11898-2:2016-compliant CAN FD
- Data rates up to 12 Mbps for CAN FD
- 5.7 kV rms signal isolated CAN FD transceiver

**CAUTION:** Without Powering the Isolated CAN BUS side of the ADM3050E, communication cannot be established.
### 6.3.4 LIN Interface

LIN communication controller that supports LIN Specification Package Revision 1.3, 2.0, 2.1, 2.2, and SAE J2602, and automatically performs frame communication and error determination.

Channel 0, 1 and 2 of LIN are mapped to the LIN transceiver on-board. Channel 1 of NCV7424 is not mapped.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>53</td>
<td>RLIN32RX</td>
<td>RLIN32RX</td>
<td>RLIN3m receive data input</td>
</tr>
<tr>
<td>54</td>
<td>RLIN32TX</td>
<td>RLIN32TX</td>
<td>RLIN3m transmit data output</td>
</tr>
<tr>
<td>55</td>
<td>RLIN31RX</td>
<td>RLIN31RX</td>
<td>RLIN3m receive data input</td>
</tr>
<tr>
<td>56</td>
<td>RLIN31TX</td>
<td>RLIN31TX</td>
<td>RLIN3m transmit data output</td>
</tr>
<tr>
<td>78</td>
<td>RLIN30RX</td>
<td>RLIN30RX</td>
<td>RLIN3m receive data input</td>
</tr>
<tr>
<td>79</td>
<td>RLIN30TX</td>
<td>RLIN30TX</td>
<td>RLIN3m transmit data output</td>
</tr>
</tbody>
</table>

**CAUTION:** RLIN_VS Power Supply for the LIN Transceiver is derived from the VBUS_EXT_PIN (expected to be 12V Power Bus Net). The maximum rated current for NCV7424D when transmitting Dominant bit is 28mA and therefore, Fuse F11 used here is 50mA. Therefore, ensure that RLIN_VS is present when troubleshooting LIN Communication.

Note the following mapping to avoid confusion while programming or referring LIN channels of MCU and Transceiver. This mapping was result of the PCB layout tracing.

**LIN Channel Mapping MCU & LIN Transceiver**

<table>
<thead>
<tr>
<th>Usage</th>
<th>MCU Channel</th>
<th>Transceiver Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Used</td>
<td>Channel 0</td>
<td>Channel 4</td>
</tr>
<tr>
<td>Used</td>
<td>Channel 1</td>
<td>Channel 3</td>
</tr>
<tr>
<td>Used</td>
<td>Channel 2</td>
<td>Channel 2</td>
</tr>
<tr>
<td>Unused</td>
<td>Channel 3</td>
<td>Channel 1</td>
</tr>
</tbody>
</table>

![Non-isolated LIN Interfaces Diagram](image-url)
6.3.5 SENT Interface

Single Edge Nibble Transmission module (RSENT) interface supports the following standard specification (SAE J2716 version JAN2010). Compatible with 3 systems, i.e., SENT standard (1-wire system), SPC extension (1-wire system), and SPC extension (2-wire system). Bidirectional communication: Between the sensor and MCU (supported in SPC mode). Data transmission protected with CRC is available. Multiple sensors can connect to the RSENT channel that has the standard expansion function. Received data from sensors is detected by software or DMA. Timestamp function: Master can only be set for RSENT0.

Variable data transmission rate
- 24.7 kbps to 64.9 kbps: 3 clock rate 6 nibble data
- 74.1 kbps to 194.7 kbps: 1 clock rate 6 nibble data

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>163</td>
<td>RSENT2RX</td>
<td>RSENT2RX</td>
<td>RSENT Input</td>
</tr>
<tr>
<td>165</td>
<td>RSENT2SPCO</td>
<td>RSENT2SPCO</td>
<td>RSENT Control Output</td>
</tr>
<tr>
<td>171</td>
<td>RSENT3RX</td>
<td>RSENT3RX</td>
<td>RSENT Input</td>
</tr>
<tr>
<td>173</td>
<td>RSENT3SPCO</td>
<td>RSENT3SPCO</td>
<td>RSENT Control Output</td>
</tr>
</tbody>
</table>

Reference design provides 2 channel SENT interfaces from channel 2 and Channel 3 as shown in the schematic below:

![Figure 6-27 RSENT Interface circuit](image)
6.4 Analog Functions

6.4.1 ADC Functional Mapping:

The C1M-A1 is equipped with 3 Unit of ADCCn, n=0,1 & 2. The ADCC resolution is 12-bit and each unit has multiple T&H (Track & Hold) inputs. The T&H circuit allows for simultaneous capture of Analog signal on Trigger. The analog input signals that must be group triggered are mapped to utilize the T&H feature provided by the ADCCn.

Each unit has 40 Virtual Channels to hold the conversion result. Analog ports on the device are dedicated pins for analog and no other function is available.

![Figure 6-28 ADCC0 Block Diagram](image-url)
Analog input Design Consideration:

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Mapped Functions</th>
<th>User Functions</th>
<th>Comment / Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ADCC2I02</td>
<td>U Phase voltage Sense</td>
<td>Optional implementation - required for Functional Safety - phase volatge monitoring</td>
</tr>
<tr>
<td>2</td>
<td>ADCC2I01</td>
<td>W Phase voltage Sense</td>
<td>Optional implementation - required for Functional Safety - phase volatge monitoring</td>
</tr>
<tr>
<td>3</td>
<td>ADCC2I00</td>
<td>V Phase voltage Sense</td>
<td>Optional implementation - required for Functional Safety - phase volatge monitoring</td>
</tr>
<tr>
<td>10</td>
<td>ADCC1I32</td>
<td>IPD_CS_OUT1</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>11</td>
<td>ADCC1I23</td>
<td>IPD_CS_OUT2</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>12</td>
<td>ADCC1I22</td>
<td>IPD_CS_OUT3</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>13</td>
<td>ADCC1I21</td>
<td>IPD_CS_OUT4</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>14</td>
<td>ADCC1I20</td>
<td>Analog Input</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>15</td>
<td>ADCC1I13</td>
<td>Coolant Temperature</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>16</td>
<td>ADCC1I12</td>
<td>Motor Temperature</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>17</td>
<td>ADCC1I11</td>
<td>Pedal Sensor</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>18</td>
<td>ADCC1I10</td>
<td>Brake Sensor</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>19</td>
<td>ADCC1I03</td>
<td>Sensor Vmonitor</td>
<td>On-board Sensor supply voltage monitoring</td>
</tr>
<tr>
<td>20</td>
<td>ADCC1I02</td>
<td>Pre-Drive Vmonitor</td>
<td>On-board pre driver Supply Monitor</td>
</tr>
<tr>
<td>21</td>
<td>ADCC1I31</td>
<td>Analog Input</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>34</td>
<td>ADCC0I21</td>
<td>Analog Input</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>35</td>
<td>ADCC0I20</td>
<td>Analog Input</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>36</td>
<td>ADCC0I13</td>
<td>Inverter Power Board Temperature 1</td>
<td>On-Board Temperature sensor1 monitoring Power Board temperature</td>
</tr>
<tr>
<td>37</td>
<td>ADCC0I12</td>
<td>Inverter Power Board Temperature 2</td>
<td>On-Board Temperature sensor2 monitoring Power Board temperature</td>
</tr>
<tr>
<td>38</td>
<td>ADCC0I11</td>
<td>DC Resolver Cosine Input</td>
<td>DC Resolver Input</td>
</tr>
<tr>
<td>39</td>
<td>ADCC0I10</td>
<td>DC Resolver Sine Input</td>
<td>DC Resolver Input</td>
</tr>
<tr>
<td>40</td>
<td>ADCC0I03</td>
<td>DC Bus Current</td>
<td>DC Bus Current Sensor input</td>
</tr>
<tr>
<td>41</td>
<td>ADCC0I02</td>
<td>U Phase Current Sense</td>
<td>25.1.2.53 EMU3n Input IP Control Register (EMU3nCTRINMD) - Refer CAUTION on the Mapping</td>
</tr>
<tr>
<td>42</td>
<td>ADCC0I01</td>
<td>W Phase Current Sense</td>
<td>25.1.2.53 EMU3n Input IP Control Register (EMU3nCTRINMD) - Refer CAUTION on the Mapping</td>
</tr>
<tr>
<td>43</td>
<td>ADCC0I00</td>
<td>V Phase Current Sense</td>
<td>25.1.2.53 EMU3n Input IP Control Register (EMU3nCTRINMD) - Refer CAUTION on the Mapping</td>
</tr>
<tr>
<td>46</td>
<td>ADCC0I30</td>
<td>VEXT Monitor</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>175</td>
<td>ADCC2I10</td>
<td>PMC Voltage Monitoring</td>
<td>Analog port only - cannot be used as IO</td>
</tr>
<tr>
<td>176</td>
<td>ADCC2I03</td>
<td>DC Bus Voltage</td>
<td>On-board DC Bus Voltage Sensor input</td>
</tr>
</tbody>
</table>

Motor Phase currents, DC Bus Current and DC resolver Sine and Cosine Input are mapped to ADCC0 on the channels that provide T&H circuit.

Gate Driver / Pre-Driver supply, Sensor supply, Brake Sensor, Pedal Sensor and Temperature monitoring inputs are then mapped onto ADCC1 on the channels that provide T&H circuit.

DC Bus Voltage and 3 Phase Motor voltages are mapped to ADCC2 on the channels that provide T&H circuit.

This mapping allows programmer to trigger start of conversion for all this inputs in a single instant. This also, enables formation of Scan Groups to start of conversion on a trigger and store the result in mapped virtual channel (result register).

**IMPORTANT:** The analog signals highlighted in “RED” text are fixed by circuit on-board and therefore, do not offer any generic interface to allow measurement of external analog signals.
6.4.2 MOSFET Gate Driver

The ISL78434 is Automotive Grade (AEC-Q100 Grade 1) high voltage, high frequency, half-bridge NMOS FET driver for driving the gates of up to 70V half-bridge topologies.

The ISL78434 has dual independent inputs for controlling the high-side and low-side driver separately. It has independent sourcing and sinking pins for each gate driver.

Patented gate-sensed adaptive dead time control provides shoot-through protection and minimized dead time.

Refer ISL78434 Datasheet for more technical details on the device specifications.

**Design Considerations:**

In design, MOSFET Pre-Driver stage consists of 3 ISL78434 ICs to drive the U, V & W Phase of the motor. These drivers are in the controller board, which controls gate signals of half-bridge for each phase in the Power board.

Controller board and Power board are interfaced through board-to-board connectors J11, J12 & J13, which carry high side and low side gate control signals for each phase from ISL78434.

These half-bridge drivers are controlled by MCU (U2), which control independently the high side and low side of the driver circuit. Each phase driver is controlled in accordance with the requirement by MCU.

A common enable signal for each driver is controlled by MCU (U2).

The high-side driver bias is handled by Bootstrap capacitor across the HB and HS pins, which provides proper gate drive to the high-side FET.

Zener diodes (D15, D16, D17, D21, D22 & D23) with a series current limiting resistor (R243, R247, R251, R300, R384 & R385) between HB & HS pins and HB & AGND pins provide over-voltage protection against violation of the electrical specification of the device.

**IMPORTANT:**

For best thermal performance, connect the driver EPAD to a low thermal impedance ground plane. Use as many vias as possible to connect the top layer PCB thermal land to GND planes on other PCB layers. Connect the VSS and AGND pins together through the EPAD to maintain a low impedance connection between the two pins.

**Protection Required:**

Voltage on HB (referenced to HS) = min 8V max 18V
Voltage on HB (referenced to VSS) = 86V MAXIMUM

**[CAUTION]**: Bootstrap related parameters: Average Current in VDD to HB FET is Max 100mA. Refer Section 5.2 Bootstrap Capacitor design.
Through 6 pin connectors, the Controller board and Power board are interfaced. As shown in below figure Half bridge gate control signals, thermistor excitation is done through EVCC (5V) and its feedback is taken through ANALOG_IN5 and ANALOG_IN6 signals.

**CAUTION:** J11, J12 & J13 must not be supplied from external source; the controller board supplies the source EVCC from on-board power supply.
### 6.4.3 Current Sensor

The LEM HC5FW family is for the electronic measurement of DC, AC or pulsed currents in high power and low voltage automotive applications with galvanic separation between the primary circuit (high power) and the secondary circuit (electronic circuit).

In this design four current sensors, HC5FW 500-S/SP1 are used to measure current consumption of DC Bus and each phase of motor individually. The measured signal is in range of 0V to 5V. The output of the sensor is connected to ADC of MCU, and op-amp based Schmitt trigger circuit for triggering fault conditions is implemented. Similar circuitry is implemented for each current measurement with low and high thresholds providing hysteresis.

[Figure 6-33 HC5FW 500-S/SP1 Current Sensor Circuit]

In design four current sensors are mounted on the control PCB, aligning to Power board through metal studs. Each current sensor is powered by VSEN (5V). As per datasheet recommendation, a ceramic capacitor of 4.7nF/50V is connected between VCC & GND pin and VREF pin is terminated to GND through 1nF/50V ceramic capacitor. GND pins are connected to AGND.

[Figure 6-34 Typical Signal Monitoring circuit]

The output of each current sensor is fed to two combined Schmitt trigger configurations with the higher & lower threshold values to generate the fault condition when it lower or exceeds the set value.

Each output when fault is observed, are handled through Logic gates to reset MCU with other reset conditions. Similar circuit is implemented for Current sensing; In this design the threshold is set for +450A and -450A for 500A Sensor in use. However, threshold values may be set different for DC Bus current and U, V, W Phase currents.
6.4.4 Voltage Sensor

Input DC power supply Monitoring:

In design, Input DC power supply which ranges from 0V to 75V is linearly reduced by voltage divider to 0V to 5V range.

The voltage divider output is fed to Op-Amp based Schmitt trigger circuit for triggering fault condition.

Lower and higher threshold levels are given, which are approximately set in the Schmitt trigger circuit as given below:

Lower Threshold: $V_{IH} = \sim34.1\text{V}$ and $V_{IL} = \sim32.0\text{V}$

Higher Threshold: $V_{IH} = \sim74.2\text{V}$ and $V_{IL} = 72.0\text{V}$

Output of Schmitt trigger circuit- DC_FAULT is connected to interrupt of MCU (U2) and Fault generator circuit.
Gate Driver Power Supply Monitoring:
The power supply GD_SUPPLY, which is in range of 15V powers Motor driver ISL78434 is fed to Op-Amp based Schmitt trigger circuit for triggering fault condition.

Required lower and higher threshold levels are given, which are approximately set in the Schmitt trigger circuit as given below.

LOWER thresholds: $V_{IH} \approx 11.0V$ and $V_{IL} \approx 10.0V$

HIGHER thresholds: $V_{IH} \approx 16.5V$ and $V_{IL} \approx 15.9V$

Output of Schmitt trigger circuit- GDU_FAULT is connected to interrupt of MCU (U2) and Fault generator circuit.
Motor Phase Voltage Monitoring:

The voltage from HS pin of GDU of each phase is linearly reduced to the range of (5V to 0V) through voltage divider.

The voltage across the divider circuit is connected to ADC followed by protection circuit and low pass filter. Each output from the driver is protected from overvoltage and negative voltage through a TVS diode.

The low pass RC filter is designed for frequency of 160Hz.
Other Analog Input Monitoring:

The board provides facility to interface external analog signals via the 6 Analog interface circuits on-board, the below figure is typical interface circuit implemented on the board.

The signals are typically pull-down via 10K resistor and therefore, will measure 0V when no sensor or connector pin is open.

Each analog input implements low pass RC filter and uses diode for voltage protection.

CAUTION: Care must be taken that excess voltage is not applied on these input pins to avoid damage to the microcontroller.

Power Supply 5V6VCC (5.6V) is converted to TEMP_VS1+, BRAKE_VS+, PEDAL_VS+ & TEMP_VS2+ through a schottky diode which is supplied to ANA connector to power up respective sensor circuits in the external system.
6.5  Digital Input / Output Functions

6.5.1  Digital Inputs: Active Low

The following four digital input signals from DIO connector are connected to MCU (U2) followed by a schottky diode in series with reverse bias condition and pull up resistor. By the circuit implementation below, the signal applied is detected by **ACTIVE LOW logic**, hence providing protection against over-voltage at the MCU pin. _IN1PIN/EMERGENCY_STOP, _CON_IN2PIN, _FREQ_IN0PIN, and _FREQ_IN1PIN

In design 2.2k resistor is tied to EVCC (5V) and 100Ω series resistor is connected to MCU (U2).

![Digital Input Circuit](image)

**Figure 6-39 Digital Input Circuit**

_IN1/EMERGENCY_STOP signal is connected to INTP5 function of the Microcontroller. Also, this signal can be used to generate system RESET on fault.

**CAUTION:** By default, the on-board hardware support C1M_RESET generation by trigger to IN1PIN/EMERGENCY_STOP input pin.

MCU_IN2 signal is connected as Active Low Logic input to port function of the microcontroller. There is TAUD Input capture function available if required.

FREQ_IN0PIN and _FREQ_IN1PIN connected as input capture pins using TAUD or TAUJ capture function on the microcontroller. These pins may also be configured as the Digital Input Pins with Active Low input.
6.5.2 Digital Inputs: Active High

Total eight digital inputs are received from DIO connector followed by TVS diodes DA7, DA8, DA13 and DA14. These inputs are connected to base of the transistor followed by Schottky diode and 1kΩ resistor.

A Zener diode and 1kΩ resistor are provided to protect from over voltage. In circuit pair of 1k resistors will form as a voltage divider.

In the design Zener diode will clamp voltage across base of the transistor to 4.7V when input signal is above voltage level of 5V. By default, the voltage observed at MCU will be 5V as the collector pin is pulled high to EVCC (5V) through a 4.7k resistor.

When active high input is applied it enables switch and make output signal logic low (0V)

**Figure 6-40 Typical Circuit for Active High Input**

**IMPORTANT:** Transistors [PDTC143ET] used have built-in biasing resistors and therefore are not shown in the schematic however, they exist.
6.5.3 Digital Output:

There are four digital output signals, three signals from MCU (U2) can be configured as PWM or Digital output which is connected to the DIO connector.

The output of the transistor is connected to the connector and by default it will be of voltage 5V. In presence of signal from the MCU (U2) it drives the transistor output to GND and pins at connector (DIO) will be pulled to logic low (0V). Inverted logic is used in this section. A 1k resistor is used at the base of the transistor and 4.7k resistor at collector pin.

![Figure 6-41 Typical Output Circuit (inverted output)](image)

Figure 6-41 Typical Output Circuit (inverted output)
6.5.4 High Voltage Open Drain Output for External Loads

Using the Circuit in below figure MCU can control external Load such as Cooling FAN running of the Main Battery Supply (typ. 48V DC). The MOSFET used is 100V and a free-wheeling diode is also implemented to allow control of contactor or relay externally.

A discrete MOSFET driver circuit is implemented to support PWM controlled output, this implementation represents Low side switching and all the 3 terminals of TMS connector are floating and need external connections to be done with supply and load.

CAUTION: The Source of the MOSFET is “floating” on the board, therefore, it is mandatory to connect the Pin3 of the TMS connector externally to Battery -ve terminal to complete the circuit of the load connected across DC Bus and Drain of the MOSFET.
7. PCB Details

This section provides information about the PCB design of the REN-INV-V2 board. The physical dimensions of the PCB are 187mm x 175mm. This 4-layer board has 2 signal layers, 1 GND layer and 1 Power plane and uses FR4 material.

<table>
<thead>
<tr>
<th>Description</th>
<th>Proto PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>187mm X 2175mm</td>
</tr>
<tr>
<td>Name</td>
<td>REN-INV-V2</td>
</tr>
<tr>
<td>Thickness</td>
<td>1.64mm</td>
</tr>
<tr>
<td>Dielectric</td>
<td>FR4 Material</td>
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<tr>
<td>Surface Finish</td>
<td>ENIG</td>
</tr>
<tr>
<td>ROHS</td>
<td>Yes</td>
</tr>
<tr>
<td>No. of Layers</td>
<td>4</td>
</tr>
<tr>
<td>Controlled Impedance</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Below is the Stack-up diagram of the reference design control board PCB.

<table>
<thead>
<tr>
<th>Layer Name</th>
<th>Type</th>
<th>Material</th>
<th>Thickness [mm]</th>
<th>Dielectric Constant</th>
<th>Orientation</th>
<th>Control Layer Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Overlay</td>
<td>Overlay</td>
<td></td>
<td></td>
<td></td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>Top Layer</td>
<td>Solder Mask/Co.</td>
<td>Solder Resist</td>
<td>0.020mm</td>
<td>3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Top Layer</td>
<td>Signal</td>
<td>Copper</td>
<td>0.070mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diel 1</td>
<td>Dielectric Core</td>
<td>FR-4</td>
<td>0.163mm</td>
<td>4.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>Internal Plane</td>
<td>Copper</td>
<td>0.070mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diel 2</td>
<td>Dielectric Core</td>
<td>FR-4</td>
<td>0.163mm</td>
<td>4.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWR</td>
<td>Internal Plane</td>
<td>Copper</td>
<td>0.070mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diel 3</td>
<td>Dielectric Core</td>
<td>FR-4</td>
<td>0.163mm</td>
<td>4.2</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>Bottom Layer</td>
<td>Signal</td>
<td>Copper</td>
<td>0.070mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bottom Layer</td>
<td>Solder Mask/Co.</td>
<td>Solder Resist</td>
<td>0.020mm</td>
<td>3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bottom Overlay</td>
<td>Overlay</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

TOTAL BOARD THICKNESS 1.64 MM +/- 10%
8. Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Acronym/Abbreviations</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog-Digital Converter</td>
</tr>
<tr>
<td>CAN</td>
<td>Controller Area Network</td>
</tr>
<tr>
<td>CAN-FD</td>
<td>Controller Area Network-Flexible Data-Rate</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal–Oxide–Semiconductor</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EMS</td>
<td>Electromagnetic Susceptibility</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic discharge</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Field Effect Transistor</td>
</tr>
<tr>
<td>FR4</td>
<td>Flame Retardant 4</td>
</tr>
<tr>
<td>GDU</td>
<td>Gate Driver Unit</td>
</tr>
<tr>
<td>IPD</td>
<td>Intelligent Power Device</td>
</tr>
<tr>
<td>LIN</td>
<td>Local Interconnect Network</td>
</tr>
<tr>
<td>MCU</td>
<td>Microcontroller Unit</td>
</tr>
<tr>
<td>MUX</td>
<td>Multiplexer</td>
</tr>
<tr>
<td>NRZ</td>
<td>Non-Return-to-Zero</td>
</tr>
<tr>
<td>OP-AMP</td>
<td>Operational Amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PMIC</td>
<td>Power Management IC</td>
</tr>
<tr>
<td>PTC</td>
<td>Positive temperature coefficient</td>
</tr>
<tr>
<td>RDC</td>
<td>Resolver-to-Digital Converter</td>
</tr>
<tr>
<td>LDO</td>
<td>Low Drop Out regulator</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
<tr>
<td>SENT</td>
<td>Single Edge Nibble Transmission</td>
</tr>
<tr>
<td>SoC</td>
<td>System on chip</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver Transmitter</td>
</tr>
<tr>
<td>ISO_GND</td>
<td>Isolated Ground</td>
</tr>
<tr>
<td>PGND</td>
<td>Power Ground</td>
</tr>
<tr>
<td>SGND</td>
<td>Signal Ground (System Ground in the board)</td>
</tr>
<tr>
<td>TVS diode</td>
<td>Transient Voltage Suppressor diode</td>
</tr>
<tr>
<td>AGND</td>
<td>Analog Ground</td>
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## Revision History

<table>
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<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Summary</th>
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<tr>
<td>1.00</td>
<td>01 Jan 2021</td>
<td></td>
<td>First Release</td>
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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