REIN_Inverter_V2

Hardware Design Document

Introduction

This Hardware Design Document serves as a technical blueprint for the Traction Motor Controller Board project. This document is intended to describe the hardware system architecture and the design details.

Target Device

RH850/C1M-A1

RAA270000KFT

ISL78434

uPC1251AGR

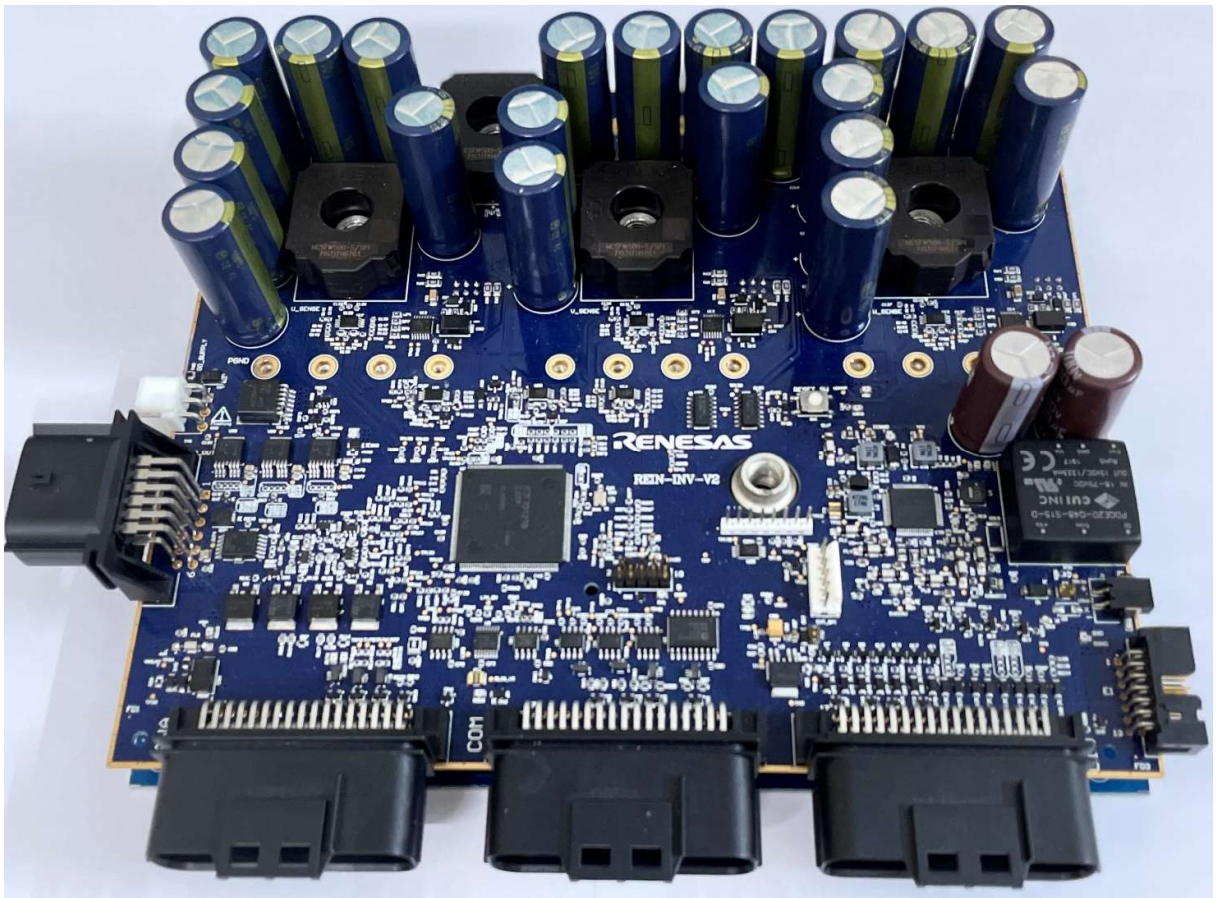


Figure 1-1 Renesas RH850/C1M-A1 Inverter Board

Contents

Table of Contents

1. Architecture

Traction Motor Controller mainly intends to drive motor control for HEV/EV based applications and these consist of two boards – Controller board which controls motor driver, digital, analog sections and Power board includes Power MOSFETs for motor drive. The Controller board controls and drives each phase of the motor windings in Power Board through MOSFET Pre-Driver Stage -ISL78434.

Traction Motor controller includes the RH850/C1M-A1 Microcontroller (R7F701278EAFP QFP), which is equipped with an RH850 Family G3MH CPU core operating at a frequency of 240MHz, providing high processing power. Along with the ROM, RAM, and DMA, it includes various timers such as a motor control timer, various serial interfaces including CAN (CAN FD compatible), a 12-bit A/D converter (ADC), an R/D converter (RDC3A) that converts the resolver output signal to digital angle data, and a CPU and parallel motor control unit (EMU3), etc., providing peripheral functions that are ideal for motor control in HEVs/EVs.

The Controller board has three ISL78434 MOSFET Pre-Driver Stage & µPC1251A Op-Amps for Analog & fault generation circuits, PMIC, LDO, and Power MOSFET Board with RBAZ25N10CHPF. The Power will be 5KW Continuous Power and 8KW peak Power. The number of MOSFET per phase shall be defined accordingly with necessary load dump protection.

The MCU in Controller board interacts with external peripherals through System I/O connectors (COM, ANA and DIO), which carries several communication interfaces, analog, and digital I/O signals. It does also include Intelligent Power Devices (IPD) for additional loads.

Protection for Over-Current, Over-Voltage, Under-Voltage, Over Temperature (Controller and Motor) and its relevant status and precaution are implemented. Interfaces such as CAN-FD, LIN, SENT, Isolated UART such as are also integrated in the design.

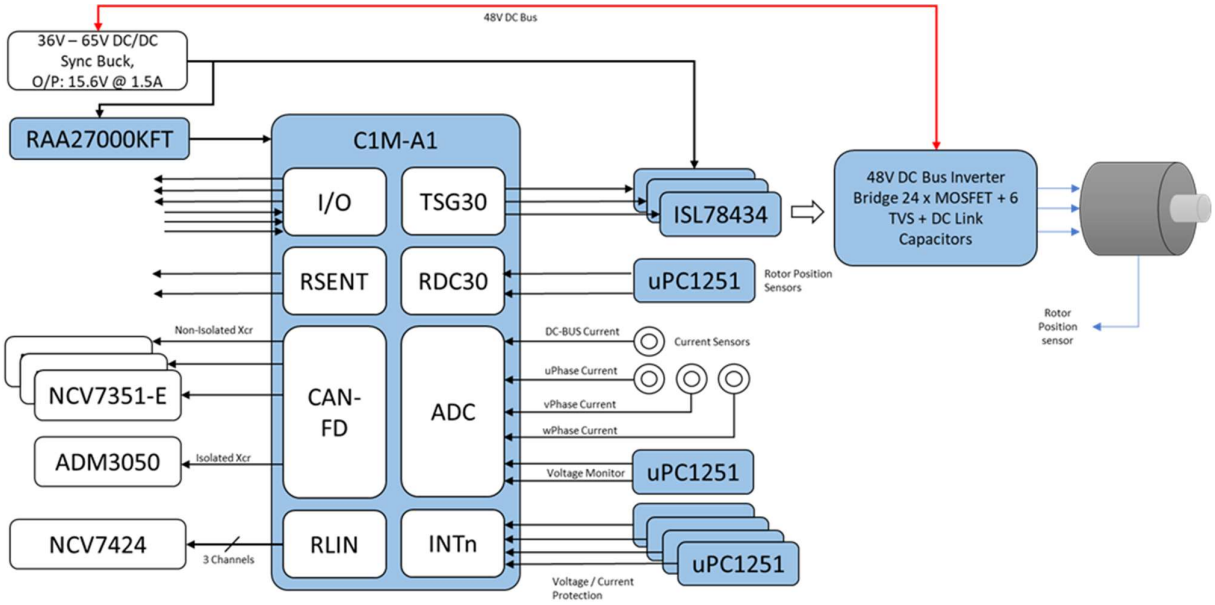


Figure 1-1 - Inverter Block Diagram

2. Hardware Design

The Hardware is categorized based on the function:

1. **Power Supply section**
2. **IPD section**
3. **System I/O connections**
4. **Microcontroller Function Mapping**
5. **Analog Functions**
6. **Digital Input and Output Functions.**

3. Power Supply Section

The DC power supply input range is limited by the specifications of Step-down DC/DC on-board. The DC/DC output is regulated at 15.6V and is used to derive other supplies required by the controller and logic on board.

The DC Supply input is provided via 20.5mm Brass Studs that directly connect to the Power Board inverter bridge and smaller 6mm studs used for coupling the Power board to control board provide mechanical strength and connect power from the DC Bus to the DC Link capacitors and Step-down DC/DC converter. The current requirement for control board is not very high and is easily managed by the M3 screws. Therefore, note that these screws are active power points on the board when assembled.

The input DC Supply current is monitored by high side current sensor, this current sensor is assembled on the control board. The DC Bus current sensor is bi-directional and therefore can be used to measure currents when motoring and when generating.

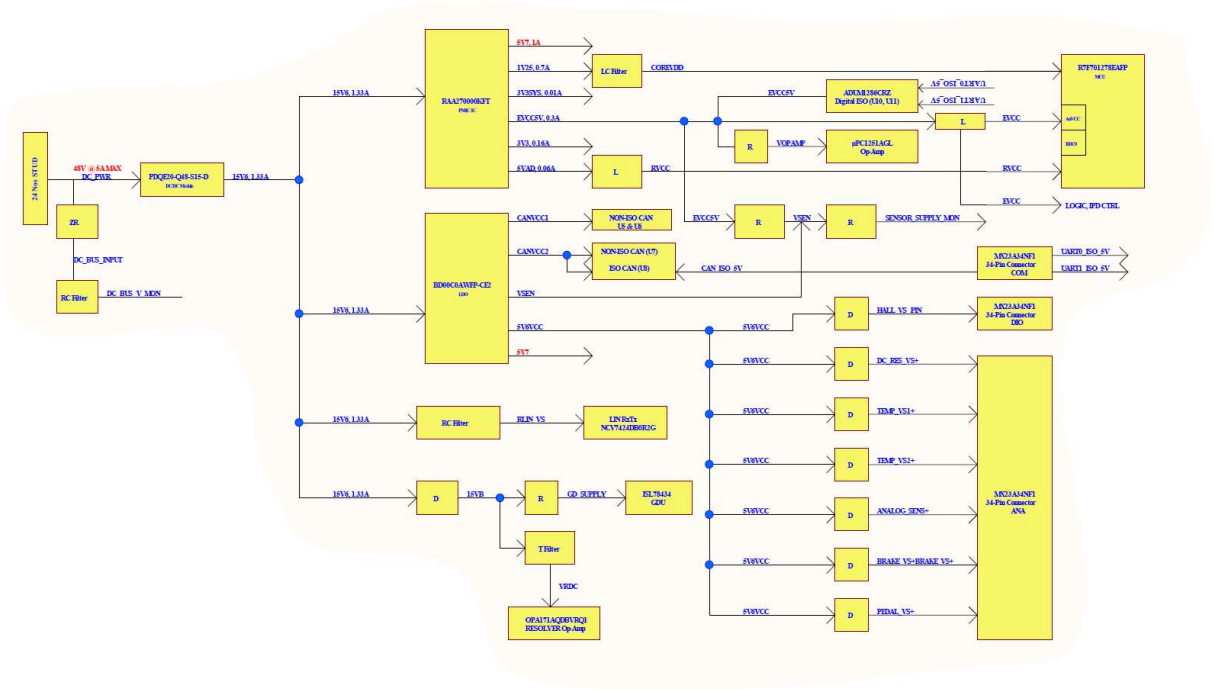


Figure 3-1 System Power Tree

3.1 DC/DC Converter Module

The PDQE20-Q48-S15-D is a DC-DC Isolated converter that provides (15.6V) 15V6 supply to the controller board. The module has isolation up to 1.5KV (if required) and provides maximum 20W output. The output voltage of 15V is nominal, which is trimmed to 15V6 by varying the resistor at the trim pin. The module provides constant output current of 1.333A.

Features:

- Ultra-wide input voltage range (18V~75V).
- 20 W isolated output.
- Single/dual regulated outputs.
- 1500 Vdc isolation.
- Extended temperature range (-40~105°C).
- Input under-voltage protection.
- Output short circuit, over-current and over-voltage protection.
- DIP package.
- Ripple of 100mV.
- Efficiency of 91%.

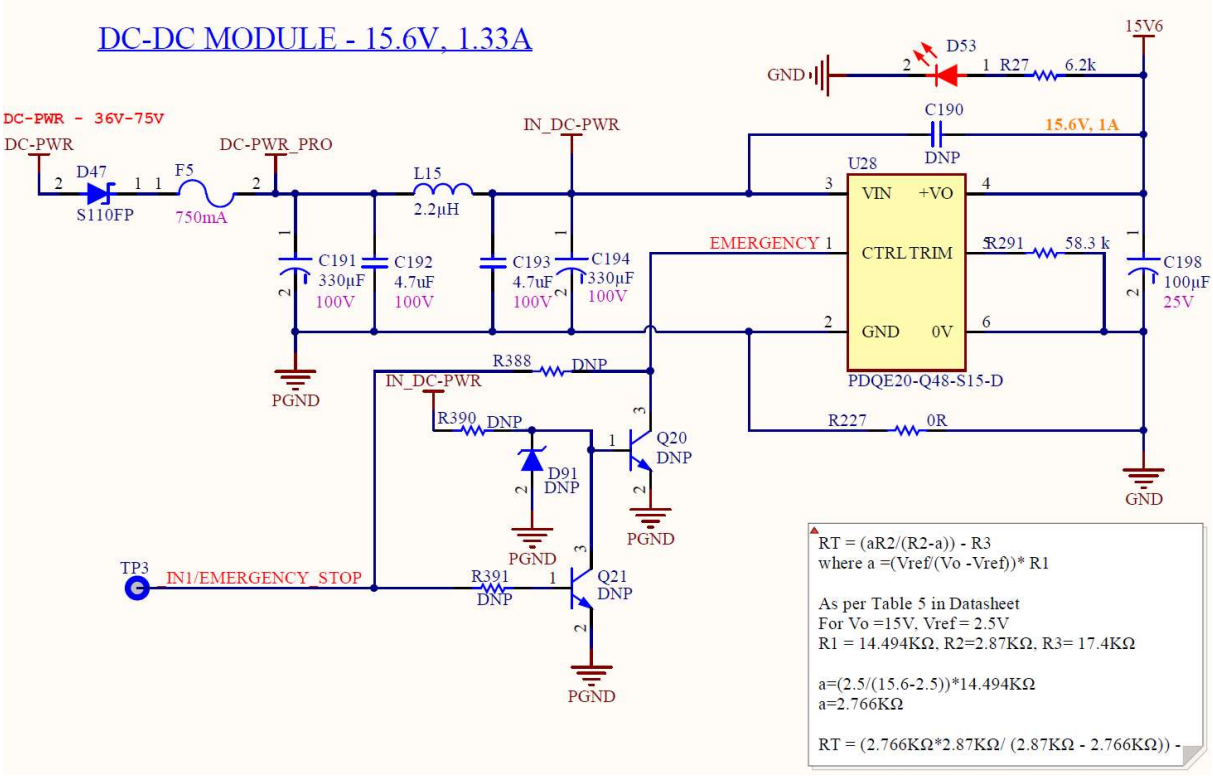


Figure 3-2 Schematics of PDQE20-Q48-S15-D

Design Consideration for DC/DC Supply Module:

VIN (3) Input supply pin: Followed by reverse voltage protection (D47) and current limiting PTC fuse (F5)-750mA, input supply **DC_PWR** is applied to this pin through filter section comprised of capacitors of 330 µF/50 V,4.7 µF/50 V and inductor of value 2.2uH. As per datasheet recommendation, in design electrolytic capacitor and ceramic capacitor are used.

CTRL (1): Remote ON/OFF: Used to enabled and disabled. In design, during emergency conditions logic low from MCU will turn off the module through transistor-based switch circuit, which avoids fault operation and disconnect supply power to rest circuitry.

TRIM (5): The Output voltage is trimmed through this pin. In design, the voltage is trimmed to 15.6V, which is the power source for the system.

The voltage is set as per the following calculation suggested in the datasheet. Figure 6 shows the calculation formula for Trim Pin.

RT = (aR2/ (R2-a)) - R3
Where a = (Vref/ (VO -Vref))* R1

As per Table 5 in Datasheet
For VO =15V, Vref = 2.5V
R1 = 14.494KΩ, R2=2.87KΩ, R3= 17.4KΩ

a= (2.5/ (15.6-2.5))*14.494KΩ
a=2.766KΩ

RT = (2.766KΩ*2.87KΩ/ (2.87KΩ - 2.766KΩ)) - 17.4KΩ
RT = 58.9KΩ

In design as per application circuit and calculations resistor RT of 58.3kΩ is used to trim voltage to 15.6V.

Formula for Trim Resistor

up: $R_T = \frac{aR_2}{R_2-a} - R_3$ $a = \frac{Vref}{Vo' - Vref} \cdot R_1$

down: $R_T = \frac{aR_1}{R_1-a} - R_3$ $a = \frac{Vo' - Vref}{Vref} \cdot R_2$

Note: Value for R1, R2, R3, and Vref refer to Table 5
R_T: Trim Resistor
a: User-defined parameter, no actual meanings
Vo': The trim up/down voltage

Table 5

Vout (Vdc)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	Vref (V)
3.3	4.829	2.87	15	1.24
5	2.894	2.87	10	2.5
12	11.000	2.87	17.4	2.5
15	14.494	2.87	17.4	2.5
24	24.872	2.87	20	2.5

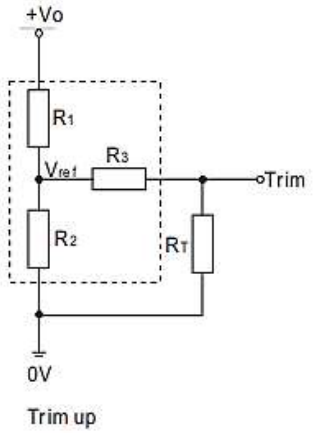
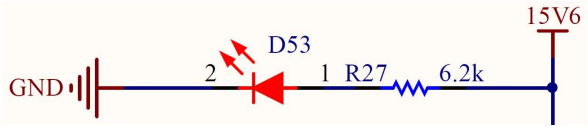
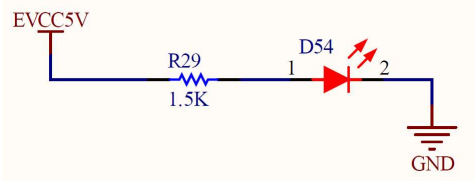


Figure 3-3 Formula for Trim Resistor and Application Circuit for Trim Pin

+VO (4): Output Voltage: A nominal output voltage of 15V is observed at this pin which is set to 15.6V using resistor (RT). In design as per datasheet recommendation output voltage is noise filtered using a tantalum capacitor of 100µF / 50V. Power LED (D53) is provided in design to indicate the generated voltage 15.6V o/p.

The Power Supply is indicated by 2 LED's on-board, LED D53 indicates 15V6 Supply output and D54 indicates EVCC5V output as shown below:





The other voltage levels can be checked by tapping into the on-board test points provided and as per schematics.

3.2 Power Management IC: RAA270000KFT (U1)

The RAA270000KFT is a Power Management IC (PMIC) for automotive RH850 microcontroller series. The RAA270000KFT contains two integrated current mode DC-DC converters, four low dropout linear regulators (LDOs) and two linear trackers. The switching frequency of the DC-DC converters is typically 2.1MHz. Also, several monitor functions and diagnostic functions such as over-voltage and under-voltage detection of the regulators and watchdog for monitoring external microcontroller are implemented.

The input voltage of the RAA270000KFT, the output of all regulators, and internal analog voltage corresponding to temperature can be monitored through ADCs in external microcontroller. Since the RAA270000KFT includes a power-up/down sequence controller, users can reduce external components for controlling the target microcontroller power-up/down sequence.

Features

- Input range: 6.0V to 18.5V to perform specified characteristics.
  - 5.4V~: Power rails, 5V/3.3V/1.25V and trackers functional (Not detect low voltage)
  - 3.9V~: Not issues reset.
- 2 switching regulators,
  - For point of load: 5.7V/1000mA
  - For MCU core: 1.25V/700mA
- 4 linear regulators
  - For MCU: 3.3V/10mA, 5.0V/300mA, 3.3V/160mA, 5.0V/60mA
- 2 linear trackers,
  - 150mA ability with short protection to battery
- Automatic power sequence
- Watchdog timer
- Analog multiplexer – Used for monitoring the PMIC voltage levels from MCU ADC
- Interrupt request to MCU
- CSI(SPI) Communication with Main MCU.
- Thermal shut down.
- Reset generator.

Design Consideration for PMIC Supply:

For further details on the PMIC please refer the datasheet or contact Renesas Engineer for any clarification.

CAUTION: Care must be taken that excess input voltage is not applied to J1 to avoid damage to the PMIC IC.

3.3 LDO: BD00C0AWFP-CE2 (U3)

The BDxxC0A-C series and the BDxxC0AW-C series are low-saturation regulators. This series feature variable and fixed voltage output with selectable Shutdown switch (referred to as SW). This series has a built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits and a thermal Shutdown circuit that protects the IC from thermal damage due to overloading.

Features

- Output current capability: 1A.
- Output voltage: Variable, 3.3V, 5.0V, 8.0V and 9.0V
- High output voltage accuracy (Ta=25°C, TO252-3/5, HRP5): ±1%
- Low saturation with PDMOS output
- Built-in over-current protection circuit that prevents the destruction of the IC due to O/P short circuits.
- Built-in thermal Shutdown circuit for protecting the IC from thermal damage due to overloading.

In Design, the BD00C0AWFP-CE2 is an independent Power source which is dedicated to generating 5V6VCC – general 5V supply for most of the circuits in the design. In addition to 5V6VCC optional power supply for CAN Sections and Current sensor are provided in case of shortage of current through diodes. The output value is set to 5V6 to counter the drop across the series diode used for distributing this supply across various on-board and off-board supplies requiring typ. 5V0 DC supply.

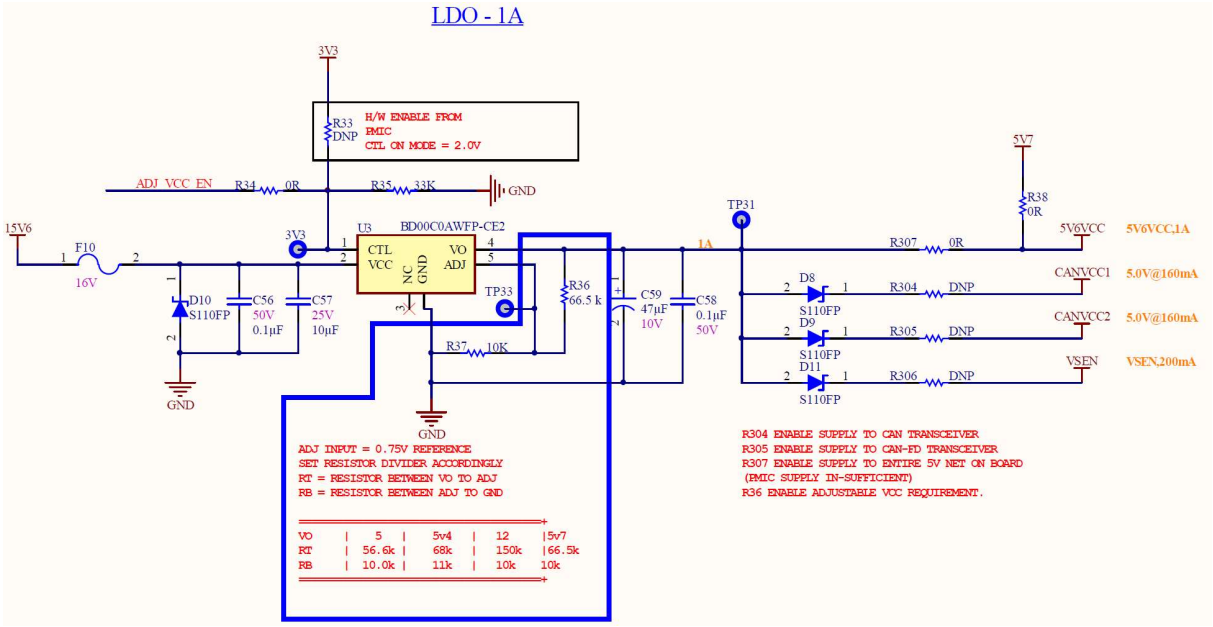


Figure 3-4 LDO Power Supply On-Board

Design considerations for the LDO supply:

CTL (Pin 1) – Output Control Pin: This pin controls the output voltage and enabled by MCU pin and optional enable is provided by tying to 3V3 supply with jumper. By default, this pin is pulled low through 33kΩ resistor. Based on requirement MCU may enable and disable this LDO output.

VCC (Pin 2) Input supply. A capacitor greater than 1-µF or larger capacitor with excellent voltage and temperature characteristics must be connected between VCC and GND for stability. Larger value capacitors result in better transient and noise performance. Although an input capacitor is not required for stability, when a 0.1-µF or larger capacitor is placed between VCC and GND, it counteracts reactive input sources and improves transient and noise performance. Higher value capacitors are necessary if large, fast rise time load transients are anticipated. In design 10-µF, 25V, X5R and 0.1-µF, 50V, X7R.

In design current is limited with PTC resettable fuse of maximum current of 20A, hold current of 500mA and trip current of 2.5A with maximum 16V. Reverse voltage protection is provided with 100V schottky diode.

ADJ (Pin 5) Adjustable Pin: The Output of LDO is set using voltage divider. The reference voltage is 0.75V and R1 is 10kΩ as recommended by datasheet.
VO ≈ ADJ × (R1+R2) / R1
Where VO = 5.7V, ADJ = 0.75
R2 = (5.7/ 0.75 – 1) * 10K
R2 = 66.5kΩ

VO (4) Output Pin: To prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. A tantalum capacitor with a capacitance 47µF, 10V is used followed by Ceramic capacitor of 0.1µF, 50V.

CAUTION: As shown in the schematic R38 is mounted connecting the PMIC 5V7 output to 5V6VCC therefore, this LDO default state on-board is "INACTIVE" by applying "Low" on CTL (Pin 1) of LDO. If user wish to enable the LDO, it can be done only after unmounting R38, then applying "High" on CTL via MCU through ADJ_VCC_EN Signal.

4. IPD Section

In this reference design there are three µPD166033T1U and one µPD166023T1J IPD devices which drive 12V load connected through J10 connector. These devices are controlled by MCU.

µPD166033T1U is part of 2nd Generation Intelligent Power Devices (IPD). They are N-channel high-side switches with charge pump, voltage-controlled input, diagnostic feedback with proportional load current sense and embedded protection function. Family includes up to 14 devices depending on on-state resistance, package and channel number combination.

µPD166023T1J is part of 2nd Generation Intelligent Power Devices (IPD). This is N-channel high-side switch with charge pump, voltage-controlled input, diagnostic feedback with proportional load current sense and embedded protection function. Family includes up to 14 devices depending on on-state resistance, package and channel number combination.

IPD feature summary:

- Built-in charge pump.
- 3.3V compatible logic interface.
- Low standby current.
- Short circuit protection.
    - Shutdown by over current detection.
    - Power limitation protection by overload detection (Power limitation: current limitation with delta Tch control).
    - Absolute Tch over temperature protection.
- Built-in diagnostic function.
    - Proportional load current sensing.
    - Defined fault signal in case of abnormal load condition.
- Loss of ground protection.
- Under voltage lock out.
- Active clamp operation at inductive load switches off.
- Cross current protection in case of H-bridge high side usage.
- Reverse battery protection by turn on the output.

Design consideration for IPD Functions:

IPD devices are powered by external connector (J10) through VBUS_EXT_PIN & optional internal supply ORING between 12VDC VBUS External and on-board 15V6 (15.6V) through series diode is possible via mounting of the diode as shown in figure below.

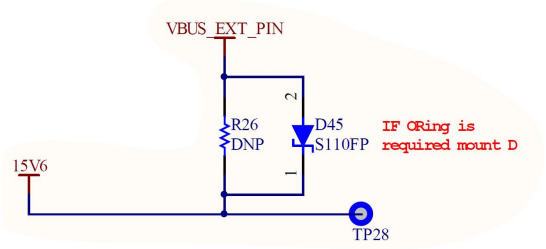


Figure 4-1

IN (Input signal): MCU (U2) enables these devices through control signals EN_IPD_OUT1, EN_IPD_OUT2, EN_IPD_OUT3 & EN_IPD_OUT4.

IS (Current sense and Diagnosis output signal): These pins are pulled low by connecting to GND, which generates voltage drop proportional to load current. MCU (U2) monitors voltage drop through ADC and analyses current consumption of the load through IPD connector (J10).

Zener diodes are provided at the IS pin, to protect MCU from over voltage, when voltage drop between IS pin and ground is greater than VCC.

SEN (Sense enable input): VSEN is set to 5V (EVCC) in design. RSEN is set to 4.7kΩ.

OUT (Protected high-side power output): The output of IPD devices, OUT1, OUT2, OUT3 & OUT4 are connected to the IPD connector (J10).

A capacitor of 0.1uF/50V and 12kΩ resistor is provided across output pin and connector (J10). TVS diode (D30) is provided across the output pin, for ESD protection of the device.

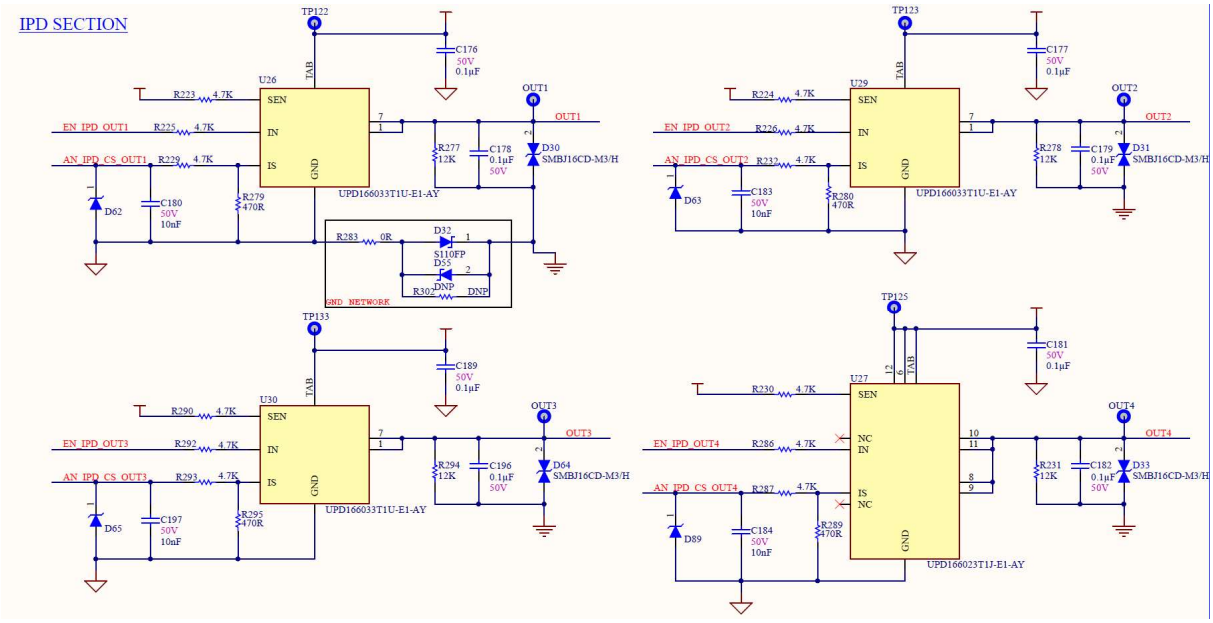


Figure 4-2

5. System I/O Connector Details

Controller board has 1 Nos of 12-Pin and 3 Nos. of 34 pin System I/O connectors, which deals with 12V External Load Drive, Control, Communication & I/O signals respectively across controller board to external system. Since these connectors carry all system related signals in and out of the board, these are classified based on type of signals.

These connectors are named as ANA, COM and DIO in the design, where ANA connector deals with analog signals such as RDC, temperature sensor, pedal, brake status. COM connector deals with communication related signals such as classical CAN, CAN-FD, LIN interfaced and UART. DIO connector deals digital I/O, Frequency Capture, and interrupts.

12-pin connector details:

- Manufacturer: Molex
- Part Number: 0367831201
- 12 Pin header Connector
- 3.20mm Pitch
- 10.5A maximum current per contact
- 28V DC maximum voltage
- Temperature Range - Operating -40° to +105°C

34-Pin header Connector details:

- Manufacturer: JAE Electronics
- Part Number: MX23A34NF1
- 2.50mm Pitch
- Board Guide
- Low profiled type with board mounting height of 18.3mm and socket connector height of 22.2mm.
- 3A rated current.
- Temperature Range - Operating -40° to +125°C

Following are the system I/O Connectors

1. IPD Connector – 12V Bus Net High Side Control ports – 4 Outputs Available.
2. ANA Connector – Analog input signal/s interfacing.
3. COM Connector – Communication signal/s interfacing.
4. DIO Connector – Digital I/O signal/s interfacing.

5.1 IPD Connector

A 12-pin connector is dedicated for IPD (**I**ntelligent **P**ower **D**evices), the 4 outputs on the connector are driven by protected High-side switches working from the 12V Bus Net Power. IPD's also provide diagnostic function to monitor the fault conditions occurring on the output or load side.

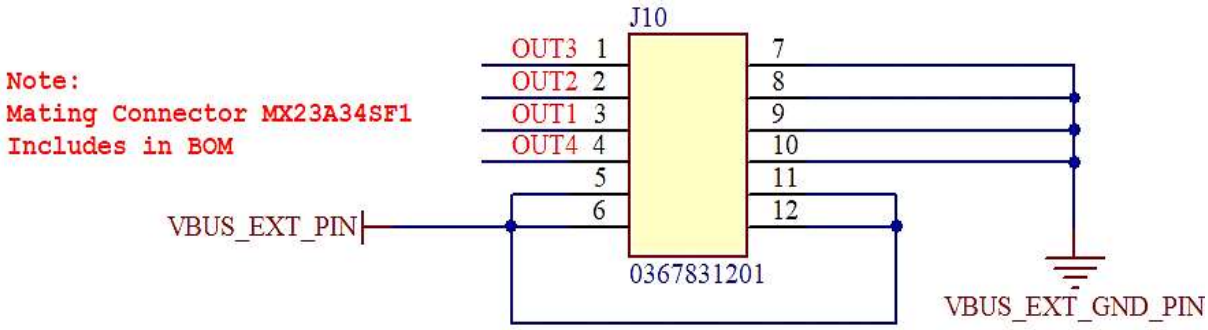


Figure 5-1 IPD Connector details

Caution: ***VBUS_EXT_PIN*** *must be supplied from* ***external 12V DC*** *supply connection only, IPD's will* ***not*** *source from Primary Supply of the Inverter Board. The J10 connector outputs can only be used with the presence of the 12V DC Supply.*

Table 5-1 IPD Connector electrical details

Pin #	Signal Name	5V	12V	Signal	Description
1	OUT3	×	✓	Output	Output signal 3 from the IPD Device (U30) to external system
2	OUT2	×	✓	Output	Output signal 2 from the IPD Device (U29) to external system
3	OUT1	×	✓	Output	Output signal 1 from the IPD Device (U26) to external system
4	OUT4	×	✓	Output	Output signal 4 from the IPD Device (U27) to external system
5	VBUS_EXT_PIN	×	✓	Power	VBUS_EXT_PIN, 12V supply to IPD devices in the board
6	VBUS_EXT_PIN	×	✓	Power	VBUS_EXT_PIN, 12V supply to IPD devices in the board
7	VBUS_EXT_GND_PIN	-	-	Ground	VBUS_EXT_GND_PIN, connected to IPD device
8	VBUS_EXT_GND_PIN	-	-	Ground	VBUS_EXT_GND_PIN, connected to IPD device
9	VBUS_EXT_GND_PIN	-	-	Ground	VBUS_EXT_GND_PIN, connected to IPD device
10	VBUS_EXT_GND_PIN	-	-	Ground	VBUS_EXT_GND_PIN, connected to IPD device
11	VBUS_EXT_PIN	×	✓	Power	VBUS_EXT_PIN, 12V supply to IPD devices in the board
12	VBUS_EXT_PIN	×	✓	Power	VBUS_EXT_PIN, 12V supply to IPD devices in the board

5.2 ANA Connector

ANA Connector provides the analog input interfaces such as Resolver sin/ cos signals, Pedal, Brake and Temperature sensor inputs. Up to 6 analog inputs are available additionally for the user specific analog signal interfacing. The connector also provides uni-directional 5V DC Power Supply for sensor interfacing.

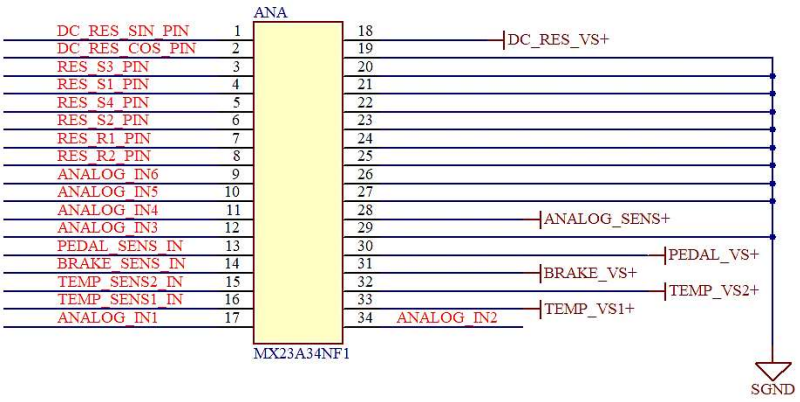


Figure 5-2 ANA Connector details

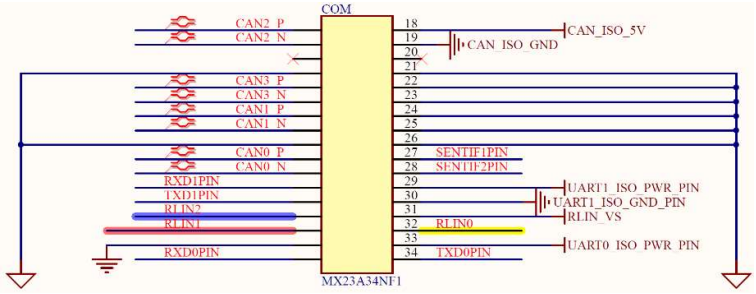
Caution: The ANA connector signals can be used as Analog inputs only and no digital input can be interfaced.

Table 5-2 ANA Connector electrical details

Pin #	Signal Name	5V	12V	Signal	Description
1	DC_RES_SIN_PIN	✓	×	Input	Analog signal related to RDC sine from ext. system to ADC of MCU (U2)
2	DC_RES_COS_PIN	✓	×	Input	Analog signal related to RDC cosine from ext. system to ADC of MCU (U2)
3	RES_S3_PIN	×	✓	Input	RDC S3 input signal from the external system to RDC of MCU (U2)
4	RES_S1_PIN	×	✓	Input	RDC S1 input signal from the external system to RDC of MCU (U2)
5	RES_S4_PIN	×	✓	Input	RDC S4 input signal from the external system to RDC of MCU (U2)
6	RES_S2_PIN	×	✓	Input	RDC S2 input signal from the external system to RDC of MCU (U2)
7	RES_R1_PIN	×	✓	Output	RDC Output R1 from RDC of MCU (U2) to external system.
8	RES_R2_PIN	×	✓	Output	RDC Output R2 from RDC of MCU (U2) to external system.
9	ANALOG_IN6	✓	×	Input	Analog input 6 signal from ext. system to ADC of MCU (U2).
10	ANALOG_IN5	✓	×	Input	Analog input 5 signal from ext. system to ADC of MCU (U2).
11	ANALOG_IN4	✓	×	Input	Analog input 4 signal from ext. system to ADC of MCU (U2).
12	ANALOG_IN3	✓	×	Input	Analog input 6 signal from ext. system to ADC of MCU (U2).
13	PEDAL_SENS_IN	✓	×	Input	Pedal sense input signal from ext. system to ADC of MCU (U2).
14	BRAKE_SENS_IN	✓	×	Input	Brake sense input signal from ext. system to ADC of MCU (U2).
15	TEMP_SENS2_IN	✓	×	Input	Temperature sense 2 input signal from ext. system to ADC of MCU (U2).
16	TEMP_SENS1_IN	✓	×	Input	Temperature sense 1 input signal from ext. system to ADC of MCU (U2).
17	ANALOG_IN1	✓	×	Input	Analog input 1 signal from external system to ADC of MCU (U2).
18	DC_RES_VS+	✓	×	Power	DC_RES_VS+, Power supply from board to connector.
19	SGND	-	-	GND	Connected to Signal Ground (SGND)
20	SGND	-	-	GND	Connected to Signal Ground (SGND)
21	SGND	-	-	GND	Connected to Signal Ground (SGND)
22	SGND	-	-	GND	Connected to Signal Ground (SGND)
23	SGND	-	-	GND	Connected to Signal Ground (SGND)
24	SGND	-	-	GND	Connected to Signal Ground (SGND)
25	SGND	-	-	GND	Connected to Signal Ground (SGND)
26	SGND	-	-	GND	Connected to Signal Ground (SGND)
27	SGND	-	-	GND	Connected to Signal Ground (SGND)
28	ANALOG_SENS+	✓	×	Power	ANALOG_SENSE+, Power supply from board to connector.
29	SGND	-	-	GND	Connected to signal ground
30	PEDAL_VS+	✓	×	Power	PEDAL_VS+, Power supply from board to connector.
31	BRAKE_VS+	✓	×	Power	BRAKE_VS+, Power supply from board to connector.
32	TEMP_VS2+	✓	×	Power	TEMP_VS2+, Power supply from board to connector.
33	TEMP_VS1+	✓	×	Power	TEMP_VS1+, Power supply from board to connector.
34	ANALOG_IN2	✓	×	Input	Analog input 2 signal from external system to ADC of MCU (U2).

5.3 COM Connector

COM Connector provides communication interfaces from C1M-A1 for interfacing other ECU, Sensors and external diagnostic tools. Communication interfaces are available with and without isolation, please see the details for the isolated interfaces.



- 3 Nos Non-isolated CAN / CAN-FD
- 3 Nos LIN
- 2 Nos SENT
- 2 Nos “Isolated” UART
- 1 Nos “Isolated” CAN / CAN-FD

Figure 5-3 COM Connector details

Caution: “Isolated” interfaces UART & CAN require Power to be provided on the isolated side of the interface. CAN_ISO_5V, UART0_ISO_PWR_PIN & UART1_ISO_PWR_PIN must be supplied with 5V DC externally and respective CAN_ISO_GND, UART0_ISO_GND_PIN & UART1_ISO_GND_PIN must be connected to GND separately.

Table 5-3 COM Connector electrical details

Pin #	Signal Name	5V	12V	Signal	Description
1	CAN2_P	✓	×	I/O	CAN2_P differential pair signal from isolated CAN-FD (U8)
2	CAN2_N	✓	×	I/O	CAN2_N differential pair signal from isolated CAN-FD(U8)
3	NC	-	-	-	No Connection
4	SGND	-	-	GND	Connected to Signal Ground (SGND)
5	CAN3_P	✓	×	I/O	CAN3_P differential pair signal from non-isolated CAN(U7)
6	CAN3_N	✓	×	I/O	CAN3_N differential pair signal from non-isolated CAN(U7)
7	CAN1_P	✓	×	I/O	CAN1_P differential pair signal from non-isolated CAN(U6)
8	CAN1_N	✓	×	I/O	CAN1_N differential pair signal from non-isolated CAN(U6)
9	SGND	-	-	GND	Connected to Signal Ground (SGND)
10	CAN0_P	✓	×	I/O	CAN0_P differential pair signal from non-isolated CAN(U6)
11	CAN0_N	✓	×	I/O	CAN0_N differential pair signal from non-isolated CAN(U6)
12	RXD1PIN	✓	×	I/O	UART(U11) receiver signal
13	TXD1PIN	✓	×	I/O	UART(U11) transmit signal
14	RLIN2	×	✓	I/O	LIN Transceiver (U9) I/O
15	RLIN1	×	✓	I/O	LIN Transceiver (U9) I/O
16	UART0_ISO_GND_PIN	-	-	GND	Isolated ground for U10
17	RXD0PIN	✓	×	I/O	UART(U10) receiver signal
18	CAN_ISO_5V	✓	×	Power	Power supply to isolated CAN-FD(U8)
19	CAN_ISO_GND	-	-	GND	Isolated ground to CAN-FD(U8)
20	NC	-	-		No Connection
21	SGND	-	-	GND	Connected to Signal Ground (SGND)
22	SGND	-	-	GND	Connected to Signal Ground (SGND)
23	SGND	-	-	GND	Connected to Signal Ground (SGND)
24	SGND	-	-	GND	Connected to Signal Ground (SGND)
25	SGND	-	-	GND	Connected to Signal Ground (SGND)
26	SGND	-	-	GND	Connected to Signal Ground (SGND)
27	SENTIF1PIN	✓	×	I/O	RSENT1 data input from the external system to MCU (U2)
28	SENTIF2PIN	✓	×	I/O	RSENT2 data input from the external system to MCU (U2)
29	UART1_ISO_PWR_PIN	✓	×	Power	Power supply to isolated UART(U11)
30	UART1_ISO_GND_PIN	-	-	GND	Isolated ground to UART (U11)
31	RLIN_VS	×	✓	Power	RLIN_VS, power supply to the COM
32	RLIN0	×	✓	I/O	LIN Transceiver (U9) I/O
33	UART0_ISO_PWR_PIN	✓	×	Power	Power supply to isolated UART(U10)
34	TXD0PIN	✓	×	I/O	UART (U10) transmit signal.

5.4 DIO Connector

DIO Connector provides digital input and output signal interfaces. For details refer the schematics to understand the Active low or Active High input support. Additionally, this connector also provides input for Hall sensor and Encoder interface for Motor control. The digital inputs are available as logic inputs, interrupts and frequency capture by selecting right function of the MCU port. The digital outputs can be configured as logic output or PWM output subject to the port configuration of the MCU.

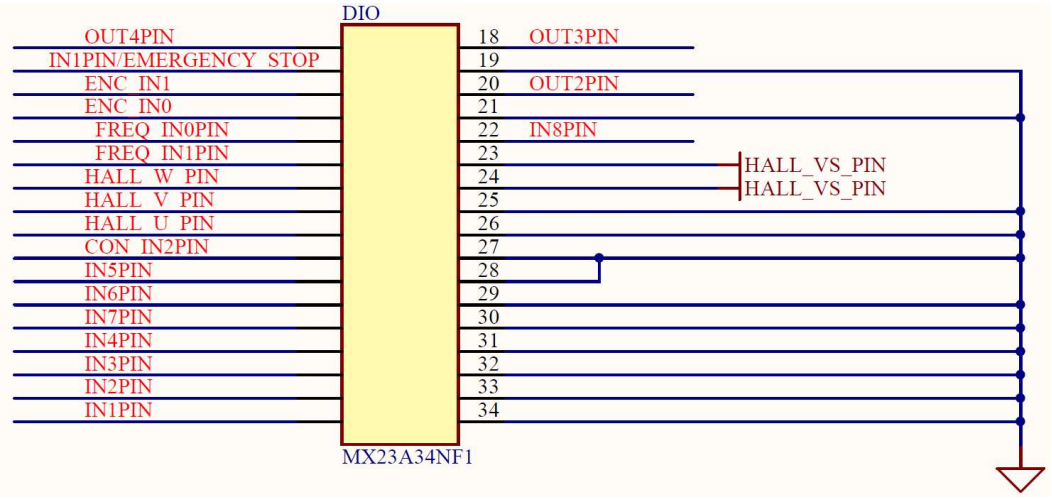


Figure 5-4 DIO Connector details

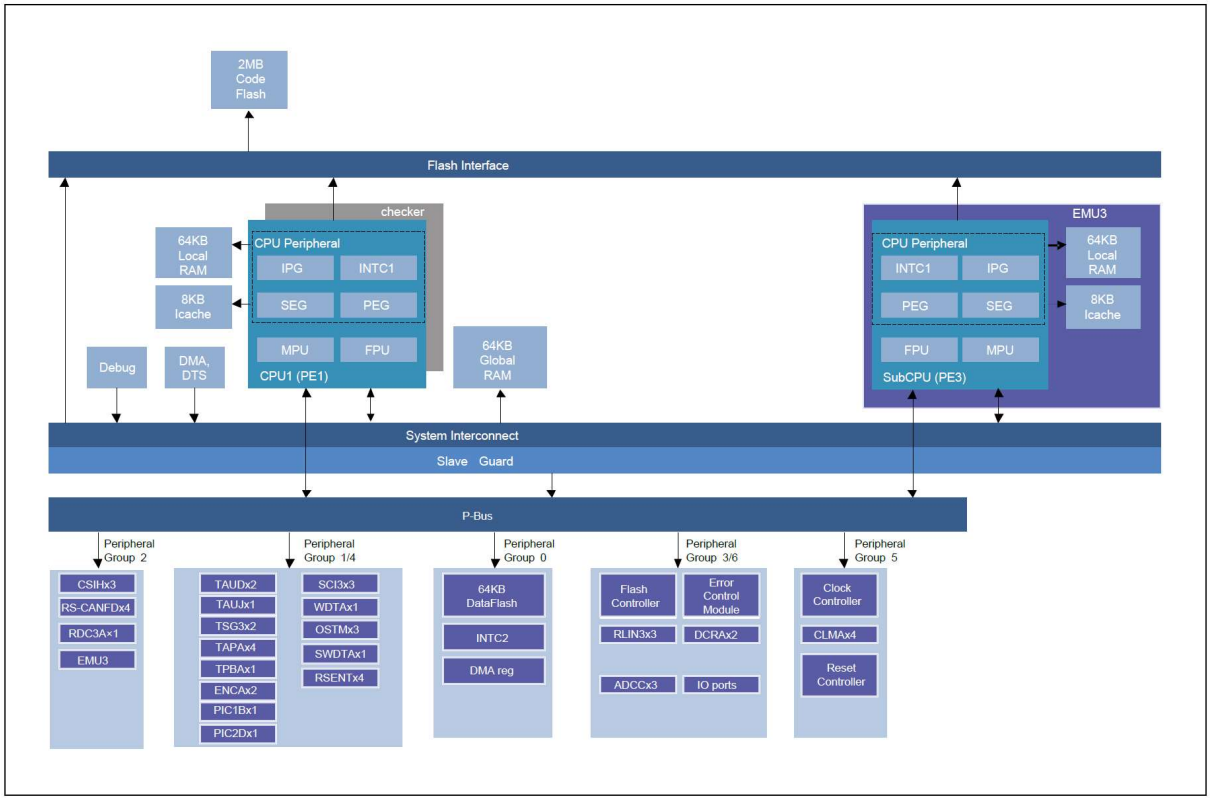
Pin #	Signal Name	5V	12V	Signal	Description
1	OUT4PIN	✓	×	Output	Digital output 4 signal from MCU (U2) to ext. system
2	_IN1PIN /EMERGENCY_STOP	✓	✓	Input	Emergency signal from ext. system through connector (DIO) to MCU (U2)
3	ENC_IN1	✓	✓	Input	Encoder input1 signal from ext. system through connector (DIO) to MCU
4	ENC_IN0	✓	✓	Input	Encoder input0 signal from ext. system through connector (DIO) to MCU
5	_FREQ_IN0PIN	✓	✓	Input	Frequency input0 signal from ext. system to MCU (U2)
6	_FREQ_IN1PIN	✓	✓	Input	Frequency inpu1 signal from ext. system to MCU (U2)
7	HALL_W_PIN	✓	✓	Input	ENCA0 encoder input 2 signal from ext. system to MCU (U2)
8	HALL_V_PIN	✓	✓	Input	ENCA0 encoder input 1 signal from ext. system to MCU (U2)
9	HALL_U_PIN	✓	✓	Input	ENCA0 encoder input 0 signal from ext. system to MCU (U2)
10	CON_IN2PIN	✓	✓	Input	CON_IN2PIN signal from ext. system to MCU (U2)
11	IN5PIN	✓	×	Input	Input 5 signal from ext. system to MCU (U2)
12	IN6PIN	✓	×	Input	Input 6 signal from ext. system to MCU (U2)
13	IN7PIN	✓	×	Input	Input 7 signal from ext. system to MCU (U2)
14	IN4PIN	✓	×	Input	Input 4 signal from ext. system to MCU (U2)
15	IN3PIN	✓	×	Input	Input 3 signal from ext. system to MCU (U2)
16	IN2PIN	✓	×	Input	Input 2 signal from ext. system to MCU (U2)
17	IN1PIN	✓	×	Input	Input 1 signal from ext. system to MCU (U2)
18	OUT3PIN	✓	×	Output	Output 3 signal from MCU (U2) to ext. system.
19	SGND	×	×	GND	Connected to Signal Ground (SGND)
20	OUT2PIN	✓	×	Output	Output 2 signal from MCU (U2) to ext. system.
21	SGND	×	×	GND	Connected to Signal Ground (SGND)
22	IN8PIN	✓	×	Input	Input 8 signal from ext. system to MCU (U2)
23	HALL_VS_PIN	✓	×	Power	Power supply from board to connector.
24	HALL_VS_PIN	✓	×	Power	Power supply from board to connector.
25	SGND	×	×	GND	Connected to Signal Ground (SGND)
26	SGND	×	×	GND	Connected to Signal Ground (SGND)
27	SGND	×	×	GND	Connected to Signal Ground (SGND)
28	SGND	×	×	GND	Connected to Signal Ground (SGND)
29	SGND	×	×	GND	Connected to Signal Ground (SGND)
30	SGND	×	×	GND	Connected to Signal Ground (SGND)
31	SGND	×	×	GND	Connected to Signal Ground (SGND)
32	SGND	×	×	GND	Connected to Signal Ground (SGND)
33	SGND	×	×	GND	Connected to Signal Ground (SGND)
34	SGND	×	×	GND	Connected to Signal Ground (SGND)

6. Microcontroller functional Mapping

The Microcontroller used in the reference design is RH850/C1M-A1, part # R7F701278EAFP is 176-pin plastic QFP (0.5-mm pin pitch). The CPU is supporting Lock-Step Dual Core (Main Core + Checker Core) and consists of G3MH core operating at 240MHz and supports FPU (Floating Point Unit) and MPU (Memory Protection Unit). Additionally, there is support for Internal Peripheral Guard (IPG) and System Error notification control function (SEG).

Some important safety and security H/W IP provided on-chip are as follows:

- Clock Monitor (CLMA)
- Error Control Module (ECM)
- Error Correcting Coding (ECC)
- Data CRC (DCRA)
- Intelligent Cryptographic Unit E (ICUSE)
- Secure Watchdog Timer A (SWDTA)



Internal Block Diagram of RH850/C1M-A1

Figure 6-1 C1M-A1 Block Diagram

For reference design of inverter, we have mapped the relevant peripherals allowing options to evaluate almost all the peripheral features of the device relevant for this application. From Top Level, we have mapped inverter application based on the I/O requirements, such as Analog Interfaces, PWM for Motor Drive, Communication Interfaces (UART, SPI, CAN, LIN and SENT).

For Motor Control Specific H/W IP on-chip include Embedded Motor Unit (EMU3) and resolver to digital converter (RDC3), these peripherals in conjunction with on-chip ADC and TSG (Timer Module) enable inverter function for Motor control. For details refer to the User's Manual of RH850/C1M-Ax.

6.1 Device Functional Mapping Summary:

The RH850/C1M-A1 device functions are mapped based on the following categories:

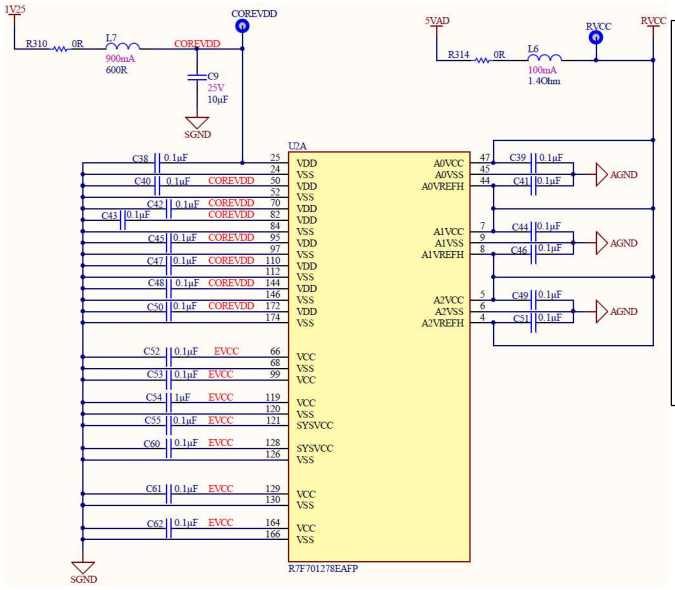
1. System functions: Power Pins, System Pins, Debugger Pins & Special Function Pins.
2. Motor Control Application Pins.
3. Communication: SPI, UART, CAN, LIN & SENT Interfaces.
4. Analog Pins: Voltages, Currents, Temperature, and external signal monitoring.
5. Digital Input / Output functional Pins.

Note: Please contact Renesas Support for Pin Mapping Excel for RH850/C1M-A1 for your use.

6.1.1 System Functions

Pin #	Mapped Functions	User Functions	Comment / Remarks
4	A2VREFH	A2VREFH	-0.3 to A2VCC + 0.3
5	A2VCC	A2VCC	4.5 V to 5.5 V Power for SAR AD
6	A2VSS	A2VSS	Analog Ground
7	A1VCC	A1VCC	4.5 V to 5.5 V Power for SAR AD
8	A1VREFH	A1VREFH	-0.3 to A1VCC + 0.3
9	A1VSS	A1VSS	Analog Ground
24	VSS	VSS	Ground
25	VDD	VDD	1.25V (Typ.) Power for the core (direct power supply) andconnection of the stabilizing capacitor for core power
32	RVCC	RVCC	4.5 V to 5.5 V Power for RDC
33	RVSS	RVSS	Resolver Ground
44	A0VREFH	A0VREFH	-0.3 to A0VCC + 0.3
45	A0VSS	A0VSS	Analog Ground
47	A0VCC	A0VCC	4.5 V to 5.5 V Power for SAR AD
50	VDD	VDD	1.25V (Typ.) Power for the core (direct power supply) andconnection of the stabilizing capacitor for core power
52	VSS	VSS	Ground
66	VCC	VCC	4.5 V to 5.5 V Power for oscillator, flash programming, and ports
68	VSS	VSS	Ground
70	VDD	VDD	1.25V (Typ.) Power for the core (direct power supply) andconnection of the stabilizing capacitor for core power
82	VDD	VDD	1.25V (Typ.) Power for the core (direct power supply) andconnection of the stabilizing capacitor for core power
84	VSS	VSS	Ground
95	VDD	VDD	1.25V (Typ.) Power for the core (direct power supply) andconnection of the stabilizing capacitor for core power
97	VSS	VSS	Ground
99	VCC	VCC	4.5 V to 5.5 V Power for oscillator, flash programming, and ports
110	VDD	VDD	1.25V (Typ.) Power for the core (direct power supply) andconnection of the stabilizing capacitor for core power
112	VSS	VSS	Ground
117	VSS	VSS	Ground
119	VCC	VCC	4.5 V to 5.5 V Power for oscillator, flash programming, and ports
120	VSS	VSS	Ground
121	SYSVCC	SYSVCC	4.5 V to 5.5 V Power for system logic
126	VSS	VSS	Ground
128	SYSVCC	SYSVCC	4.5 V to 5.5 V Power for system logic
129	VCC	VCC	4.5 V to 5.5 V Power for oscillator, flash programming, and ports
130	VSS	VSS	Ground
144	VDD	VDD	1.25V (Typ.) Power for the core (direct power supply) andconnection of the stabilizing capacitor for core power
146	VSS	VSS	Ground
164	VCC	VCC	4.5 V to 5.5 V Power for oscillator, flash programming, and ports
166	VSS	VSS	Ground
172	VDD	VDD	1.25V (Typ.) Power for the core (direct power supply) andconnection of the stabilizing capacitor for core power
174	VSS	VSS	Ground

Figure 6-2 Power Supply Pins




```
AS PER SECTION: 39.2.19 OF REV1.10 USERS MANUAL

UNDER RESET:
VDD SUPPLY CURRENT     = 335mA [MAX]
VCC SUPPLY CURRENT     = 15mA  [MAX]
SYSVCC SUPPLY CURRENT = 3mA    [MAX]

NORMAL OPERATION:
VDD SUPPLY CURRENT = 540mA [MAX]
VCC SUPPLY CURRENT = 60mA  [MAX]
SYSVCC SUPPLY CURRENT = 7mA [MAX]
A0VCC, A1VCC, A2VCC SUPPLY CURRENT = 30mA [MAX]
A0VREF, A1VREF, A2VREF SUPPLY CURRENT = 0.5mA [MAX]

CURRENT MEASUREMENT SUPPORT:
R-IDD IS FOR MEASUREMENT OF CORE CURRENT
RIAVCC IS FOR MEASUREMENT OF ANALOG SUPPLY CURRENT
R-ICC IS FOR MEASUREMENT OF SYSTEM LOGIC CURRENT
(WILL INCLUDE IO PORT AND NOT MATCH 39.2.19)
```

Pin #	Mapped Functions	User Functions	Comment / Remarks
116	X2	X2	Crystal oscillator connections
118	X1	X1	Crystal oscillator connections
122	MD1	MD1	Operating mode select pin
124	RESET	RESET	External reset input
125	FLMODE	FLMODE	Operating mode select pin
127	MD0	MD0	Operating mode select pin

Figure 6-3 System Pins

Pin #	Mapped Functions	User Functions	Comment / Remarks
83	AUDRST	AUDRST	AUD Debug
85	AUDCK	AUDCK	AUD Debug
86	AUDSYNC	AUDSYNC	AUD Debug
87	AUDATA3	AUDATA3	AUD Debug
88	AUDATA2	AUDATA2	AUD Debug
89	AUDATA1	AUDATA1	AUD Debug
90	AUDATA0	AUDATA0	AUD Debug
108	DCUTDO	DCUTDO	LPD / NEXUS debug
109	DCURDY	DCURDY	LPD / NEXUS debug
111	DCUTDI	DCUTDI	LPD / NEXUS debug
113	DCUTCK	DCUTCK	LPD / NEXUS debug
114	DCUTMS	DCUTMS	LPD / NEXUS debug
115	DCUTRST	DCUTRST	LPD / NEXUS debug

Figure 6-4 Debug Pins

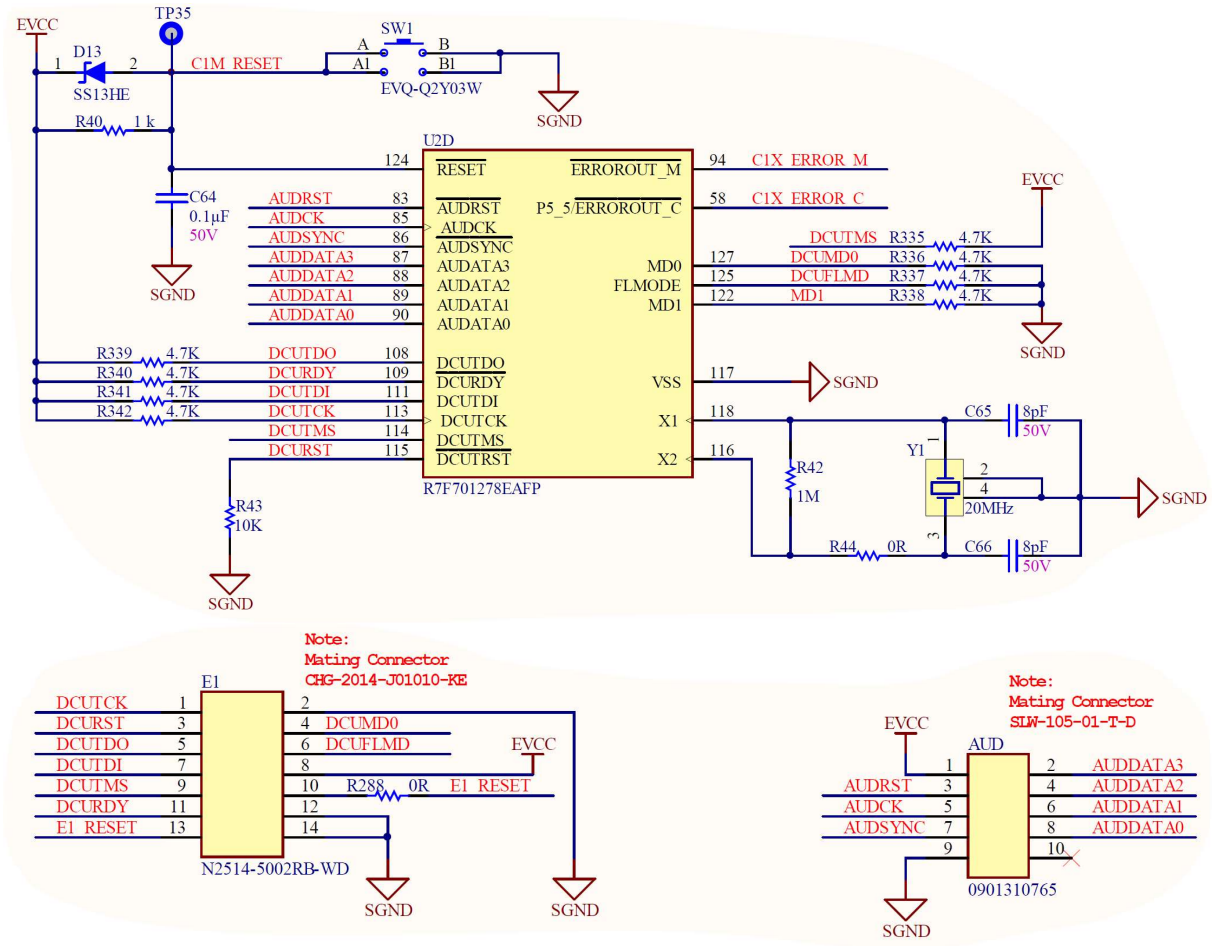


Figure 6-5 Debugger Connectors

CAUTION: DO NOT PRESS SW1 when DEBUGGER (E1/ E2) is connected to the system.

6.1.2 Reset Function

The Reset Circuit is a logical implementation with waterfall priority triggering interrupt or system reset. C1M_RESET is prioritized based on the critical signals on-board that can potentially damage the system if it continues to function under fault.

Priority	C1M-RESET CAUSE
3	PMIC_RESET
2	E1_RESET
1	EMERGENCY_STOP
1	CKT_FAULT

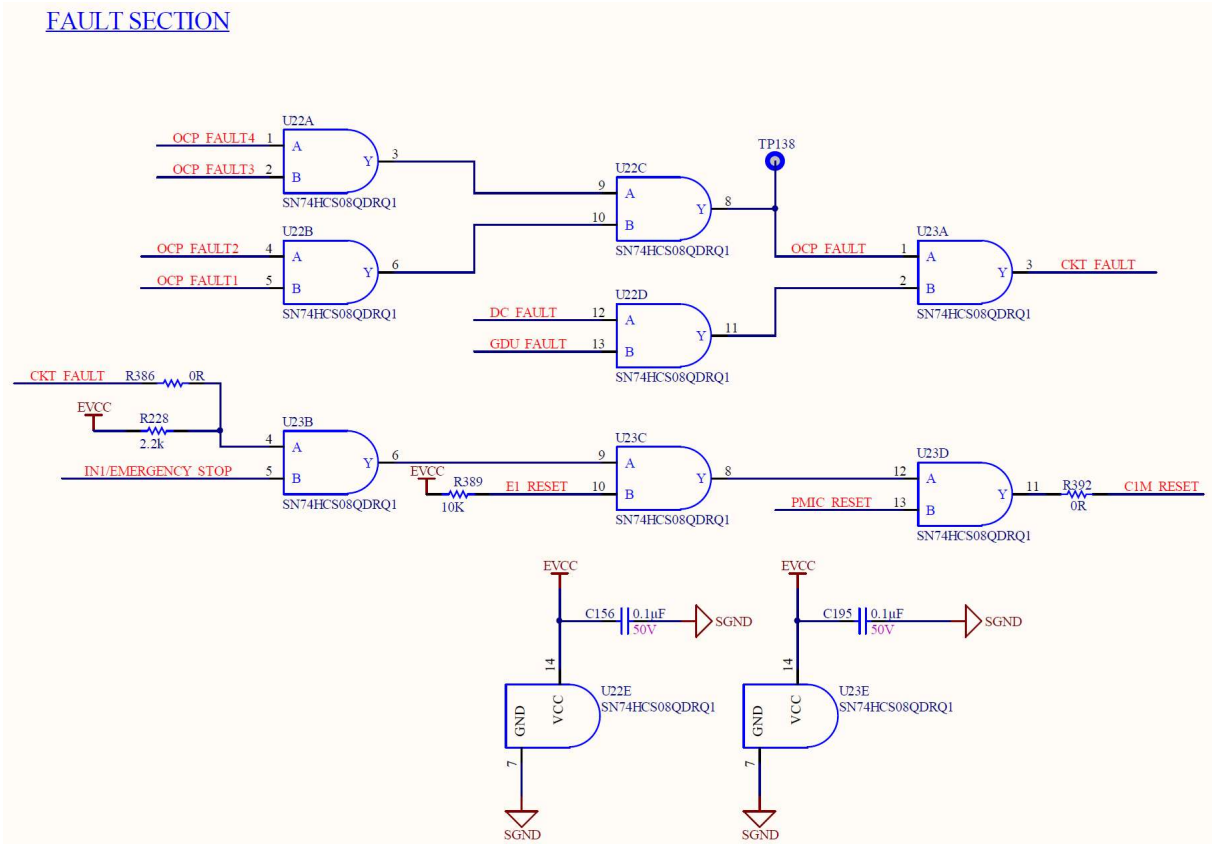


Figure 6-6 Fault and Reset Circuit

Design Consideration for Fault Monitoring:

The design implements Over Current and Voltage Monitoring by window comparator functions, therefore, if the signal falls out of bound of their respective upper / lower limits then trigger is generated notifying the controller of the fault. OCP_FAULTx are current monitoring for DC Bus and Motor Phase currents. DC_FAULT is DC BUS monitoring and GDU_FAULT is Gate-driver Supply monitoring output. The CKT_FAULT is combined fault signal. The Priority of CKT_FAULT is same as EMERGENCY_STOP signal and is lower than the priority of E1_RESET and PMIC_RESET. C1M_RESET is direct Push-button hard reset for MCU.

Priority C1M_RESET > PMIC_RESET > E1_RESET > EMERGENCY_STOP == CKT_FAULT.

Unmount R386 to disable the CKT_FAULT reset generation capability, R228 Pull-up will take care of keeping the EMERGENCY_STOP, E1_RESET and PMIC_RESET functionality in-tact.

6.2 Motor control

Design Consideration for Motor control functions:

Motor control signaling includes Input (Sensor input / triggers) and output (PWM Signal). Using the on-chip peripherals there is combination of peripherals that can be deployed for implementing Inverter Motor control. The ADC, RDC3A & ENCA peripherals are used for sensor and analog interfaces, while TSG and TAUD timer modules are used for PWM generation.

6.2.1 Encoder Input

Rotor Position Sensor Interface is achieved using digital and analog signals from the sensor in use. The on-chip peripheral like ENCA provides the functionality to utilize the Encoder input pins to connect incremental encoder (A, B & Z) as well as Hall sensor signals (HA, HB, HC), the selection is possible depending on the mode of operation. However, same pins are used from MCU side, therefore, user can either connect incremental encoder or Hall Sensor.

As you can see below, for ease of use, we have listed Encoder input pins as HALL_U_PIN, HALL_V_PIN and HALL_W_PIN connecting them to Encoder inputs ENCA0E0, ENCA0E1 and ENCA0EC pins of MCU, respectively.

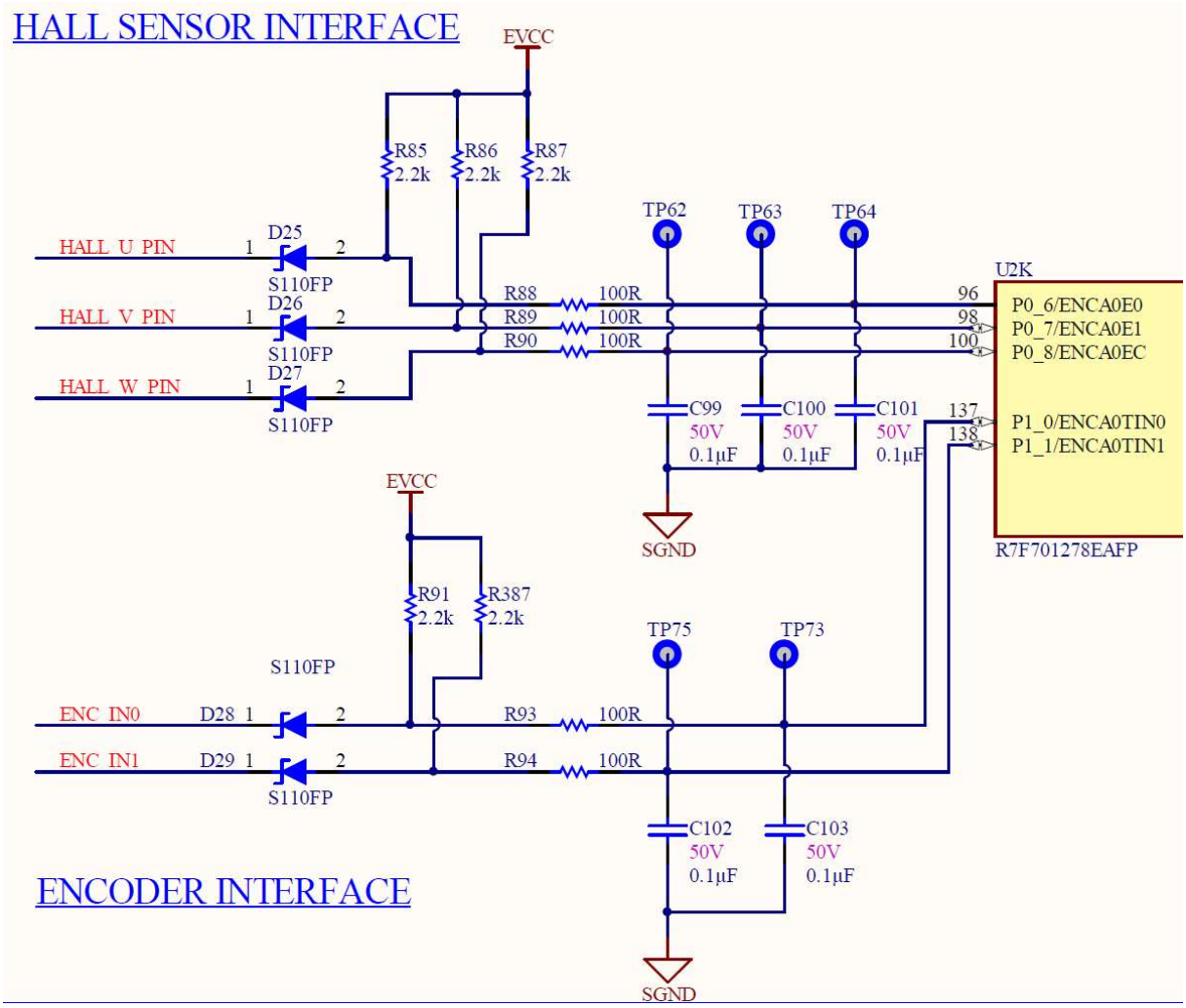


Figure 6-7 Encoder / Hall sensor Interface

IMPORTANT: When no sensor is connected to these connector pins, then, the pins will show 'High' due to pull-up to EVCC. Logic 'HIGH' indicates no motion when using encoder function and invalid pattern when using Hall-sensors, therefore, this is the safe state. The series diode ensure that only Active 'Low' signal is captured and any voltage above EVCC when applied to these input pins is blocked preventing damage to the MCU pins.

6.2.2 RDC Input

The R/D (resolver-to-digital) converter 3A converts the analog value (angle information) indicating the rotor angle of the resolver into a 16-bit (at maximum) digital value. RDC3A allows interfacing VR resolver (e.g. Tamagawa Seiki), the RDC3A provides option to interface DC resolver with Sin/Cosine signal output for absolute rotor position sensing. Selection of VR resolver or DC resolver is matter of configuration and tweaking the Hardware Input circuit to support the DC signaling with correct offset.

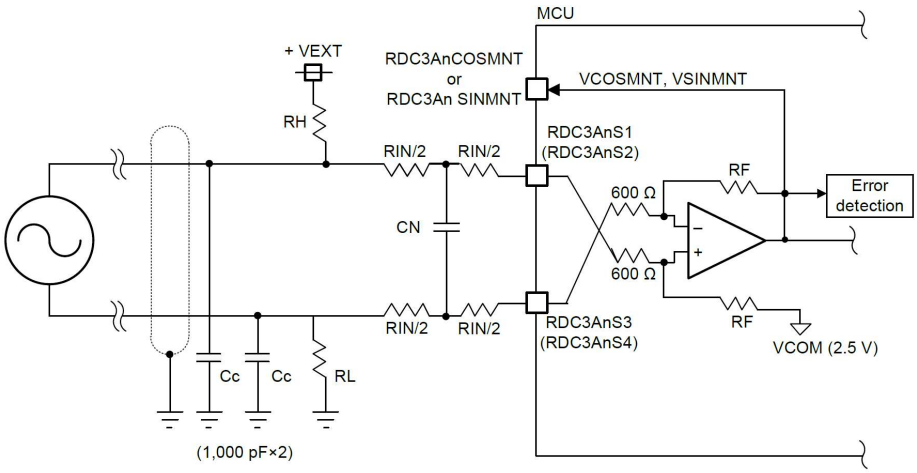
SENS Required Sensor Selection Function

Selects the required sensor.

0: Use the DC resolver*1

1: Use the VR resolver (default)

Figure 6-8 Selection of DC or VR Resolver



Note: The input resistance (RIN) tolerance (%) can affect the conversion accuracy (LSB). Approximately 0.3% corresponds with 1 LSB.

VCOSMNT, VSINMNT: Resolver signal monitor voltage
VCOM: IC internal reference voltage (= RVCC/2)
RF: 21 kΩ (typ). Subject to register setting and automatic adjustment function.

Figure 6-9 VR Resolver Signal Input Circuit

RIN: Resolver signal level

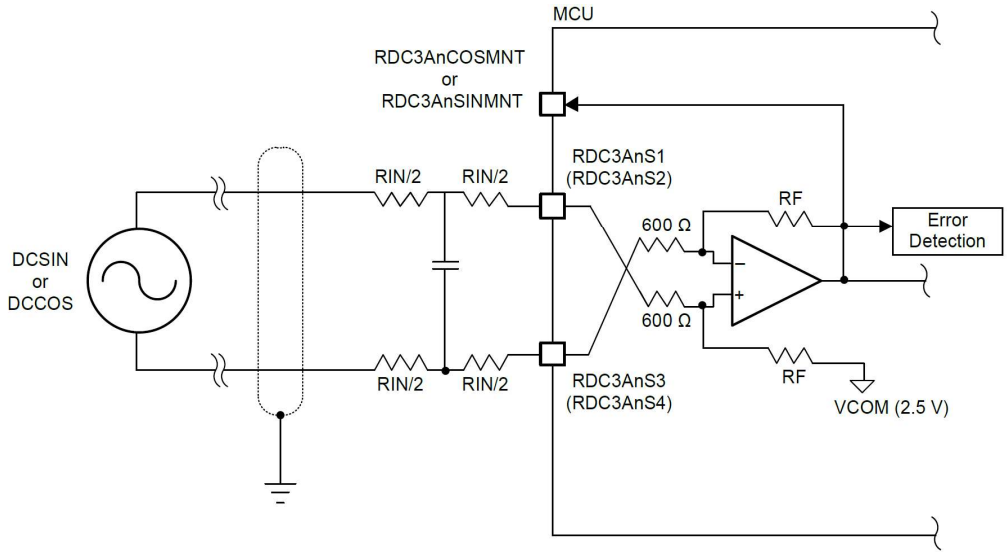
Adjust the signal level so that,

VCOSMNT or VSINMNT = (VIN) × (RF / (RIN + 600 Ω)) falls within the range from 0.36 × RVCC to 0.64 × RVCC [Vpp].

(where VIN denotes the signal output voltage between resolver pins [Vpp], RIN ≥ 2[kΩ])

RH and RL: Determine a resistance value in an 89% to 100% range from the following calculated values:

1. RH ≈ {(RVCC – VCOM) / (22.0 × 10^{-6})} – RIN, where VCOM = RVCC/2[V]
2. RL ≈ {VCOM/(22.0 × 10^{-6})} – RIN, where VCOM = RVCC/2[V]



Note: The input resistance (RIN) tolerance (%) can affect the conversion accuracy (LSB). Approximately 0.3% corresponds with 1 LSB. Differences in input signal conditions and peripheral circuits can affect the RD conversion accuracy and the error detection function.

Figure 6-10 DC Resolver Input Circuit

CAUTION: The reference design implements the Excitation Voltage Booster Amplifier Circuit (Single Power Supply) on-board, allowing to interface VR resolver. If the DC resolver must be interfaced via RDC3A pins RDC3AnS1 (RDC3AnS2) and RDC3AnS3 (RDC3AnS4) then please consult Renesas technical support.

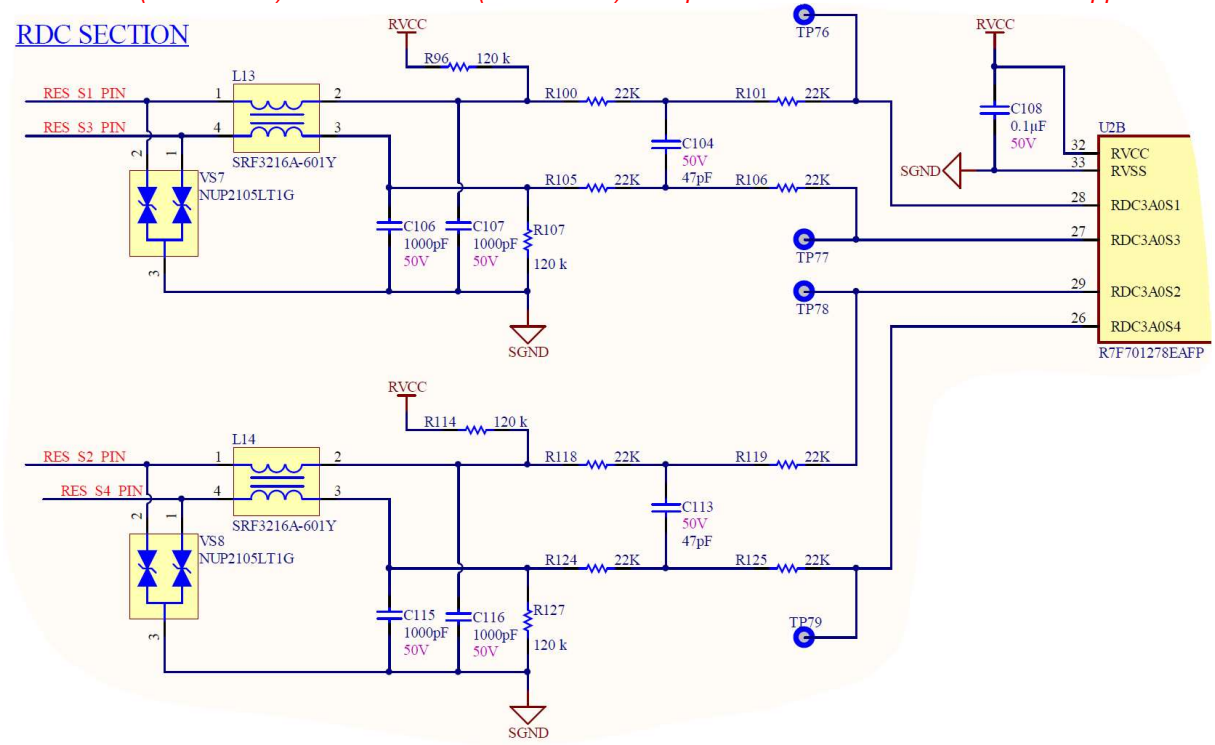


Figure 6-11 RDC Input Circuit

IMPORTANT: DC Resolver interface, Unmount the following: R96, R107, R114 and R127. The Applied DC Resolver SIN/COSINE signal must be applied with 2.5V DC offset for the RDC to compute angle correctly.

6.2.3 Output: TSG3 for 3 Phase Motor Control

The TSG3n is an 18-bit timer counter with various motor control functions, the counter clock of 80MHz offers minimum resolution of 12.5nsec. Independent dead-time can be set for positive to inverse phase change and vice-versa. Forced output stop function allows the Hi-z control of the TSG output pins TSG3nO1~O6. Additionally, ADC Trigger signal generation from the TSG compare match is possible without any software intervention.

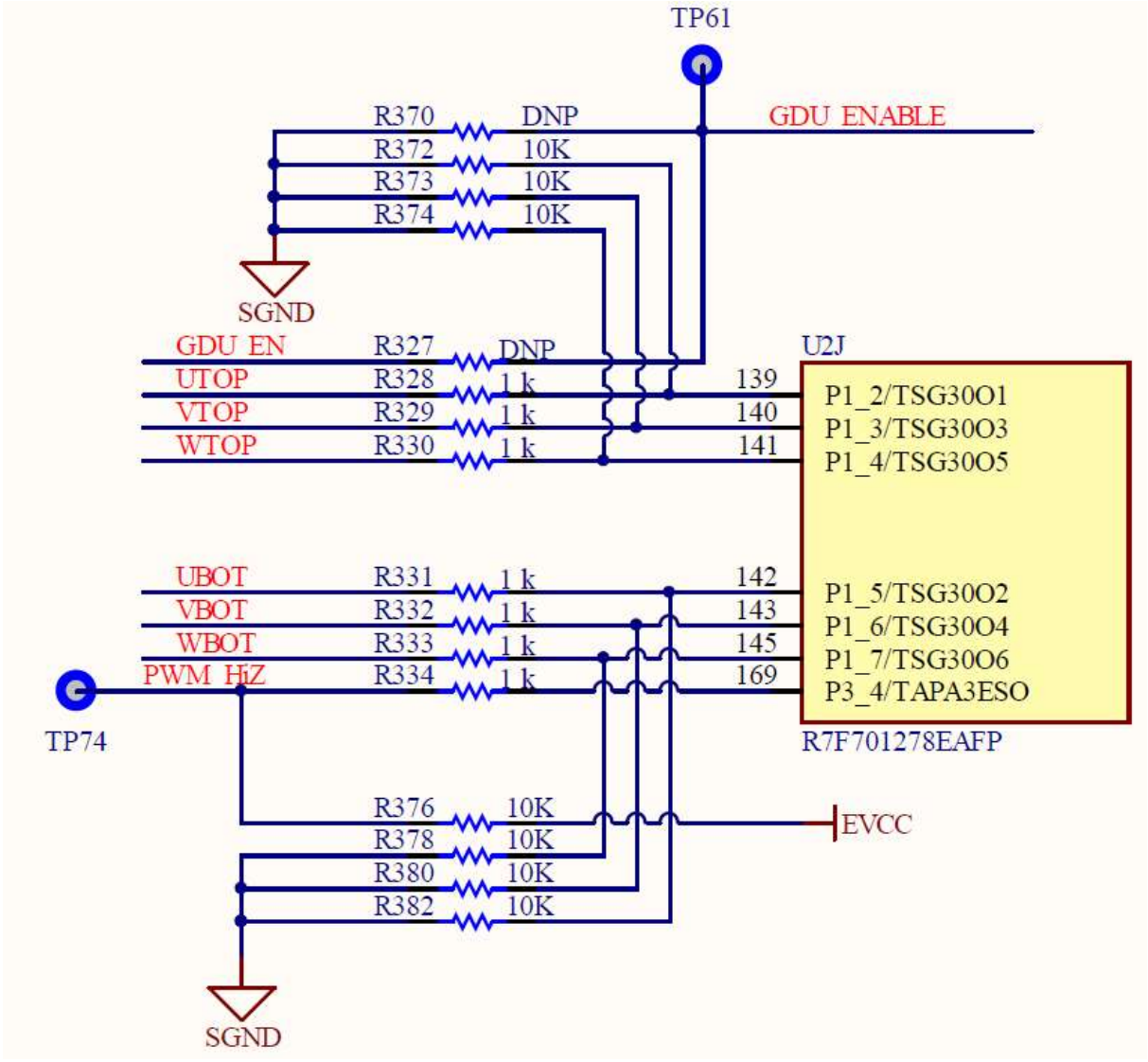


Figure 6-12 TSG30 PWM Output with TAPA3ESO Hi-z Control

The HT-PWM mode is commonly used for Inverter control. In this mode, the 18-bit counter (up/down count by ± 2 bits, practically 17 bits) and the 18-bit compare registers (LSB is used to control additional pulse) are used to generate a 6-phase PWM signal.

1. Set the carrier wave period to TSG3nCMP0E.
2. Set the duty cycle of the voltage data signals of the U phase, V phase, and W phase with TSG3nCMPUE, TSG3nCMPVE, and TSG3nCMPWE. (The values set to TSG3nCMPUE, TSG3nCMPVE, and TSG3nCMPWE are reflected immediately to the corresponding TSG3nCMPmE (m = 1, 2, 5, 6, 9, 10)).
3. The INTTSG3nIPEK interrupt (Peak Intr.) is generated only when TSG3nCTL4.TSG3nPRE = 1.
4. The INTTSG3nIVLY interrupt (Trough Intr.) is generated only when TSG3nCTL4.TSG3nVRE = 1.
5. The ADC conversion trigger can be enabled from TSG in HT-PWM mode, please refer User's Manual for details.

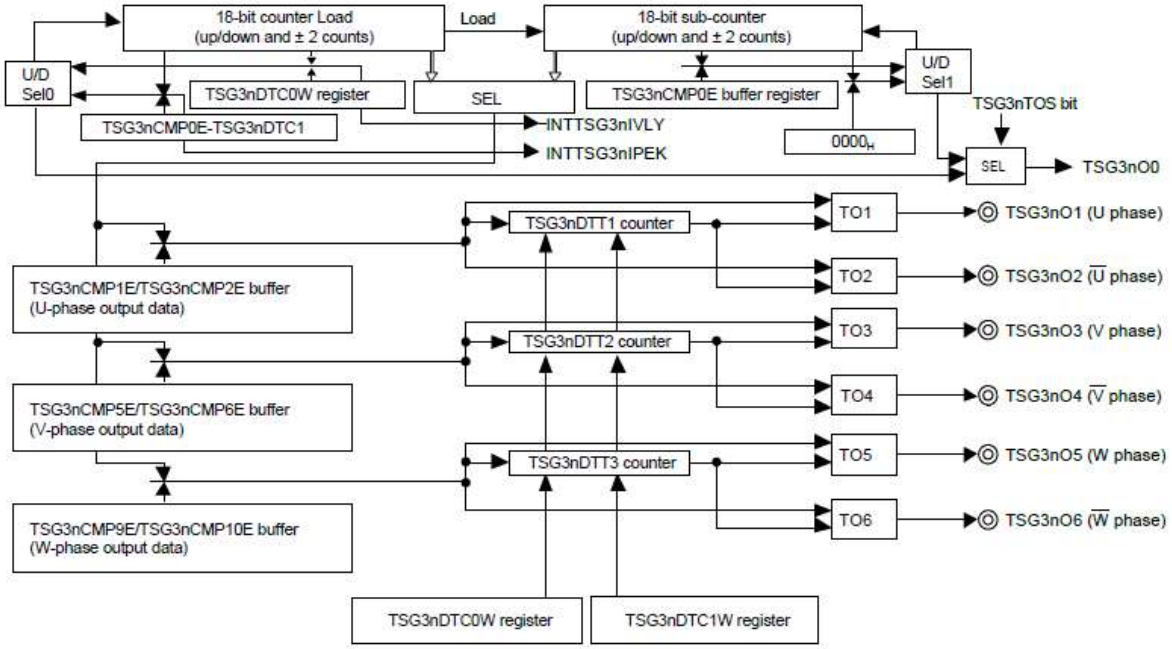


Figure 6-13 HT-PWM Mode Block Diagram

The 120-DC Mode: In this mode, PWM output period set to TSG3nCMP0E and timer output (TSG3nO1 to TSG3nO6) according to the duty cycle set to TSG3nCMP1E to TSG3nCMP12E are controlled with three types of pattern inputs (software output control method, pattern switch method, and trigger switch method) to perform 120-DC control.

1. Set the PWM period to TSG3nCMP0E.
2. Set the PWM duty to TSG3nCMP1E to TSG3nCMP12E and set the output pattern to TSG3nPAT0W and TSG3nPAT1W.
3. INTTSG3nIPEK Peak interrupt (generated at the same timing as INTTSG3nI0)
4. INTTSG3nIWN Warning interrupt → when illegal pattern is detected.
5. The ADC conversion trigger can be enabled from TSG in HT-PWM mode, please refer User's Manual for details.

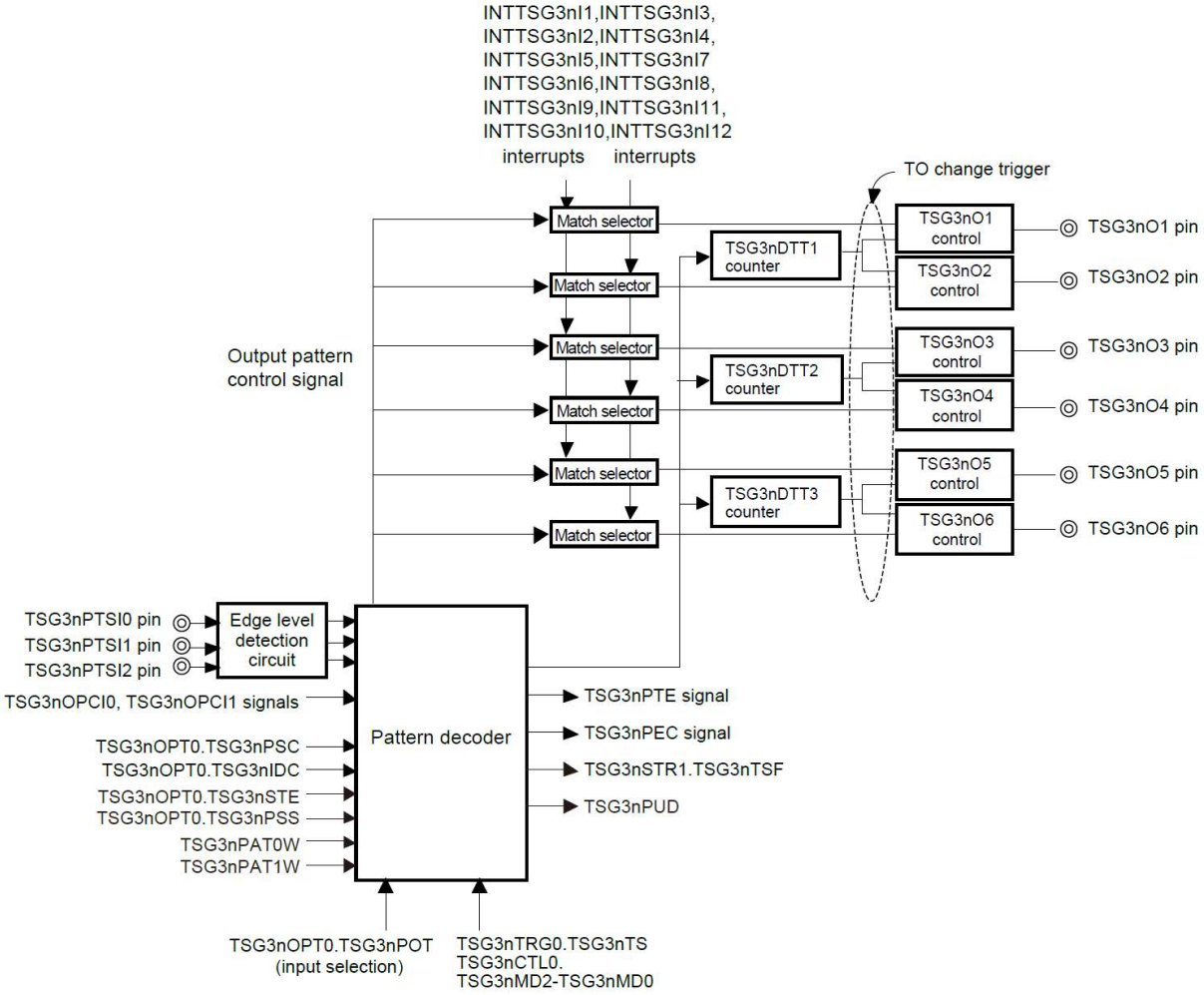


Figure 6-14 120-DC Mode Block Diagram

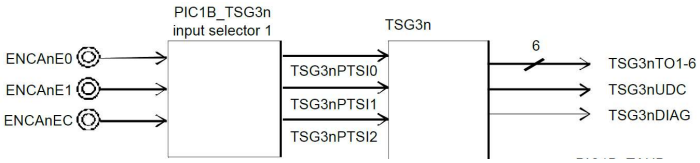


Figure 6-15 ENCAnEx to TSG3nPTSIx signal via PIC1B

IMPORTANT: The TSG3nPTSIx pin signal shown in Fig 6-13 is connected to ENCAnEx pin of the MCU. There is no TSG3nPTSIx pin on the MCU.

6.2.4 Output: TAUD for 3 Phase Motor Control

The high accuracy triangle wave PWM output function with the dead time is realized by using the triangle wave PWM output function/one-shot pulse output function of TAUD0 and PIC1B in combination. The following figure shows the block diagram of the high accuracy triangle wave PWM output function with the dead time.

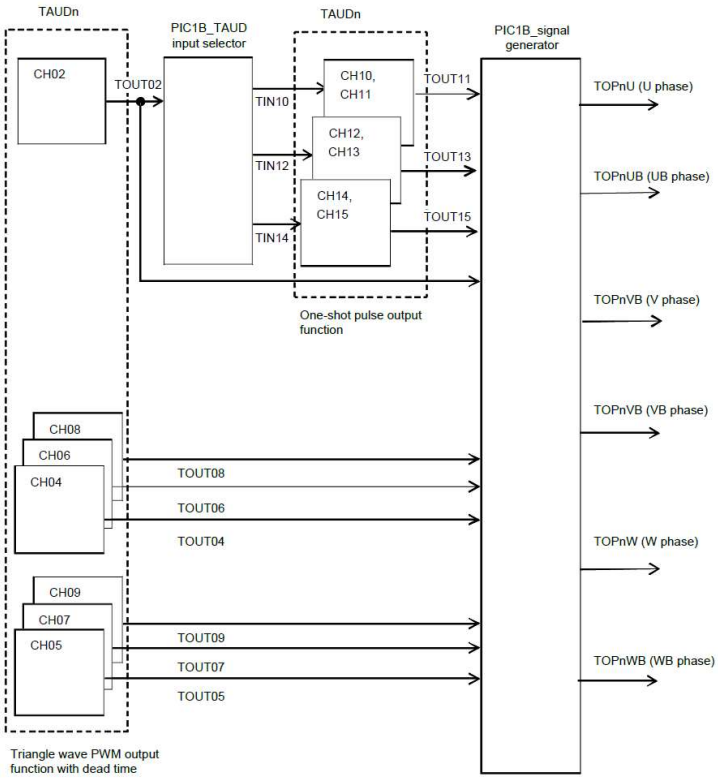


Figure 6-16 Block Diagram of High Accuracy Triangle Wave Three-Phase PWM Output with Dead Time

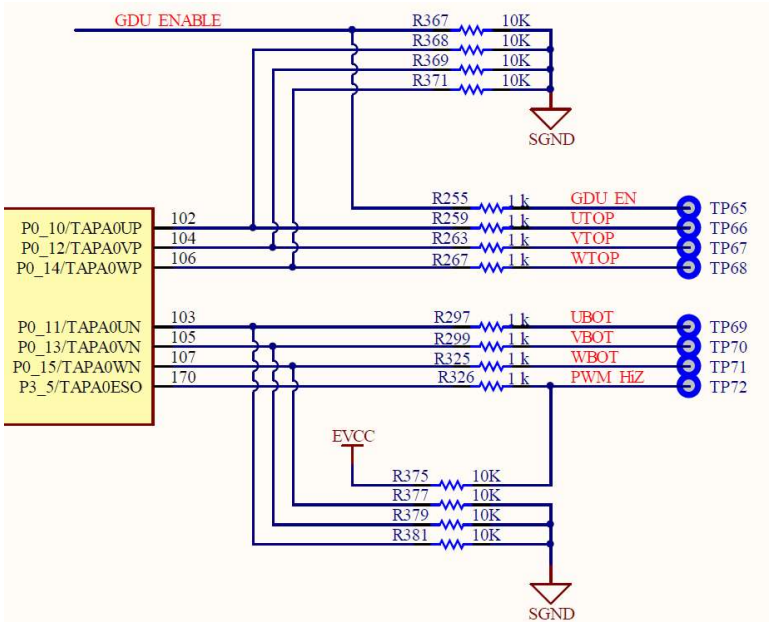


Figure 6-17 TAUD0 uses TAPA0 3Phase PWM Outputs

6.2.5 Output: Hi-z Control

Abnormal operation in timer motor-control under CPU control leads to rotation of the externally connected motor also becoming abnormal. In such a case, this function forcibly sets the motor control output to the Hi-Z state, independently of control by the CPU.

TAPA3 connects ESO3 to enable Hi-z control of TSG30 6-phase PWM outputs.

TAPA0 connects ESO0 to enable Hi-z control of TAUD0 PWM Outputs.

Table 24.84 Setting Value

Register Name	Bit 5	Bit 4	Bit 3	Bit 0	Register to be Controlled	TAPA to be Connected
PIC1BHIZCEN00	ERROROUTZ	—	—	ESO0	TAUD0	TAPA0
PIC1BHIZCEN01	ERROROUTZ	—	—	ESO1	TAUD1	TAPA1
PIC1BHIZCEN02	ERROROUTZ	—	INTTSG30IER	ESO3	TSG30	TAPA3
PIC1BHIZCEN03	ERROROUTZ	INTTSG31IER	—	ESO4	TSG31	TAPA4
PIC1BHIZCEN10*1	ERROROUTZ	—	—	ESO2	TAUD2	TAPA2
PIC1BHIZCEN12*1	ERROROUTZ	—	INTTSG32IER	ESO5	TSG32	TAPA5

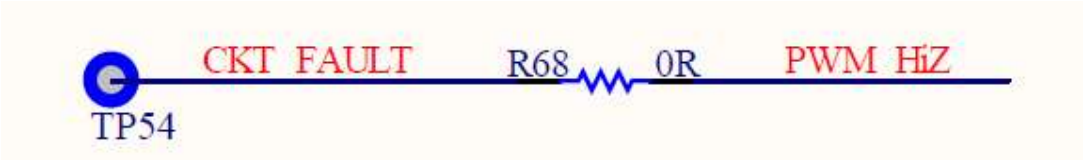


Figure 6-18 Circuit Fault Signal Connects to PWM Hi-z Control.

6.2.6 Motor Control with RDC3A and EMU3

Pin #	Mapped Functions	User Functions	Comment / Remarks	
21	RDC3A0COSMNT	RDC3A0COSMNT	COS-side monitoring signal output	Dedicated to RDC3A
23	RDC3A0SINMNT	RDC3A0SINMNT	SIN-side monitoring signal output	Dedicated to RDC3A
26	RDC3A0S4	RDC3A0S4	Resolver signal input	Dedicated to RDC3A
27	RDC3A0S3	RDC3A0S3	Resolver signal input	Dedicated to RDC3A
28	RDC3A0S1	RDC3A0S1	Resolver signal input	Dedicated to RDC3A
29	RDC3A0S2	RDC3A0S2	Resolver signal input	Dedicated to RDC3A
30	RDC3A0RSO	RDC3A0RSO	Excitation signal input/output	Dedicated to RDC3A
31	RDC3A0COM	RDC3A0COM	Excitation common signal input/output	Dedicated to RDC3A
91	RDC3A0_OUT_W	RDC3A0_OUT_W	RD0_OUT_W Encoder pulse output *-optional	
92	RDC3A0_OUT_V	RDC3A0_OUT_V	RD0_OUT_V Encoder pulse output *-optional	
93	RDC3A0_OUT_U	RDC3A0_OUT_U	RD0_OUT_U Encoder pulse output *-optional	
139	TSG30O1	TSG30O1	Uphase +	TSG PWM Output
140	TSG30O3	TSG30O3	Vphase +	TSG PWM Output
141	TSG30O5	TSG30O5	Wphase +	TSG PWM Output
142	TSG30O2	TSG30O2	Uphase -	TSG PWM Output
143	TSG30O4	TSG30O4	Vphase -	TSG PWM Output
145	TSG30O6	TSG30O6	Wphase -	TSG PWM Output
169	TAPA3ESO	TAPA3ESO	Emergency Hi-Z request input (for TSG30 PWM)	H/W Cut-off Trigger Input for PWM Output by TSG30

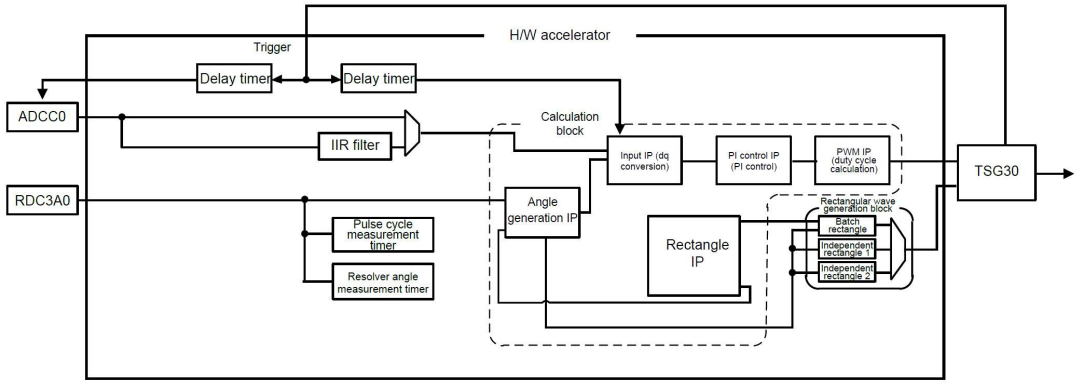


Figure 6-19 EMU30 Block Diagram

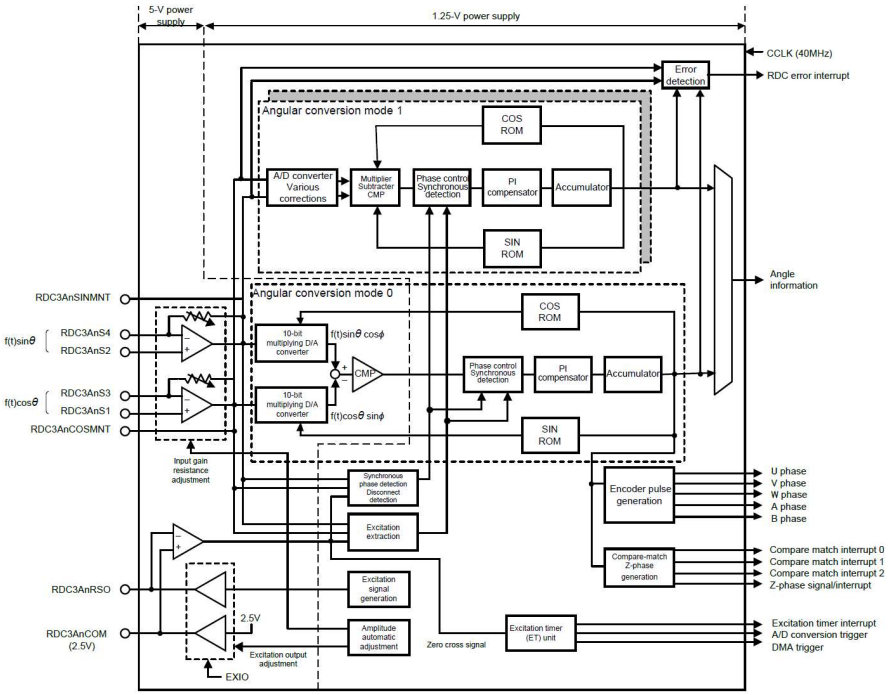


Figure 6-20 RDC3A Block Diagram

6.2.7 Motor Control with ENCA and EMU3

Pin #	Mapped Functions	User Functions	Comment / Remarks	
96	ENCA0E0	ENCA0E0	encoder input 0 (count pluse 0) - TSG30PTSI0	
98	ENCA0E1	ENCA0E1	encoder input 1 (count pluse 1) - TSG30PTSI1	
100	ENCA0EC	ENCA0EC	encoder input (clear Pulse) - TSG30PTSI2	
137	ENCA0TIN0	ENCA0TIN0	Timer I/O , Port	Encoder Trigger Input
138	ENCA0TIN1	ENCA0TIN1	Timer I/O , Port	Encoder Trigger Input
139	TSG30O1	TSG30O1	Uphase +	TSG PWM Output
140	TSG30O3	TSG30O3	Vphase +	TSG PWM Output
141	TSG30O5	TSG30O5	Wphase +	TSG PWM Output
142	TSG30O2	TSG30O2	Uphase -	TSG PWM Output
143	TSG30O4	TSG30O4	Vphase -	TSG PWM Output
145	TSG30O6	TSG30O6	Wphase -	TSG PWM Output
169	TAPA3ESO	TAPA3ESO	Emergency Hi-Z request input (for TSG30 PWM)	H/W Cut-off Trigger Input for PWM Output by TSG30

6.2.8 Motor Control with ENCA and TAUD0 – 120 Deg Trapezoidal S/W Control

The ENCA0Ex pins can be used as Hall Sensor Input pins when using 120 Trapezoidal function using Software control implementation.

Pin #	Mapped Functions	User Functions	Comment / Remarks	
96	ENCA0E0	ENCA0E0	encoder input 0 (count pluse 0) - TSG30PTSI0	TSG3nPTSI0 is used as HALL SENSOR Inputs in 120 deg Commutation mode.
98	ENCA0E1	ENCA0E1	encoder input 1 (count pluse 1) - TSG30PTSI1	TSG3nPTSI1 is used as HALL SENSOR Inputs in 120 deg Commutation mode.
100	ENCA0EC	ENCA0EC	encoder input (clear Pulse) - TSG30PTSI2	TSG3nPTSI2 is used as HALL SENSOR Inputs in 120 deg Commutation mode.
102	TAPA0UP	TAPA0UP	Motor control output U phase (positive)	TAUD Output
103	TAPA0UN	TAPA0UN	Motor control output U phase (negative)	TAUD Output
104	TAPA0VP	TAPA0VP	Motor control output V phase (positive)	TAUD Output
105	TAPA0VN	TAPA0VN	Motor control output V phase (negative)	TAUD Output
106	TAPA0WP	TAPA0WP	Motor control output W phase (positive)	TAUD Output
107	TAPA0WN	TAPA0WN	Motor control output W phase (negative)	TAUD Output
170	TAPA0ESO	TAPA0ESO	Emergency Hi-Z request input (for TAUD0 PWM)	H/W Cut-off Trigger Input for PWM Output by TAUD0

6.2.9 Motor Control with ENCA and TSG30 – 120DC Mode H/W Control

Pin #	Mapped Functions	User Functions	Comment / Remarks	
96	ENCA0E0	ENCA0E0	encoder input 0 (count pluse 0) - TSG30PTSI0	TSG3nPTSI0 is used as HALL SENSOR Inputs in 120 deg Commutation mode.
98	ENCA0E1	ENCA0E1	encoder input 1 (count pluse 1) - TSG30PTSI1	TSG3nPTSI1 is used as HALL SENSOR Inputs in 120 deg Commutation mode.
100	ENCA0EC	ENCA0EC	encoder input (clear Pulse) - TSG30PTSI2	TSG3nPTSI2 is used as HALL SENSOR Inputs in 120 deg Commutation mode.
139	TSG30O1	TSG30O1	Uphase +	TSG PWM Output
140	TSG30O3	TSG30O3	Vphase +	TSG PWM Output
141	TSG30O5	TSG30O5	Wphase +	TSG PWM Output
142	TSG30O2	TSG30O2	Uphase -	TSG PWM Output
143	TSG30O4	TSG30O4	Vphase -	TSG PWM Output
145	TSG30O6	TSG30O6	Wphase -	TSG PWM Output
169	TAPA3ESO	TAPA3ESO	Emergency Hi-Z request input (for TSG30 PWM)	H/W Cut-off Trigger Input for PWM Output by TSG30

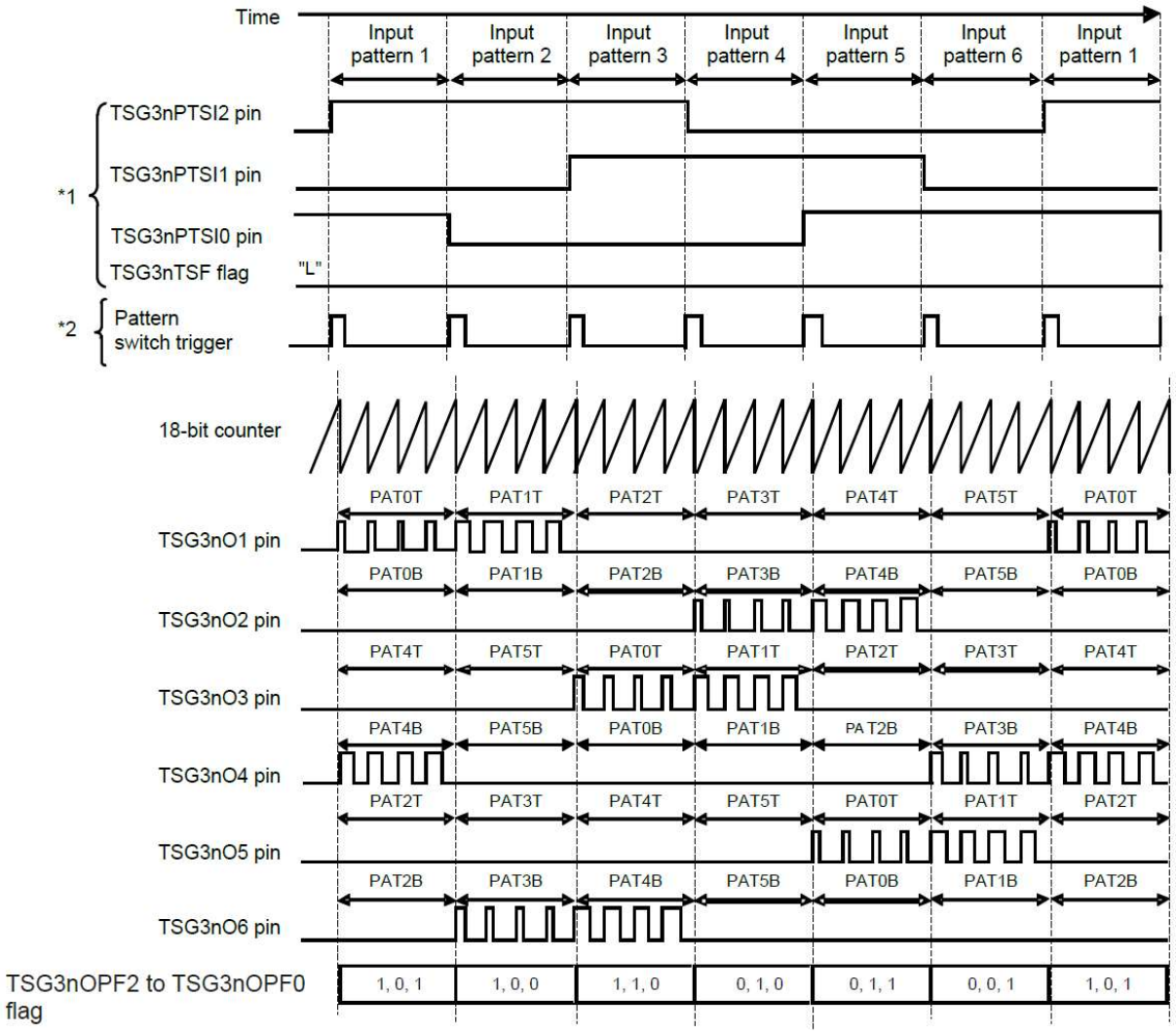


Figure 6-21 Example of 120DC Mode Operation

6.3 Communication Functions

6.3.1 SPI Interface

SPI Communication is mapped to control PMIC and additional CS is provided to the user via on-board connector as shown below:

Pin #	Mapped Functions	User Functions	Comment / Remarks
73	CSIH0SI	CSIH0SI	Serial data input signals
74	CSIH0SO	CSIH0SO	Serial data output signals
75	CSIH0SC	CSIH0SC	Serial clock input signal
76	CSIH0CSS0	CSIH0CSS0	Chip select signals
77	CSIH0CSS1	CSIH0CSS1	Chip select signals

Figure 6-22 SPI Signals

CSIH0CSS0 is used as Chip Select for on-board PMIC. The PMIC tracker output required by CAN Transceiver and other functions are controlled via SPI communication from the processor.

CSIH0CSS1 is mapped to EXT_SPI connector on-board and can be utilized by user for interfacing any other external communication module such as BT or additional high capacity NOR Flash for logging etc…

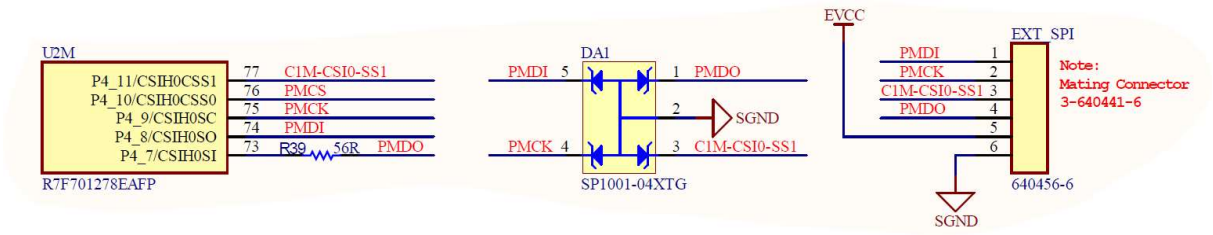


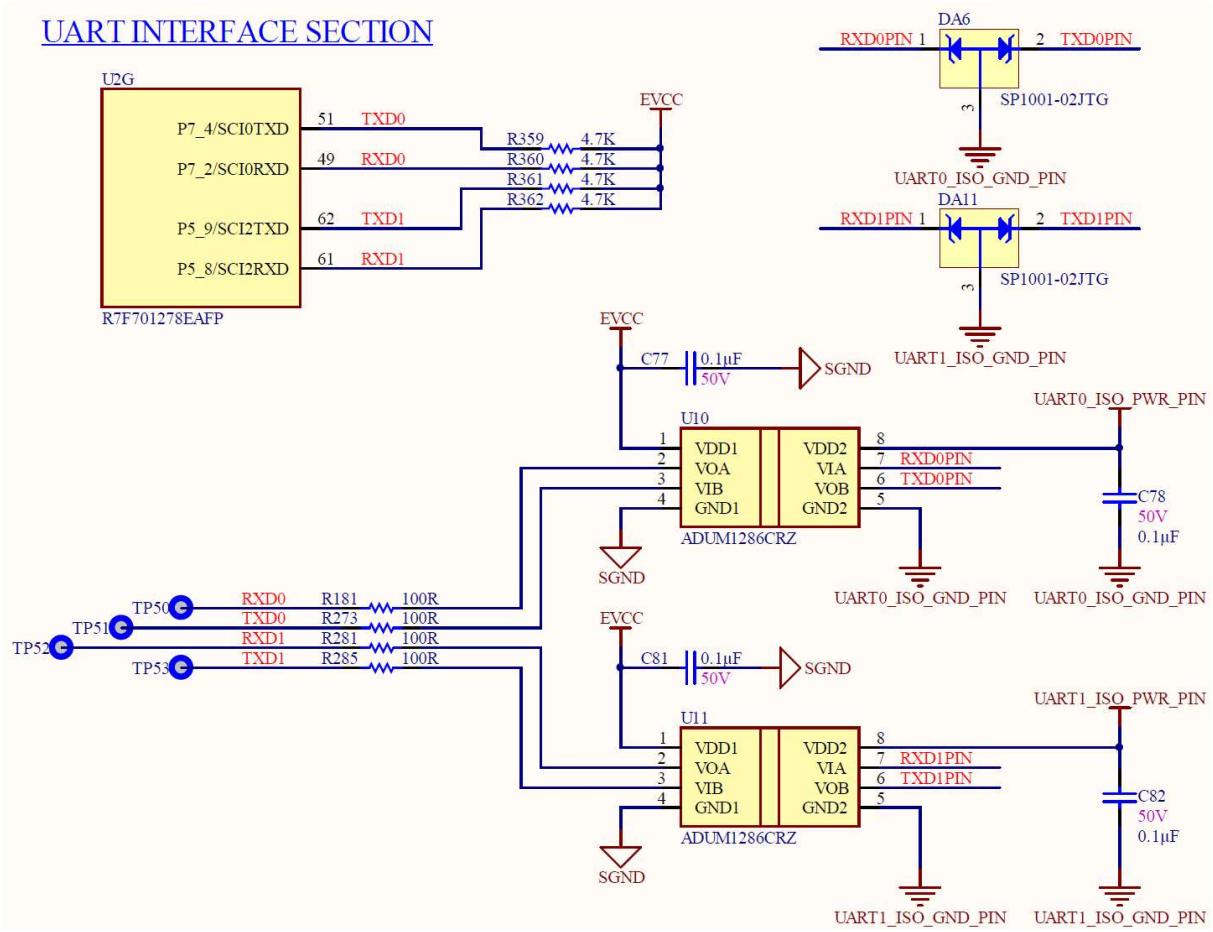
Figure 6-23 SPI Signalling used for PMIC and External SPI

CAUTION: EVCC = 5V is mapped to EXT_SPI, therefore, do not connect module operating at lower voltage such as 3.0V / 3.3V / 3.6V / 4.2V. If the EVCC is used for powering the external module, then due care to be taken by user, so that, it does not cause any harm to external module or Inverter control board power supply.

6.3.2 UART Interface

Pin #	Mapped Functions	User Functions	Comment / Remarks
49	SCI0RXD	SCI0RXD	SCIn receive data
51	SCI0TXD	SCI0TXD	SCIn transmit data
61	SCI2RXD	SCI2RXD	SCIn receive data
62	SCI2TXD	SCI2TXD	SCIn transmit data

The 2 Nos of UART Channels are provided to the user for communicating externally. The Signals are isolated and therefore, require external power to be provided on the isolated side. E.g., if UART to USB module is connected to the Inverter via port then UARTx_ISO_PWR_PIN needs to be powered by 3.0V ~ 5V from the module side and on the Microcontroller side the isolator is powered by EVCC = 5V as shown in schematic. Refer COM Connector Detail for UARTx_ISO_PWR_PIN.



CAUTION: Without Powering the Isolated side of the ADUM1286CRZ, communication cannot be established.

6.3.3 CAN Interface

The On-chip RS-CANFD Module support 2 interface modes:

1. Classical CAN mode: Handles only classical CAN frames.
2. CAN FD mode: Handles classical CAN frames and CAN FD frames.

This product supports ISO 11898-1:2015 compatible CAN FD with a new CRC field containing a stuff counter. It can also support the CRC field that conforms to ISO/CD 11898-1 (2014-08-12 version) when the NIE bit of the RSCFDnCFDGCRCCFG register is set to 1.

The RS-CANFD module support 320 Buffers in total for details refer User's Manual & ECC is supported.

The reference design provides 4 CAN Channels to the user allowing to fully utilize the RS-CANFD.

Pin #	Mapped Functions	User Functions	Comment / Remarks
67	CAN0RX	CAN0RX	CANm receive data input
69	CAN0TX	CAN0TX	CANm transmit data output
71	CAN1RX	CAN1RX	CANm receive data input
72	CAN1TX	CAN1TX	CANm transmit data output
80	CAN3RX	CAN3RX	CANm receive data input
81	CAN3TX	CAN3TX	CANm transmit data output
134	CAN2RX	CAN2RX	CANm receive data input
135	CAN2TX	CAN2TX	CANm transmit data output

CAN0,1 and 3 provide Non-isolated Classic CAN interface via NCV7351D1ER2G transceiver. *EN Pin* on NCV7351D1E Version Allowing Switching the Transceiver to a *Very Low Current OFF Mode*.

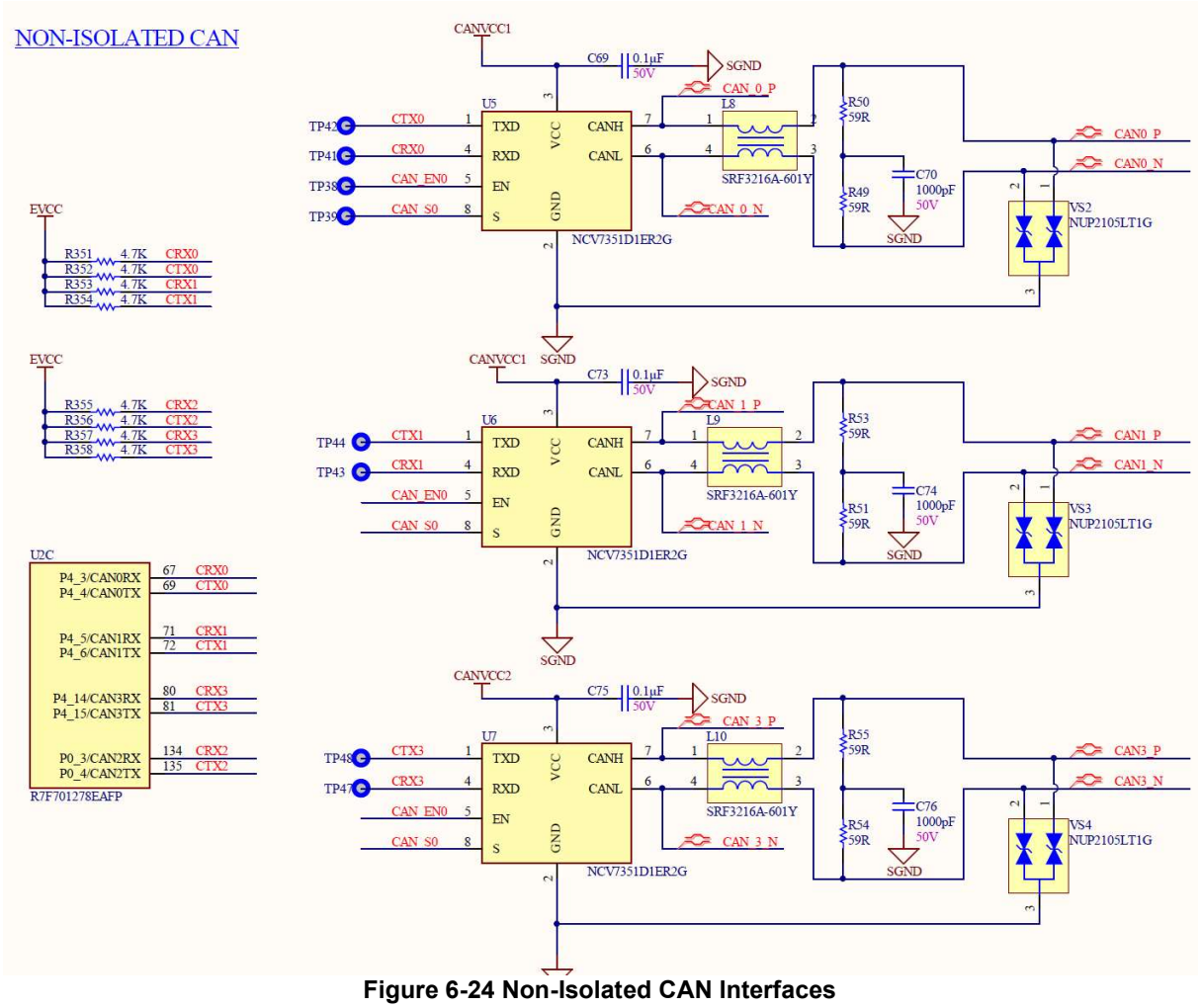


Figure 6-24 Non-Isolated CAN Interfaces

CAN2 provides CANFD isolated interface via ADM3050EBRWZ. The transceiver features support for the following:

- 1.7 V to 5.5 V supply and logic side levels
- 4.5 V to 5.5 V supply on bus side
- ISO 11898-2:2016-compliant CAN FD
- Data rates up to 12 Mbps for CAN FD
- 5.7 kV rms signal isolated CAN FD transceiver

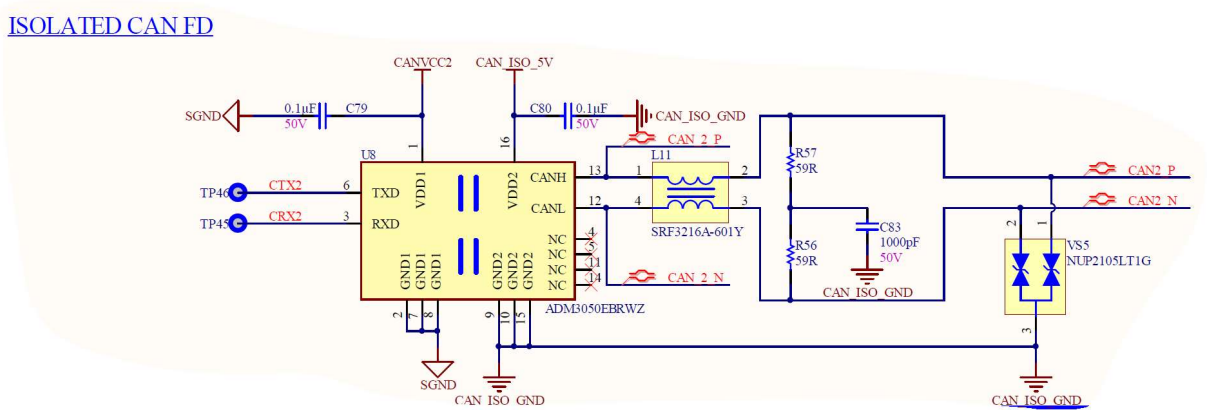


Figure 6-25 Isolated CANFD Interface

CAUTION: Without Powering the Isolated CAN BUS side of the ADM3050E, communication cannot be established.

6.3.4 LIN Interface

LIN communication controller that supports LIN Specification Package Revision 1.3, 2.0, 2.1, 2.2, and SAE J2602, and automatically performs frame communication and error determination.

Channel 0,1 and 2 of LIN are mapped to the LIN transceiver on-board. Channel 1 of NCV7424 is not mapped.

Pin #	Mapped Functions	User Functions	Comment / Remarks
53	RLIN32RX	RLIN32RX	RLIN3m receive data input
54	RLIN32TX	RLIN32TX	RLIN3m transmit data output
55	RLIN31RX	RLIN31RX	RLIN3m receive data input
56	RLIN31TX	RLIN31TX	RLIN3m transmit data output
78	RLIN30RX	RLIN30RX	RLIN3m receive data input
79	RLIN30TX	RLIN30TX	RLIN3m transmit data output

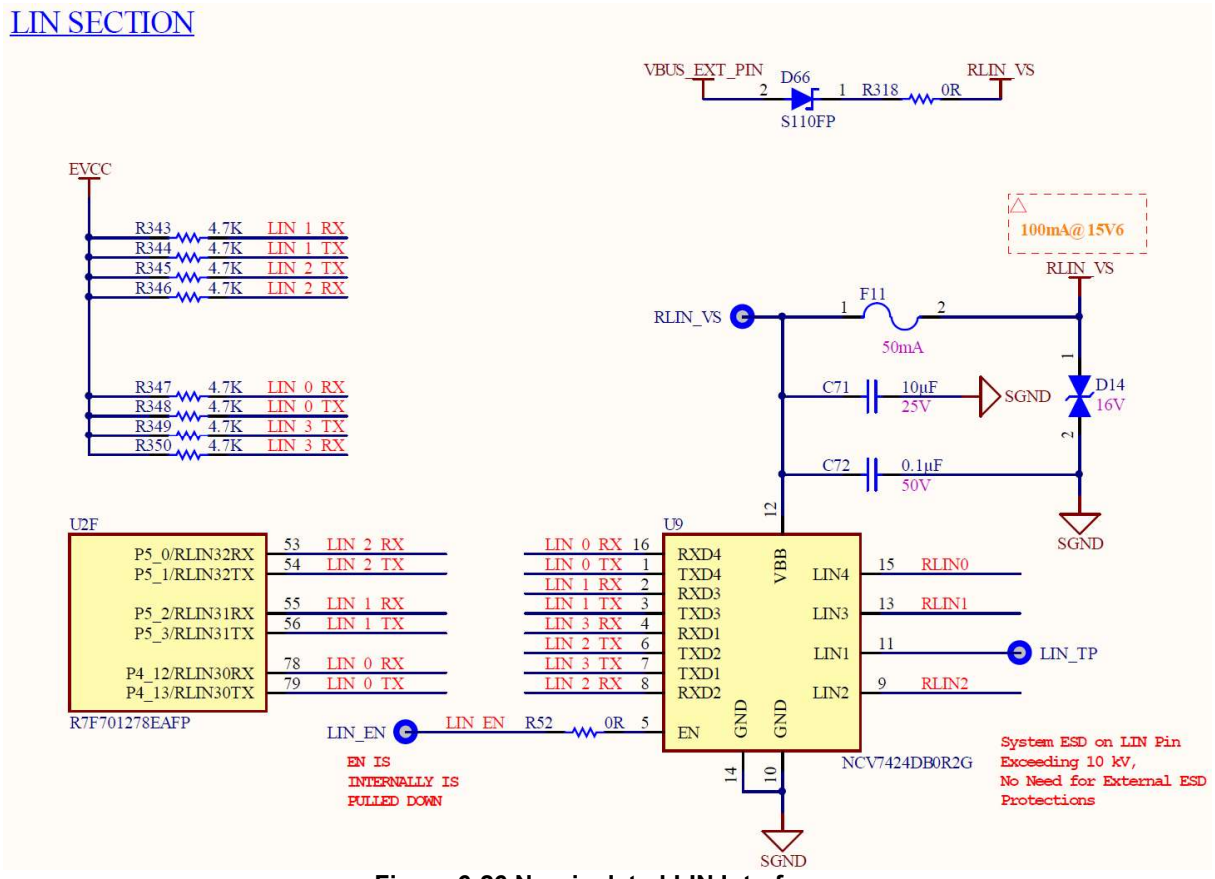


Figure 6-26 Non-isolated LIN Interfaces

CAUTION: RLIN_VS Power Supply for the LIN Transceiver is derived from the VBUS_EXT_PIN (expected to be 12V Power Bus Net). The maximum rated current for NCV7424D when transmitting Dominant bit is 28mA and therefore, Fuse F11 used here is 50mA. Therefore, ensure that RLIN_VS is present when troubleshooting LIN Communication.

Note the following mapping to avoid confusion while programming or referring LIN channels of MCU and Transceiver. This mapping was result of the PCB layout tracing.

LIN Channel Mapping MCU & LIN Transceiver

Usage	MCU Channel	Transceiver Channel
Used	Channel 0	Channel 4
Used	Channel 1	Channel 3
Used	Channel 2	Channel 2
Unused	Channel 3	Channel 1

6.3.5 SENT Interface

Single Edge Nibble Transmission module (RSENT) interface supports the following standard specification (SAE J2716 version JAN2010). Compatible with 3 systems, i.e., SENT standard (1-wire system), SPC extension (1-wire system), and SPC extension (2-wire system). Bidirectional communication: Between the sensor and MCU (supported in SPC mode). Data transmission protected with CRC is available. Multiple sensors can connect to the RSENT channel that has the standard expansion function. Received data from sensors is detected by software or DMA. Timestamp function: Master can only be set for RSENT0.

Variable data transmission rate

− 24.7 kbps to 64.9 kbps: 3 clock rate 6 nibble data

− 74.1 kbps to 194.7 kbps: 1 clock rate 6 nibble data

Pin #	Mapped Functions	User Functions	Comment / Remarks
163	RSENT2RX	RSENT2RX	RSENT Input
165	RSENT2SPCO	RSENT2SPCO	RSENT Control Output
171	RSENT3RX	RSENT3RX	RSENT Input
173	RSENT3SPCO	RSENT3SPCO	RSENT Control Output

Reference design provides 2 channel SENT interfaces from channel 2 and Channel 3 as shown in the schematic below:

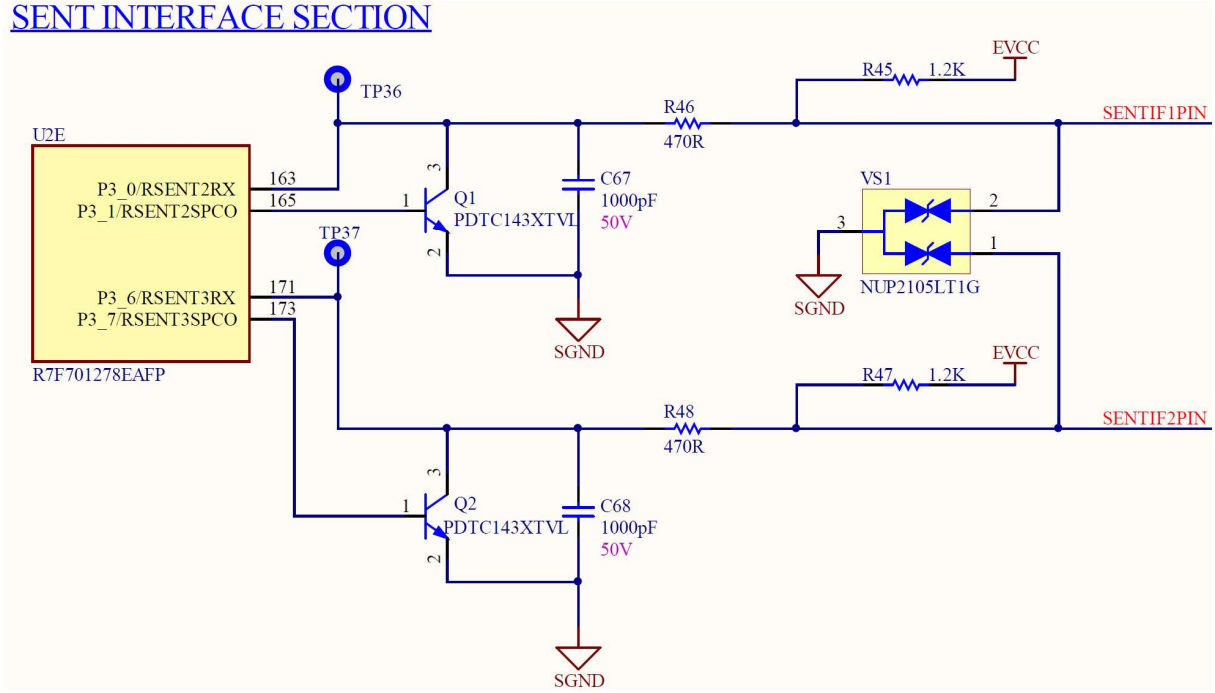


Figure 6-27 RSENT Interface circuit

6.4 Analog Functions

6.4.1 ADC Functional Mapping:

The C1M-A1 is equipped with 3 Unit of ADCCn, n=0,1 & 2. The ADCC resolution is 12-bit and each unit has multiple T&H (Track & Hold) inputs. The T&H circuit allows for simultaneous capture of Analog signal on Trigger. The analog input signals that must be group triggered are mapped to utilize the T&H feature provided by the ADCCn.

Each unit has 40 Virtual Channels to hold the conversion result. Analog ports on the device are dedicated pins for analog and no other function is available.

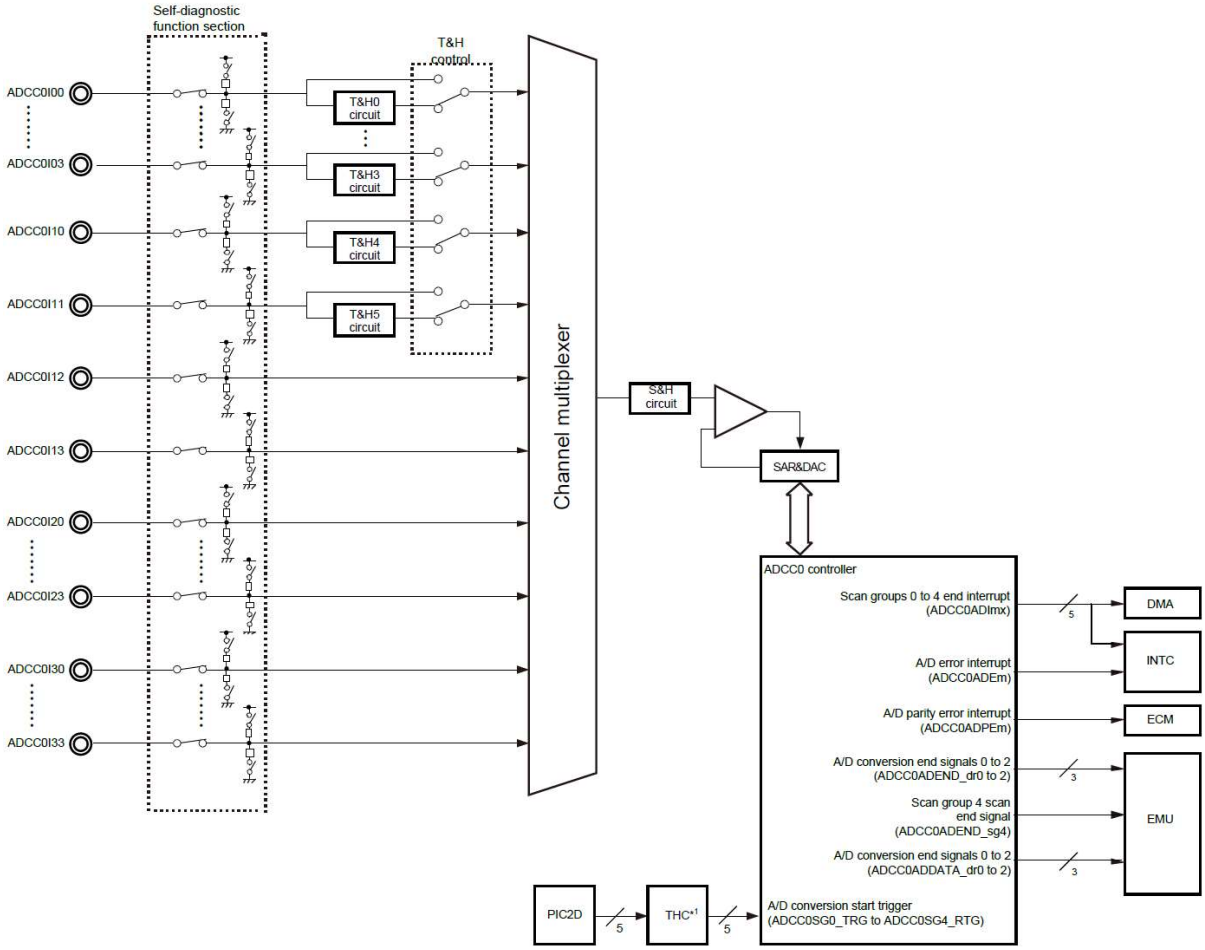


Figure 6-28 ADCC0 Block Diagram

Analog input Design Consideration:

ADCC0 - T&H 0 to 5
ADCC1 - T&H 0 to 5
ADCC2 - T&H 0 to 3

Figure 6-29 ADCC Input ports with T&H circuit

Pin #	Mapped Functions	User Functions	Comment / Remarks
1	ADCC2I02	U Phase voltage Sense	Optional implementation - required for Functional Safety - phase volatge monitoring
2	ADCC2I01	W Phase voltage Sense	Optional implementation - required for Functional Safety - phase volatge monitoring
3	ADCC2I00	V Phase voltage Sense	Optional implementation - required for Functional Safety - phase volatge monitoring
10	ADCC1I32	IPD_CS_OUT1	Analog port only - cannot be used as IO
11	ADCC1I23	IPD_CS_OUT2	Analog port only - cannot be used as IO
12	ADCC1I22	IPD_CS_OUT3	Analog port only - cannot be used as IO
13	ADCC1I21	IPD_CS_OUT4	Analog port only - cannot be used as IO
14	ADCC1I20	Analog Input	Analog port only - cannot be used as IO
15	ADCC1I13	Coolant Temperature	Analog port only - cannot be used as IO
16	ADCC1I12	Motor Temperature	Analog port only - cannot be used as IO
17	ADCC1I11	Pedal Sensor	Analog port only - cannot be used as IO
18	ADCC1I10	Brake Sensor	Analog port only - cannot be used as IO
19	ADCC1I03	Sensor Vmonitor	On-board Sensor supply voltage monitoring
20	ADCC1I02	Pre-Drive Vmonitor	On-board pre driver Supply Monitor
22	ADCC1I31	Analog Input	Analog port only - cannot be used as IO
34	ADCC0I21	Analog Input	Analog port only - cannot be used as IO
35	ADCC0I20	Analog Input	Analog port only - cannot be used as IO
36	ADCC0I13	Inverter Power Board Temperature 1	On-Board Temperature sensor1 monitoring Power Board temperature
37	ADCC0I12	Inverter Power Board Temperature 2	On-Board Temperature sensor2 monitoring Power Board temperature
38	ADCC0I11	DC Resolver Cosine Input	DC Resolver Input
39	ADCC0I10	DC Resolver Sine Input	DC Resolver Input
40	ADCC0I03	DC Bus Current	DC Bus Current Sensor input
41	ADCC0I02	U Phase Current Sense	25.3.2.53 EMU3n Input IP Control Register (EMU3nCTRINMD) - Refer CAUTION on the Mapping
42	ADCC0I01	W Phase Current Sense	25.3.2.53 EMU3n Input IP Control Register (EMU3nCTRINMD) - Refer CAUTION on the Mapping
43	ADCC0I00	V Phase Current Sense	25.3.2.53 EMU3n Input IP Control Register (EMU3nCTRINMD) - Refer CAUTION on the Mapping
46	ADCC0I30	VEXT Monitor	Analog port only - cannot be used as IO
175	ADCC2I10	PMIC Voltage Monitoring	Analog port only - cannot be used as IO
176	ADCC2I03	DC Bus Voltage	On-board DC Bus Voltage Sensor input

Figure 6-30 Analog Functional Mapping

Motor Phase currents, DC Bus Current and DC resolver Sine and Cosine Input are mapped to ADCC0 on the channels that provide T&H circuit.

Gate Driver / Pre-Driver supply, Sensor supply, Brake Sensor, Pedal Sensor and Temperature monitoring inputs are then mapped onto ADCC1 on the channels that provide T&H circuit.

DC Bus Voltage and 3 Phase Motor voltages are mapped to ADCC2 on the channels that provide T&H circuit.

This mapping allows programmer to trigger start of conversion for all this inputs in a single instant. This also, enables formation of Scan Groups to start of conversion on a trigger and store the result in mapped virtual channel (result register).

IMPORTANT: The analog signals highlighted in "RED" text are fixed by circuit on-board and therefore, do not offer any generic interface to allow measurement of external analog signals.

6.4.2 MOSFET Gate Driver

The ISL78434 is Automotive Grade (AEC-Q100 Grade 1) high voltage, high frequency, half-bridge NMOS FET driver for driving the gates of up to 70V half-bridge topologies.

The ISL78434 has dual independent inputs for controlling the high-side and low-side driver separately. It has independent sourcing and sinking pins for each gate driver.

Patented gate-sensed adaptive dead time control provides shoot-through protection shoot-through protection and minimized dead time.

Refer ISL78434 Datasheet for more technical details on the device specifications.

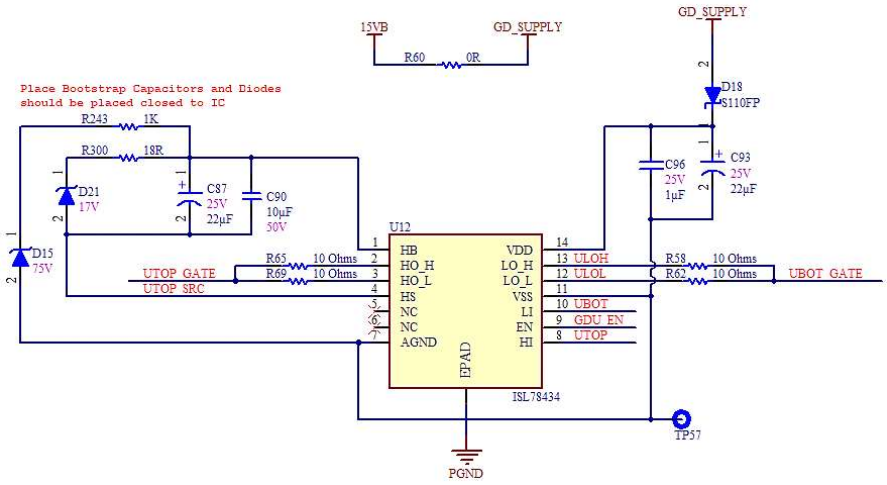


Figure 6-31 Typical Gate Driver Circuit

Design Considerations:

In design, MOSFET Pre-Driver stage consists of 3 ISL78434 ICs to drive the U, V & W Phase of the motor. These drivers are in the controller board, which controls gate signals of half-bridge for each phase in the Power board.

Controller board and Power board are interfaced through board-to-board connectors J11, J12 & J13, which carry high side and low side gate control signals for each phase from ISL78434.

These half-bridge drivers are controlled by MCU (U2), which control independently the high side and low side of the driver circuit. Each phase driver is controlled in accordance with the requirement by MCU.

A common enable signal for each driver is controlled by MCU (U2).

The high-side driver bias is handled by Bootstrap capacitor across the HB and HS pins, which provides proper gate drive to the high-side FET.

Zener diodes (D15, D16, D17, D21, D22 & D23) with a series current limiting resistor (R243, R247, R251, R300, R384 & R385) between HB & HS pins and HB & AGND pins provide over-voltage protection against violation of the electrical specification of the device.

IMPORTANT:
For best thermal performance, connect the driver EPAD to a low thermal impedance ground plane. Use as many vias as possible to connect the top layer PCB thermal land to GND planes on other PCB layers.
Connect the VSS and AGND pins together through the EPAD to maintain a low impedance connection between the two pins.
Protection Required:
Voltage on HB (referenced to HS) = min 8V max 18V
Voltage on HB (referenced to VSS) = 86V MAXIMUM

[CAUTION]: Bootstrap related parameters: Average Current in VDD to HB FET is Max 100mA.
Refer Section 5.2 Bootstrap Capacitor design.

Through 6 pin connectors, the Controller board and Power board are interfaced. As shown in below figure Half bridge gate control signals, thermistor excitation is done through EVCC (5V) and its feedback is taken through ANALOG_IN5 and ANALOG_IN6 signals.

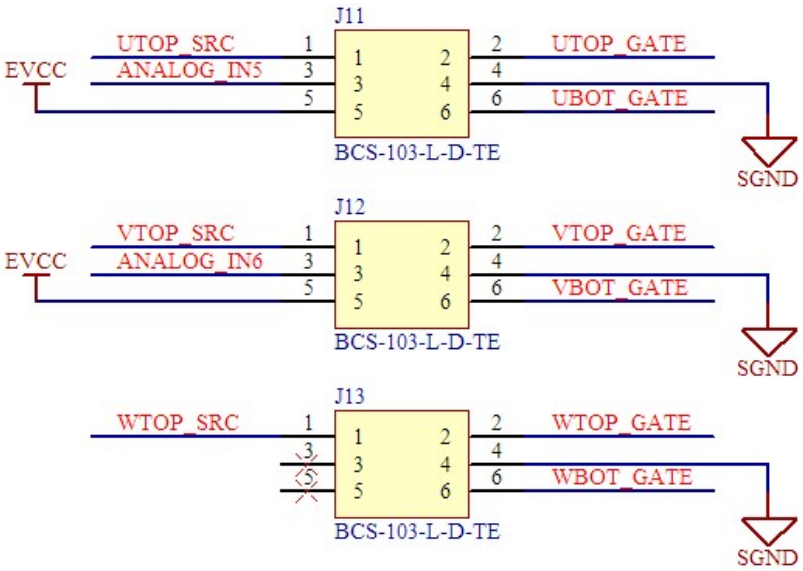


Figure 6-32 Schematic Section of B2B connector

***CAUTION**: J11, J12 & J13 must not be supplied from external source; the controller board supplies the source EVCC from on-board power supply.*

6.4.3 Current Sensor

The LEM HC5FW family is for the electronic measurement of DC, AC or pulsed currents in high power and low voltage automotive applications with galvanic separation between the primary circuit (high power) and the secondary circuit (electronic circuit).

In this design four current sensors, HC5FW 500-S/SP1 are used to measure current consumption of DC Bus and each phase of motor individually. The measured signal is in range of 0V to 5V. The output of the sensor is connected to ADC of MCU, and op-amp based Schmitt trigger circuit for triggering fault conditions is implemented. Similar circuitry is implemented for each current measurement with low and high thresholds providing hysteresis.

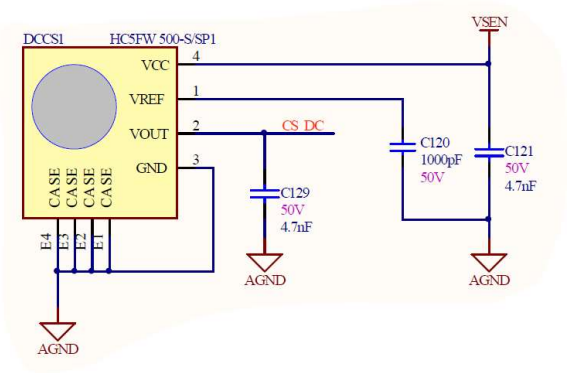


Figure 6-33 HC5FW 500-S/SP1 Current Sensor Circuit

In design four current sensors are mounted on the control PCB, aligning to Power board through metal studs. Each current sensor is powered by VSEN (5V). As per datasheet recommendation, a ceramic capacitor of 4.7nF/50V is connected between VCC & GND pin and VREF pin is terminated to GND through 1nF/50V ceramic capacitor. GND pins are connected to AGND.

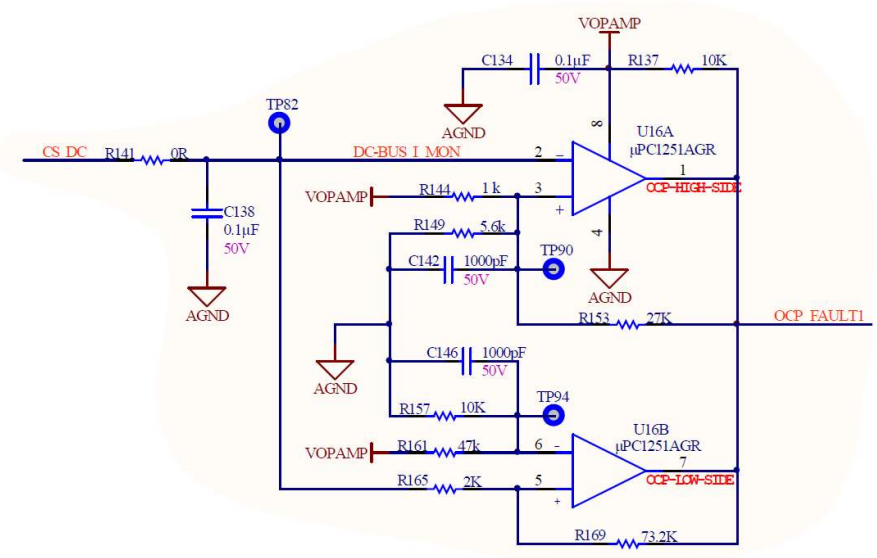


Figure 6-34 Typical Signal Monitoring circuit

The output of each current sensor is fed to two combined Schmitt trigger configurations with the higher & lower threshold values to generate the fault condition when it lower or exceeds the set value.

Each output when fault is observed, are handled through Logic gates to reset MCU with other reset conditions.

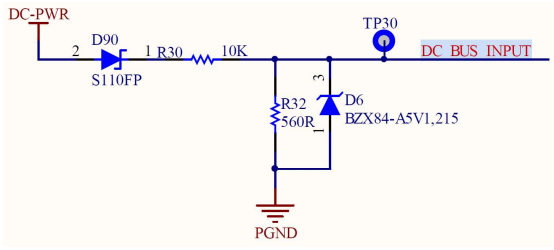
Similar circuit is implemented for Current sensing; In this design the threshold is set for +450A and -450A for 500A Sensor in use. However, threshold values *may be set* different for DC Bus current and U, V, W Phase currents.

6.4.4 Voltage Sensor

Input DC power supply Monitoring:

In design, Input DC power supply which ranges from 0V to 75V is linearly reduced by voltage divider to 0V to 5V range.

The voltage divider output is fed to Op-Amp based Schmitt trigger circuit for triggering fault condition.



Input Supply DC Fault Vout=Vi*(R2/(R1+R2))

Parameter	Value		
Vi	36	V	Minimum input
R1	1.00E+04	Ohm	
R2	5.60E+02	Ohm	
Vo	1.91	V	
Vil	~1.8	V	
Hys	100	mV	

Parameter	Value		
Vi	75	V	Maximum Input
R1	1.00E+04	Ohm	
R2	5.60E+02	Ohm	
Vo	3.98	V	
Vih	~3.9	V	
Hys	80	mV	

Lower and higher threshold levels are given, which are approximately set in the Schmitt trigger circuit as given below:

Lower Threshold: VIH = ~34.1V and VIL = ~32.0V

Higher Threshold: VIH= ~74.2V and VIL = 72.0V

Output of Schmitt trigger circuit- DC_FAULT is connected to interrupt of MCU (U2) and Fault generator circuit.

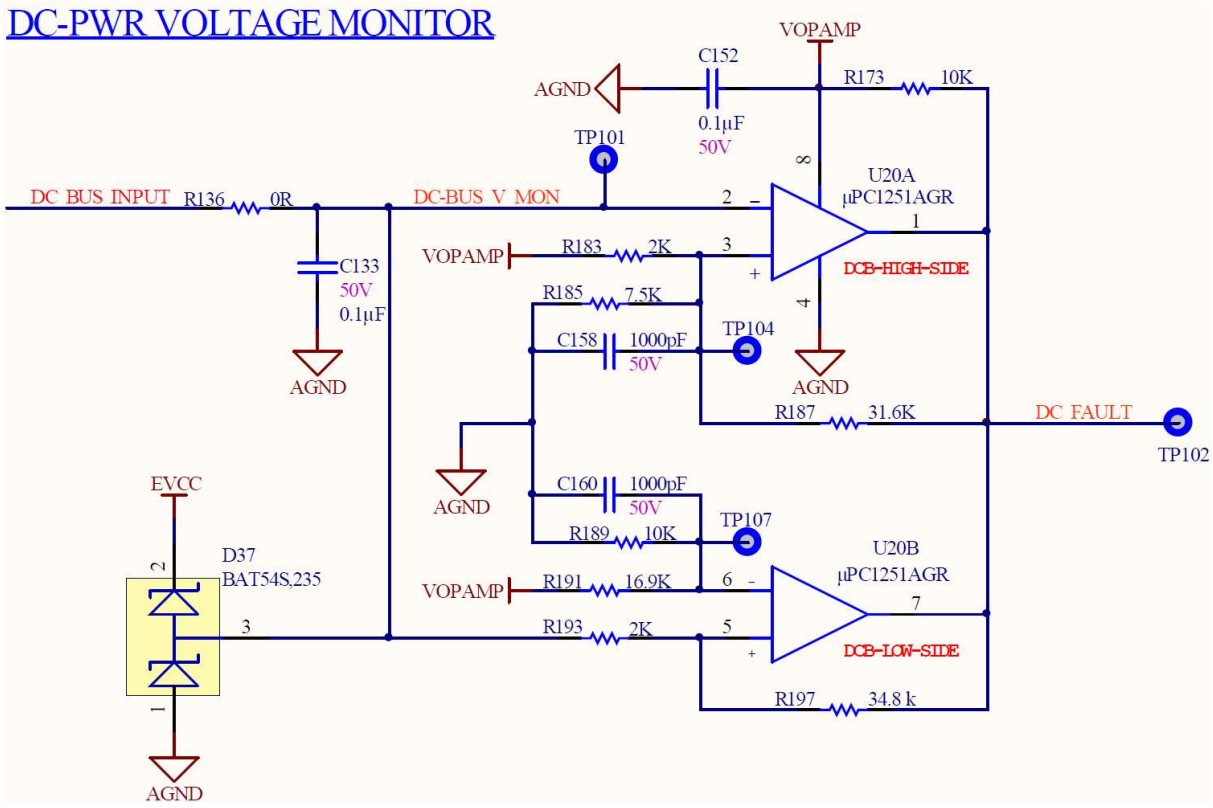


Figure 6-35 DC BUS Voltage Monitor

Gate Driver Power Supply Monitoring:

The power supply GD_SUPPLY, which is in range of 15V powers Motor driver ISL78434 is fed to Op-Amp based Schmitt trigger circuit for triggering fault condition.

Required lower and higher threshold levels are given, which are approximately set in the Schmitt trigger circuit as given below.

LOWER thresholds: VIH ≈ 11.0V and VIL ≈ 10.0V

HIGHER thresholds: VIH ≈ 16.5V and VIL ≈ 15.9V

Output of Schmitt trigger circuit- GDU_FAULT is connected to interrupt of MCU (U2) and Fault generator circuit.

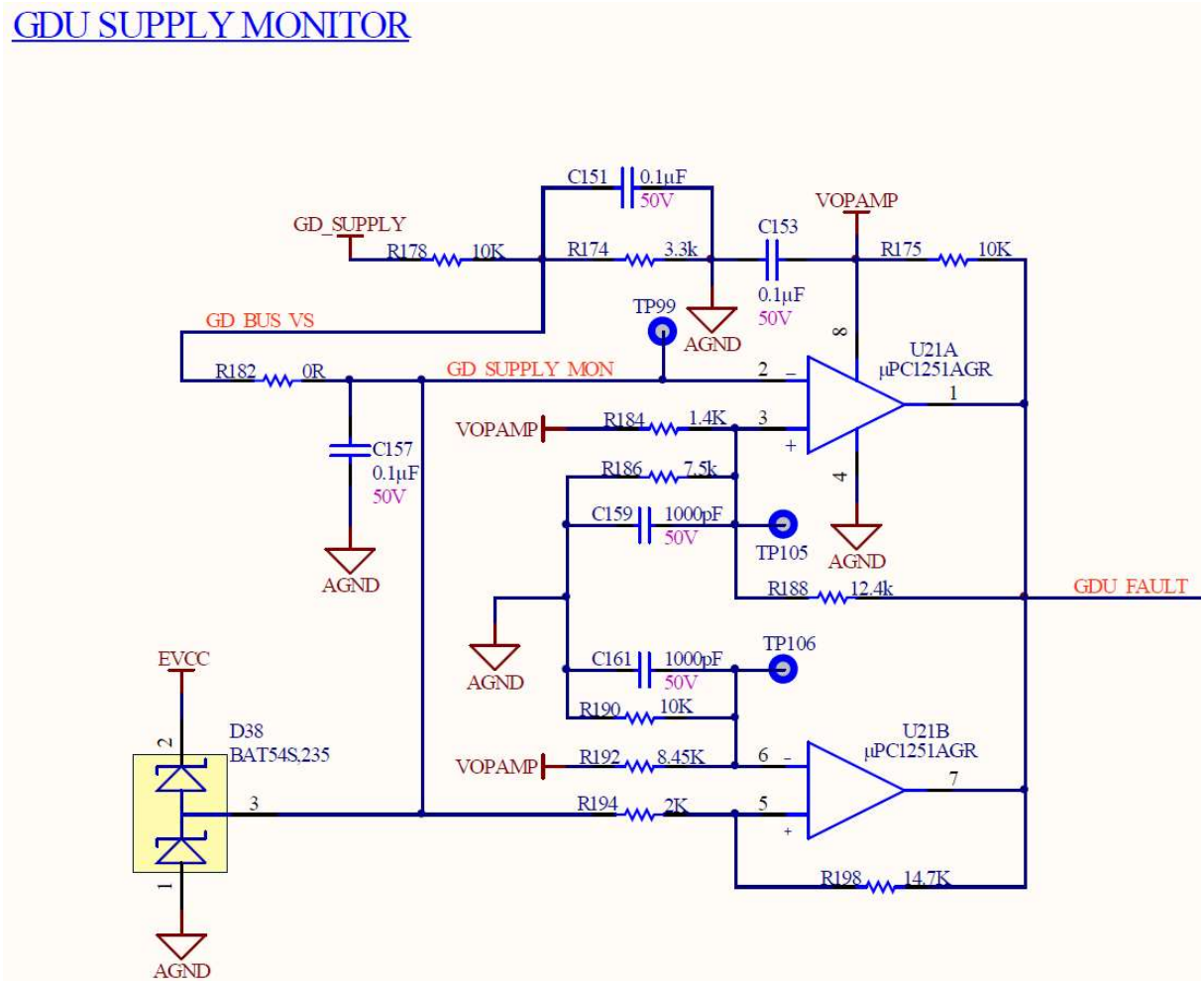
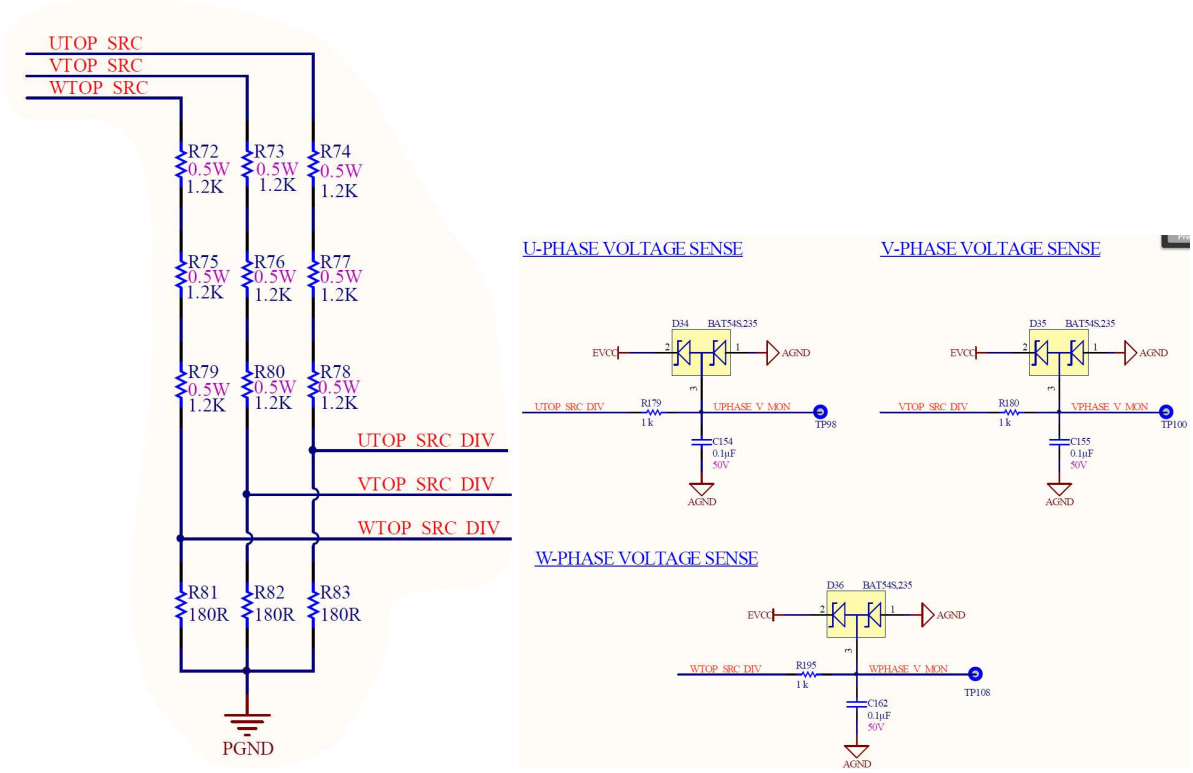


Figure 6-36 Gate Driver Unit Supply Monitor

Motor Phase Voltage Monitoring:

The voltage from HS pin of GDU of each phase is linearly reduced to the range of (5V to 0V) through voltage divider.



The voltage across the divider circuit is connected to ADC followed by protection circuit and low pass filter.

Each output from the driver is protected from overvoltage and negative voltage through a TVS diode.

The low pass RC filter is designed for frequency of 160Hz.

Other Analog Input Monitoring:

The board provides facility to interface external analog signals via the 6 Analog interface circuits on-board, the below figure is typical interface circuit implemented on the board.

The signals are typically pull-down via 10K resistor and therefore, will measure 0V when no sensor or connector pin is open.

Each analog input implements low pass RC filter and uses diode for voltage protection.

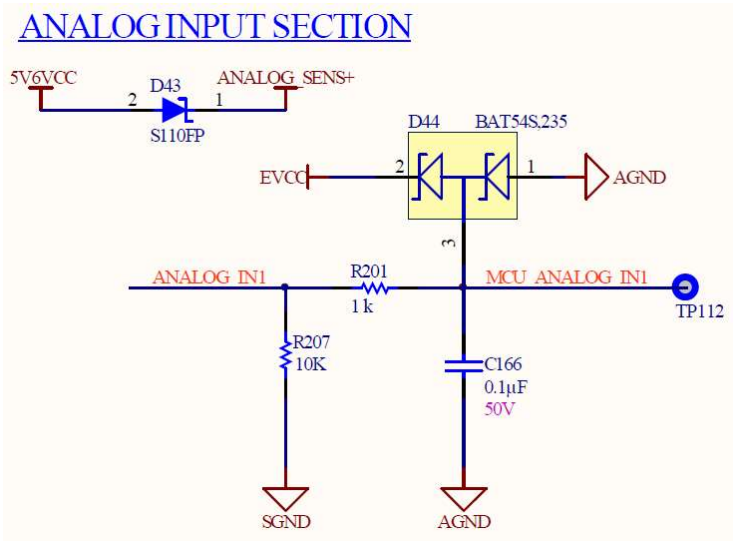


Figure 6-37 Typical Analog Input Circuit

CAUTION: Care must be taken that excess voltage is not applied on these input pins to avoid damage to the microcontroller.

Power Supply 5V6VCC (5.6V) is converted to TEMP_VS1+, BRAKE_VS+, PEDAL_VS+ & TEMP_VS2+ through a schottky diode which is supplied to ANA connector to power up respective sensor circuits in the external system.

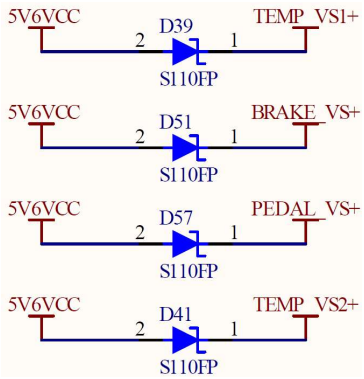


Figure 6-38 Power Supply for external sensors

6.5 Digital Input / Output Functions

6.5.1 Digital Inputs: Active Low

The following four digital input signals from DIO connector are connected to MCU (U2) followed by a schottky diode in series with reverse bias condition and pull up resistor. By the circuit implementation below, the signal applied is detected by *ACTIVE LOW logic*, hence providing protection against over-voltage at the MCU pin.

_IN1PIN/EMERGENCY_STOP, CON_IN2PIN, _FREQ_IN0PIN, and _FREQ_IN1PIN

In design 2.2k resistor is tied to EVCC (5V) and 100Ω series resistor is connected to MCU (U2).

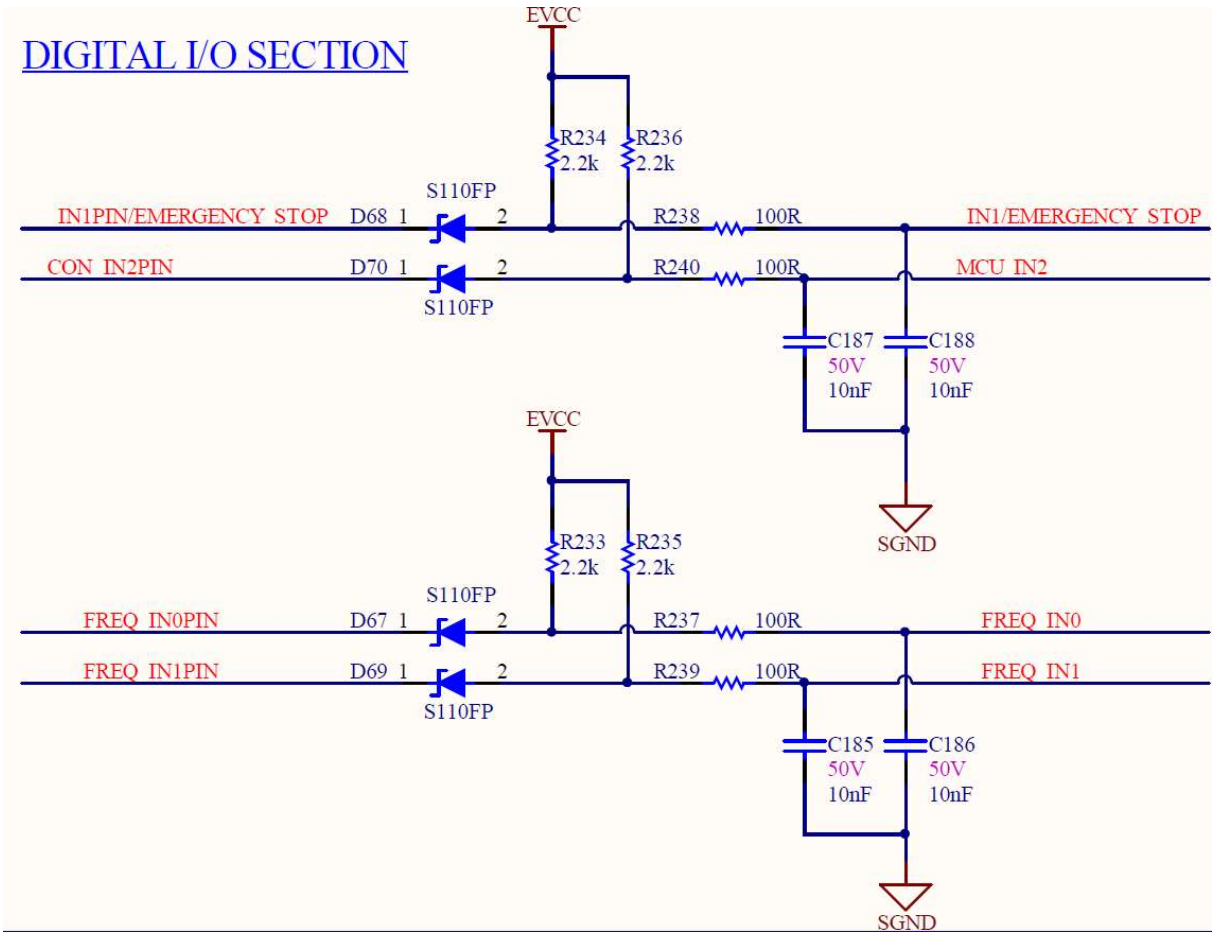


Figure 6-39 Digital Input Circuit

IN1/ EMERGENCY_STOP signal is connected to INTP5 function of the Microcontroller. Also, this signal can be used to generate system RESET on fault.

CAUTION: By default, the on-board hardware support C1M_RESET generation by trigger to IN1PIN/ EMERGENCY_STOP input pin.

MCU_IN2 signal is connected as Active Low Logic input to port function of the microcontroller. There is TAUD Input capture function available if required.

FREQ_IN0PIN and FREQ_IN1PIN connected as input capture pins using TAUD or TAUJ capture function on the microcontroller. These pins may also be configured as the Digital Input Pins with Active Low input.

6.5.2 Digital Inputs: Active High

Total eight digital inputs are received from DIO connector followed by TVS diodes DA7, DA8, DA13 and DA14. These inputs are connected to base of the transistor followed by Schottky diode and 1kΩ resistor.

A Zener diode and 1kΩ resistor are provided to protect from over voltage. In circuit pair of 1k resistors will form as a voltage divider.

In the design Zener diode will clamp voltage across base of the transistor to 4.7V when input signal is above voltage level of 5V. By default, the voltage observed at MCU will be 5V as the collector pin is pulled high to EVCC (5V) through a 4.7k resistor.

When *active high input* is applied it enables switch and make output signal logic low (0V)

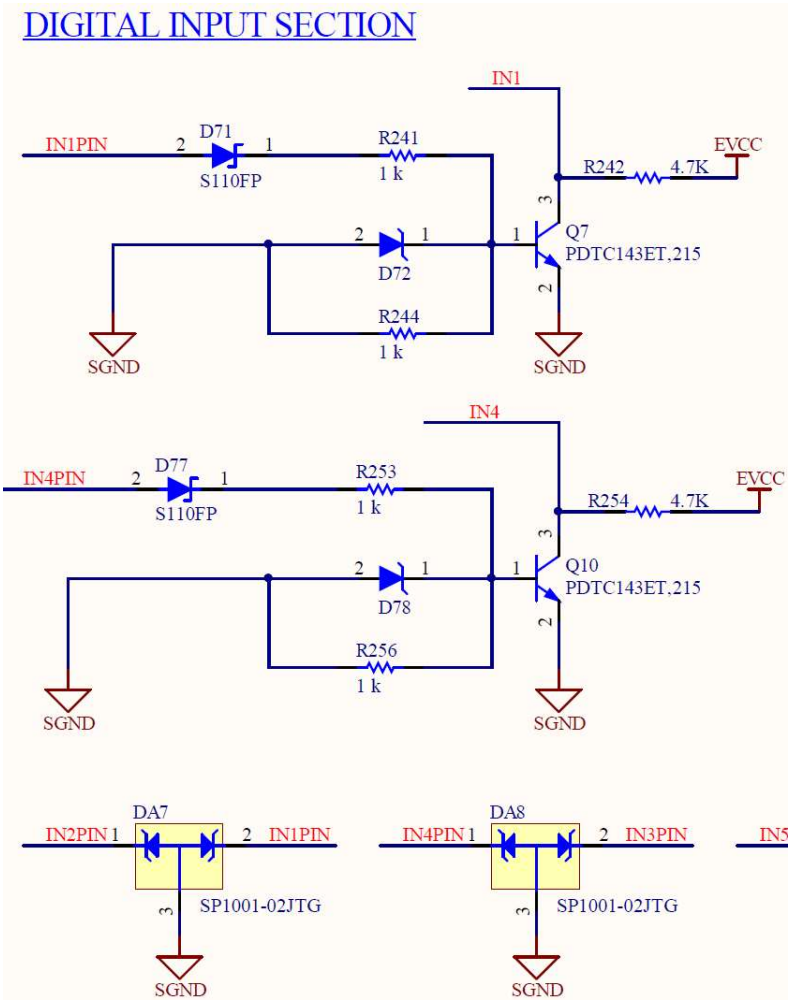


Figure 6-40 Typical Circuit for Active High Input

IMPORTANT: Transistors [PDTC143ET] used have built-in biasing resistors and therefore are not shown in the schematic however, they exist.

6.5.3 Digital Output:

There are four digital output signals, three signals from MCU (U2) can be configured as PWM or Digital output which is connected to the DIO connector.

The output of the transistor is connected to the connector and by default it will be of voltage 5V. In presence of signal from the MCU (U2) it drives the transistor output to GND and pins at connector (DIO) will be pulled to logic low (0V). *Inverted logic is used in this section*. A 1k resistor is used at the base of the transistor and 4.7k resistor at collector pin.

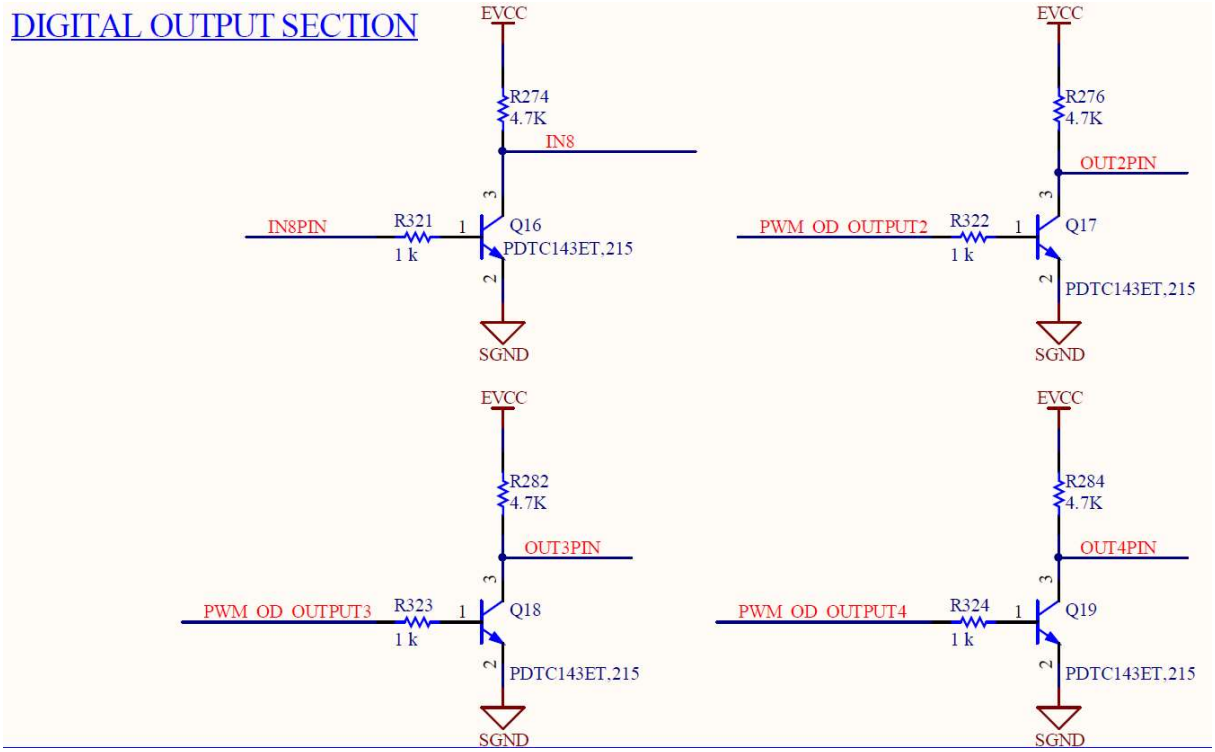


Figure 6-41 Typical Output Circuit (inverted output)

6.5.4 High Voltage Open Drain Output for External Loads

Using the Circuit in below figure MCU can control external Load such as Cooling FAN running of the Main Battery Supply (typ. 48V DC). The MOSFET used is 100V and a free-wheeling diode is also implemented to allow control of contactor or relay externally.

A discrete MOSFET driver circuit is implemented to support PWM controlled output, this implementation represents Low side switching and all the 3 terminals of TMS connector are floating and need external connections to be done with supply and load.

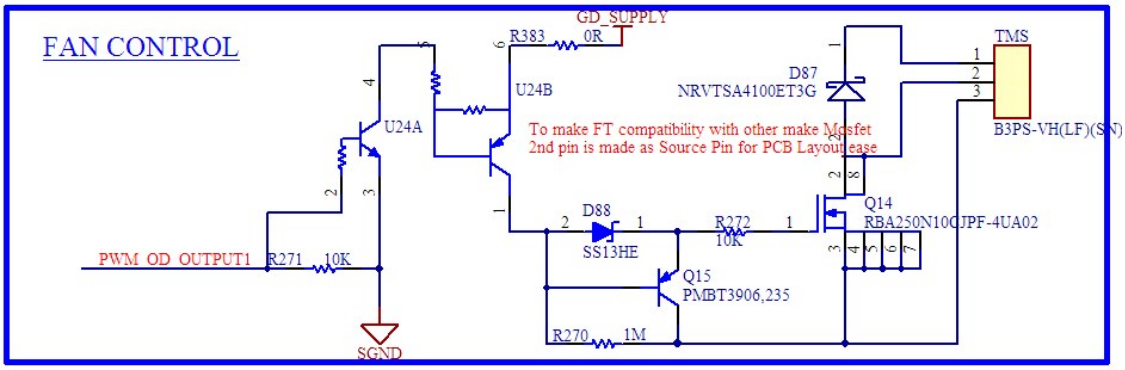


Figure 6-42 Open Drain output from 100V MOSFET

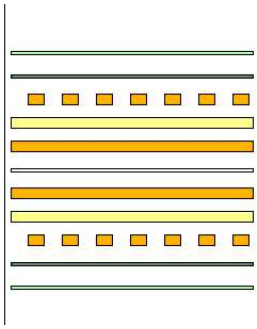
CAUTION: The Source of the MOSFET is "floating" on the board, therefore, it is mandatory to connect the Pin3 of the TMS connector externally to Battery -ve terminal to complete the circuit of the load connected across DC Bus and Drain of the MOSFET.

7. PCB Details

This section provides information about the PCB design of the REN-INV-V2 board. The physical dimensions of the PCB are 187mm x 175mm. This 4-layer board has 2 signal layers, 1 GND layer and 1 Power plane and uses FR4 material.

Description	Proto PCB
Size	187mm X 2175mm
Name	REN-INV-V2
Thickness	1.64mm
Dielectric	FR4 Material
Surface Finish	ENIG
ROHS	Yes
No. of Layers	4
Controlled Impedance	Yes

Below is the Stack-up diagram of the reference design control board PCB.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Co...	Surface Material	0.787	Solder Resist	3.5			0
Top Layer	Signal	Copper	2.756				Top	
Dielectric 1	Dielectric	Core	6.417	FR-4	4.2			
GND	Internal Plane	Copper	2.756			20		
Dielectric 2	Dielectric	Prepreg	39.37		4.2			
PWR	Internal Plane	Copper	2.756			20		
Dielectric 3	Dielectric	Core	6.417	FR-4	4.2			
Bottom Layer	Signal	Copper	2.756				Bottom	
Bottom Solder	Solder Mask/Co...	Surface Material	0.787	Solder Resist	3.5			0
Bottom Overlay	Overlay							

LAYER STACK UP TABLE

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.020mm	3.5	
3	Top Layer	Copper	0.070mm		
4	Dielectric 1	FR-4	0.163mm	4.2	
5	GND	Copper	0.070mm		
6	Dielectric 2		1.000mm	4.2	
7	PWR	Copper	0.070mm		
8	Dielectric 3	FR-4	0.163mm	4.2	
9	Bottom Layer	Copper	0.070mm		
10	Bottom Solder	Solder Resist	0.020mm	3.5	
11	Bottom Overlay				

TOTAL BOARD THICKNESS 1.64 MM +/- 10%

8. Acronyms and Abbreviations

Acronym/Abbreviations	Explanation
ADC	Analog-Digital Converter
CAN	Controller Area Network
CAN-FD	Controller Area Network-Flexible Data-Rate
CMOS	Complementary Metal–Oxide–Semiconductor
DC	Direct Current
EMS	Electromagnetic Susceptibility
ESD	Electrostatic discharge
MOSFET	Metal Oxide Field Effect Transistor
FR4	Flame Retardant 4
GDU	Gate Driver Unit
IPD	Intelligent Power Device
LIN	Local Interconnect Network
MCU	Microcontroller Unit
MUX	Multiplexer
NRZ	Non-Return-to-Zero
OP-AMP	Operational Amplifier
PCB	Printed Circuit Board
PMIC	Power Management IC
PTC	Positive temperature coefficient
RDC	Resolver-to-Digital Converter
LDO	Low Drop Out regulator
LED	Light Emitting Diode
SENT	Single Edge Nibble Transmission
SoC	System on chip
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
ISO_GND	Isolated Ground
PGND	Power Ground
SGND	Signal Ground (System Ground in the board)
TVS diode	Transient Voltage Suppressor diode
AGND	Analog Ground

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	01 Jan 2021		First Release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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