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SH7137 Group

Reception of Serial Data by the SCI in Clock-Synchronous Mode (Unidirectional Communication)

Introduction

This application note describes reception of serial data by using the clock-synchronous transfer function of the serial communications interface (SCI). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7137

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1. Preface

1.1 Specifications

This sample application employs the clock-synchronous serial transfer function of the serial communications interface (SCI) to perform data reception. Figure 1 shows an example of connection for reception by the SCI in clock-synchronous mode.

- SCI_0 is used.
- The communications format has a fixed 8-bit data length.
- The character strings are received by using the receive-data-full interrupt.
- Once 20 bytes of data have been received, operation for reception is halted.

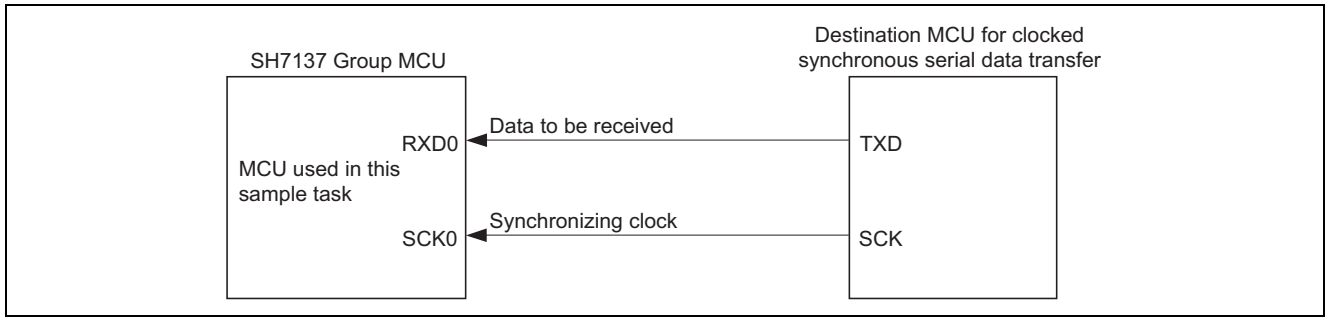


Figure 1 Connection Example for Reception by the SCI in Clock-Synchronous Mode

1.2 Module Used

Serial communications interface (SCI_0)

1.3 Applicable Conditions

MCU:	SH7137	
Operating frequency:	Internal clock	80 MHz
	Bus clock	40 MHz
	Peripheral clock	40 MHz
C compiler:	SuperH RISC Engine Family C/C++ Compiler Package Ver.9.11	
	(from Renesas Technology Corp.)	

2. Description of the Sample Application

This sample application employs the receive-data-full-interrupt (RXI) source of the serial communications interface (SCI) to receive serial data in clock-synchronous mode. In clock-synchronous mode, the SCI receives serial data in synchronization with clock pulses.

2.1 Summary of MCU Module Used

In clock-synchronous mode, the SCI transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communications. An internal clock or an external clock from the SCK pin can be selected as the SCI clock source. When an internal clock has been selected, a synchronizing clock is output from the SCK pin. When an external clock has been selected, a synchronizing clock is input into the SCK pin.

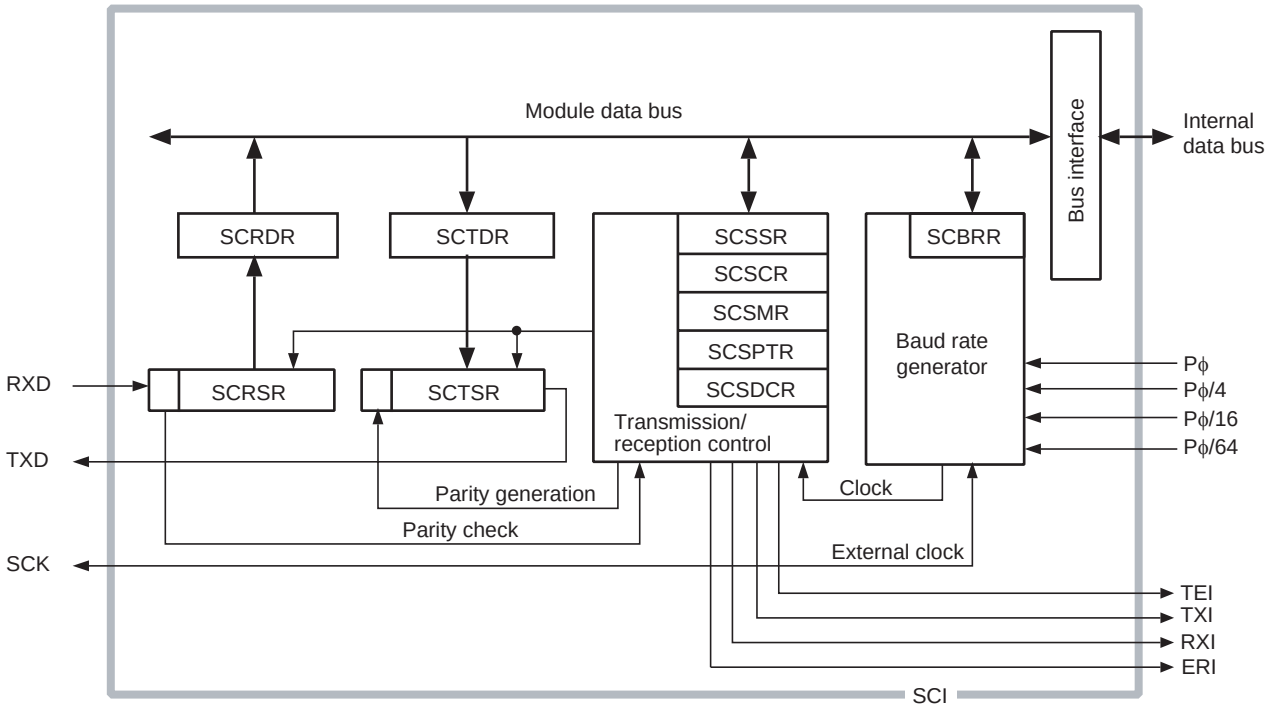
The transmitting and receiving sections of the SCI are independent, so full-duplex communications is possible while sharing the same clock. Both the transmitter and receiver have a double-buffered structure so that data can be read or written during transmission and reception, which enables continuous data transfer.

For details on the SCI, please refer to the section on serial communications interface in the *SH7137 Group Hardware Manual.*

Table 1 gives an overview of serial communications in clock-synchronous mode. Figure 2 shows a block diagram of the SCI.

Table 1 Overview of Serial Data Communications in Clock-Synchronous Mode

Item	Description
Number of interfaces	3 (SCI_0, SCI_1, SCI_2)
Clock sources	For internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: peripheral clock) For external clock: input clock on the SCK pin
Data format	Transfer data length: Fixed at 8 bits Order: LSB first and MSB first are selectable
Baud rate	For internal clock: 250 bps to 5,000,000 bps (Pϕ = 40 MHz) For external clock: up to 6,666,666.7 bps (Pϕ = 40 MHz, external input clock of 6.6667 MHz)
Error detection	Overrun error
Interrupt requests	Transmit-data-empty interrupt (TXI) Receive-data-full interrupt (RXI)
Clock sources	Internal and external clocks are selectable • Internal clock When the internal clock has been selected, the SCI operates using the clock from the baud-rate generator and outputs this clock to external devices as the synchronizing clock. • External clock When the external clock has been selected, the SCI operates on the input synchronizing clock, not using the on-chip baud rate generator.



[Legend]
SCRSR: Receive shift register
SCRDR: Receive data register
SCTSR: Transmit shift register
SCTDR: Transmit data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCSSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCSDCR: Serial direction control register

Figure 2 Block Diagram of the SCI

2.2 Description of the Sample Program

Table 2 gives the settings for SCI communications function of this sample program, and figure 3 shows the operations in data reception.

Table 2 Settings for Communications Function of the Sample Program

Item	Description
Module	SCI_0
Communications mode	Clock-synchronous mode
Interrupts	Receive-data-full interrupt (RXI)
Transfer rate	100 kbps
Rounds of reception	20 (20 bytes)
Data length	8-bit data (fixed)
Bit order	LSB-first
Synchronizing clock	External clock/synchronizing clock on the SCK pin

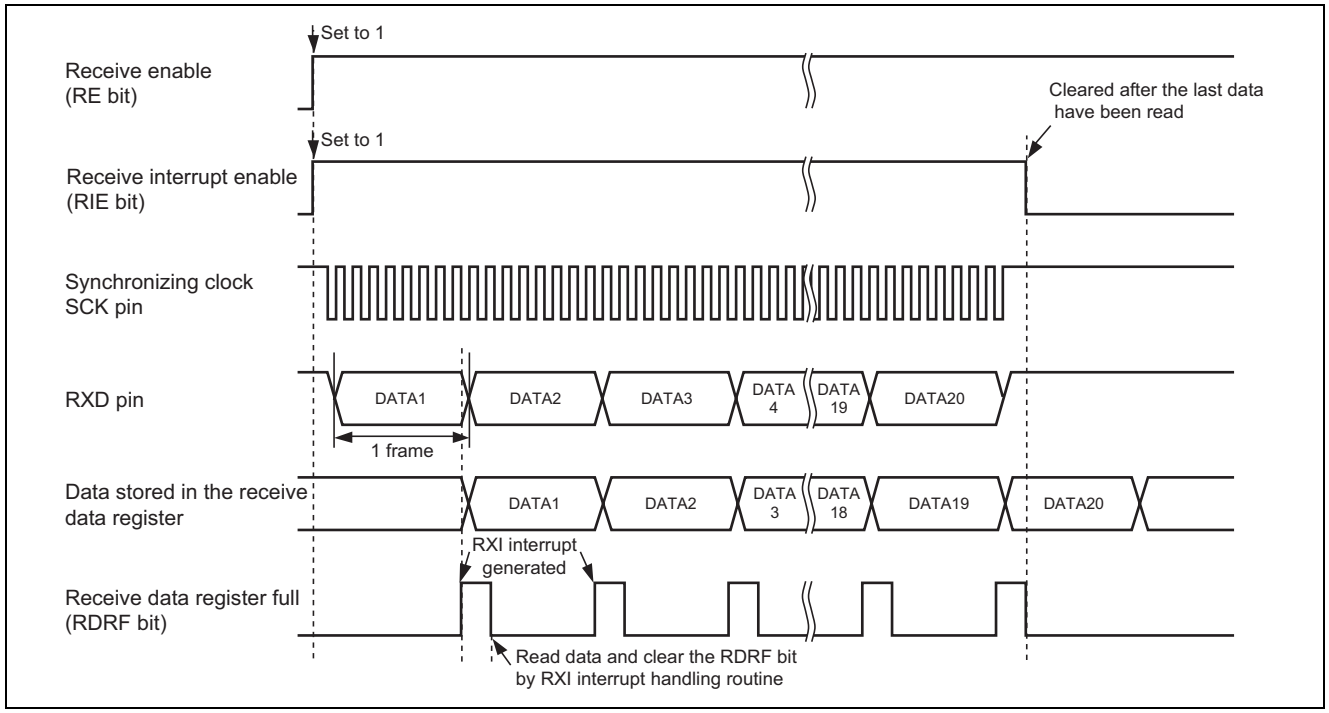


Figure 3 Operations for Data Reception

2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCI_0 for clock-synchronous mode operation.

Figure 4 shows the flow of processing by the sample program, figure 5 shows the flow of settings for release from module-standby mode, figure 6 shows the flow for setting up the pin function controller, and figure 7 shows the flow for initialization of data reception in clock-synchronous mode. Furthermore, figure 8 shows the flow for handling receive interrupts in clock-synchronous mode.

For details on the settings of individual registers, see the *SH7137 Group Hardware Manual*.

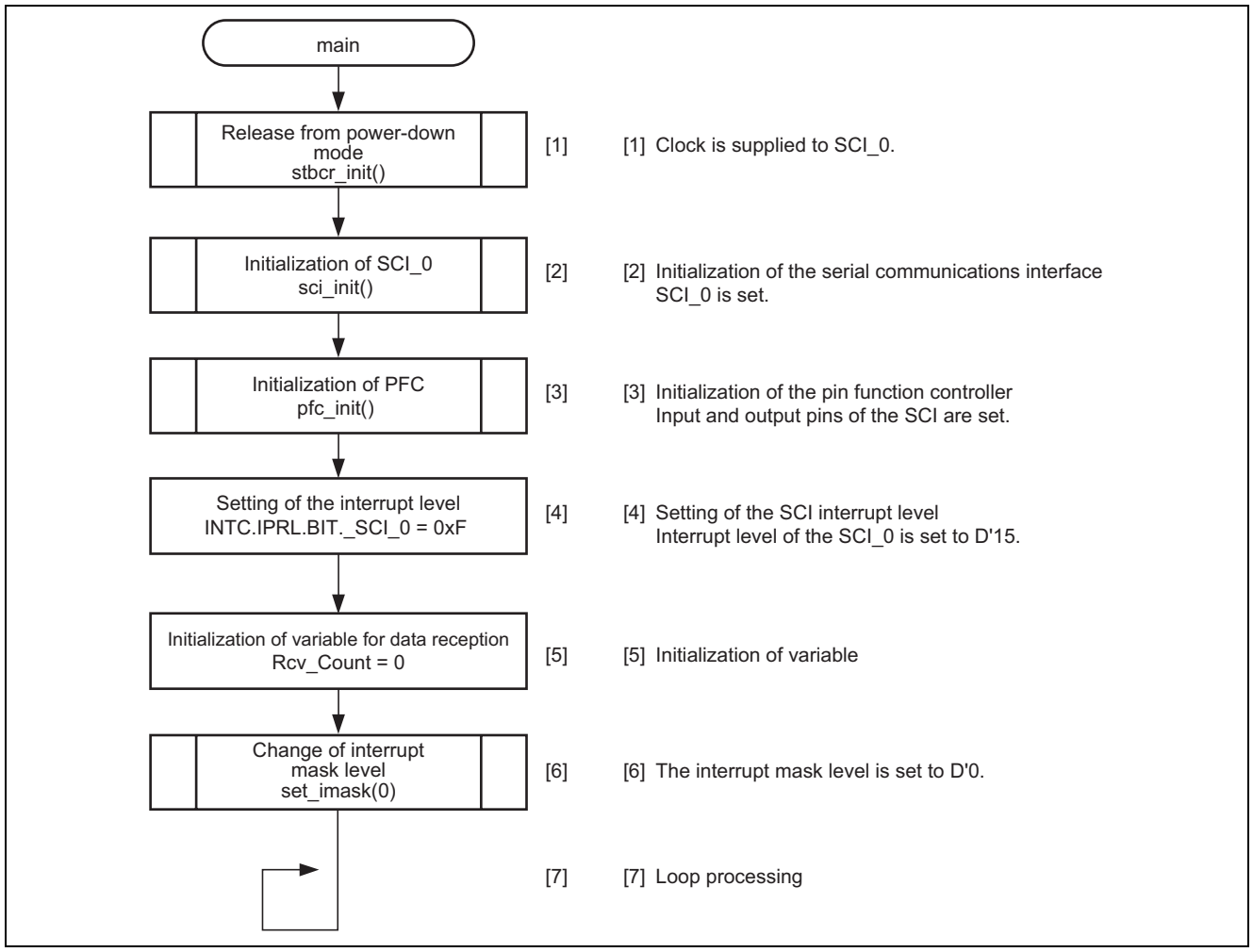


Figure 4 Flow of Processing by the Sample Program

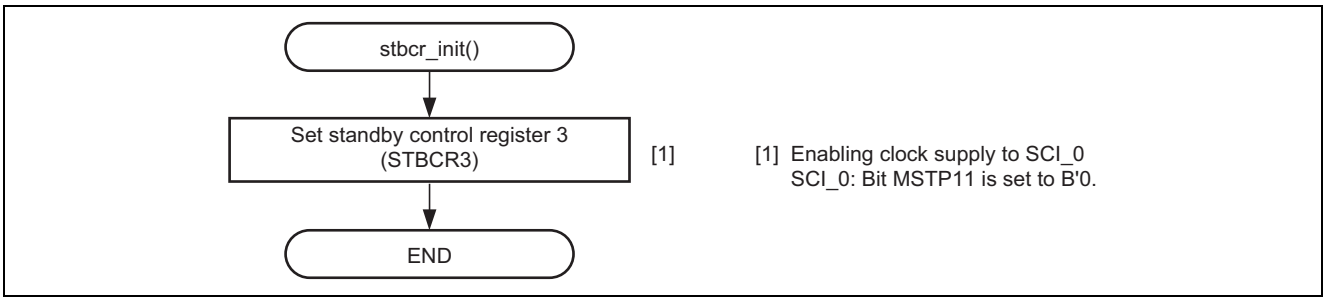


Figure 5 Flow of Settings for Release from Module-Standby Mode

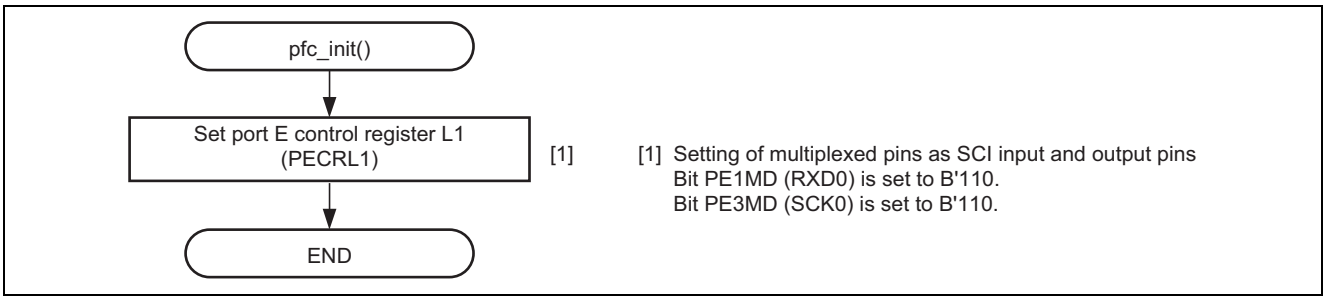


Figure 6 Flow for Setting up the Pin Function Controller

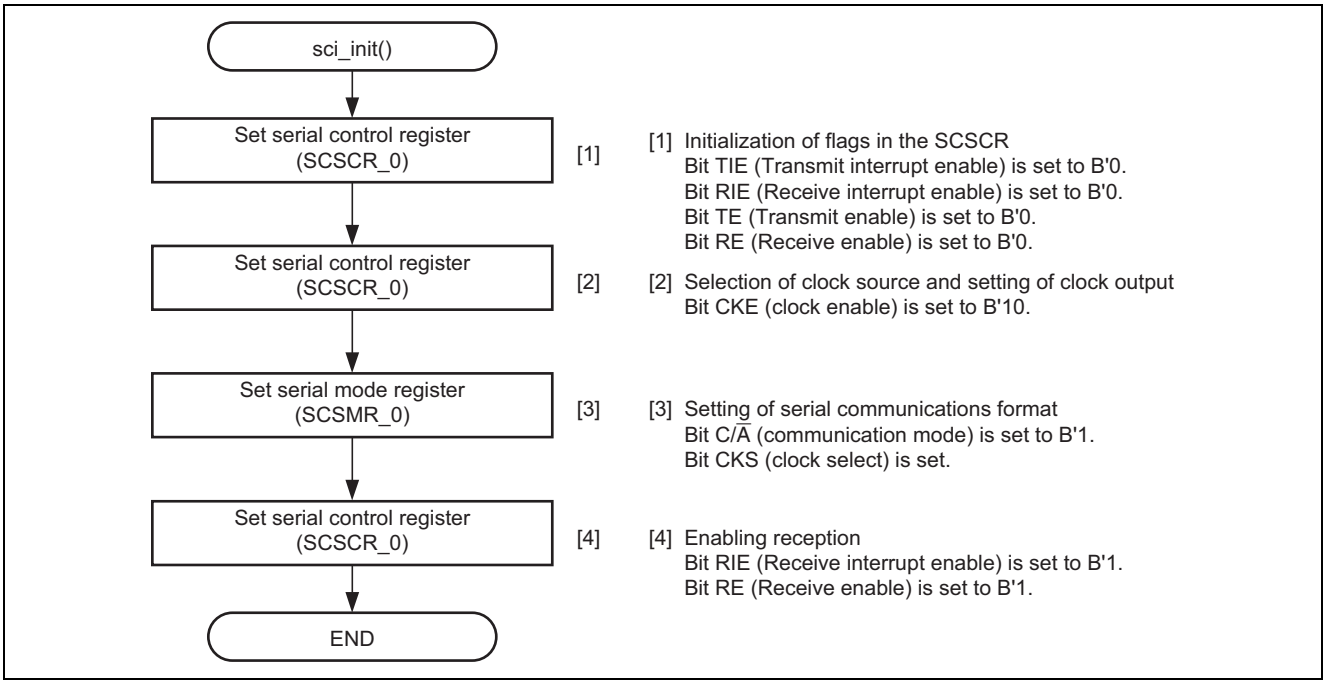


Figure 7 Flow for Initialization of Data Reception in Clock-Synchronous Mode

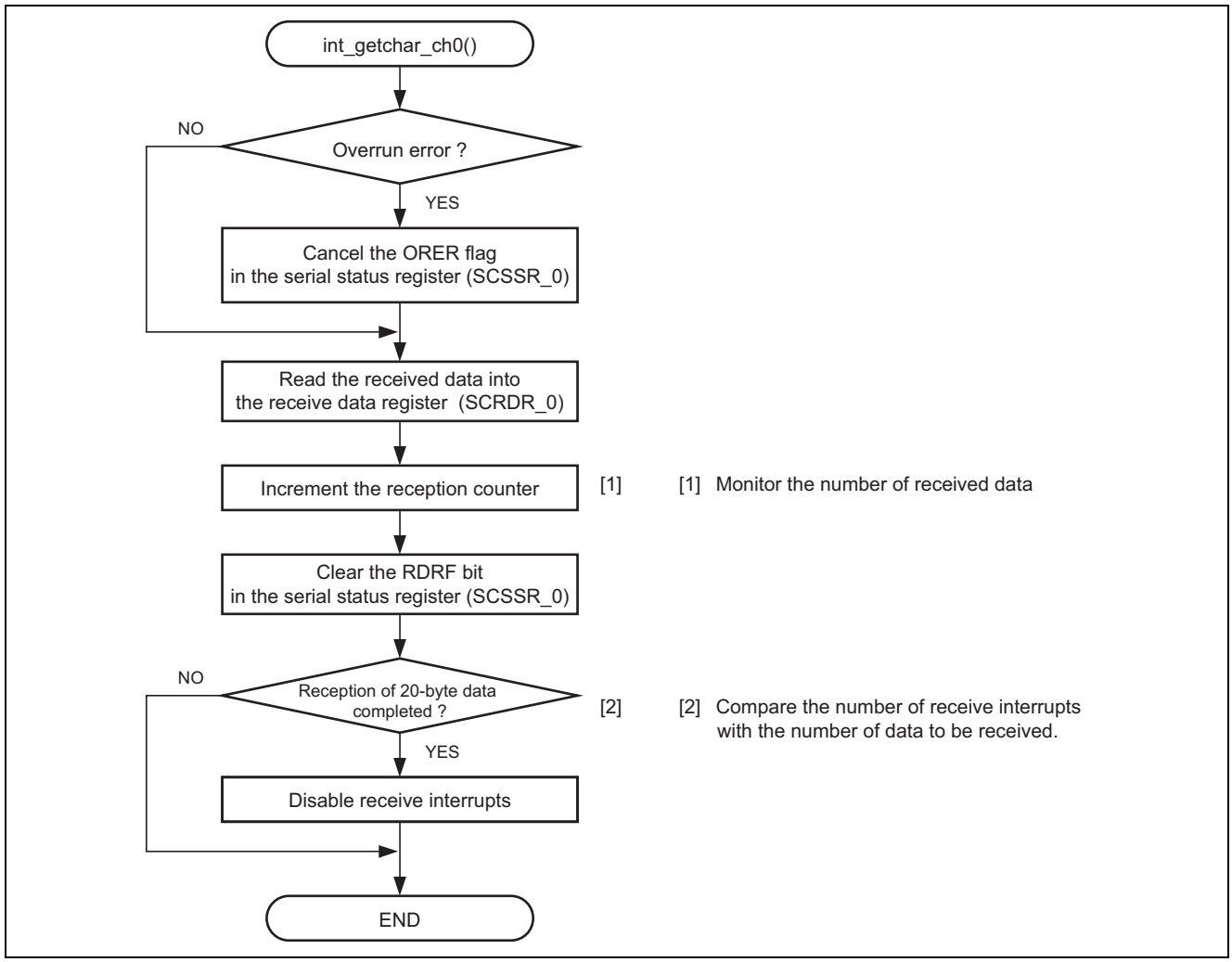


Figure 8 Flow for Handling Receive Interrupts in Clock-Synchronous Mode

2.4 Procedure for Processing by the Sample Program

In this sample program, character strings are received after initialization of SCI_0.

2.4.1 Clock Pulse Generator (CPG)

Table 3 gives settings for the register of the clock pulse generator in the sample program.

Table 3 Settings for Register in Clock Pulse Generator

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFF E800	H'0241	IFC [2:0] = B'000: × 1 (Iϕ) BFC [2:0] = B'001: × 1/2 (Bϕ) PFC [2:0] = B'001: × 1/2 (Pϕ) MIFC [2:0] = B'000: × 1 (MIϕ) MPFC [2:0] = B'001: × 1/2 (MPϕ)

2.4.2 Standby Control Register

Table 4 gives settings for the standby control register in the sample program.

Table 4 Settings for Standby Control Register

Register Name	Address	Setting	Description
Standby control register 3 (STBCR3)	H'FFFF E806	H'F7	MSTP11 = B'0: SCI_0 operates

2.4.3 Interrupt Controller (INTC)

Table 5 gives settings for the register of the interrupt controller in the sample program.

Table 5 Settings for Register of Interrupt Controller

Register Name	Address	Setting	Description
Interrupt priority register L (IPRL)	H'FFFF E992	H'F000	IPR [15:12] = H'F: SCI_0 is at a level 15

2.4.4 Pin Function Controller (PFC)

Table 6 gives settings for the register of the pin function controller in the sample program.

Table 6 Settings for Register of Pin Function Controller

Register Name	Address	Setting	Description
Port E control register L1 (PECRL1)	H'FFFF D316	H'1010	PE3MD [2:0] = B'110: SCK0 input/output PE1MD [2:0] = B'110: RXD0 input

2.4.5 Serial Communications Interface

Table 7 gives settings for the registers of the SCI in the sample program.

Table 7 Settings for SCI Register

Register Name	Address	Setting	Description
Serial mode register (SCSMR_0)	H'FFFF C000	H'80	C/$\overline{A}$ = B'1: Clock-synchronous mode CHR = B'0: 8-bit data CKS [1:0] = B'00: Pϕ clock
Bit-rate register (SCBRR_0)	H'FFFF C002	D'99	Clock-synchronous mode Bit rate: 100k (bit/s) *1
Serial control register (SCSCR_0)	H'FFFF C004	H'02	Initialization TIE = B'0: Disables transmit-data-empty-interrupt (TXI) request RIE = B'0: Disables receive-data-full-interrupt (RXI) and receive-error-interrupt (ERI) requests TE = B'0: Disables transmission of data RE = B'0: Disables reception of data
			At the time of setting Clock-synchronous mode CKE [1:0] = B'10: External clock, the SCK pin is used for synchronizing clock input
		H'52	When receiving operation is enabled RIE = B'1: Enables receive-data-full-interrupt (RXI) request RE = B'1: Enables reception of data
Serial status register (SCSSR_0)	H'FFFF C008	H'84	Initial value TDRE = B'1: Transmit data register empty flag TEND = B'1: Transmit end flag

Note: 1. For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communication interface in the *SH7137 Group Hardware Manual*.

3. Documents for Reference

- Software Manual
  SH-1/SH-2/SH2-DSP Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7137 Group Hardware Manual
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