

SH7216 Group

REJ06B0905-0101

Rev.1.01

Reception by the I²C Bus Interface 3 Module in Slave Operation

Jun 25, 2010

Introduction

This application note describes reception by the I²C bus interface 3 module (IIC3) of the SH7216 in the case of a single slave on the I²C bus.

Target Device

SH7216

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1. Preface

1.1 Specifications

- Data are transferred from a master transmitter to a slave receiver, with SH7216 MCUs serving as both master and slave devices.
- The transfer rate is set at 403 kHz.

Note: Two SH7216 CPU boards (R0K572167) are used to run this sample program, and code included in the SH7216 Application Note *Transmission by the I²C Bus Interface 3 Module in Master Operation* (REJ06B0904) is used for the master transmitter software.

1.2 Module Used

- I²C bus interface 3 (IIC3)
- Clock pulse generator (CPG)
- Power-Down Modes
- Pin function controller (PFC)

1.3 Applicable Conditions

- MCU SH7216
- Operating frequency Internal clock: 200 MHz
Bus clock: 100 MHz
Peripheral clock: 50 MHz
- Integrated development environment High-performance Embedded Workshop Ver.4.05.01
(from Renesas Electronics Corp.)
- C compiler SuperH RISC Engine Family C/C++ Compiler Package Ver.9.03.00 Release01
from Renesas Electronics
- Compiler options Default settings of the High-performance Embedded Workshop
(-cpu=sh2afpu -pic=1 -object="\$(CONFIGDIR)¥\$(FILELEAF).obj"
-debug -gbr=auto -chgincpath -errorpath -global_volatile=0
-opt_range=all -infinite_loop=0 -del_vacant_loop=0
-struct_alloc=1 -nologo)
- Slave receive module SH7216 CPU board (R0K572167)

1.4 Related Application Note

- SH7216 Group Application Note: *Transmission by the I²C Bus Interface 3 Module in Master Operation* (REJ06B0905)

2. Overview

In this sample program, the SH7216 (master device) transfers data to the SH7216 (slave device) by using I²C bus interface 3 (IIC3) module.

2.1 Operational Overview of Module Used

The I²C bus interface 3 (IIC3) module conforms to and provides a subset of the Philips I²C (Inter-IC) bus interface functions. However, the configuration of the registers that control the I²C bus differs in some respects from the register configuration implemented by Philips.

The features of the SH7216's I²C bus interface 3 (IIC3) are described below.

- I²C bus format and clock-synchronous serial format are selectable.
- Continuous transmission/reception
Since the shift register, transmit data register, and receive data register are independent of each other, continuous data transfer is possible.

Table 1 is a list of the features of the available formats, and figure 1 shows a block diagram of the IIC3 module.

Table 1 Features of the Formats

Format	Features
I ² C bus format	<ul style="list-style-type: none"> • Start and stop conditions are generated automatically in master mode. • Acknowledge output levels are selectable in data reception. • Acknowledge bit is automatically loaded in data transmission • On-chip bit synchronization/wait function In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically. If transmission/reception is not yet possible, set the SCL to low until preparations are completed. • Six interrupt sources <ol style="list-style-type: none"> 1. Transmit data empty (including slave-address match) 2. Transmit end 3. Receive data full (including slave-address match) 4. Arbitration lost 5. NACK detection 6. Stop condition detection • Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request. • Direct bus drive Two pins, SCL and SDA pins, function as NMOS open-drain outputs when the bus drive function is selected.
Clock-synchronous serial format	<ul style="list-style-type: none"> • Four interrupt sources <ol style="list-style-type: none"> 1. Transmit-data-empty 2. Transmit-end 3. Receive-data-full 4. Overrun error • Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request.

Note: For details on IIC3, see the section on I²C Bus Interface 3 (IIC3) of the *SH7216 Group Hardware Manual (REJ09B0543)*.

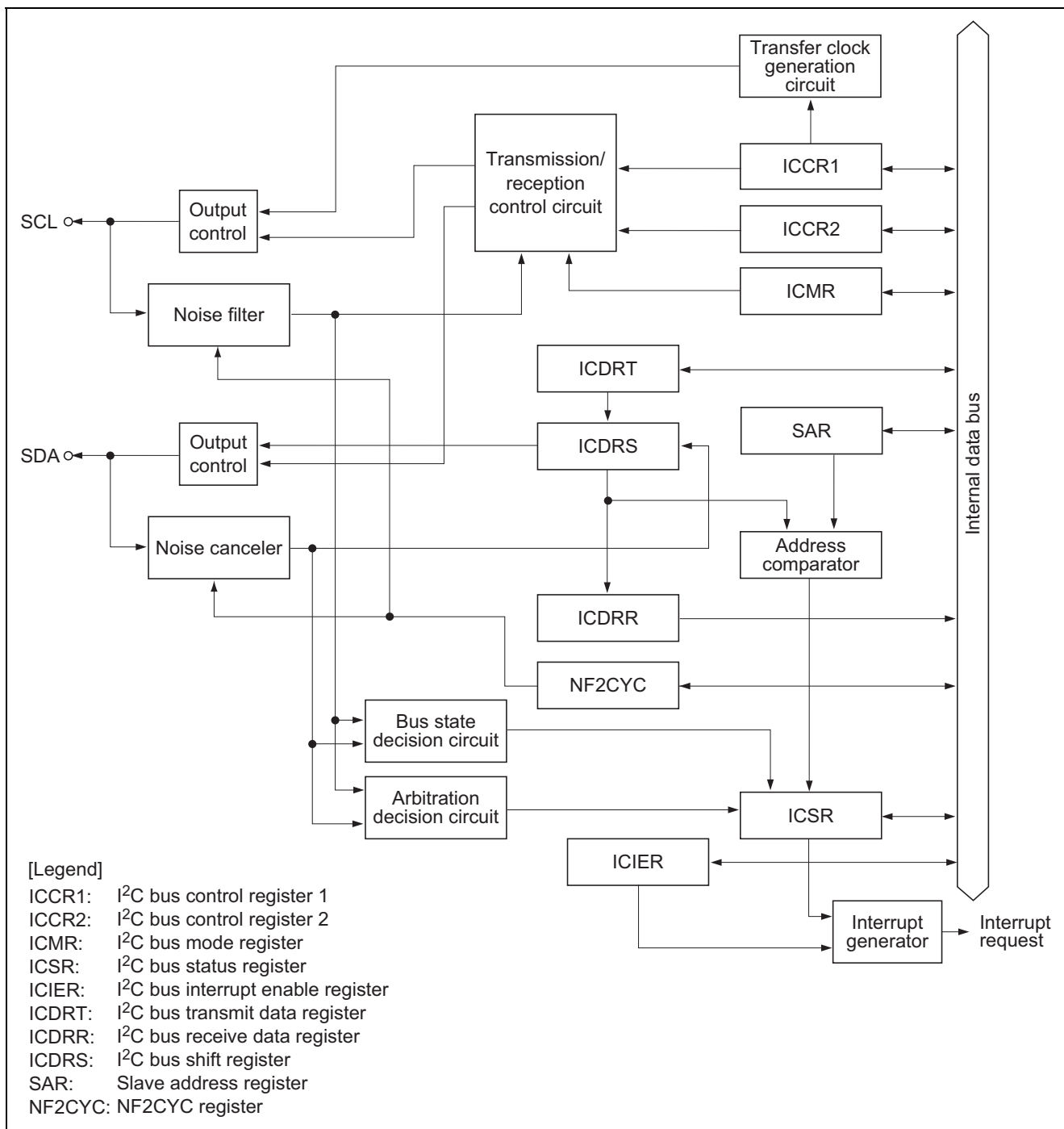


Figure 1 Overview of I²C Bus Interface 3

2.2 Procedure for Setting Module Used

This section describes the procedure for making initial settings for IIC3. The transfer rate must be set to meet the external specification. In this sample program, P ϕ /124 is specified as the transfer rate. Figure 2 shows an example of the initialization sequence for IIC3. For details on the settings of individual registers, see the *SH7216 Group Hardware Manual (REJ09B0543)*.

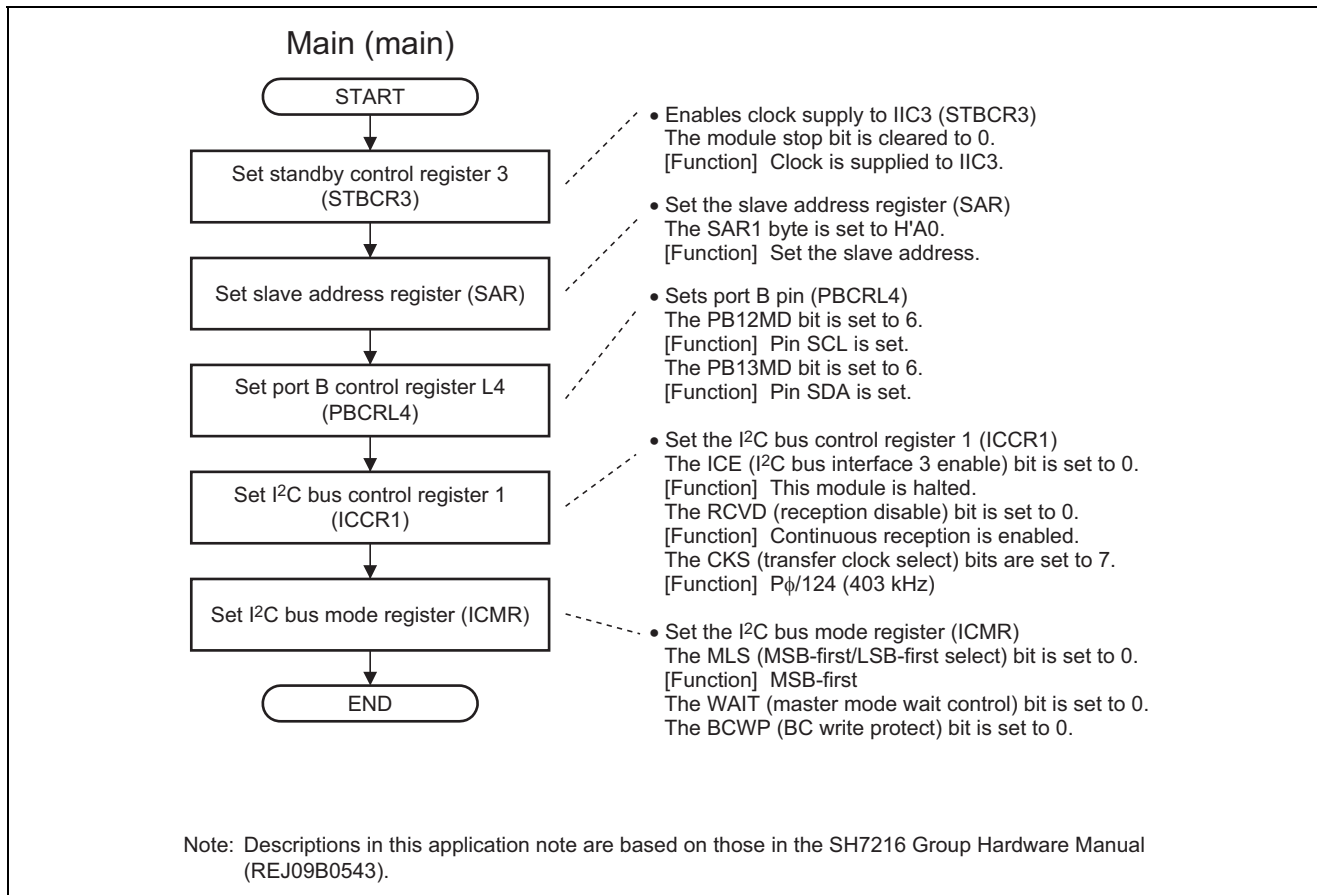


Figure 2 Example of the Initialization Sequence for I²C Bus Interface 3

2.3 Operation of the Sample Program

In this sample program, IIC3 is placed in slave receive mode, and receives 10 bytes for reading from a page within the SH7216.

The device code b'1010 and the device address b'000 are used.

Figure 3 shows the operations for reading from a single page, and figure 4 shows the operating environment of this sample program.

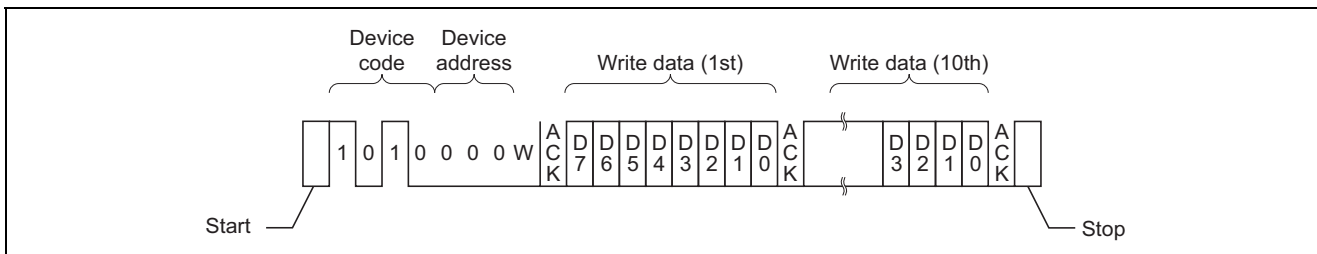


Figure 3 Page Read Operation

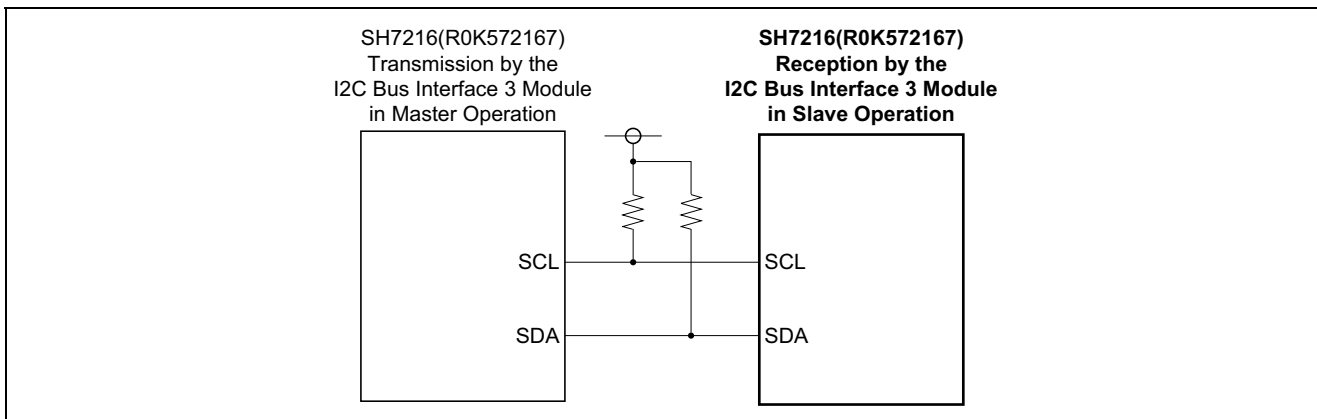


Figure 4 Operating Environment of the Sample Program

2.4 Sequence of Processing by the Sample Program

Table 2 gives the register settings in the sample program. Table 3 shows macro definitions in the sample program. Figures 5 to 8 show the flow of processing by the sample program.

Table 2 Register Settings Used in Sample Program

Register Name	Address	Setting Value	Description
Standby control register 3 (STBCR3)	H'FFFE0408	H'00	MSTP33 = "0": IIC3 operates.
I ² C bus control register 1 (ICCR1)	H'FFFEE000	H'87	ICE = "1": SCL and SDA pins are placed in bus-drive state. RCVD = "0": Continuous reception is enabled. MST = "0", TRS = "0": Slave receive mode CKS = "B'0111": transfer rate P _φ /124
I ² C bus mode register (ICMR)	H'FFFEE002	H'30	MLS = "0": MSB-first BCWP = "0": Allows the writing of values to the BC bits. BC = "B'000": 9 bits

Table 3 Macro Definitions Used in Sample Program

Macro Definition	Setting Value	Description
DEVICE_CODE	H'A0	Device code
DEVICE_ADDR	H'00	Device address
IIC_DATA_WR	H'00	Write code
IIC_DATA_RD	H'01	Read code
IIC3_DATA	10	Data transfer size

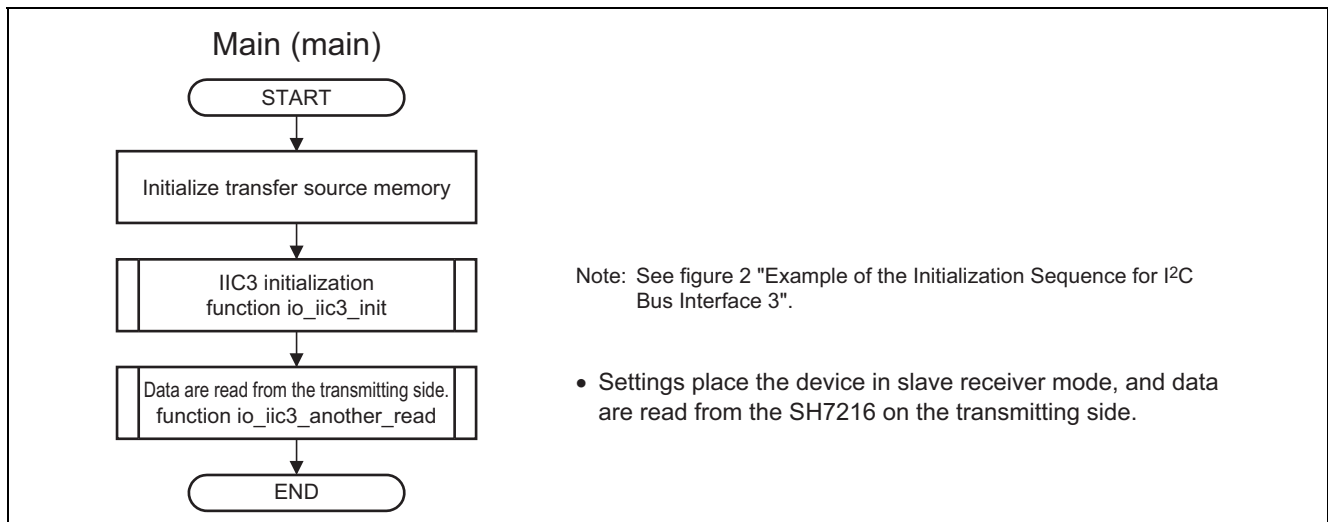


Figure 5 Flow of Processing by the Sample Program (1)

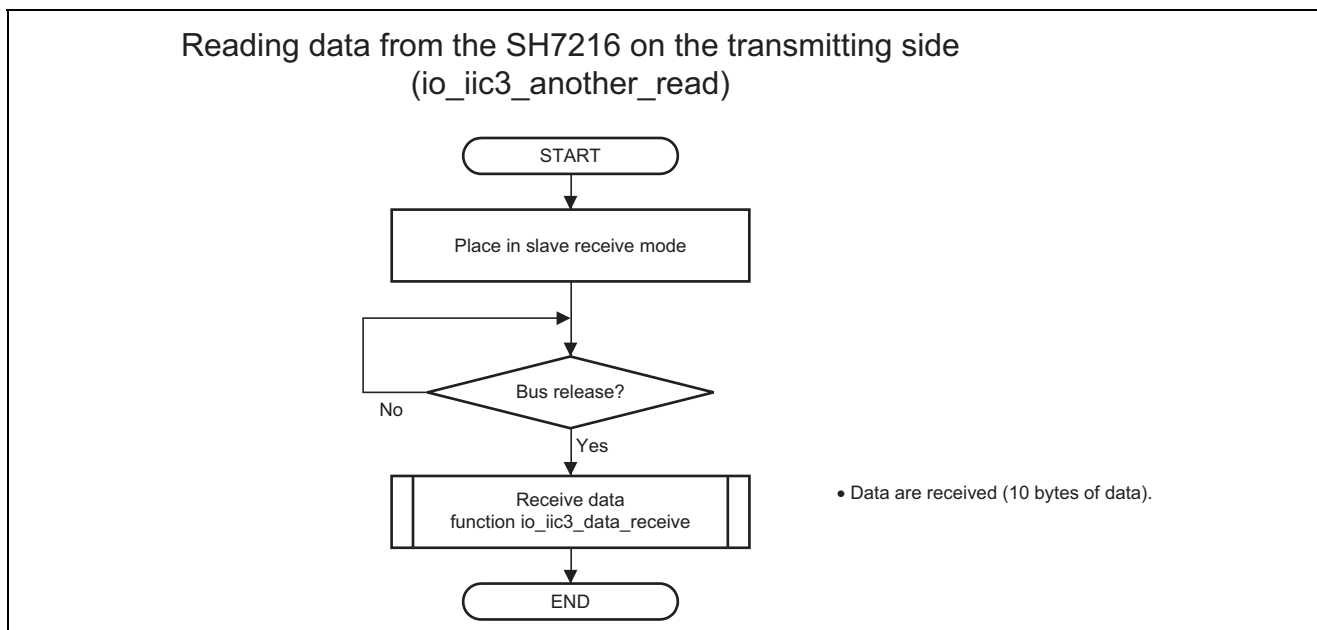


Figure 6 Flow of Processing by the Sample Program (2)

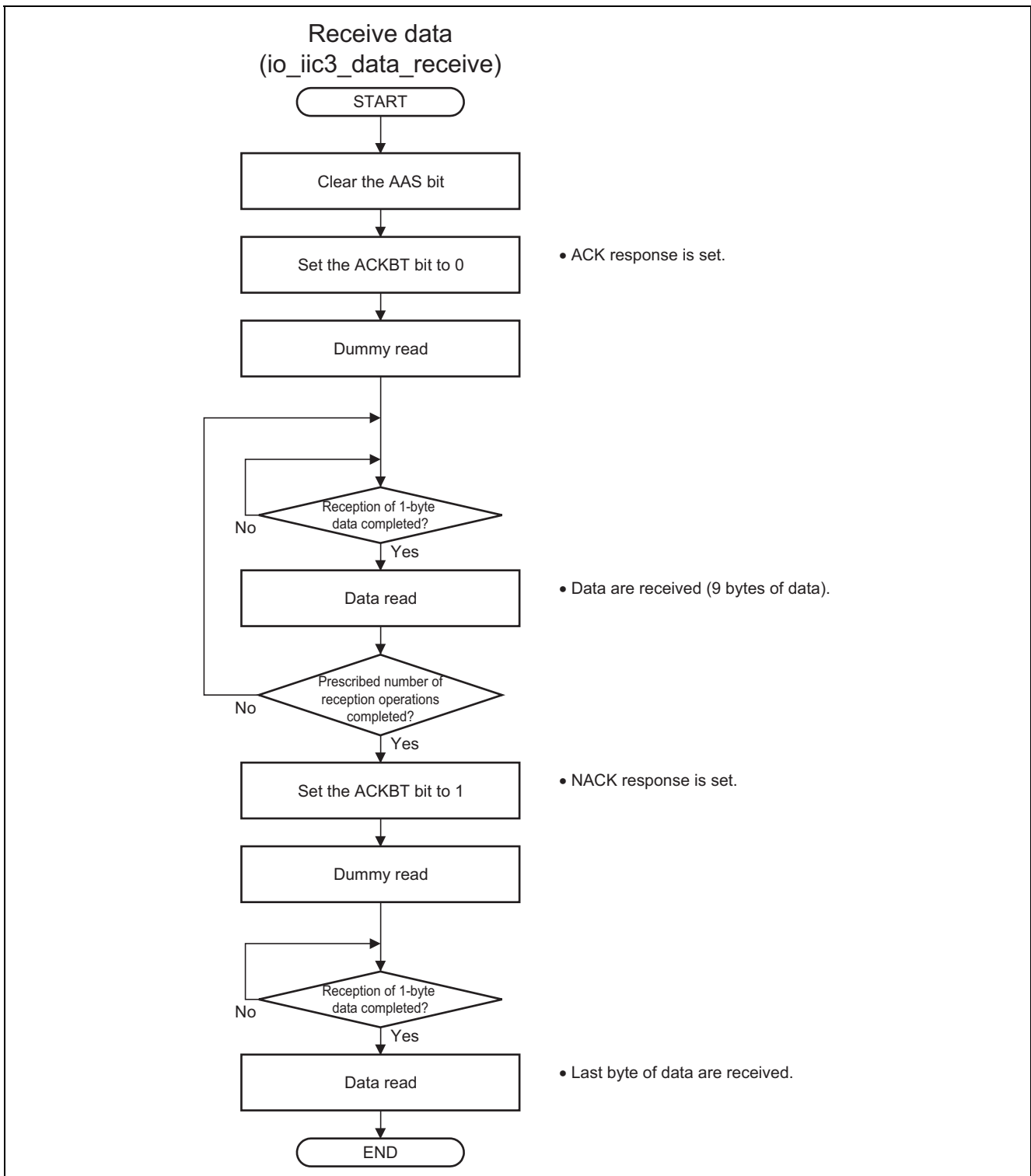


Figure 7 Flow of Processing by the Sample Program (3)

3. Listing of the Sample Program

```

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**"FILE COMMENT"***** Technical reference data *****
*   System Name : SH7216 Sample Program
*   File Name   : main.c
*   Abstract    : Sample Program of Compare Match Timer
*   Version     : 0.00.00
*   Device      : SH7216
*   Tool-Chain  : High-performance Embedded Workshop (Ver.4.05.01).
*                : C/C++ compiler package for the SuperH RISC engine family
*                :                               (Ver.9.03 Release01).
*   OS          : None
*   H/W Platform: R0K572167 (CPU board)
*   Description :
*   note       : This program receives data to the SH7211 base on the
*               : master-send side by using the slave-read mode of IIC3.
*****/
*   History     : Apr.15,2009 Ver.0.00.00
**"FILE COMMENT END"*****/
#include <machine.h>
#include "iodefine.h"      /* SH7216 iodefine */

/* ==== symbol definition ==== */
#define DEVICE_CODE 0xA0      /* another device code   : b'1010   */
#define DEVICE_ADDR 0x00     /* another device address : b'000   */
#define IIC_DATA_WR 0x00     /* Data write code       : b'0     */
#define IIC_DATA_RD 0x01     /* Data read code        : b'1     */
#define IIC3_DATA 10

#define E_OK 0
#define E_ERR -1
#define HIGH 1
#define LOW 0

/* ==== RAM allocation variable declaration ==== */
unsigned char ReadData[IIC3_DATA];

```

Figure 8 Sample Program Listing: main.c (1)

```

/* ==== prototype declaration ==== */
void main(void);
void io_iic3_mst_send_end(void);
int io_iic3_init(void);
int io_iic3_another_read(unsigned int r_size, unsigned char *r_buf);
int io_iic3_data_receive(unsigned char *r_buf, unsigned int r_size);
int io_iic3_data_send(unsigned char data);
int io_iic3_address_send(unsigned char *data);

void io_led_ini(void);
void io_init_cmt0(void);

/* "FUNC COMMENT" "*****" */
* Outline      : sumple program main
* -----
* Include      :
* -----
* Declaration  : void main(void);
* -----
* Function     : sumple program main
* -----
* Argument     : void
* -----
* Return Value : none
* -----
* Notice      :
* "FUNC COMMENT END" "*****" /
void main(void)
{
    int i;
    /* ==== Reading data creation ==== */
    for(i = 0; i < IIC3_DATA; i++){
        ReadData[i] = 0x00;
    }
    /* ==== IIC3 initialization ==== */
    io_iic3_init();

    /* ==== IIC3 slave-receive mode ==== */
    io_iic3_another_read(sizeof(WriteData), /* Writing data's size */
                        WriteData);        /* Store the writing data */

    while(1){
        /* Loop */
    }
}

```

Figure 9 Sample Program Listing: main.c (2)

```

/*"FUNC COMMENT"*****
* Outline      : IIC3-module initial setting
*-----
* Include      : #include "iodefine.h"
*-----
* Declaration  : int io_iic3_init(void);
*-----
* Function     : IIC3-module initial setting
*-----
* Argument     : void
*-----
* Return Value : E_OK
*-----
* Notice      :
*"FUNC COMMENT END"*****/
int io_iic3_init(void)
{
    STB.CR3.BIT._IIC3 = 0x00;          /* Clear the IIC3 module standby mode */

    /* slave-address setting */
    IIC3.SAR.BYTE = (DEVICE_CODE | ((DEVICE_ADDR & 0x7) << 1) | LOW);

    /* ---- PFC setting ---- */
    PFC.PBCRL4.BIT.PB12MD = 0x06;     /* SCL selection */
    PFC.PBCRL4.BIT.PB13MD = 0x06;     /* SDA selection */
    /* ----IIC31 module operation disabled ---- */
    IIC3.ICCR1.BIT.ICE = 0x00;        /* IIC transfer disabled state */
    IIC3.ICCR1.BIT.ICE = 0x01;        /* IIC3 transfer enabled */
    IIC3.ICCR1.BIT.RCVD = 0x00;       /* Continue the next receive data */
    IIC3.ICCR1.BIT.CKS = 0x07;        /* Transfer clock rate : Pφ/124(403kHz) */

    /* ---IIC bus mode register (ICMR) setting --- */
    IIC3.ICMR.BYTE = 0x30;
    /*
        bit7   : MLS:0 ----- MSB first
        bit6   : WAIT:0 ----- No WAIT insertion
        bit5-4 : Reserve:1 ----- Reserve bits
        bit3   : BCWP:0 ----- Unsetting
        bit2-0 : BC2:0, BC1:0, BC0:0 ----- IIC bus format: 9 bits
    */

    return(E_OK);
}

```

Figure 10 Sample Program Listing: main.c (3)

```

/* "FUNC COMMENT"*****
 * Outline      : Read data for master-side
 *-----
 * Include      : #include "iodefine.h"
 *-----
 * Declaration  : int io_iic3_another_read( unsigned int r_size,
 *                                     : unsigned char *r_buf);
 *-----
 * Function     : Receiving data to be readed in master-side is specified
 * : by w_buf, and the data is "w_size"BYTE.
 * : (sizeof(WriteData) = w_size, WriteData = *w_buf)
 *-----
 * Argument     : unsigned int r_size ; Reading data size
 * : unsigned char* r_buf ; Store the reading data
 *-----
 * Return Value : E_OK ; ACK response
 * : E_ERR ; No ACK response
 *-----
 * Notice      :
 * "FUNC COMMENT END"*****/
int io_iic3_another_read(unsigned int r_size, unsigned char *r_buf)
{
    int ack = E_OK;

    IIC3.ICCR1.BYTE &= 0xcf;          /* slave-receive mode */

    while(IIC3.ICCR2.BIT.BBSY == 0x01){
        /* It waits untill the bus is opened */
    }
    r_buf = r_buf - 1;
    io_iic3_data_receive(r_buf, r_size);

    return(ack);
}

```

Figure 11 Sample Program Listing: main.c (4)

```

/* "FUNC COMMENT"*****
 * Outline      : lbyte data receiving(slave-read mode)
 *-----
 * Include      : #include "iodef.h"
 *-----
 * Declaration  : int io_iic3_data_receive(unsigned char *r_buf,
 *                               :                unsigned int r_size);
 *-----
 * Function     : It sets to the slave reception mode,
 *               : it receives for the number of bytes specified with r_size,
 *               : and receive data is stored in r_buf.
 *-----
 * Argument     : unsigned char *r_buf ; Reading data storage
 *               : unsigned int r_size ; Reading data size
 *-----
 * Return Value : E_OK ; ACK response
 *-----
 * Notice      :
 * "FUNC COMMENT END"*****/
int io_iic3_data_receive(unsigned char *r_buf, unsigned int r_size)
{
    int i;
    unsigned char dummy;

    IIC3.ICSR.BIT.AAS = 0x00;          /* AAS Clear */

    IIC3.ICIER.BIT.ACKBT = 0x00;      /* ACK setting"L" */
    dummy = IIC3.ICDRR;               /* Dummy read */

    for(i = 0; i < r_size + 1; i++){
        while(IIC3.ICSR.BIT.RDRF == 0x00){
            /* It waits until the reception is completed. (1BYTE) */
        }
        *r_buf++ = IIC3.ICDRR;        /* Data read */
    }

    IIC3.ICIER.BIT.ACKBT = 0x01;      /* ACK setting"H" */

    dummy = IIC3.ICDRR;

    while(IIC3.ICSR.BIT.RDRF == 0x00 && i < r_size - 1){
        /* It waits until the reception is completed. (1BYTE) */
    }
    *r_buf--;
    *r_buf = IIC3.ICDRR;              /* Last BYTE */

    return(E_OK);
}

/* End of File */

```

Figure 12 Sample Program Listing: main.c (5)

4. Documents for Reference

- Software Manual
SH-2A, SH2A-FPU Software Manual (REJ09B0051)
The most up-to-date version of this document is available on the Renesas Electronics Website.
- Hardware Manual
SH7216 Group Hardware Manual (REJ09B0543)
The most up-to-date version of this document is available on the Renesas Electronics Website.

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1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

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