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SH7263/SH7203 Group

Reception by the I²C Bus Interface 3 Module in Single-Master Operation (EEPROM Reading)

Introduction

This application note describes reception by the I²C bus interface 3 module (IIC3) of the SH7263/SH7203 in the case of a single master on the I²C bus.

Target Device

SH7263/SH7203

Contents

1. Preface

1.1 Specifications

- Data are read from an EEPROM with the SH7263/SH7203 as the master device and the EEPROM as a slave device.
- The transfer rate is set at 397 kHz.

Note: Please adjust settings as required to match the specifications of the EEPROM you are using.

1.2 Module Used

- I²C bus interface 3 (IIC3) channel 3

1.3 Applicable Conditions

- MCU: SH7263/SH7203
- Operating frequency: Internal clock 200 MHz
  Bus clock 66.67 MHz
  Peripheral clock 33.33 MHz
- C compiler: SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01
  from Renesas Technology
- Compiler options: -cpu = sh2a -include = "$(WORKSPDIR)\inc"
  -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath
  -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo
- EEPROM: HN58X24128FPIE (128 Kbits)
  from Renesas Technology

1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note “Example of Initial Configuration” for the SH7263/SH7203 (REJ06B0740). Please refer to that document when setting up this sample task.

2. Description of the Sample Application

In this sample program, the SH7263/SH7203 (master device) receives data from the EEPROM (slave device) by using the I²C bus interface 3 (IIC3) module.

2.1 Operational Overview of Module Used

The I²C bus interface 3 (IIC3) module conforms to and provides a subset of the Philips I²C (Inter-IC) bus interface functions. However, the configuration of the registers that control the I²C bus differs in some respects from the register configuration implemented by Philips.

The features of the I²C bus interface 3 (IIC3) for the SH7263/SH7203 are described below.

- I²C bus format and clock-synchronous serial format are selectable.
- Continuous transmission/reception
  Since the shift register, transmit data register, and receive data register are independent of each other, continuous data transfer is possible.

Table 1 is a list of the features of the available formats, and figure 1 shows a block diagram of the IIC3 module.

Table 1 Features of the Formats

Format	Features
I²C bus format	• Start and stop conditions are generated automatically in master mode. • Acknowledge output levels are selectable in data reception. • Acknowledge bit is automatically loaded in data transmission • On-chip bit synchronization/wait function In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically. If transmission/reception is not yet possible, set the SCL to low until preparations are completed. • Six interrupt sources 1. Transmit data empty (including slave-address match) 2. Transmit end 3. Receive data full (including slave-address match) 4. Arbitration lost 5. NACK detection 6. Stop condition detection • Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request. • Direct bus drive Two pins, SCL and SDA pins, function as NMOS open-drain outputs when the bus drive function is selected.
Clock-synchronous serial format	• Four interrupt sources 1. Transmit-data-empty 2. Transmit-end 3. Receive-data-full 4. Overrun error • Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request.

Note: For details on IIC3, see the section on I²C Bus Interface 3 (IIC3) in the *SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313)*.

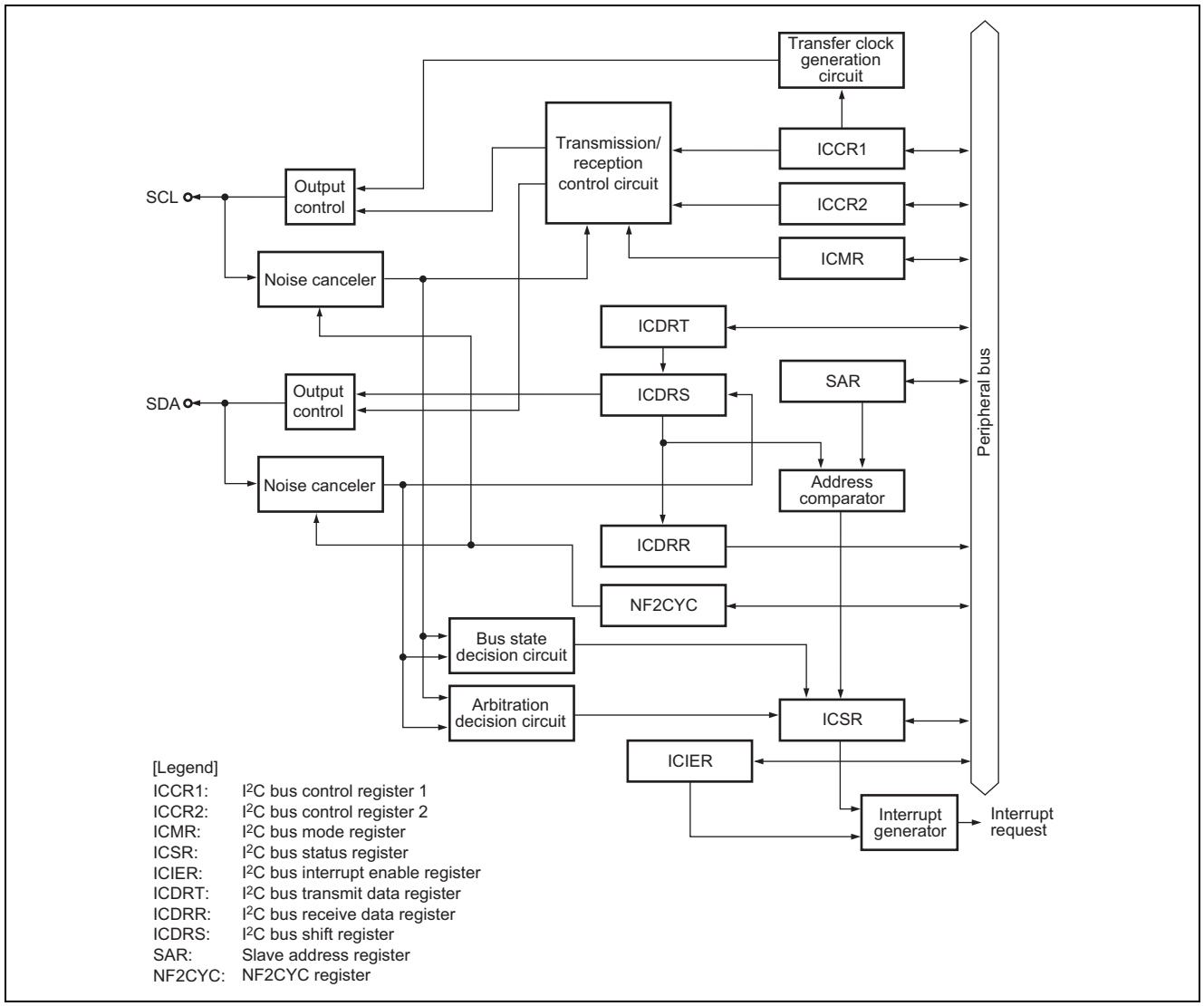

Figure 1 Overview of I²C Bus Interface 3

2.2 Procedure for Setting the Module Used

This section describes the procedure for making initial settings for IIC3. The transfer rate must be set to meet the external specification. In this sample program, Pϕ/84 is specified as the transfer rate. Figure 2 shows an example of the initialization sequence for IIC3. For details on the settings of individual registers, see the *SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313).*

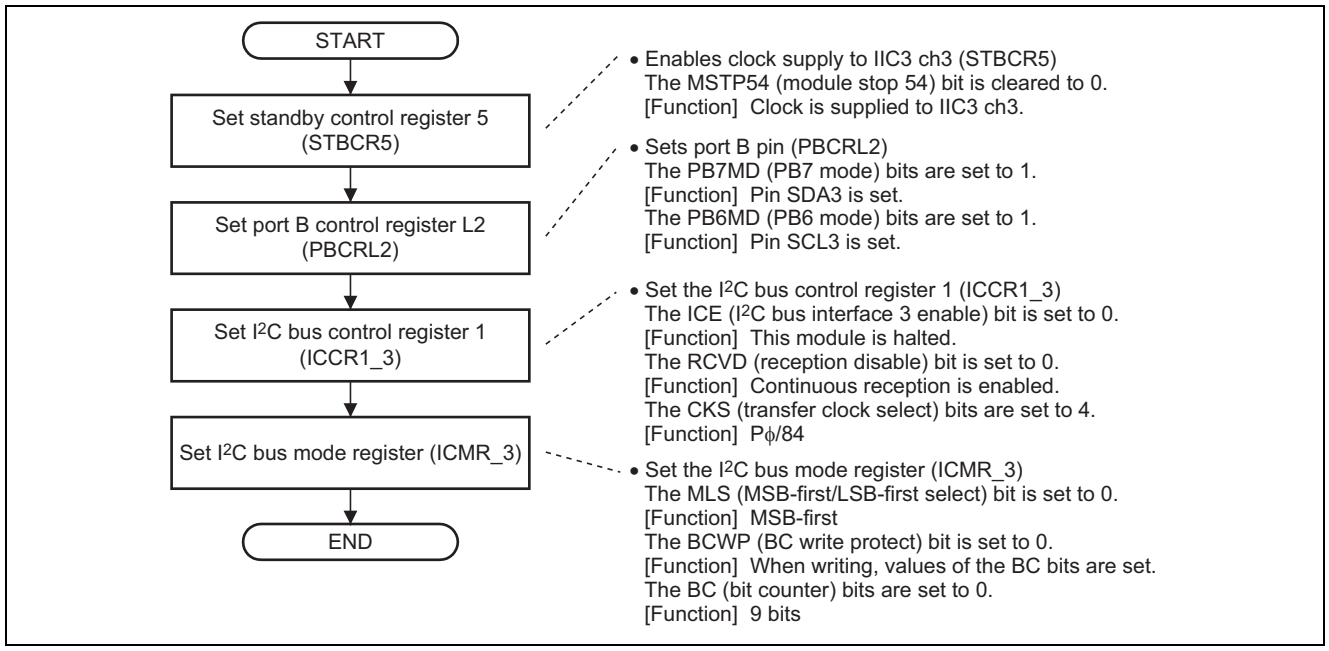

Figure 2 Example of the Initialization Sequence for I²C Bus Interface 3

2.3 Operation of the Sample Program

In this sample program, IIC3 is placed in master transmit mode, and reads out 10 bytes of data in sequence from the EEPROM.

The device code employed in this sample program is “B’1010”. Consult the datasheet of the EEPROM you are using for its device code.

The device address employed in this sample program is “B’000”. Consult the datasheet of the EEPROM you are using for its device address.

The memory address indicates the point where reading of EEPROM starts. Each time EEPROM is read, the address is incremented.

Figure 3 shows the operations for sequential reading, and figure 4 shows the operating environment of this sample program.

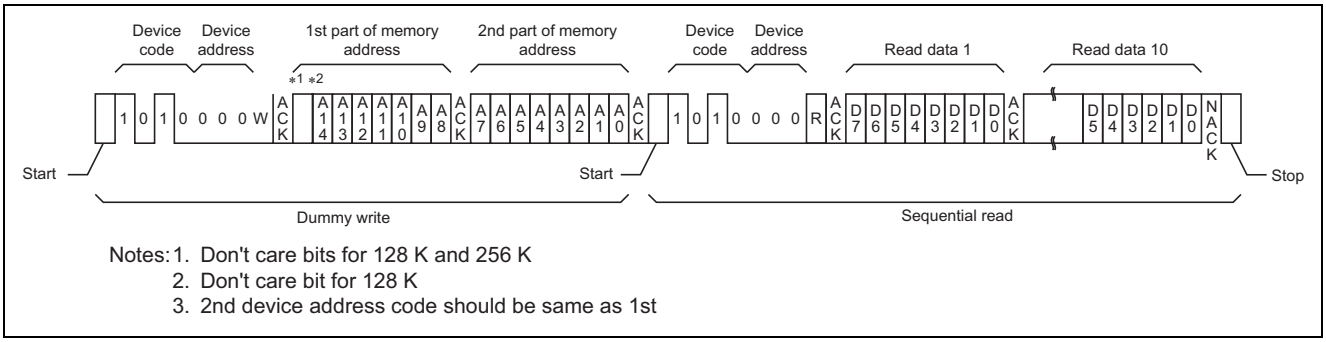

Figure 3 Operations for Sequential Reading

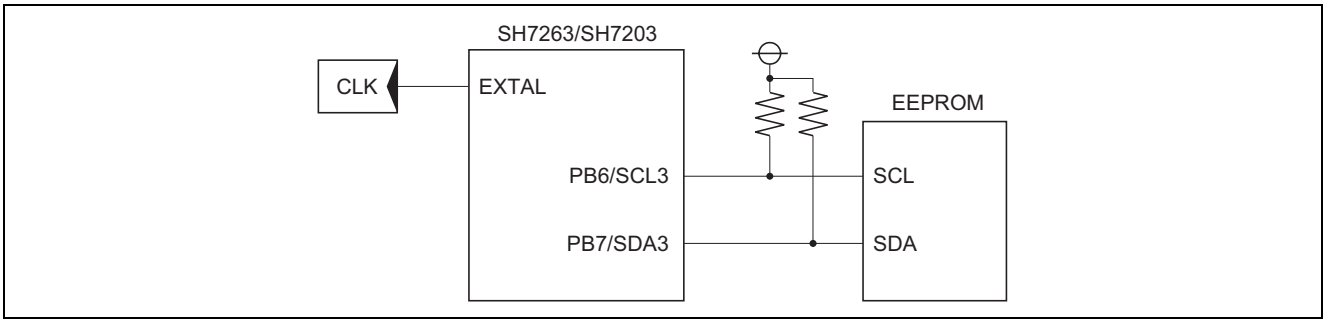

Figure 4 Operating Environment of the Sample Program

2.4 Sequence of Processing by the Sample Program

Table 2 gives the register settings in the sample program. Table 3 shows macro definitions in the sample program. Figures 5 to 10 show the flow of processing by the sample program.

Table 2 Register Settings Used in Sample Program

Register Name	Address	Setting Value	Description
Standby control register 5 (STBCR5)	H'FFFE 0410	H'00	MSTP54 = "0": IIC3-3 operates.
I²C bus control register 1 (ICCR1_3)	H'FFFE EC00	H'E4	ICE = "1": SCL and SDA pins are placed in the bus-drive state. RCVD = "1": Continuous reception is disabled. MST = "1", TRS = "0": Master receive mode CKS = "B'0100": transfer rate Pϕ/84
I²C bus mode register (ICMR_3)	H'FFFE EC02	H'30	MLS = "0": MSB-first BCWP = "0": Allows the writing of values to the BC bits. BC = "B'000": 9 bits

Table 3 Macro Definitions Used in Sample Program

Macro Definition	Setting Value	Description
EEPROM_MEM_ADDR	H'0000	EEPROM start address
DEVICE_CODE	H'A0	Device code
DEVICE_ADDR	H'00	Device address
IIC_DATA_WR	H'00	Write code
IIC_DATA_RD	H'01	Read code
IIC3_DATA	10	Data transfer size

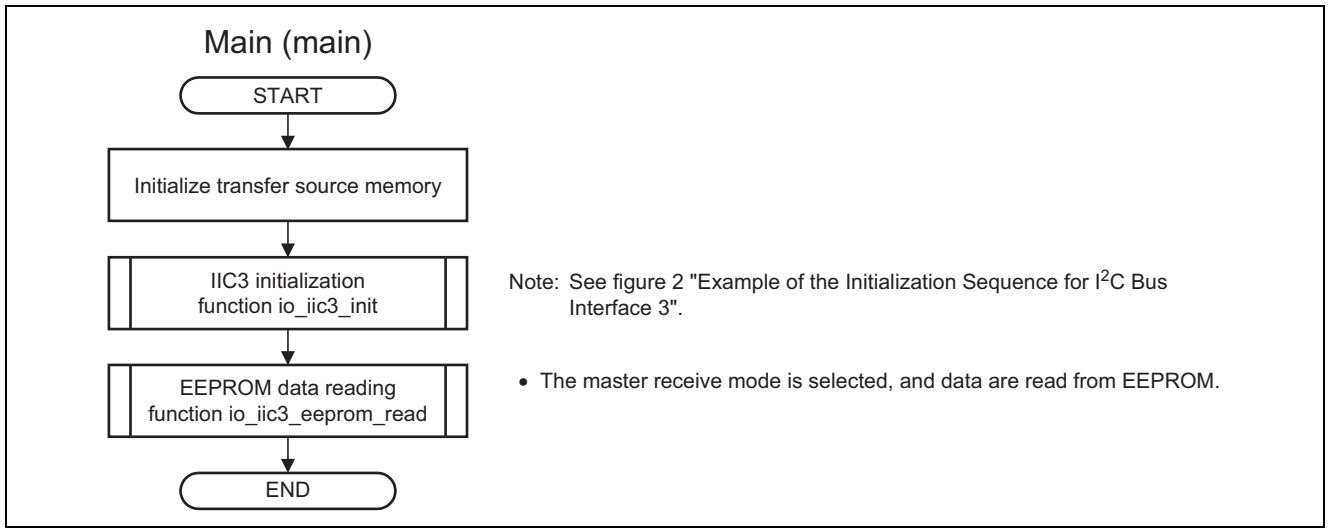

Figure 5 Flow of Processing by the Sample Program (1)

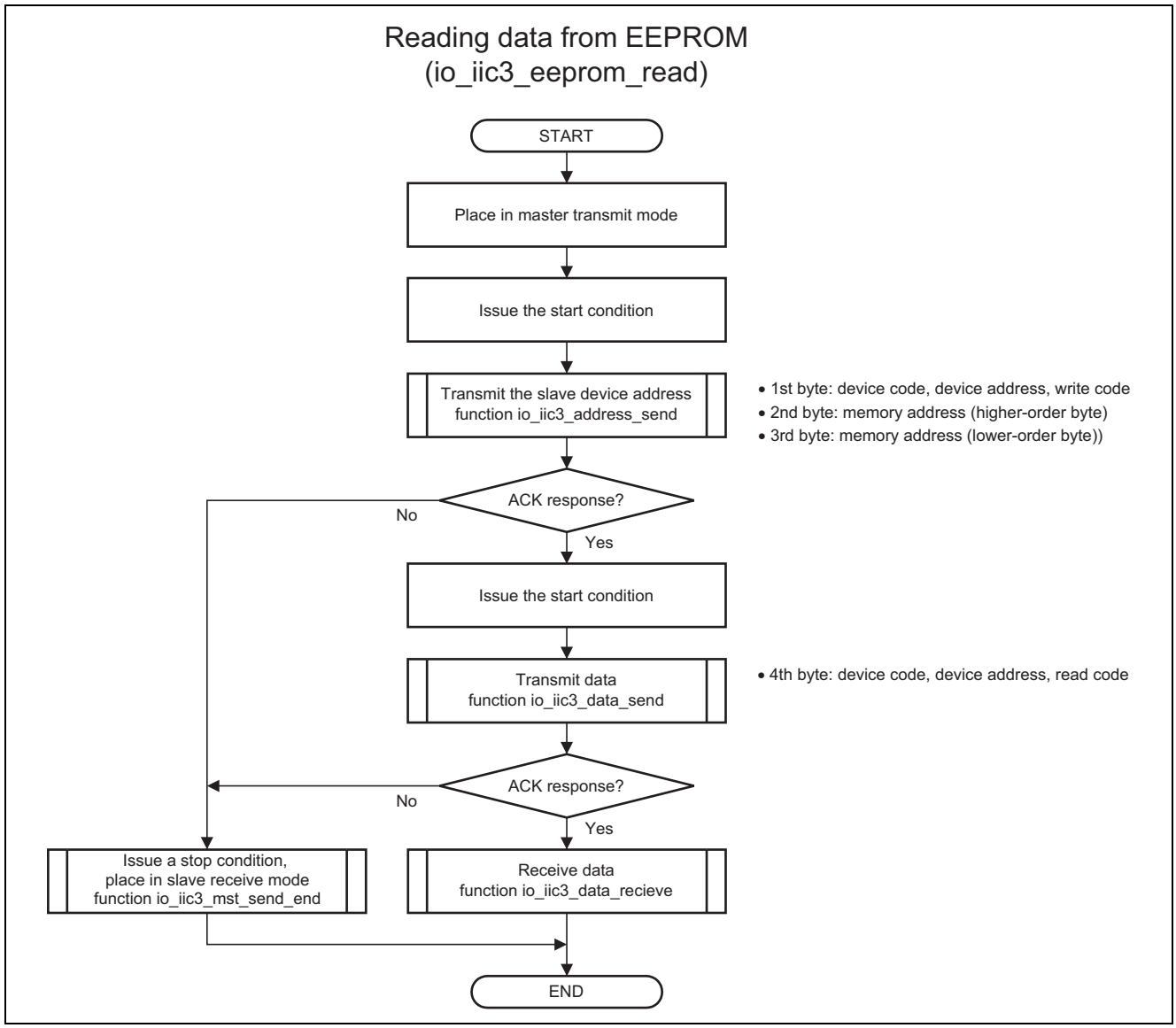

Figure 6 Flow of Processing by the Sample Program (2)

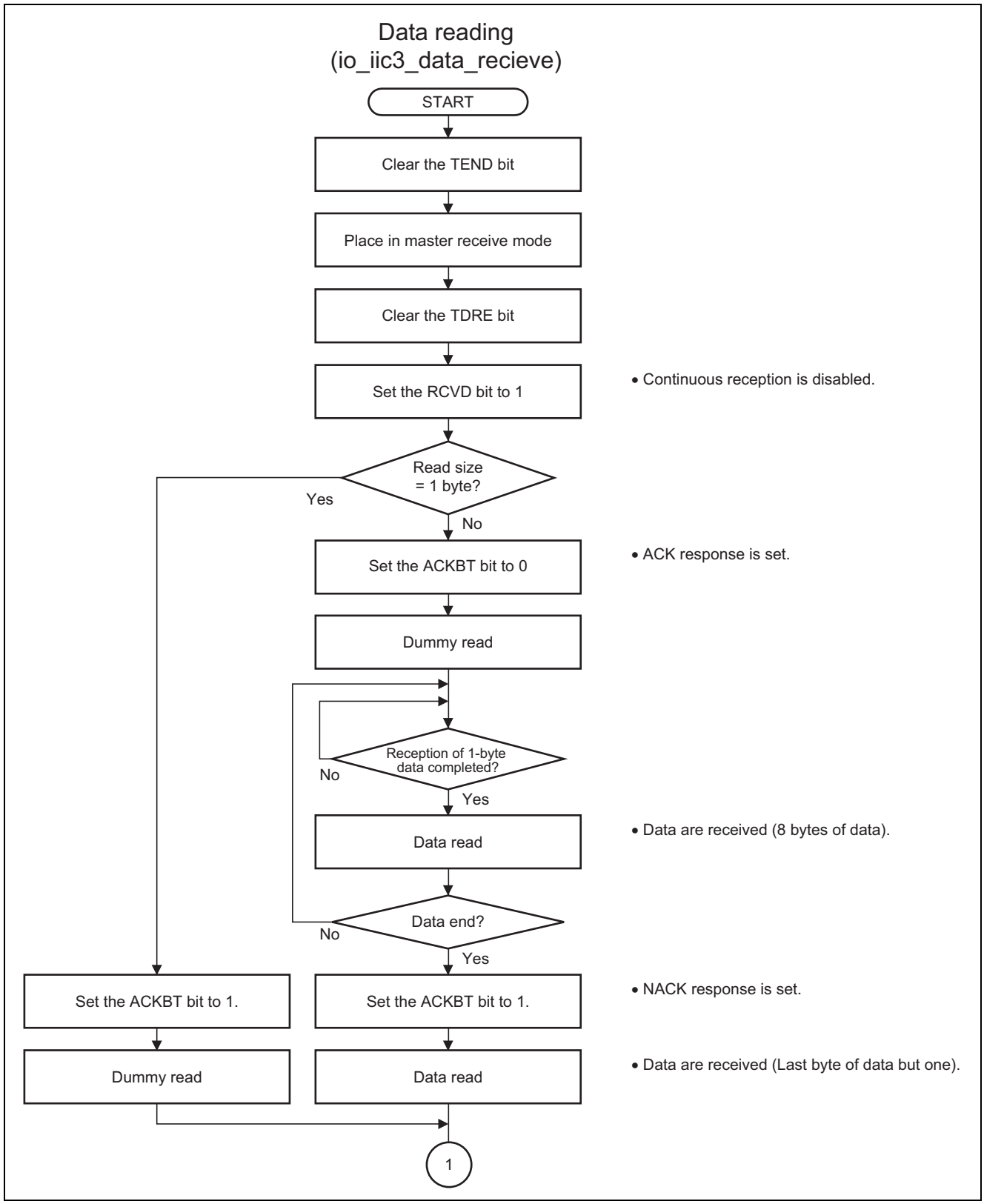

Figure 7 Flow of Processing by the Sample Program (3)

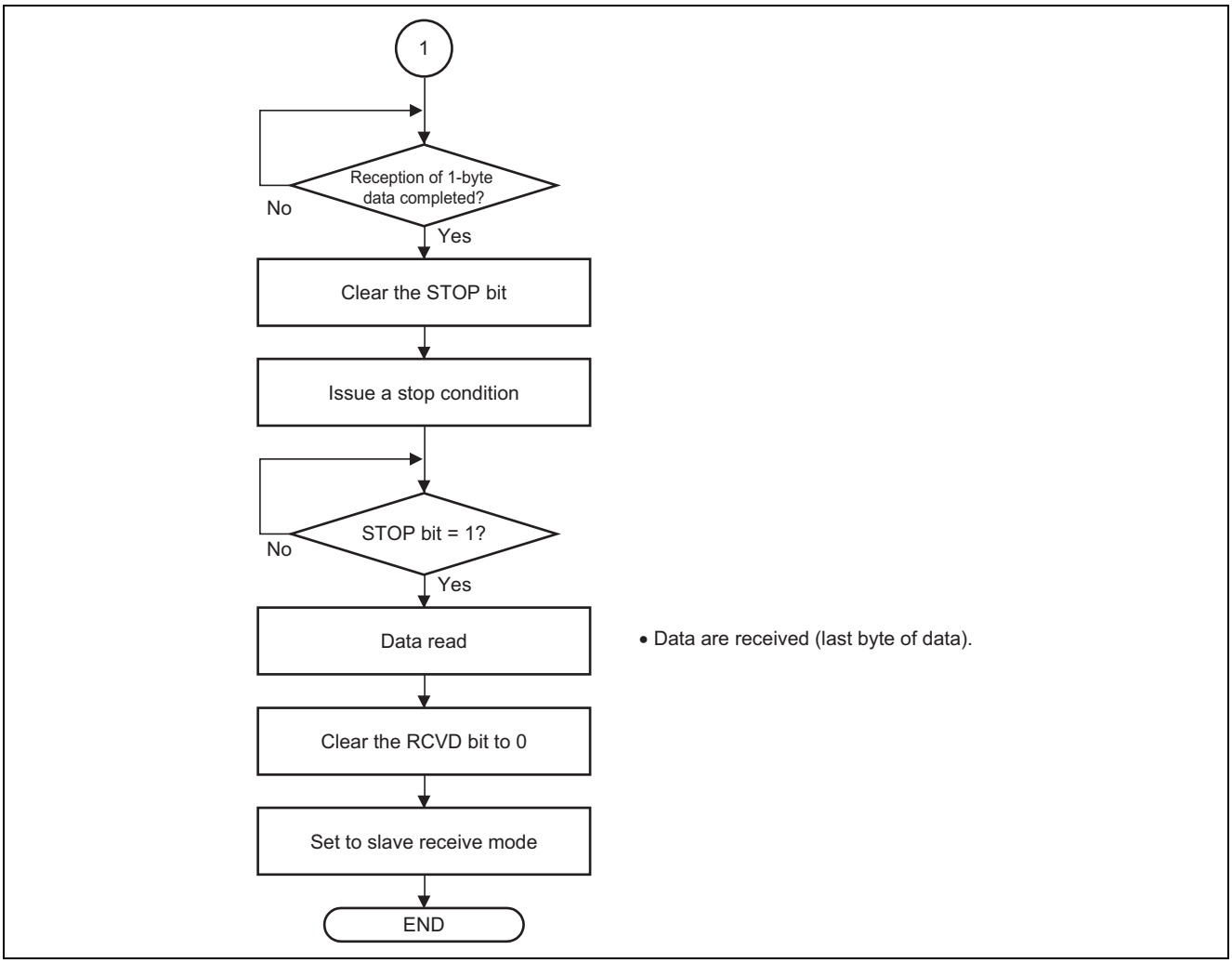

Figure 8 Flow of Processing by the Sample Program (4)

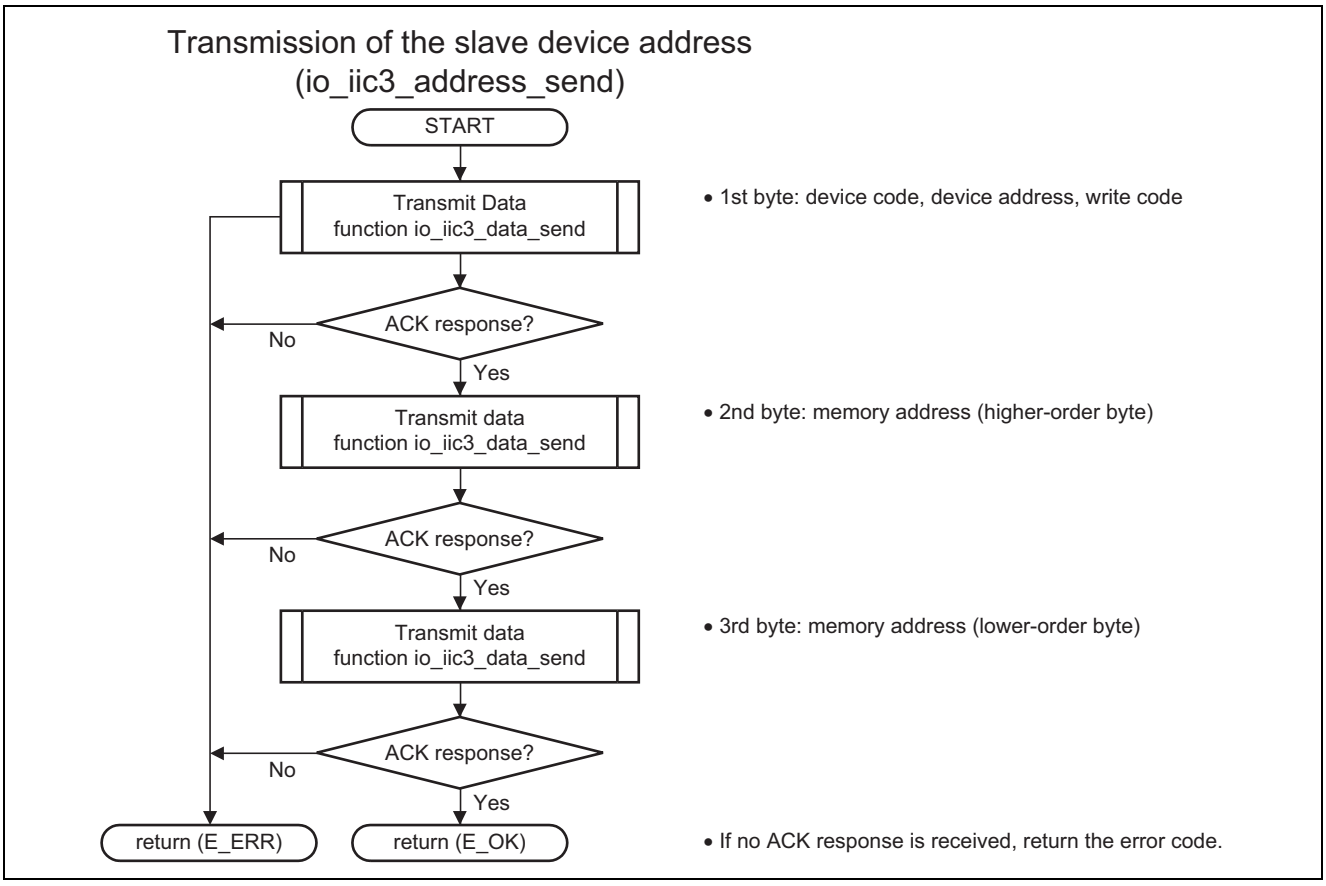

Figure 9 Flow of Processing by the Sample Program (5)

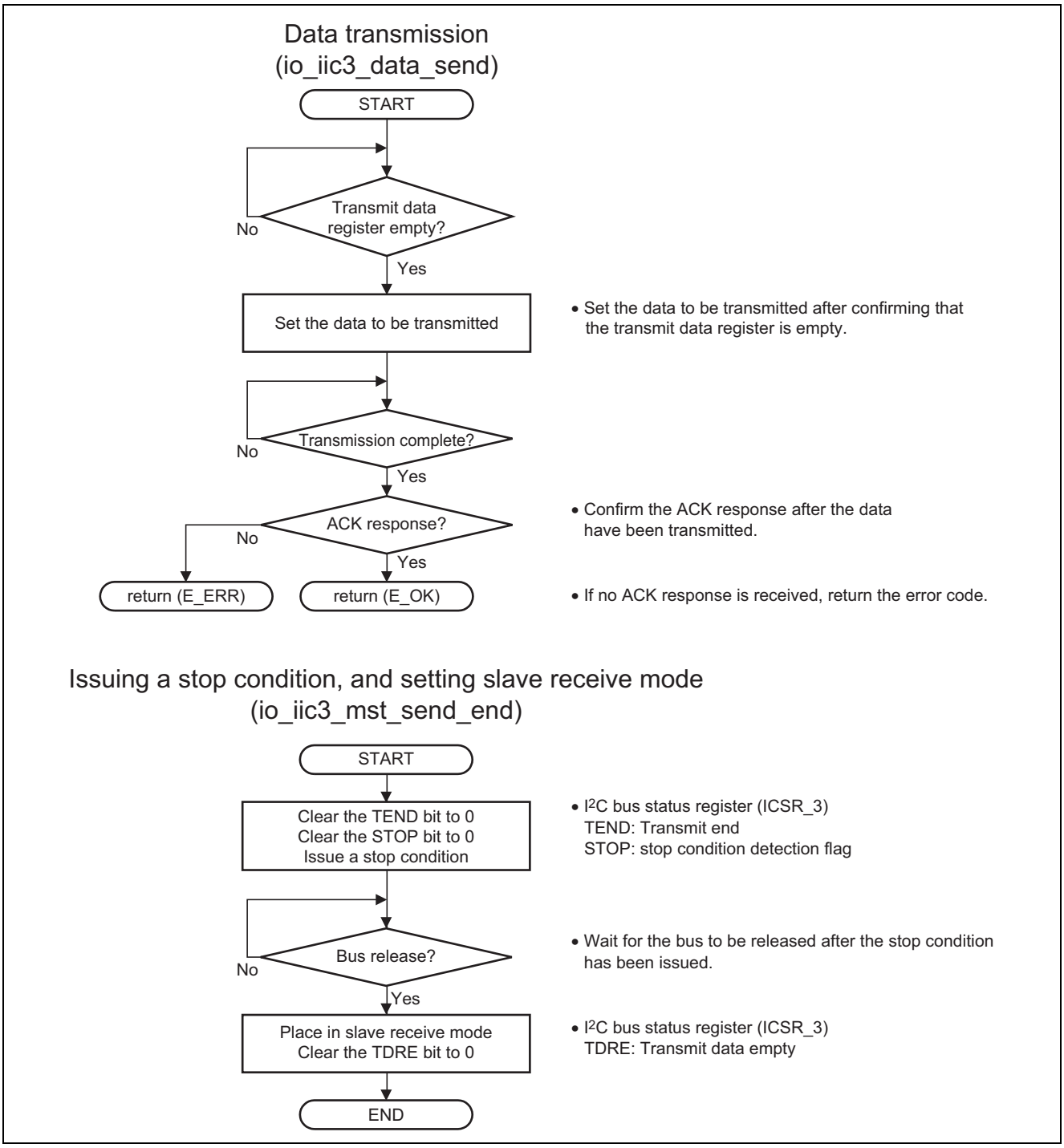

Figure 10 Flow of Processing by the Sample Program (6)

2.5 Note on Master Receive Mode

If the I2C bus receive data register (ICDRR) is read near the falling edge of the 8th clock cycle, the data will not be received in some cases. In addition, if the reception disable (RCVD) bit in the I2C bus control register 1 is set to 1 near the falling edge of the 8th clock cycle while the receive buffer is full, a stop condition cannot be issued in some cases. To prevent these errors, one of the following two methods should be selected.
In this sample program, the RCVD bit is set to 1 to select data reception in byte units.

1. In master receive mode, reading the ICDRR must proceed before the falling edge of the 8th clock cycle.
2. In master receive mode, the RCVD bit should be set to 1 and the processing should be performed in byte units.

2.6 Note on Master Receive Mode with ACKBT Setting

In master receive mode operation, the ACKBT bit must be set before the falling edge of the 8th clock cycle on pin SCL falls in the final data transfer of consecutive data transfer. Otherwise, an overrun may occur on the slave device.

In the sample program, the RCVD bit is set to 1 to select data transfer in byte units; therefore, this note does not apply to this sample program.

3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```
/*""FILE COMMENT""*****************************************************************
*
* System Name  : SH7263 Sample Program
* File Name    : main.c
* Contents     : Sample program for reception by IIC3 in master receive mode
* Version      : 1.00.00
* Model        : R0K572630D001BR
* CPU          : SH7263
* Compiler     : SHC9.1.1.0
* note         : Data are received from EEPROM
*                using IIC3 in master receive mode.
*
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*
* history : 2008.06.05 ver.1.00.00
*""FILE COMMENT END""*************************************************************/
#include <machine.h>
#include "iodefine.h"         /* SH7263 iodefine */

/* ==== symbol definition ==== */
#define EEPROM_MEM_ADDR 0x0000
#define DEVICE_CODE 0xA0      /* EEPROM device code :b'1010  */
#define DEVICE_ADDR 0x00      /* EEPROM device address:b'000 */
#define IIC_DATA_WR 0x00      /* Data write code :b'0        */
#define IIC_DATA_RD 0x01      /* Data read code :b'1         */
#define IIC3_DATA 10

#define E_OK 0
#define E_ERR -1
#define HIGH 1
#define LOW 0

/* ==== RAM allocation variable declaration ==== */
unsigned char ReadData[IIC3_DATA];

/* ==== Prototype declaration ==== */
void main(void);
void io_iic3_mst_send_end(void);
int io_iic3_init(void);
int io_iic3_eeprom_read(unsigned char d_code,unsigned char d_adr,unsigned short r_adr,
                        unsigned int r_size,unsigned char* r_buf);
int io_iic3_data_recieve(unsigned char* r_buf,unsigned int r_size);
int io_iic3_data_send(unsigned char data);
int io_iic3_address_send(unsigned char* data);
```

2. Sample Program Listing: main.c (2)

```
/*""FUNC COMMENT""*******************************************************
* Outline      : Sample program main
*-----------------------------------------------------------------------
* Include      :
*-----------------------------------------------------------------------
* Declaration  : void main(void);
*-----------------------------------------------------------------------
* Function     : Sample program main
*-----------------------------------------------------------------------
* Argument     : void
*-----------------------------------------------------------------------
* Return Value : void
*-----------------------------------------------------------------------
* Notice       :
*""FUNC COMMENT END""*************************************************/
void main(void)
{
    int i;
    /* ==== Clear the data storage location ==== */
    for(i=0;i<IIC3_DATA;i++){
           ReadData[i] = 0x00;
    }
    /* ==== IIC3 initialization setting ==== */
    io_iic3_init();

    /* ==== Reception by IIC3 in master receive mode ==== */
    io_iic3_eeprom_read(   DEVICE_CODE,       /* Device code */
                           DEVICE_ADDR,       /* Device address */
                           0x0000,            /* Start address for reading out data */
                           sizeof(ReadData),  /* Read data size */
                           ReadData);         /* Data storage location */
    while(1){
               /* Loop */
    }
}

```

3. Sample Program Listing: main.c (3)

```
 87    /*""FUNC COMMENT""*****************************************************
 88    * Outline      : IIC3 module initialization
 89    *-----------------------------------------------------------------------
 90    * Include      : #include "iodefine.h"
 91    *-----------------------------------------------------------------------
 92    * Declaration  : int io_iic3_init(void);
 93    *-----------------------------------------------------------------------
 94    * Function     : IIC3 module initialization
 95    *-----------------------------------------------------------------------
 96    * Argument     : void
 97    *-----------------------------------------------------------------------
 98    * Return Value : E_OK
 99    *-----------------------------------------------------------------------
100    * Notice       :
101    *""FUNC COMMENT END""*************************************************/
102    int io_iic3_init(void)
103    {
104        CPG.STBCR5.BIT.MSTP54 = 0u;       /* Clear the IIC3_3 module standby mode */
105
106        /* ---- PFC setting ---- */
107        PORT.PBCRL2.BIT.PB6MD = 1u;       /* SCL3 selection */
108        PORT.PBCRL2.BIT.PB7MD = 1u;       /* SDA3 selection */
109        /* ----IIC31 module operation disabled ---- */
110        IIC33.ICCR1.BIT.ICE = 0u;         /* IIC transfer disabled state */
111        IIC33.ICCR1.BIT.ICE = 1u;         /* IIC3 module operation is enabled */
112        IIC33.ICCR1.BIT.RCVD = 0u;        /* Continuous reception is to proceed */
113        IIC33.ICCR1.BIT.CKS = 4u;         /* Transfer rate: Pϕ/84(397 kHz) */
114
115    /* ---IIC bus mode register (ICMR) setting --- */
116        IIC33.ICMR.BYTE = 0x30u;
117                    /*
118                                bit7    : MLS:0 --------------------  MSB first
119                                bit6    : WAIT:0 -------------------  No WAIT insertion
120                                bit5-4  : Reserve:1 ----------------  Reserve bit
121                                bit3    : BCWP:0--------------------  Unsetting
122                                bit2-0  : BC0:0, BC1:0,BC0:0--------  IIC format 9-bit
123                    */
124        return(E_OK);
125    }
126
```

4. Sample Program Listing: main.c (4)

```
/*""FUNC COMMENT""*******************************************************
* Outline      : EEPROM data read
*-----------------------------------------------------------------------
* Include      : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration  : int io_iic3_eeprom_read( unsigned char d_code,
*              :                          unsigned char d_adr,
*              :                          unsigned short r_adr,
*              :                          unsigned int r_size,
*              :                          unsigned char* r_buf);
*-----------------------------------------------------------------------
* Function     : The amount of data specified by “r_size” are read out from the
*              : EEPROM specified by device code “d_code” and device address “d_adr”,
*              : and are stored in the area specified by “r_buf”.
*              : Memory addresses within the EEPROM are specified by “r_adr”.
*-----------------------------------------------------------------------
* Argument     : unsigned char d_code    : Device code
*              : unsigned char d_adr     : Device address
*              : unsigned short r_adr    : Address where data to be read in starts
*              : unsigned int r_size     : Amount of data to be read-in
*              : unsigned char* r_buf    : Location of data to be read-in
*-----------------------------------------------------------------------
* Return Value : With ACK response       : E_OK
*              : With no ACK response    : E_ERR
*-----------------------------------------------------------------------
* Notice :
*""FUNC COMMENT END""*************************************************/
int io_iic3_eeprom_read(unsigned char d_code,unsigned char d_adr,unsigned short r_adr,
                        unsigned int r_size,unsigned char* r_buf)
{
    int ack = E_OK;
    unsigned char send[4];

    send[0] = (unsigned char)(d_code|((d_adr & 0x7)<<1)|IIC_DATA_WR);
    send[1] = (unsigned char)((r_adr>>8) & 0x00ff);
    send[2] = (unsigned char)(r_adr & 0x00ff);
    send[3] = (unsigned char)(d_code|((d_adr & 0x7)<<1)|IIC_DATA_RD);

    while(IIC33.ICCR2.BIT.BBSY == 1u){
                /* Waiting for bus release */
    }
    IIC33.ICCR1.BYTE |= 0x30u;                      /* Set to master transmission mode */
    IIC33.ICCR2.BYTE = ((IIC33.ICCR2.BYTE & 0xbfu)|0x80u);  /* Issue the start condition */

    ack = io_iic3_address_send(send);   /* Transmit the first, second, and third bytes of data */

    if(ack == E_OK){
            /* ACK response is received from the specified device */
            IIC33.ICCR2.BYTE=((IIC33.ICCR2.BYTE & 0xbfu) | 0x80u);  /* Issue a start condition */
            ack = io_iic3_data_send(send[3]);     /* Transmit the fourth byte of data */
            if(ack == E_OK){
                    io_iic3_data_recieve(r_buf,r_size);   /* Data reception */
            }
            else{
                    io_iic3_mst_send_end();
            }
    }
    else{
            /* ACK response is not received from the specified device */
            io_iic3_mst_send_end();
    }
    return(ack);
}

```

5. Sample Program Listing: main.c (5)

```
/*""FUNC COMMENT""*************************************************************
* Outline      : Master receive mode
*------------------------------------------------------------------------------
* Include      : #include "iodefine.h"
*------------------------------------------------------------------------------
* Declaration  : int io_iic3_data_recieve(unsigned char* r_buf,
*              :                          unsigned int r_size);
*------------------------------------------------------------------------------
* Function     : The amount of data specified by “r_size” are received
*              : in master receive mode and are stored in the area specified by
*              : “r_buf”. After the specified number of data have been received,
*              : slave receive mode is selected.
*------------------------------------------------------------------------------
* Argument     : unsigned char* r_buf     : Location of data to be read in
*              : unsigned int r_size      : Amount of data to be read in
*------------------------------------------------------------------------------
* Return Value : Always E_OK
*------------------------------------------------------------------------------
* Notice       :
*""FUNC COMMENT END""*************************************************/
int io_iic3_data_recieve(unsigned char* r_buf,unsigned int r_size)
{
    int i;
    unsigned char dummy;
    IIC33.ICSR.BIT.TEND = 0u;                   /* Clear bit TEND */
    IIC33.ICCR1.BIT.TRS = 0u;                   /* Master receive mode */
    IIC33.ICSR.BIT.TDRE = 0u;                   /* Clear bit TDRE */
    IIC33.ICCR1.BIT.RCVD = 1u;                  /* Disable continuous reception */
    if(r_size == 1){                            /* When one byte of data is received */
                IIC33.ICIER.BIT.ACKBT = 1u;     /* Acknowledge setting “H” */
                dummy = IIC33.ICDRR;            /* Dummy read */
    }
    else{
                IIC33.ICIER.BIT.ACKBT = 0u;         /* Acknowledge setting “L”  */
                dummy = IIC33.ICDRR;                /* Dummy read */
                for(i=0;i<r_size - 2;i++){
                        while(IIC33.ICSR.BIT.RDRF == 0u){
                                /* Waiting for reception of one byte of data */
                        }
                        *r_buf++ = IIC33.ICDRR;     /* Data read */
                }
                while(IIC33.ICSR.BIT.RDRF == 0u){
                        /* Waiting for reception of one byte of data */
              }

                IIC33.ICIER.BIT.ACKBT = 1u;         /* Acknowledge setting “H” */
                *r_buf++ = IIC33.ICDRR;             /* Next to last byte of data */
    }
    while(IIC33.ICSR.BIT.RDRF == 0u){
            /* Waiting for reception of one byte of data */
    }
    IIC33.ICSR.BIT.STOP = 0u;                       /* Clear the STOP flag */
    IIC33.ICCR2.BYTE &= 0x3fu;                      /* Issue a stop condition */
    while(IIC33.ICSR.BIT.STOP == 0u){
            /* Waiting for generation of a stop condition */
    }

    *r_buf = IIC33.ICDRR;                           /* Last byte of data */
    IIC33.ICCR1.BIT.RCVD = 0u;                      /* Clear bit RCVD */
    IIC33.ICCR1.BYTE &= 0xcfu;                      /* Slave receive mode */

    return(E_OK);
}
```

6. Sample Program Listing: main.c (6)

```
254    /*""FUNC COMMENT""*************************************************************
255    * Outline      : Transmission of the slave device address
256    *-------------------------------------------------------------------------
257    * Include      :
258    *-------------------------------------------------------------------------
259    * Declaration  : int io_iic3_address_send(unsigned char* data);
260    *-------------------------------------------------------------------------
261    * Function     : Transmission of the slave device address specified by “data” (one byte)
262    *              : and the memory address (two bytes)
263    *-------------------------------------------------------------------------
264    * Argument     : unsigned char* data  : Transmit data
265    *-------------------------------------------------------------------------
266    * Return Value : With ACK response    : E_OK
267    *              : With no ACK response     : E_ERR
268    *-------------------------------------------------------------------------
269    * Notice       :
270    *""FUNC COMMENT END""*************************************************/
271    int io_iic3_address_send(unsigned char* data)
272    {
273        int ack;
274
275        ack = io_iic3_data_send(*data++);        /* Slave device address */
276        if(ack == E_ERR){
277                   return(ack);
278        }
279        ack = io_iic3_data_send(*data++);        /* 1st part of memory address */
280        if(ack == E_ERR){
281                   return(ack);
282        }
283        ack = io_iic3_data_send(*data);          /* 2nd part of memory address */
284        if(ack == E_ERR){
285                   return(ack);
286        }
287        return(ack);
288    }
289    /*""FUNC COMMENT""*************************************************************
290    * Outline      : Transmission of one byte of data
291    *-------------------------------------------------------------------------
292    * Include      : #include "iodefine.h"
293    *-------------------------------------------------------------------------
294    * Declaration  : int io_iic3_data_send(unsigned char data);
295    *-------------------------------------------------------------------------
296    * Function     : Data are transmitted according to the following procedure.
297    *              : 1.Wait for ICDRT to become empty.
298    *              : 2.Set the data to be transmitted.
299    *              : 3.Check completion of data transmission.
300    *              : 4.Check the ACK response.
301    *-------------------------------------------------------------------------
302    * Argument     : unsigned char data   : Data for transmission
303    *-------------------------------------------------------------------------
304    * Return Value : With ACK response       : E_OK
305    *              : With no ACK response    : E_ERR
306    *-------------------------------------------------------------------------
307    * Notice       :
308    *""FUNC COMMENT END""*************************************************/
```

7. Sample Program Listing: main.c (7)

```
309    int io_iic3_data_send(unsigned char data)
310    {
311        int ack;
312
313        while(IIC33.ICSR.BIT.TDRE == 0x0){
314                    /* Wait for ICDRT to become empty. */
315        }
316        IIC33.ICDRT = data;
317        while(IIC33.ICSR.BIT.TEND == 0x00){
318                    /* Wait for completion of data transmission */
319        }
320        if(IIC33.ICIER.BIT.ACKBR == 0){
321                    ack = E_OK;
322        }
323        else{
324                    ack = E_ERR;
325        }
326        return(ack);
327    }
328    /*""FUNC COMMENT""*****************************************************
329    * Outline      : Issuing a stop condition
330    *-----------------------------------------------------------------------
331    * Include      : #include "iodefine.h"
332    *-----------------------------------------------------------------------
333    * Declaration  : void io_iic3_mst_send_end(void);
334    *-----------------------------------------------------------------------
335    * Function     : A stop condition is issued and slave receive mode is set.
336    *-----------------------------------------------------------------------
337    * Argument     : void
338    *-----------------------------------------------------------------------
339    * Return Value : void
340    *-----------------------------------------------------------------------
341    * Notice       :
342    *""FUNC COMMENT END""*************************************************/
343    void io_iic3_mst_send_end(void)
344    {
345        IIC33.ICSR.BIT.TEND = 0u;     /* Clear the TEND flag */
346        IIC33.ICSR.BIT.STOP = 0u;     /* Clear the STOP flag */
347        IIC33.ICCR2.BYTE &= 0x3fu;    /* Issue a stop condition */
348
349        while(IIC33.ICSR.BIT.STOP == 0u){
350                    /* Wait for bus release */
351        }
352
353        IIC33.ICCR1.BYTE &= 0xcfu;    /* Slave receive mode */
354        IIC33.ICSR.BIT.TDRE = 0u;     /* Clear bit TDRE */
355    }
356    /* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7203 Group Hardware Manual (REJ09B0313)
  The most up-to-date version of this document is available on the Renesas Technology Website.
  SH7263 Group Hardware Manual (REJ09B0290)
  The most up-to-date version of this document is available on the Renesas Technology Website.

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