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April 1\textsuperscript{st}, 2010
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SH7263/SH7203 Group

Reception by the I²C Bus Interface 3 Module in Single-Master Operation (EEPROM Reading)

Introduction

This application note describes reception by the I²C bus interface 3 module (IIC3) of the SH7263/SH7203 in the case of a single master on the I²C bus.

Target Device

SH7263/SH7203

Contents

1. Preface .................................................................................................................................................. 2
2. Description of the Sample Application .............................................................................................. 3
3. Listing of the Sample Program .......................................................................................................... 15
4. Documents for Reference ................................................................................................................... 22
1. Preface

1.1 Specifications

- Data are read from an EEPROM with the SH7263/SH7203 as the master device and the EEPROM as a slave device.
- The transfer rate is set at 397 kHz.

Note: Please adjust settings as required to match the specifications of the EEPROM you are using.

1.2 Module Used

- I²C bus interface 3 (IIC3) channel 3

1.3 Applicable Conditions

- MCU: SH7263/SH7203
- Operating frequency: Internal clock 200 MHz
  Bus clock 66.67 MHz
  Peripheral clock 33.33 MHz
- C compiler: SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01 from Renesas Technology
- Compiler options: -cpu = sh2a -include = "$(WORKSPDIR)\inc"
  -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath
  -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo
- EEPROM: HN58X24128FPIE (128 Kbits) from Renesas Technology

1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note “Example of Initial Configuration” for the SH7263/SH7203 (REJ06B0740). Please refer to that document when setting up this sample task.
2. Description of the Sample Application

In this sample program, the SH7263/SH7203 (master device) receives data from the EEPROM (slave device) by using the I²C bus interface 3 (IIC3) module.

2.1 Operational Overview of Module Used

The I²C bus interface 3 (IIC3) module conforms to and provides a subset of the Philips I²C (Inter-IC) bus interface functions. However, the configuration of the registers that control the I²C bus differs in some respects from the register configuration implemented by Philips.

The features of the I²C bus interface 3 (IIC3) for the SH7263/SH7203 are described below.

- I²C bus format and clock-synchronous serial format are selectable.
- Continuous transmission/reception
  - Since the shift register, transmit data register, and receive data register are independent of each other, continuous data transfer is possible.

Table 1 is a list of the features of the available formats, and figure 1 shows a block diagram of the IIC3 module.

### Table 1 Features of the Formats

<table>
<thead>
<tr>
<th>Format</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>I²C bus format</td>
<td>• Start and stop conditions are generated automatically in master mode.</td>
</tr>
<tr>
<td></td>
<td>• Acknowledge output levels are selectable in data reception.</td>
</tr>
<tr>
<td></td>
<td>• Acknowledge bit is automatically loaded in data transmission</td>
</tr>
<tr>
<td></td>
<td>• On-chip bit synchronization/wait function</td>
</tr>
<tr>
<td></td>
<td>- In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically. If transmission/reception is not yet possible, set the SCL to low until preparations are completed.</td>
</tr>
<tr>
<td></td>
<td>• Six interrupt sources</td>
</tr>
<tr>
<td></td>
<td>1. Transmit data empty (including slave-address match)</td>
</tr>
<tr>
<td></td>
<td>2. Transmit end</td>
</tr>
<tr>
<td></td>
<td>3. Receive data full (including slave-address match)</td>
</tr>
<tr>
<td></td>
<td>4. Arbitration lost</td>
</tr>
<tr>
<td></td>
<td>5. NACK detection</td>
</tr>
<tr>
<td></td>
<td>6. Stop condition detection</td>
</tr>
<tr>
<td></td>
<td>• Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request.</td>
</tr>
<tr>
<td></td>
<td>• Direct bus drive</td>
</tr>
<tr>
<td></td>
<td>Two pins, SCL and SDA pins, function as NMOS open-drain outputs when the bus drive function is selected.</td>
</tr>
<tr>
<td>Clock-synchronous</td>
<td>• Four interrupt sources</td>
</tr>
<tr>
<td>serial format</td>
<td>1. Transmit-data-empty</td>
</tr>
<tr>
<td></td>
<td>2. Transmit-end</td>
</tr>
<tr>
<td></td>
<td>3. Receive-data-full</td>
</tr>
<tr>
<td></td>
<td>4. Overrun error</td>
</tr>
<tr>
<td></td>
<td>• Data transfer by the direct memory access controller (DMAC) can be activated by a transmit-data-empty or receive-data-full interrupt request.</td>
</tr>
</tbody>
</table>

Note: For details on IIC3, see the section on I²C Bus Interface 3 (IIC3) in the SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313).
Figure 1  Overview of I²C Bus Interface 3

[Legend]
ICCR1: I²C bus control register 1
ICCR2: I²C bus control register 2
ICMR: I²C bus mode register
ICSR: I²C bus status register
ICIER: I²C bus interrupt enable register
ICDRT: I²C bus transmit data register
ICDRR: I²C bus receive data register
ICDRS: I²C bus shift register
SAR: Slave address register
NF2CYC: NF2CYC register
2.2 Procedure for Setting the Module Used

This section describes the procedure for making initial settings for IIC3. The transfer rate must be set to meet the external specification. In this sample program, $P0/84$ is specified as the transfer rate. Figure 2 shows an example of the initialization sequence for IIC3. For details on the settings of individual registers, see the SH7263/SH7203 Group Hardware Manual (REJ09B0290/REJ09B0313).

![Diagram of Initialization Sequence for IIC3]

Figure 2  Example of the Initialization Sequence for IIC Bus Interface 3
2.3 Operation of the Sample Program

In this sample program, IIC3 is placed in master transmit mode, and reads out 10 bytes of data in sequence from the EEPROM.

The device code employed in this sample program is “B’1010”. Consult the datasheet of the EEPROM you are using for its device code.

The device address employed in this sample program is “B’000”. Consult the datasheet of the EEPROM you are using for its device address.

The memory address indicates the point where reading of EEPROM starts. Each time EEPROM is read, the address is incremented.

Figure 3 shows the operations for sequential reading, and figure 4 shows the operating environment of this sample program.

---

**Figure 3  Operations for Sequential Reading**

**Figure 4  Operating Environment of the Sample Program**
### 2.4 Sequence of Processing by the Sample Program

Table 2 gives the register settings in the sample program. Table 3 shows macro definitions in the sample program. Figures 5 to 10 show the flow of processing by the sample program.

#### Table 2 Register Settings Used in Sample Program

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby control register 5</td>
<td>H'FFFFE</td>
<td>H'00</td>
<td>MSTP54 = &quot;0&quot;: IIC3-3 operates.</td>
</tr>
<tr>
<td>(STBCR5)</td>
<td>0410</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I2C bus control register 1</td>
<td>H'FFFFE</td>
<td>H'E4</td>
<td>ICE = &quot;1&quot;: SCL and SDA pins are placed in the bus-drive state.</td>
</tr>
<tr>
<td>(ICCR1_3)</td>
<td>EC00</td>
<td></td>
<td>RCVD = &quot;1&quot;: Continuous reception is disabled.</td>
</tr>
<tr>
<td>I2C bus mode register</td>
<td>H'FFFFE</td>
<td>H'30</td>
<td>MLS = &quot;0&quot;: MSB-first</td>
</tr>
<tr>
<td>(ICMR_3)</td>
<td>EC02</td>
<td></td>
<td>BCWP = &quot;0&quot;: Allows the writing of values to the BC bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>BC = &quot;B'000&quot;: 9 bits</td>
</tr>
</tbody>
</table>

#### Table 3 Macro Definitions Used in Sample Program

<table>
<thead>
<tr>
<th>Macro Definition</th>
<th>Setting Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM_MEM_ADDR</td>
<td>H'0000</td>
<td>EEPROM start address</td>
</tr>
<tr>
<td>DEVICE_CODE</td>
<td>H'A0</td>
<td>Device code</td>
</tr>
<tr>
<td>DEVICE_ADDR</td>
<td>H'00</td>
<td>Device address</td>
</tr>
<tr>
<td>IIC_DATA_WR</td>
<td>H'00</td>
<td>Write code</td>
</tr>
<tr>
<td>IIC_DATA_RD</td>
<td>H'01</td>
<td>Read code</td>
</tr>
<tr>
<td>IIC3_DATA</td>
<td>10</td>
<td>Data transfer size</td>
</tr>
</tbody>
</table>
Main (main)

START

Initialize transfer source memory

IIC3 initialization
function io_iic3_init

EEPROM data reading
function io_iic3_eeprom_read

END

Note: See figure 2 "Example of the Initialization Sequence for I²C Bus Interface 3".

• The master receive mode is selected, and data are read from EEPROM.

Figure 5  Flow of Processing by the Sample Program (1)
Issue the start condition

- 1st byte: device code, device address, write code
- 2nd byte: memory address (higher-order byte)
- 3rd byte: memory address (lower-order byte)

ACK response?

No

Place in master transmit mode

Issue the start condition

Transmit the slave device address
function io_iic3_address_send

Yes

Issue the start condition

Transmit data
function io_iic3_data_send

ACK response?

No

Issue a stop condition,
place in slave receive mode
function io_iic3_mst_send_end

Yes

Receive data
function io_iic3_data_receive

END

Figure 6 Flow of Processing by the Sample Program (2)
Clear the TEND bit

Place in master receive mode

Clear the TDRE bit

Set the RCVD bit to 1

Read size = 1 byte?

Yes

Set the ACKBT bit to 0

Dummy read

No

Reception of 1-byte data completed?

No

Data read

No

Data end?

Yes

Set the ACKBT bit to 1.

Data read

Set the ACKBT bit to 1.

Dummy read

• Continuous reception is disabled.

• ACK response is set.

• Data are received (8 bytes of data).

• NACK response is set.

• Data are received (Last byte of data but one).

Figure 7 Flow of Processing by the Sample Program (3)
Reception by the I²C Bus Interface 3 Module in Single-Master Operation

• Data are received (last byte of data).

Figure 8  Flow of Processing by the Sample Program (4)
Transmission of the slave device address
(io_iic3_address_send)

START

Transmit Data
function io_iic3_data_send

ACK response?
No

Yes

Transmit data
function io_iic3_data_send

ACK response?
No

Yes

Transmit data
function io_iic3_data_send

ACK response?
No

Yes

return (E_OK)

return (E_ERR)

• 1st byte: device code, device address, write code

• 2nd byte: memory address (higher-order byte)

• 3rd byte: memory address (lower-order byte)

• If no ACK response is received, return the error code.

Figure 9  Flow of Processing by the Sample Program (5)
Data transmission (io_iic3_data_send)

START

Transmit data register empty?

Yes

Set the data to be transmitted

No

Transmission complete?

Yes

ACK response?

Yes

return (E_OK)

No

return (E_ERR)

• Set the data to be transmitted after confirming that the transmit data register is empty.

• Confirm the ACK response after the data have been transmitted.

• If no ACK response is received, return the error code.

Issuing a stop condition, and setting slave receive mode (io_iic3_mst_send_end)

START

Clear the TEND bit to 0
Clear the STOP bit to 0
Issue a stop condition

Bus release?

No

Yes

Place in slave receive mode
Clear the TDRE bit to 0

• I²C bus status register (ICSR_3)
  TEND: Transmit end
  STOP: stop condition detection flag

• Wait for the bus to be released after the stop condition has been issued.

• I²C bus status register (ICSR_3)
  TDRE: Transmit data empty

Figure 10  Flow of Processing by the Sample Program (6)
2.5  Note on Master Receive Mode

If the I²C bus receive data register (ICDRR) is read near the falling edge of the 8th clock cycle, the data will not be received in some cases. In addition, if the reception disable (RCVD) bit in the I²C bus control register 1 is set to 1 near the falling edge of the 8th clock cycle while the receive buffer is full, a stop condition cannot be issued in some cases. To prevent these errors, one of the following two methods should be selected.

In this sample program, the RCVD bit is set to 1 to select data reception in byte units.

1. In master receive mode, reading the ICDRR must proceed before the falling edge of the 8th clock cycle.
2. In master receive mode, the RCVD bit should be set to 1 and the processing should be performed in byte units.

2.6  Note on Master Receive Mode with ACKBT Setting

In master receive mode operation, the ACKBT bit must be set before the falling edge of the 8th clock cycle on pin SCL falls in the final data transfer of consecutive data transfer. Otherwise, an overrun may occur on the slave device.

In the sample program, the RCVD bit is set to 1 to select data transfer in byte units; therefore, this note does not apply to this sample program.
3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```c
/* FILE COMMENT *******************************************************/
* System Name  : SH7263 Sample Program
* File Name  : main.c
* Contents   : Sample program for reception by IIC3 in master receive mode
* Version    : 1.00.00
* Model      : R0K572630D001BR
* CPU        : SH7263
* Compiler   : SHC9.1.1.0
* note       : Data are received from EEPROM using IIC3 in master receive mode.
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* history : 2008.06.05 ver.1.00.00
**FILE COMMENT END******************************************************/
#include <machine.h>
#include "iodefine.h" /* SH7263 iodefine */

/* symbol definition */
declare EEPROM_MEM_ADDR 0x0000
declare DEVICE_CODE 0xA0  /* EEPROM device code :b'1010 */
declare DEVICE_ADDR 0x00   /* EEPROM device address:b'000 */
declare IIC_DATA_WR 0x00   /* Data write code :b'0 */
declare IIC_DATA_RD 0x01   /* Data read code :b'1 */
declare IIC3_DATA 10

declare E_OK 0
#define E_ERR -1
#define HIGH 1
#define LOW 0

/* RAM allocation variable declaration */
unsigned char ReadData[IIC3_DATA];

/* Prototype declaration */
void main(void);
void io_iic3_mst_send_end(void);
int io_iic3_init(void);
int io_iic3_eeprom_read(unsigned char d_code,unsigned char d_adr,unsigned short r_adr,
unsigned int r_size,unsigned char* r_buf);
int io_iic3_data_recieve(unsigned char* r_buf,unsigned int r_size);
int io_iic3_data_send(unsigned char data);
int io_iic3_address_send(unsigned char* data);
```
2. Sample Program Listing: main.c (2)

```c
/*""FUNC COMMENT""******************************************************
* Outline   : Sample program main
*-----------------------------------------------------------------------
* Include   :
*-----------------------------------------------------------------------
* Declaration  : void main(void);
*-----------------------------------------------------------------------
* Function    : Sample program main
*-----------------------------------------------------------------------
* Argument    : void
*-----------------------------------------------------------------------
* Return Value : void
*-----------------------------------------------------------------------
* Notice      :
*""FUNC COMMENT END""**************************************************/

void main(void)
{
    int i;
    /* ==== Clear the data storage location ==== */
    for(i=0; i<IIC3_DATA; i++) {
        ReadData[i] = 0x00;
    }
    /* ==== IIC3 initialization setting ==== */
    io_iic3_init();
    /* ==== Reception by IIC3 in master receive mode ==== */
    io_iic3_eeprom_read(DEVICE_CODE, DEVICE_ADDR, 0x0000, sizeof(ReadData), ReadData);
    while(1){
        /* Loop */
    }
}
```

3. Sample Program Listing: main.c (3)

```c
/*""FUNC COMMENT"***************************************************************
* Outline   : IIC3 module initialization
*-----------------------------------------------------------------------
* Include   : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration  : int io_iic3_init(void);
*-----------------------------------------------------------------------
* Function    : IIC3 module initialization
*-----------------------------------------------------------------------
* Argument    : void
*-----------------------------------------------------------------------
* Return Value : E_OK
*-----------------------------------------------------------------------
* Notice      :
*""FUNC COMMENT END"**********************************************************/
int io_iic3_init(void)
{
    CPG.STCRS5.BIT.MSTP54 = 0u; /* Clear the IIC3_3 module standby mode */
    /* ---- PFC setting ---- */
    PORT.PBCL2.BIT.PB6MD = 1u; /* SCL3 selection */
    PORT.PBCL2.BIT.PB7MD = 1u; /* SDA3 selection */
    /* ----IIC31 module operation disabled ---- */
    IIC33.ICCR1.BIT.ICE = 0u; /* IIC transfer disabled state */
    IIC33.ICCR1.BIT.ICE = 1u; /* IIC3 module operation is enabled */
    IIC33.ICCR1.BIT.RCVD = 0u; /* Continuous reception is to proceed */
    IIC33.ICCR1.BIT.CKS = 4u; /* Transfer rate: Pφ/84(397 kHz) */
    /* ----IIC bus mode register (ICMR) setting --- */
    IIC33.ICMR.BYTE = 0x30u;
    /*
    bit7 : MLS:0 ------------------ MSB first
    bit6 : WAIT:0 ----------------- No WAIT insertion
    bit5-4 : Reserve:1 ------------ Reserve bit
    bit3  : BCWP:0---------------- Unsetting
    bit2-0 : BC0:0, BC1:0,BC0:0----- IIC format 9-bit
    */
    return(E_OK);
}
```
4. Sample Program Listing: main.c (4)

```c
/*""FUNC COMMENT"******************************************************
Outline   : EEPROM data read
---
* Include   : #include "iodefine.h"
---
* Declaration : int io_iic3_eeprom_read(unsigned char d_code,
  unsigned char d_adr,
  unsigned short r_adr,
  unsigned int r_size,
  unsigned char* r_buf);
---
* Function : The amount of data specified by "r_size" are read out from the
   EEPROM specified by device code "d_code" and device address "d_adr",
   and are stored in the area specified by "r_buf".
---
* Argument : unsigned char d_code  : Device code
  unsigned char d_adr   : Device address
  unsigned short r_adr  : Address where data to be read-in
  unsigned int r_size   : Amount of data to be read-in
  unsigned char* r_buf  : Location of data to be read-in
---
* Return Value : With ACK response  : E_OK
  With no ACK response  : E_ERR
---
* Notice :
""FUNC COMMENT END"***************************************************/

int io_iic3_eeprom_read(unsigned char d_code,unsigned char d_adr,unsigned short r_adr,
unsigned int r_size,unsigned char* r_buf)
{
    int ack = E_OK;
    unsigned char send[4];
    send[0] = (unsigned char)(d_code|((d_adr & 0x7)<<1)|IIC_DATA_WR);
    send[1] = (unsigned char)((r_adr>>8) & 0x00ff);
    send[2] = (unsigned char)(r_adr & 0x00ff);
    send[3] = (unsigned char)(d_code|((d_adr & 0x7)<<1)|IIC_DATA_RD);
    while(IIC33.ICCR2.BIT.BBSY == 1u){
        IIC33.ICCR1.BYTE |= 0x30u;       /* Set to master transmission mode */
        IIC33.ICCR2.BYTE=((IIC33.ICCR2.BYTE & 0xbfu) | 0x80u);  /* Issue the start condition */
        ack = io_iic3_address_send(send);  /* Transmit the first, second, and third bytes of data */
        if(ack == E_OK){
            /* ACK response is received from the specified device */
            if(ack == E_OK){
                /* Transmit the fourth byte of data */
                io_iic3_data_send(send[3]);
            } else{
                /* Data reception */
                io_iic3_data_recieve(r_buf,r_size);
            }
        } else{
            /* ACK response is not received from the specified device */
        }
    }
    return(ack);
}
```
### 5. Sample Program Listing: main.c (5)

```c
int io_iic3_data_recieve(unsigned char* r_buf,unsigned int r_size)
{
    int i;
    unsigned char dummy;
    IIC33.ICSR.BIT.TEND = 0u;  /* Clear bit TEND */
    IIC33.ICCR1.BIT.TRS = 0u;  /* Master receive mode */
    IIC33.ICSR.BIT.TDRE = 0u;  /* Clear bit TDRE */
    IIC33.ICCR1.BIT.RCVD = 1u; /* Disable continuous reception */
    if(r_size == 1){         /* When one byte of data is received */
        IIC33.ICIER.BIT.ACKBT = 1u;   /* Acknowledge setting "H" */
        dummy = IIC33.ICDRR;     /* Dummy read */
    }else{
        IIC33.ICIER.BIT.ACKBT = 0u;   /* Acknowledge setting "L" */
        dummy = IIC33.ICDRR;     /* Dummy read */
        for(i=0;i<r_size - 2;i++){
            while(IIC33.ICSR.BIT.RDRF == 0u){
                /* Waiting for reception of one byte of data */
                *r_buf++ = IIC33.ICDRR;    /* Data read */
            }
        }
        IIC33.ICIER.BIT.ACKBT = 1u; /* Acknowledge setting "H" */
        *r_buf++ = IIC33.ICDRR;    /* Next to last byte of data */
    }
    while(IIC33.ICSR.BIT.RDRF == 0u){
        /* Waiting for reception of one byte of data */
        IIC33.ICSR.BIT.STOP = 0u;     /* Clear the STOP flag */
        IIC33.ICCR2.BYTE &= 0x3fu;   /* Issue a stop condition */
        while(IIC33.ICSR.BIT.STOP == 0u){
            /* Waiting for generation of a stop condition */
        }
        *r_buf = IIC33.ICDRR;        /* Last byte of data */
        IIC33.ICCR1.BIT.RCVD = 0u;   /* Clear bit RCVD */
        IIC33.ICCR1.BYTE &= 0xcfu;   /* Slave receive mode */
    }
    return(E_OK);
}
```
6. Sample Program Listing: main.c (6)

```c
/****FUNC COMMENT******************************************
* Outline : Transmission of the slave device address
*-----------------------------------------------------------------------
* Include :
*-----------------------------------------------------------------------
* Declaration : int io_iic3_address_send(unsigned char* data);
*-----------------------------------------------------------------------
* Function : Transmission of the slave device address specified by “data” (one byte)
* and the memory address (two bytes)
*-----------------------------------------------------------------------
* Argument : unsigned char* data : Transmit data
*-----------------------------------------------------------------------
* Return Value : With ACK response : E_OK
* : With no ACK response : E_ERR
*-----------------------------------------------------------------------
* Notice :
****FUNC COMMENT END******************************************/

int io_iic3_address_send(unsigned char* data)
{
  int ack;

  ack = io_iic3_data_send(*data++); /* Slave device address */
  if(ack == E_ERR){
    return(ack);
  }
  ack = io_iic3_data_send(*data++); /* 1st part of memory address */
  if(ack == E_ERR){
    return(ack);
  }
  ack = io_iic3_data_send(*data);    /* 2nd part of memory address */
  if(ack == E_ERR){
    return(ack);
  }
  return(ack);
}

/****FUNC COMMENT******************************************
* Outline : Transmission of one byte of data
*-----------------------------------------------------------------------
* Include : #include "iodefine.h"
*-----------------------------------------------------------------------
* Declaration : int io_iic3_data_send(unsigned char data);
*-----------------------------------------------------------------------
* Function : Data are transmitted according to the following procedure.
* : 1.Wait for ICDRT to become empty.
* : 2.Set the data to be transmitted.
* : 3.Check completion of data transmission.
* : 4.Check the ACK response.
*-----------------------------------------------------------------------
* Argument : unsigned char data : Data for transmission
*-----------------------------------------------------------------------
* Return Value : With ACK response : E_OK
* : With no ACK response : E_ERR
*-----------------------------------------------------------------------
* Notice :
****FUNC COMMENT END******************************************/
```
int io_iic3_data_send(unsigned char data)
{
    int ack;

    while(IIC33.ICSR.BIT.TDRE == 0x0){
        /* Wait for ICDRT to become empty. */
    }

    IIC33.ICDRT = data;

    while(IIC33.ICSR.BIT.TEND == 0x00){
        /* Wait for completion of data transmission */
    }

    if(IIC33.ICIER.BIT.ACKBR == 0){
        ack = E_OK;
    }
    else{
        ack = E_ERR;
    }

    return(ack);
}

void io_iic3_mst_send_end(void)
{
    IIC33.ICSR.BIT.TEND = 0u;  /* Clear the TEND flag */
    IIC33.ICSR.BIT.STOP = 0u;  /* Clear the STOP flag */
    IIC33.ICCR2.BYTE &= 0x3fu; /* Issue a stop condition */

    while(IIC33.ICSR.BIT.STOP == 0u){
        /* Wait for bus release */
    }

    IIC33.ICCR1.BYTE &= 0xcfu; /* Slave receive mode */
    IIC33.ICSR.BIT.TDRE = 0u; /* Clear bit TDRE */
}

/* End of File */
4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7203 Group Hardware Manual (REJ09B0313)
  The most up-to-date version of this document is available on the Renesas Technology Website.
  SH7263 Group Hardware Manual (REJ09B0290)
  The most up-to-date version of this document is available on the Renesas Technology Website.
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