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## R8C/25 Group

### Reading Standards When Using Power-On Reset Function and Voltage Monitor 0 Reset

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#### 1. Abstract

This document describes how to read standard values when using the power-on reset function and voltage monitor 0 reset.

#### 2. Introduction

The standard values described in this document are applied to the following MCU and parameter(s):

- MCU: R8C/25 Group

### 3. Standard Value Description

#### 3.1 Power-ON Reset Function

When the  $\overline{\text{RESET}}$  pin is connected to VCC via a pull-up resistor of approximately 5 k $\Omega$  and VCC voltage rises, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFRs.

When a capacitor is connected to the  $\overline{\text{RESET}}$  pin, always hold the voltage to the  $\overline{\text{RESET}}$  pin at 0.8 VCC or more. Figure 3.1 shows a Power-On Reset Circuit Example.

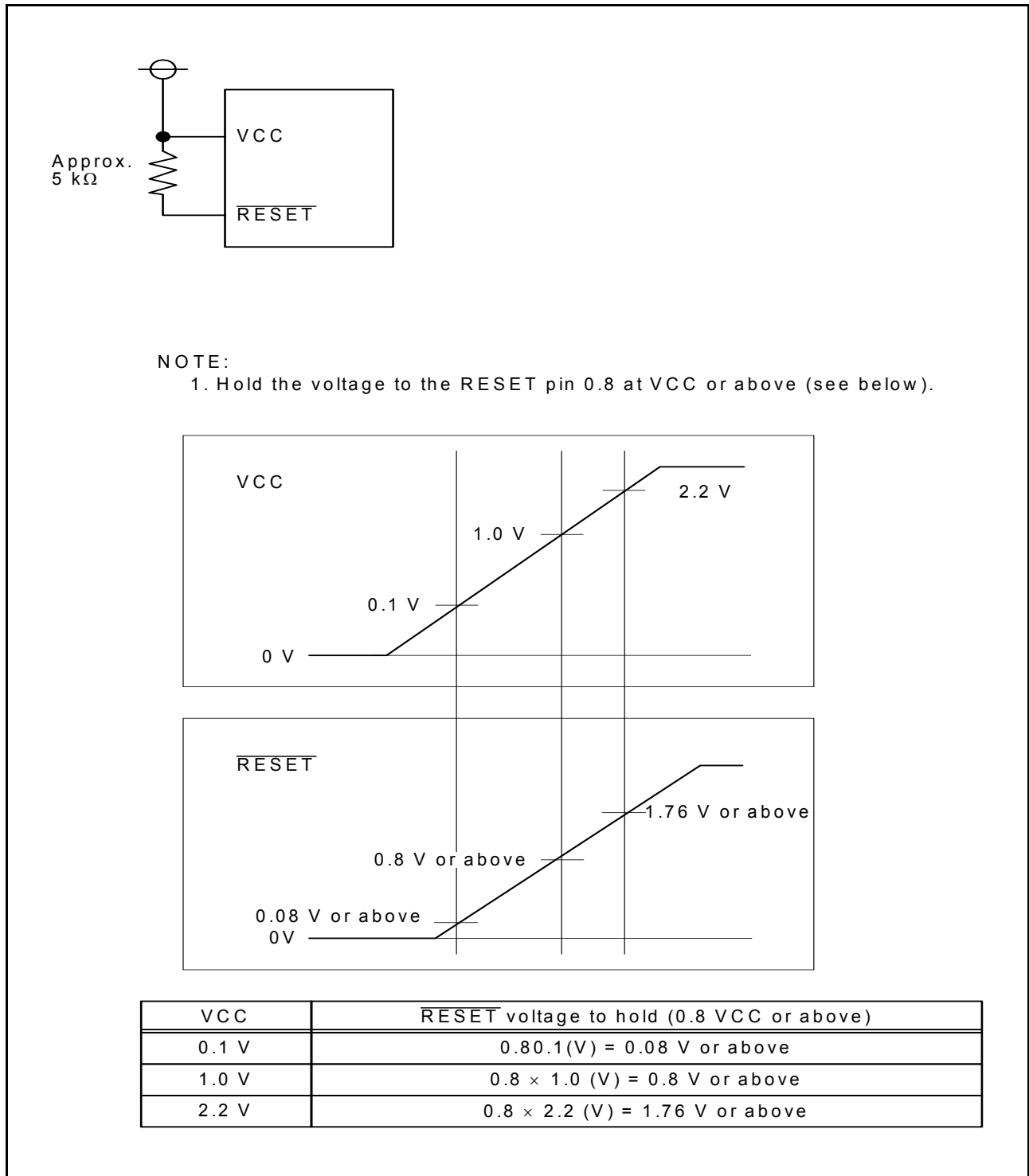


Figure 3.1 Power-On Reset Circuit Example

### 3.2 Voltage Transition Patterns and Operating Functions

Figure 3.2 shows the Voltage Transition Patterns and Operating Functions, and Table 3.1 shows the Electrical Characteristics of Power-On Reset Circuit and Voltage Monitor 0 Reset.

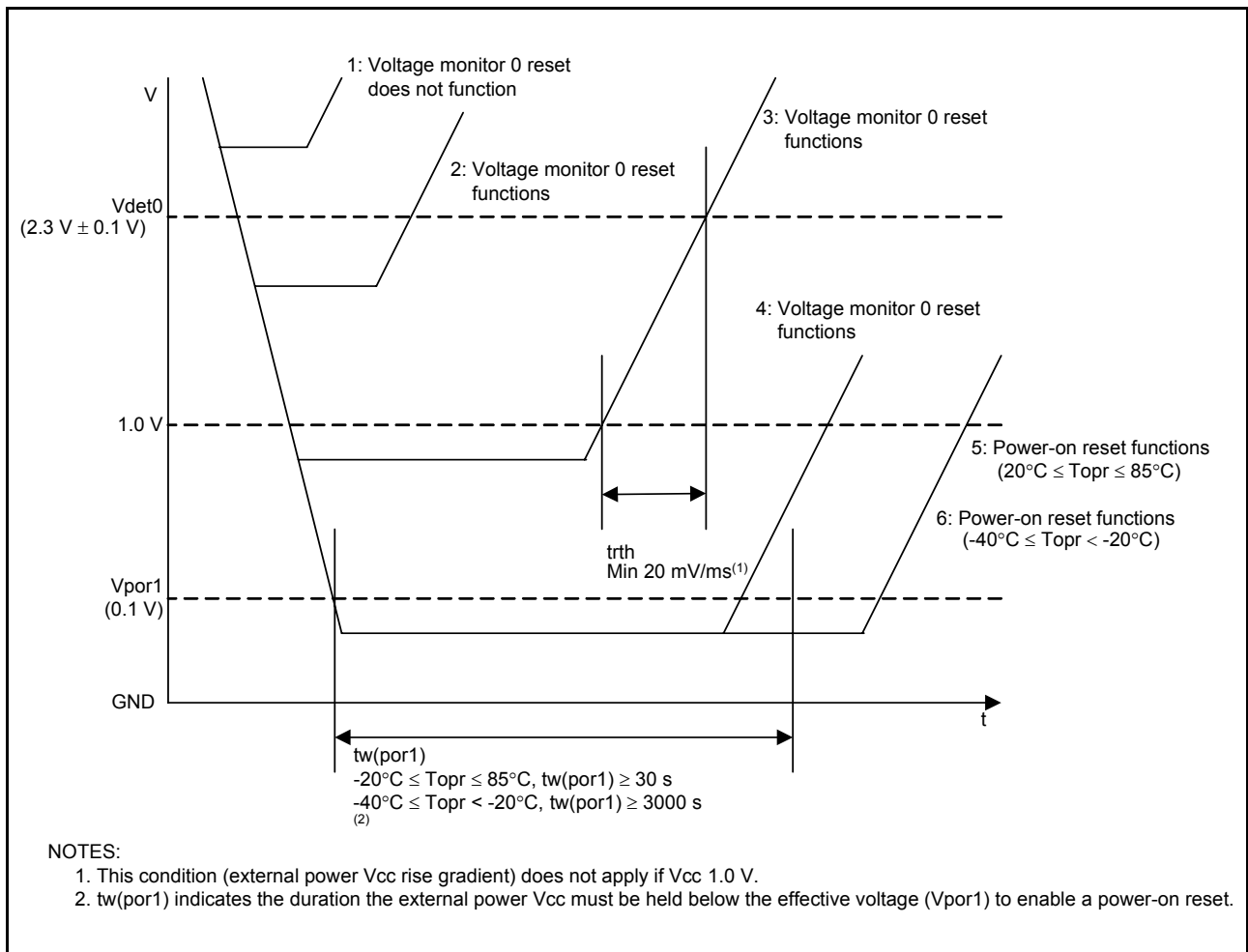


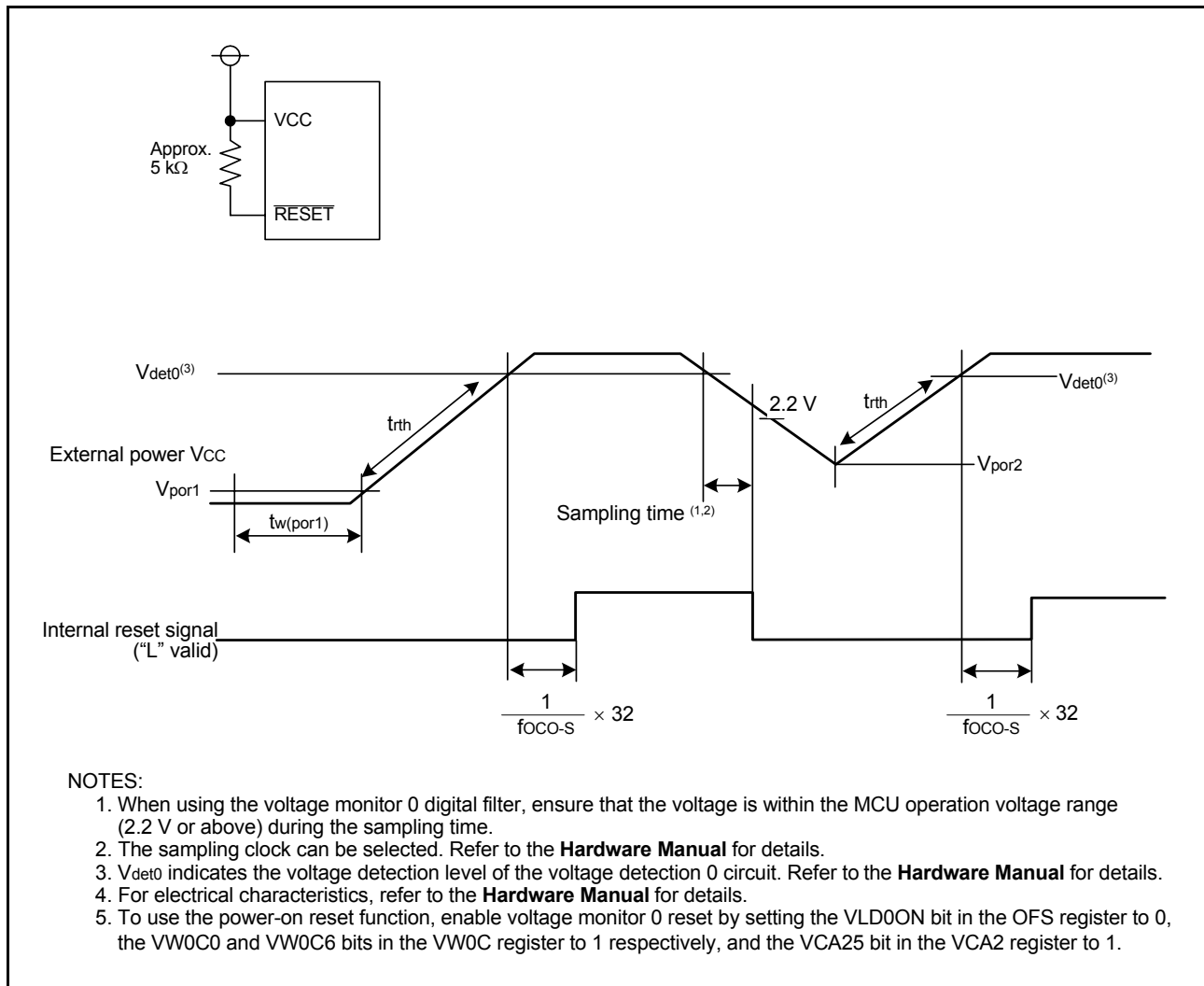
Figure 3.2 Voltage Transition Patterns and Operating Functions

**Table 3.1 Electrical Characteristics of Power-On Reset Circuit and Voltage Monitor 0 Reset**

Symbol	Parameter	Condition	Standard			Unit	Pattern in Fig.3.2
			Min	Typ.	Max.		
$V_{por1}$	Power-on reset valid voltage <sup>(4)</sup>		-	-	0.1	V	4, 5, 6
$V_{por2}$	Power-on reset circuit or voltage monitor 0 reset valid voltage		0	-	Vdet0	V	
$t_{rth}$	External power Vcc rise gradient <sup>(2)</sup>		20	-	-	mV/ msec	2, 3

**NOTES:**

1. The measurement condition is  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version) /  $-40$  to  $85^{\circ}\text{C}$  (D version) unless otherwise specified.
2. This condition (external power Vcc rise gradient) does not apply if  $V_{cc} \geq 1.0$  V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the VLD0ON bit in the OFS register to 0, the VW0Co and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4.  $t_{w(por1)}$  indicates the duration the external power Vcc must be held below the effective voltage ( $V_{por1}$ ) to enable a power-on reset. When turning on the power for the first time, maintain  $t_{w(por1)}$  for 30 s or more if  $-20^{\circ}\text{C}$ , maintain  $t_{w(por1)}$  for 3,000 s or more if  $-40^{\circ}\text{C} \leq T_{opr} < -20^{\circ}\text{C}$ .



**Figure 3.3 Example of Power-On Reset Circuit and Operation**

#### 4. Reference Document

Hardware Manual

R8C/25 Group Hardware Manual

The latest version can be downloaded from the Renesas Technology website.

Technical News/Technical Update

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REVISION HISTORY	R8C/25 Group Reading Standards When Using Power-On Reset Function and Voltage Monitor 0 Reset
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