RE01 256KB Group

Hardware Design Guide

R01AN5490EJ0100
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Summary

This application note has been written to help engineers to design hardware using the RE01 256KB group products.

Target Device

•RE01 256KB group

Table of Contents

1. Introduction

1.1 About This Manual

This manual is the hardware design guide for the RE01 256KB group products. For detail product functions, refer to the document for Table 1-1.

Table 1-1 List of Related Documents

Document Type	Description	Document Name	Document No.
UMH (Hardware Edition of the User's Manual)	Specification description of the RE01 256KB group products	RE01 Group (with 256Kbyte Flash Memory) User's Manual: Hardware	R01UH0894
UM (User's Manual)	E2 emulator connection explanation when using RE01	E2 emulator, E2 emulator Lite Additional Document for User's Manual (Notes on Connection of RE Devices)	R20UT4582

This manual describes the processing of pins to set startup modes in chapter 1, the power supply pin processing in chapter 2, the clock, reset, and processing of other pins in chapter 3, and the processing when using EHC in chapter 4.

1.2 Features of MCU

This MCU incorporates an energy harvesting control circuit (EHC). The EHC starts operation from before reset cancellation upon connection with a power generation element, and uses the current generated by the power generation element to charge a storage capacitor and a secondary battery, as well as supplying a power supply to the internal VCC/IOVCC of the MCU. When the amount of current generated by the power generation element is less than the current consumption of the MCU, operation can be continued using the charged storage capacitor and secondary battery. For details, refer to section 14.3, Operation, in the UMH.

This MCU is provided with a back bias voltage control function employing SOTB™ process technology that enables low-leakage current operation. It is possible to transition to this low-leakage current operation mode (VBB OPE) immediately after energy harvesting startup. For details, refer to chapter 13, Power-Saving Functions, in the UMH.

1.3 List of Pins

This manual describes the processing of the following pins in particular. The pin details are given in the sections shown in Table 1-2.

Table 1-2 List of Pins

Type	Pin Name	Section No.														
		1.4 1.5	2.1 2.2	2.3	2.4	3.1	3.2	3.3	4.2	4.3	4.4	4.5	4.6	4.7	4.8	4.9
Mode selection	MD	○	-	-	-	-	-	○	-	-	-	-	-	-	○	-
	EHMD	○	-	-	-	-	-	○	-	-	-	-	-	-	-	-
Power supply system	VCC/IOVCC	-	○	○	○	-	○	○	○	-	-	-	○	○	-	○
	VSC_VCC	-	○	-	-	-	-	-	○	○	-	○	○	○	-	○
	VCC_SU	-	○	-	-	-	-	-	○	○	-	○	○	○	-	○
	VBAT_EHC	-	○	-	-	-	-	-	○	○	○	-	○	○	-	○
	IOVCC0/1	-	○	○	-	-	-	○	○	-	-	-	○	○	-	-
	AVCC0	-	○	○	-	-	-	○	○	-	-	-	○	○	-	-
	VREFH0	-	○	○	-	-	-	○	○	-	-	-	○	○	-	-
	VCL	-	○	-	-	-	-	-	-	-	-	-	-	-	-	-
	VCLH	-	○	-	-	-	-	-	-	-	-	-	-	-	-	-
	VBN	-	○	-	-	-	-	-	-	-	-	-	-	-	-	-
	VBP	-	○	-	-	-	-	-	-	-	-	-	-	-	-	-
Clock	EXTAL	-	-	-	-	○	-	○	-	-	-	-	-	-	-	-
	XTAL	-	-	-	-	○	-	○	-	-	-	-	-	-	-	-
	XCIN	-	-	-	-	○	-	-	-	-	-	-	-	-	-	-
	XCOUT	-	-	-	-	○	-	-	-	-	-	-	-	-	-	-
Reset	RES#	○	-	-	-	-	○	○	-	-	-	-	-	-	-	○
Boot mode	RXD9_A	-	-	-	-	-	-	-	-	-	-	-	-	-	○	-
	TXD9_A	-	-	-	-	-	-	-	-	-	-	-	-	-	○	-
Debugging	SWCLK	-	-	-	-	○	-	-	-	-	-	-	-	-	-	○
	SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	○
Other	Other pins	-	-	-	-	○	-	○	-	-	-	-	-	-	-	-

1.4 Startup Mode Types and Mode Selection

Various startup modes can be set for this MCU, determined by specific input pin settings upon reset cancellation. The MCU startup mode is determined by the combination of the MD and EHMD pin levels.

Table 1-3 indicates the relationship between the levels of the startup mode setting pins (MD, EHMD) at the time of reset cancellation and the startup mode selected at that time. Regardless of the mode upon startup, operation is started with the internal flash memory enabled.

Table 1-3 Selection of Startup Mode Using Mode Setting Pin and Energy Harvesting Setting Pin

Mode Setting Pin		Startup Mode
MD	EHMD	
High	High	Energy harvesting startup mode
	Low	Normal startup mode
Low	-	SCI boot mode

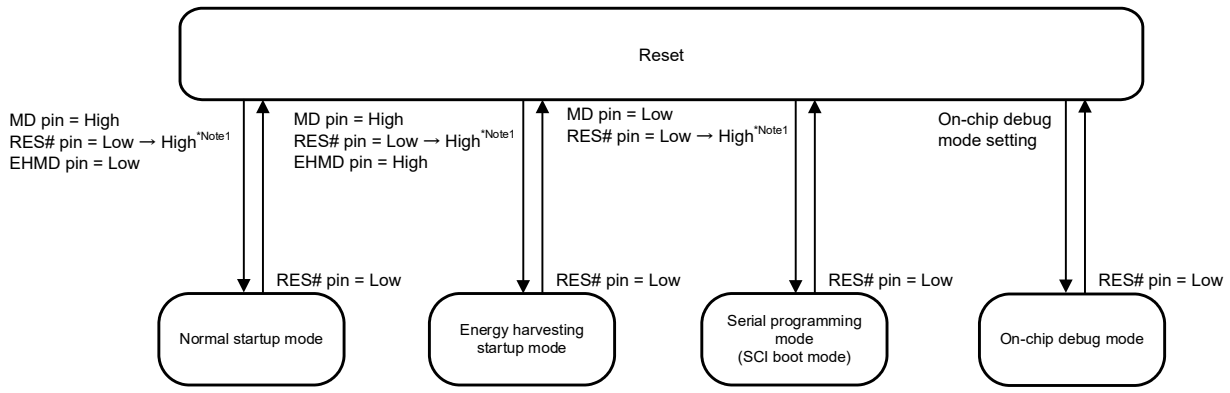
Table 1-4 shows the input pins to control startup modes.

Table 1-4 Input Pins to Control Startup Modes

Pin Name	I/O	Function
MD	Input	Mode setting pin. The signal level at this pin should not be changed during startup mode transition upon reset cancellation.
EHMD	Input	Energy harvesting mode setting pin

1.5 Startup Mode Transitions Using Mode Setting Pins

Figure 1.1 shows a state transition diagram for startup mode transitions using the MD and EHMD pin settings.



Note 1. Low level should continue to be applied to RES# pin for the period of RES# pulse width specified in section 51, Electrical Characteristics, in the UMH.

Figure 1.1 Pin Levels and Startup Modes for Mode Setting Pins and Energy Harvesting Pins

2. Power Supplies

This chapter describes the types of power supply pins, the capacitors that are required for correct operation, power supply allocation to modules, and power supply domains.

2.1 Power Supply Voltage Pins

Table 2-1 is a list of the power supply voltage pins for this MCU.

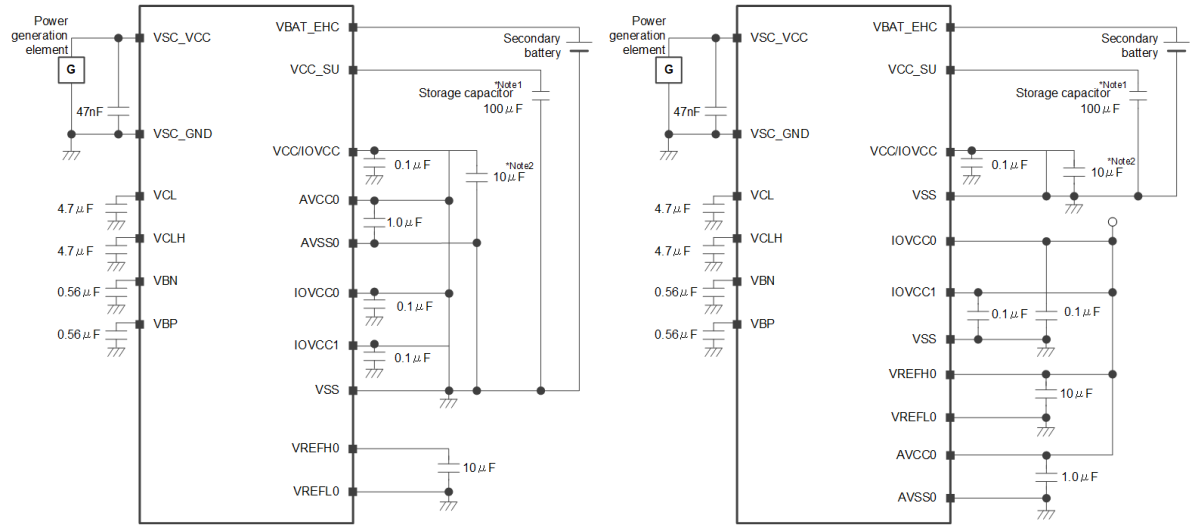
Table 2-1 Power Supply Voltage Pins

Intended Use	Pin Name	Function
Power supply	VCC/IOVCC	Power supply pin
	VSS	Ground pin
Internal power supply stabilization	VCL	Pin to stabilize the internal power supply
	VCLH	Pin to stabilize the internal power supply
Back bias	VBN	Pin to stabilize the back-bias voltage
	VBP	Pin to stabilize the back-bias voltage
Energy harvesting	VSC_VCC	Power supply pin to which power is supplied from a power generation element
	VSC_GND	Ground pin for VSC_VCC
	VCC_SU	Power supply pin to which power is supplied from a storage capacitor
	VBAT_EHC	Power supply pin to which power is supplied from a secondary battery
I/O power supply	IOVCC0/1	Power supply pins for I/O
Analog power supply	AVCC0	Analog power supply pin for a 14-bit A/D converter, reference voltage generation circuit, or temperature sensor
	AVSS0	Ground pin for AVCC0
	VREFH0	Analog reference voltage pin for the 14-bit A/D converter
	VREFL0	Analog reference ground pin for the 14-bit A/D converter

2.2 Capacitors for Connection to Power Supply Pins

In order to reduce noise, capacitors must be connected to the power supply pins. Figure 2.1 shows examples for reference.

When using EHC (Reference Voltage Generation Circuit is used)



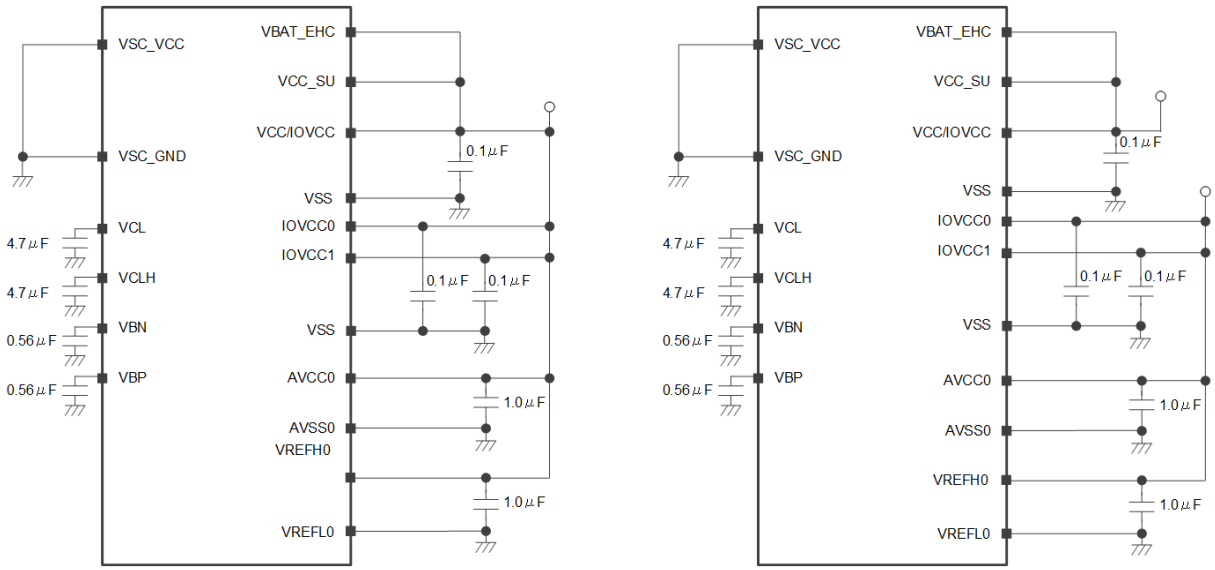
Note 1. For the storage capacitor value, refer to the capacitance values of the storage capacitor in the VCC_SU side shown in Table 51.43, EHC Characteristics in the UMH.

Note 2. The capacitance should be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.

Connections with VCC/IOVCC and other power supply pins at same potential

Connections with VCC/IOVCC and other power supply pins at different potentials

Normal operation (Reference Voltage Generation Circuit is not used)



Connections with VCC/IOVCC and other power supply pins at the same potential

Connections with VCC/IOVCC and other power supply pins at different potentials

Figure 2.1 Examples of Capacitor Connections to Power Supply Pins

2.3 Power Supply Allocation to Modules

This MCU can independently set the voltage for each power supply. Power supplies in addition to VCC/IOVCC include AVCC0, AVSS0, VREFH0, VREFL0, IOVCC0, and IOVCC1. Table 2-2 shows module allocations for each power supply. For details on power supplies corresponding to each I/O pin, the “Applicable Power Supplies” columns in Tables 1.15 to 1.7 in section 1.7, List of Pins, in the UMH.

Table 2-2 Module Allocations for Each Power Supply Pin

Power Supply Pin	Module
VCC/IOVCC	Other than modules listed below
AVCC0	14-bit A/D converter(P000 – P007), temperature sensor, reference voltage generation circuit
AVSS0	
IOVCC0	I/O functions that are allocated to port 8
IOVCC1	I/O functions that are allocated to port 1, 3, 5, 6, and 7, and P202 to P205

If any power supply is unused and there is no supply of power, a module not being supplied with power may cause an undefined value to propagate to a circuit of a module that is operating. Hence the power supply open control register (VOCR) should be set so as to suppress the effect of such occurrences. For details, refer to section 13.2.22 VOCR: Power Supply Open Control Register, in the UMH.

2.4 Power Supply Domains

In this MCU, the power supply supplied from the VCC/IOVCC pin is divided into four domains within the chip, and by controlling the power supply for each domain, a reduction of the device power consumption is made possible.

As indicated in Table 2-3, the four domains are AWO domain, and ISO1 to ISO3 domains. To reduce power consumption, the power supply can be disabled for each of ISO1 to ISO3 domains. For details, refer to chapter 13, Power-Saving Functions, in the UMH.

Table 2-3 Modules for Each Power Supply Domain

Function Category	Power Domain Function Category			
	AWO Domain	ISO1 Domain	ISO2 Domain	ISO3 Domain
CPU	-	CPU	-	-
Power supply system	Power-on reset circuit (POR) Low-voltage detection circuit 0 (LVD0) Low-voltage detection circuit 1 (LVD1) Low-voltage detection circuit BAT (LVDBAT) Back-bias voltage control (VBBC) Energy harvesting control (EHC)	-	-	-
Memory	-	RAM	-	Flash memory
Clock	Sub-clock oscillator (SOSC) Clock correction circuit (CCC)	Main clock oscillator (MOSC) Middle-speed on-chip oscillator (MOCO) low-speed on-chip oscillator (LOCO) IWDT-dedicated oscillator (IWDTLOCO) Main clock oscillator stop detection function Clock output function	High-speed on-chip oscillator (HOCO)	-
Peripheral function	Realtime Clock (RTC) Wakeup timer (WUPT)	Data transfer controller (DTC) DMA controller (DMAC) Memory protection unit (MPU) Interrupt controller (ICU) Event link controller (ELC) Asynchronous General Purpose Timers n : 16 bit (AGTn (n = 0, 1)) Asynchronous General Purpose Timers n : 32 bit (AGTWn (n = 0, 1)) Independent watchdog timer (IWDT) SysTick timer Serial communication interface 0 (SCI0) I2C bus interface 0 (IIC0) MIP LCD controller (MLCD) Key interrupt function (KINT) Low-speed clock timer (LST)	Other functions	-
Analog function	-	-	14-bit A/D converter (ADC14) Temperature Sensor (TSN) Reference voltage generation circuit (VREF)	-
Pin interrupt	NMI pin IRQ0_DS to IRQ3_DS pins	IRQ0 to IRQ9 pins	-	-

3. Topics Common to Normal and EHC Operation

This chapter describes clock generation circuits, reset, and pin processing.

3.1 Clock Generation Circuits

This MCU can use various clock signals. Table 3-1 indicates the clock types in this MCU. For details, refer to chapter 9, Clock Generation Circuit, in the UMH.

Table 3-1 Clock Types

Connection	Clock Name	Connection Pin	Clock Source	Frequency
External connection	Main clock oscillator (MOSC)	EXTAL, XTAL	Resonator	8 MHz to 32 MHz
		EXTAL	External clock input	32 MHz max.
	Sub-clock oscillator (SOSC)	XCIN, XCOUT	Resonator	32.768 kHz
	JTAG external clock input (TCK)	TCK	External clock input	10 MHz max.
	SWD external clock input (SWCLK)	SWCLK	External clock input	12.5 MHz max.
On-chip	High-speed on-chip oscillator (HOCO)	-	-	24/32/48/64 MHz
	Middle-speed on-chip oscillator (MOCO)	-	-	2 MHz
	Low-speed on-chip oscillator (LOCO)	-	-	32.768 kHz
	IWDT-dedicated on-chip oscillator (IWDTLOCO)	-	-	16 kHz

3.1.1 Main Clock Oscillator

There are two methods for supplying a clock signal to the main clock oscillator.

- Connect an oscillator
- Connect an external clock signal input

○ Method of connecting a resonator

An example of connection of a resonator is shown in Figure 3.1.

A damping resistor (Rd) can be added to the circuit as necessary. The resistor value will differ depending on the specification of the resonator and the oscillation driving capability, and so the value recommended by the resonator manufacturer should be used. If the manufacturer specifies that a feedback resistor (Rf) should be added externally, the resistor Rf should be inserted between EXTAL and XTAL as per the manufacturer's instruction.

As indicated in Table 3-1, when a resonator is connected to supply a clock signal, the resonator frequency should be within the range of oscillation frequencies of the main clock oscillator.

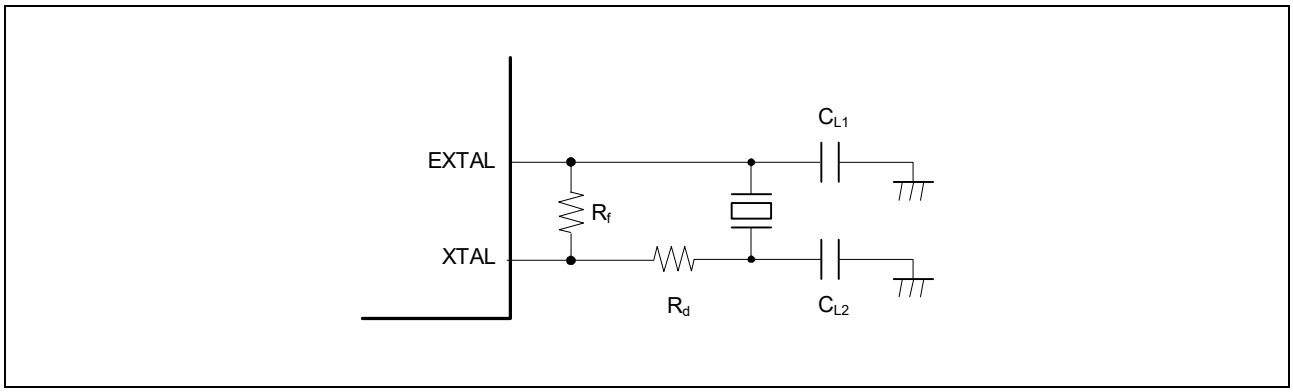


Figure 3.1 Connection Example of Resonator

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown is Figure 3.2 to prevent electromagnetic induction from interfering with correct oscillation.

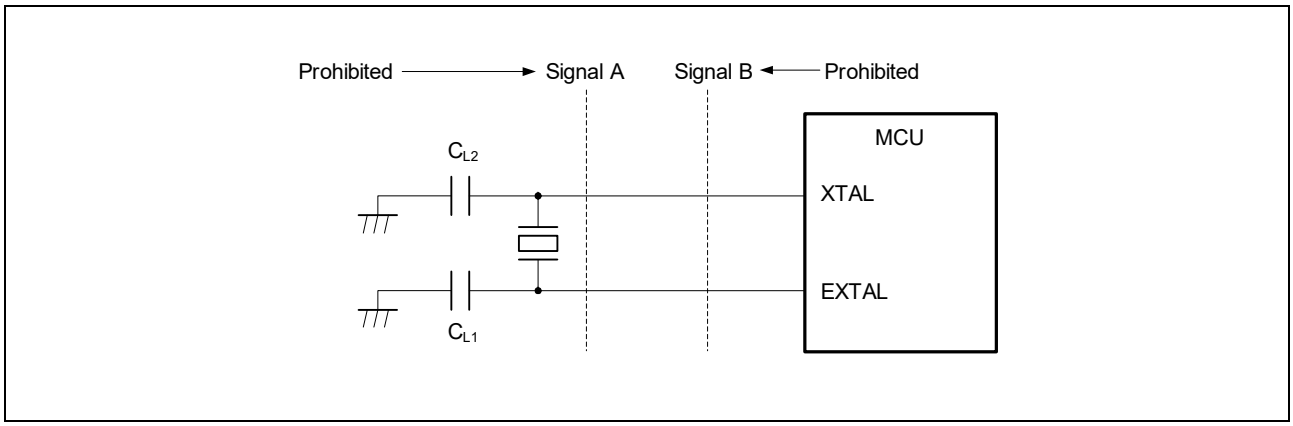


Figure 3.2 Precautions Relating to Board Design of Oscillation Circuit

○ External clock input method

Figure 3.3 shows an example for connecting an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin becomes high impedance.

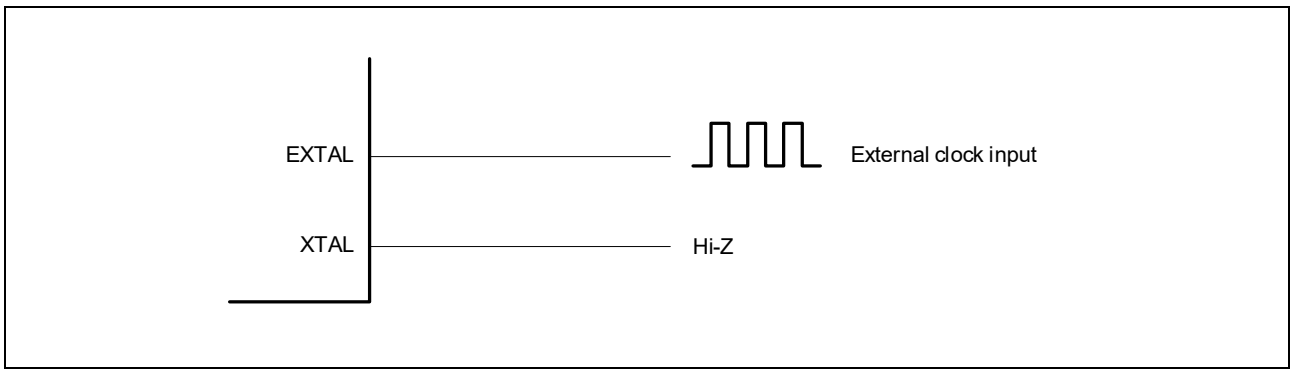


Figure 3.3 External Clock Equivalent Circuit

○ Notes on external clock input

The frequency of the external clock input can only be changed when the main clock oscillator is stopped. Do not change the frequency of the external clock input when the setting of the Main Click Oscillator Stop bit (MOSCCR.MOSTP) is 0.

3.1.2 Sub-Clock Oscillator

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

○ Method of connecting a 32.768 kHz crystal resonator

In order to supply a clock signal to the sub-clock oscillator, a 32.768 kHz crystal resonator is connected as shown in Figure 3.4. A damping resistor (Rd) can be inserted as necessary. The resistor value differs depending on the resonator and the oscillation driving capability, and so the value recommended by the resonator manufacturer should be used. When the resonator manufacturer recommends use of an external feedback resistor (Rf), Rf should be inserted between XCIN and XCOUT according to the manufacturer instructions.

As indicated in Table 3-1, when connecting a resonator to supply a clock signal, the frequency of the resonator should be within the range of oscillation frequencies of the sub-clock oscillator.

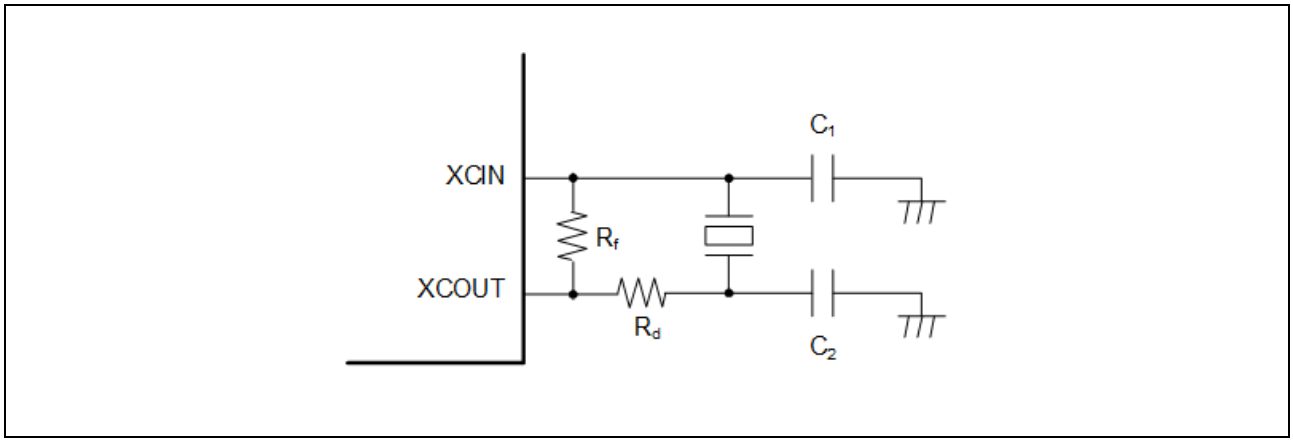


Figure 3.4 Connection Example of 32.768 kHz Crystal Resonator

○ Pin processing when the sub-clock oscillator is not used

When the sub-clock oscillator is not used, the XCIN pin should be connected to VSS (pulled down) via a resistor, and the XCOUT pin should be left open, as shown in Figure 3.5. In addition, when the oscillator is not connected, the sub-clock oscillator stop bit (SOSCCR.SOSTP) should be set to 1 to stop the oscillator.

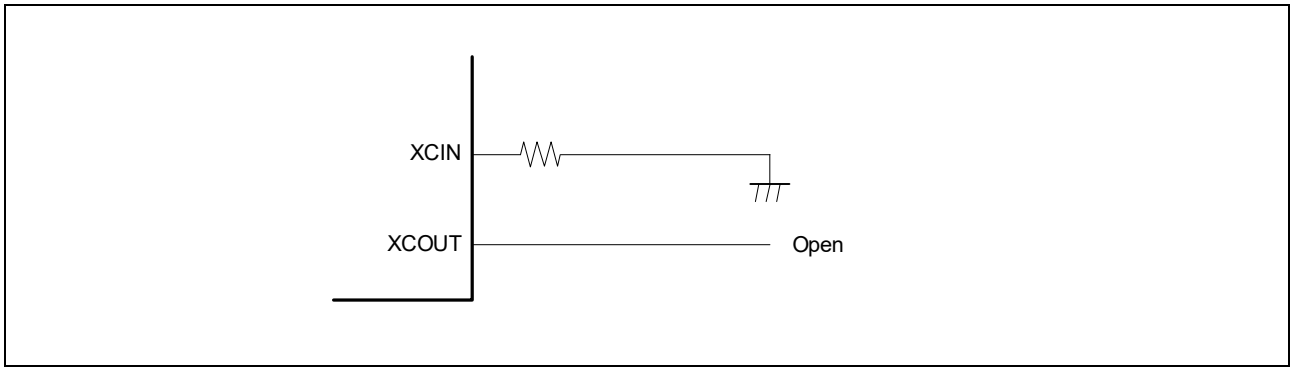


Figure 3.5 Pin Processing When Sub-Clock Oscillator is Not Used

3.1.3 Trace Design

This section explains important points to minimize the risk of erroneous operation due to noise when connecting a crystal resonator. This explanation is for the sub-clock circuit, but similar considerations apply when using a crystal resonator with the main clock circuit.

○ Points on XCIN and XCOUT Wiring

(1) to (6) below describe points on wiring for XCIN and XCOUT. Figure 3.6 shows an example of preferred trace for XCIN and XCOUT wiring. Figure 3.7 shows an example of alternate trace for XCIN and XCOUT wiring.

(1) Do not cross the XCIN and XCOUT wires with other signal wires.
(2) Do not add an observation pin to XCIN and XCOUT.
(3) Make the XCIN and XCOUT wire width between 0.1 and 0.3 mm. The wire length from the MCU pins to the crystal resonator pins should be less than 10 mm, or at least as close to 10 mm as possible if longer.
(4) The wire connected to the XCIN pin and the wire connected to the XCOUT pin should have as much space between them (at least 0.3 mm) as possible.
(5) Connect external capacitors as close together as possible. Connect the wire for the capacitors to the ground trace (hereinafter referred to as ground shield) on the component side. For details, see the points on the ground shield. When the capacitors cannot be laid out as shown in Figure 3.6, use the layout shown in Figure 3.7.
(6) In order to decrease the parasitic capacitance between XCIN and XCOUT, include a ground trace between the resonator and the MCU.

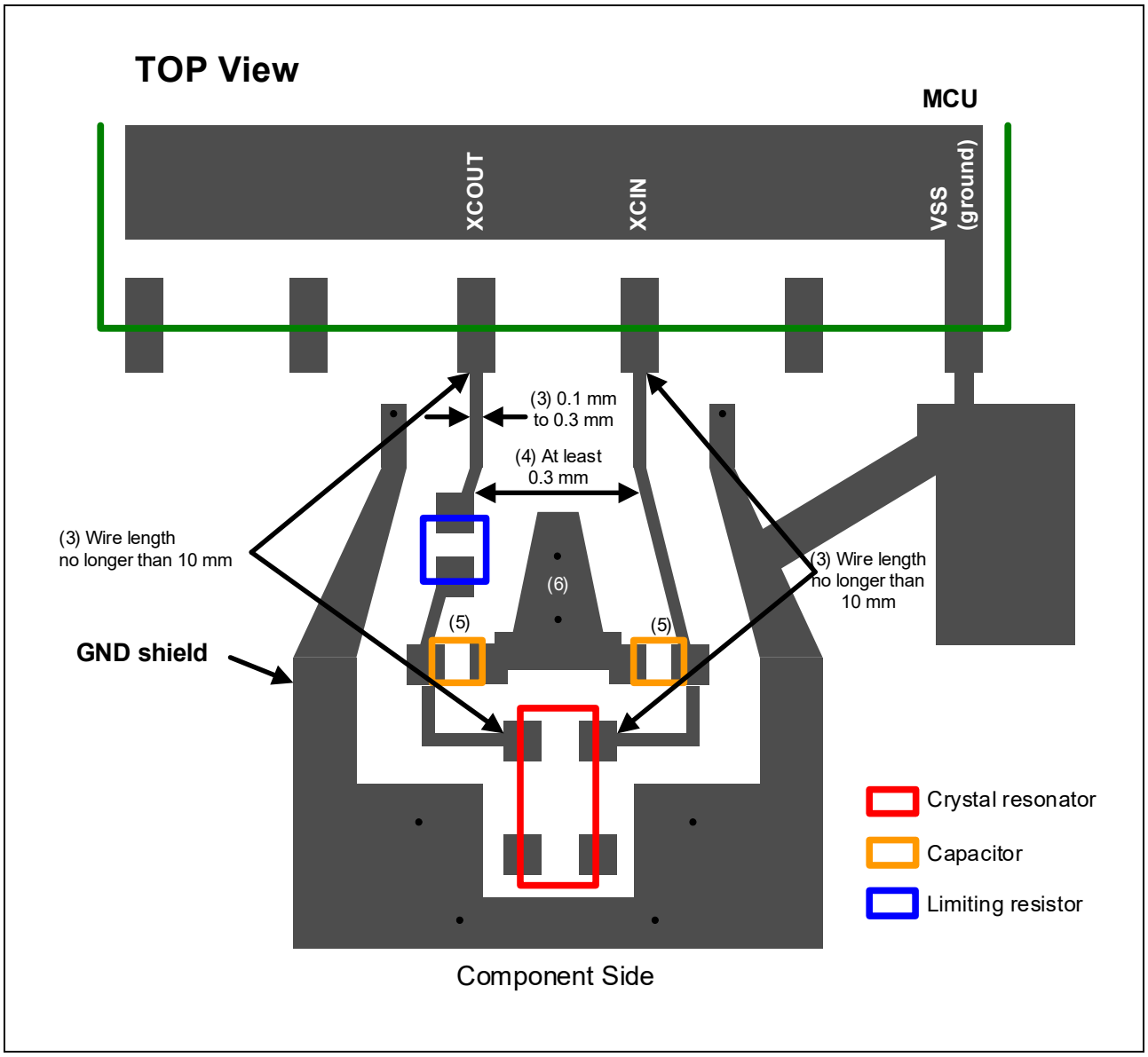


Figure 3.6 Example of Preferred Trace for XCIN and XCOUT Wiring

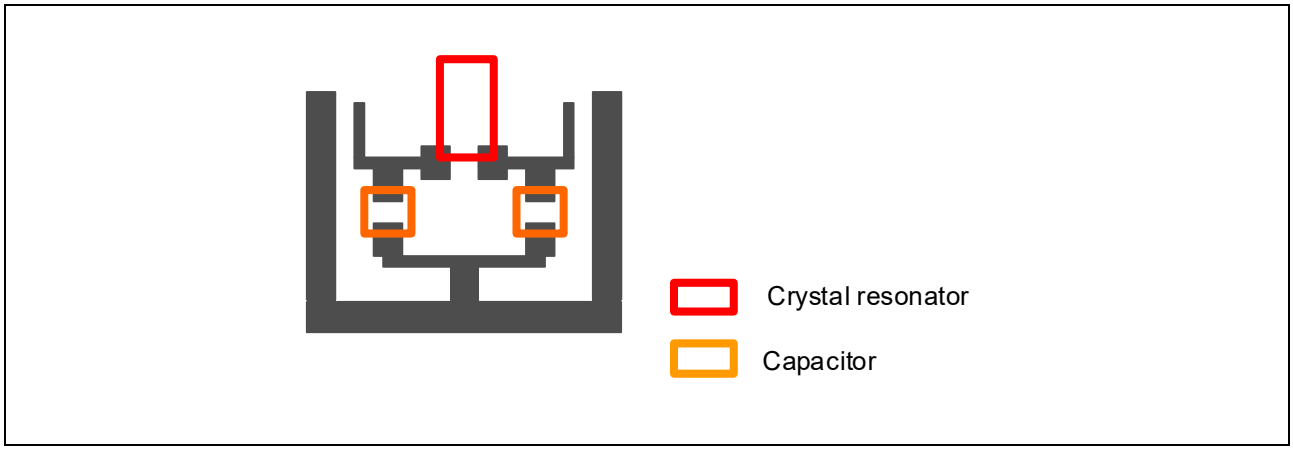


Figure 3.7 Example of Alternate Trace for XCIN and XCOUT Wiring

○ Points Regarding the Ground Shield

Shield the crystal resonator with a ground trace. (1) to (4) below describe the points regarding the ground shield, and Figure 3.8 shows a trace example.

(1) Lay out the ground shield on the same layer as the crystal resonator wiring.
(2) Wire the ground shield as close to the VSS pin on the MCU as possible, and ensure that the wire width is at least 0.3 mm.
(3) To prevent current from running to the ground shield, branch the ground shield and the ground on the board near the VSS pin on the board.
(4) Make the ground shield wire width at least 0.3 mm, and leave a 0.3 to 2.0 mm gap in between wires. Do not cross the XCIN and XCOUT wires with other signal wires.

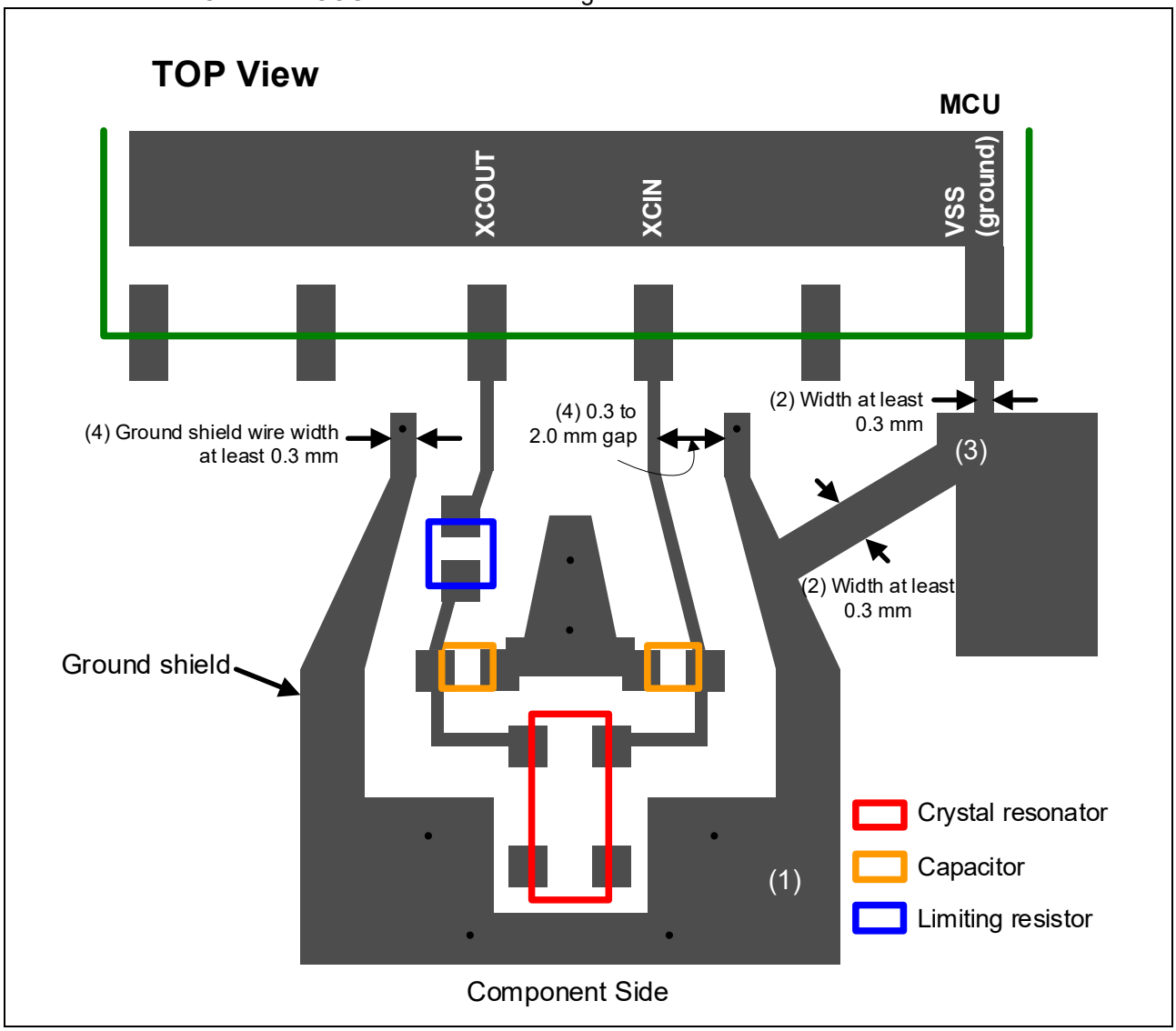


Figure 3.8 Trace Example for the Ground Shield

○ Points Regarding the Bottom Ground

For boards that are at least 1.2 mm thick, lay out a ground trace on the solder side (hereinafter referred to as bottom ground) of the crystal resonator area (see Figure 3.9).

(1) through (3) describe points when making a multilayered board that is at least 1.2 mm thick, and Figure 3.9 shows a trace example.

(1) Do not lay out any traces in the middle layers of the crystal resonator area. Do not lay out power supply and ground traces in this area. Do not pass signal wires through this area either.
(2) Make the bottom ground at least 0.1 mm bigger than the ground shield. Connect the bottom ground on the solder side only to the ground shield on the component side before connecting it to the VSS pin.
(3) Connect the ground shield terminator to the bottom ground.

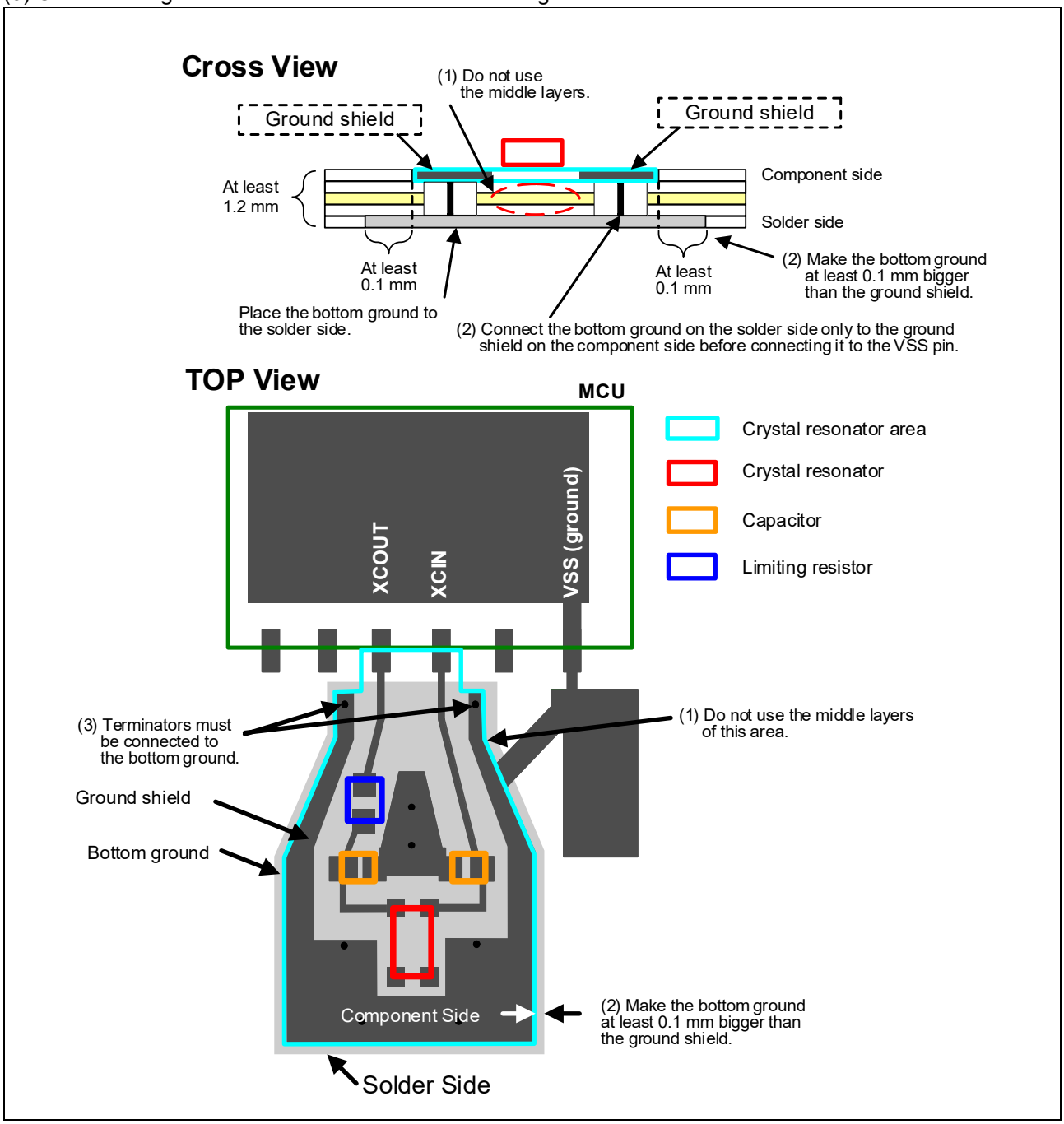


Figure 3.9 Trace Example When a Multilayered Board is at Least 1.2 mm Thick

When making a multilayered board that is less than 1.2 mm thick, do not lay out any traces to layers other than the component side for the crystal resonator area. Do not lay out power supply and ground traces in this area. Do not pass signal wires through this area either. Figure 3.10 shows a trace example.

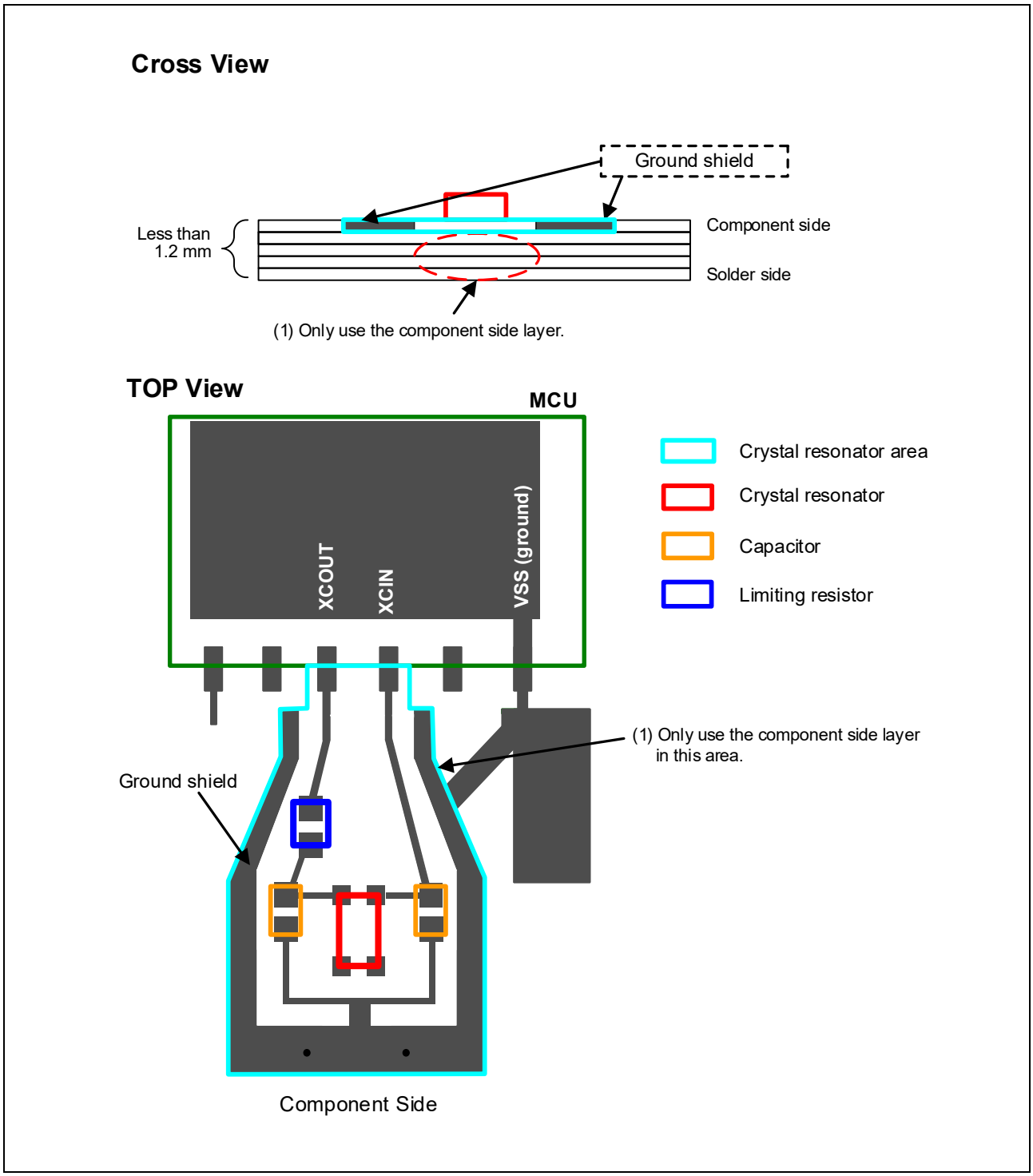


Figure 3.10 Trace Example When a Multilayered Board is Less Than 1.2 mm Thick

○ Other Points

(1) to (4) below describe other points, and Figure 3.11 shows a trace example.

(1) Do not place the XCIN and XCOUT wires near wires that have large changes in current.
(2) Do not run the XCIN and XCOUT wires parallel to other signal wires like those for adjacent pins.
(3) Pin wiring that runs adjacent to the XCIN and XCOUT pins should not just be laid out outside the MCU. Lay out the wiring through the bottom side of the MCU first and then lay out the wiring to an area away from the XCIN and XCOUT pins (to avoid the wiring from laying out the wiring parallel with the XCIN and XCOUT wiring).
(4) Lay out as much of the ground trace on the bottom side of the MCU as possible.

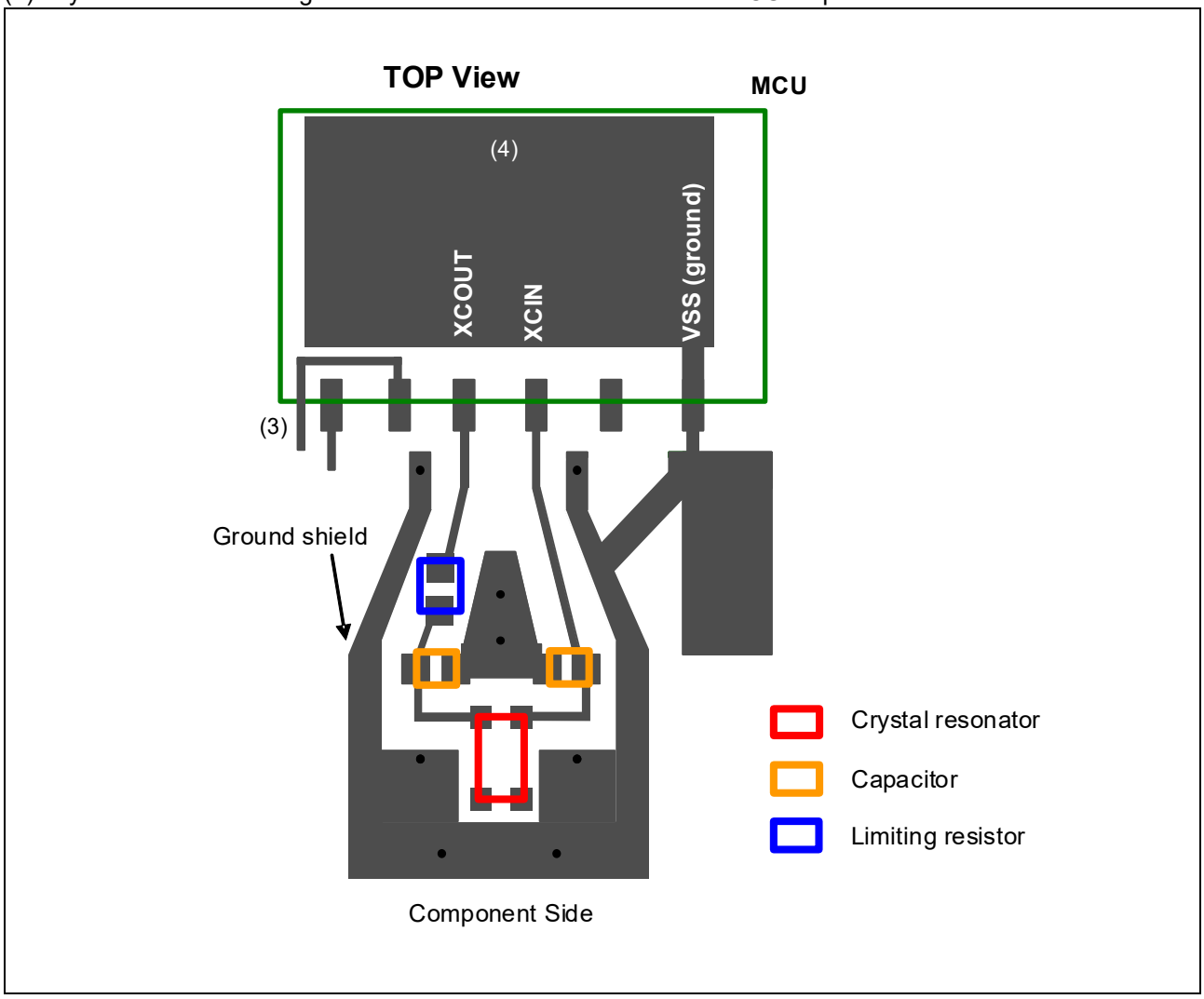


Figure 3.11 Trace Example for Other Points

○ Points on Wiring the Main Clock Resonator

Shield the main clock resonator wiring with a ground. Do not connect the ground shield for the main clock and sub-clock together. Note that if the main clock ground shield is connected directly to the sub-clock ground shield, there is a possibility that noise from the main clock resonator may transfer through and affect the sub-clock. Figure 3.12 shows a trace example.

[Reference Diagram]

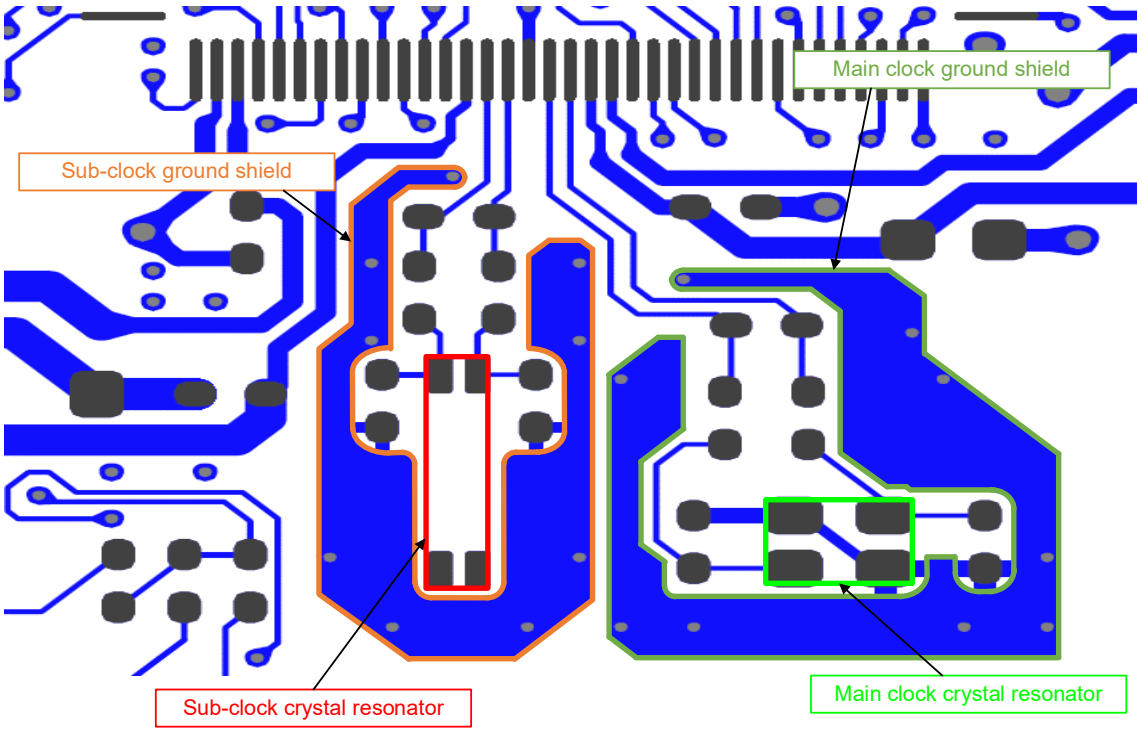


Figure 3.12 Trace Example When Shielding the Main Clock Resonator Wiring with Ground

○ Trace Example Showing a High Risk of incorrect Operation Due to Noise

Do not lay out traces described in (1) through (9). Laying out the traces below may cause the low CL resonator to not oscillate correctly. Figure 3.13 shows a trace example.

(1) XCIN and XCOUT wires cross other signal wires (risk of incorrect operation).
(2) Observation pins are attached to XCIN and XCOUT (risk of oscillation stopping).
(3) XCIN and XCOUT wires are long (risk of erroneous operation or decreased accuracy).
(4) The ground shield does not cover the entire area, and where there is a ground shield, the wiring is long and narrow (easily affected by noise, and there is a risk that accuracy will decrease from the ground potential difference generated by the MCU and external capacitor).
(5) Ground shield is not detached near VSS pin (risk of incorrect operation from MCU current flowing to the ground shield).
(6) Power supply or ground trace are under the XCIN and XCOUT wiring (risk of losing the clock or oscillation stopping).
(7) A wire with a large-current is routed nearby (risk of incorrect operation).
(8) Parallel wiring for adjacent pins is close and long (risk of losing the clock or oscillation stopping).
(9) The middle layers are used (risk of oscillation characteristics decreasing or signals operating incorrectly).

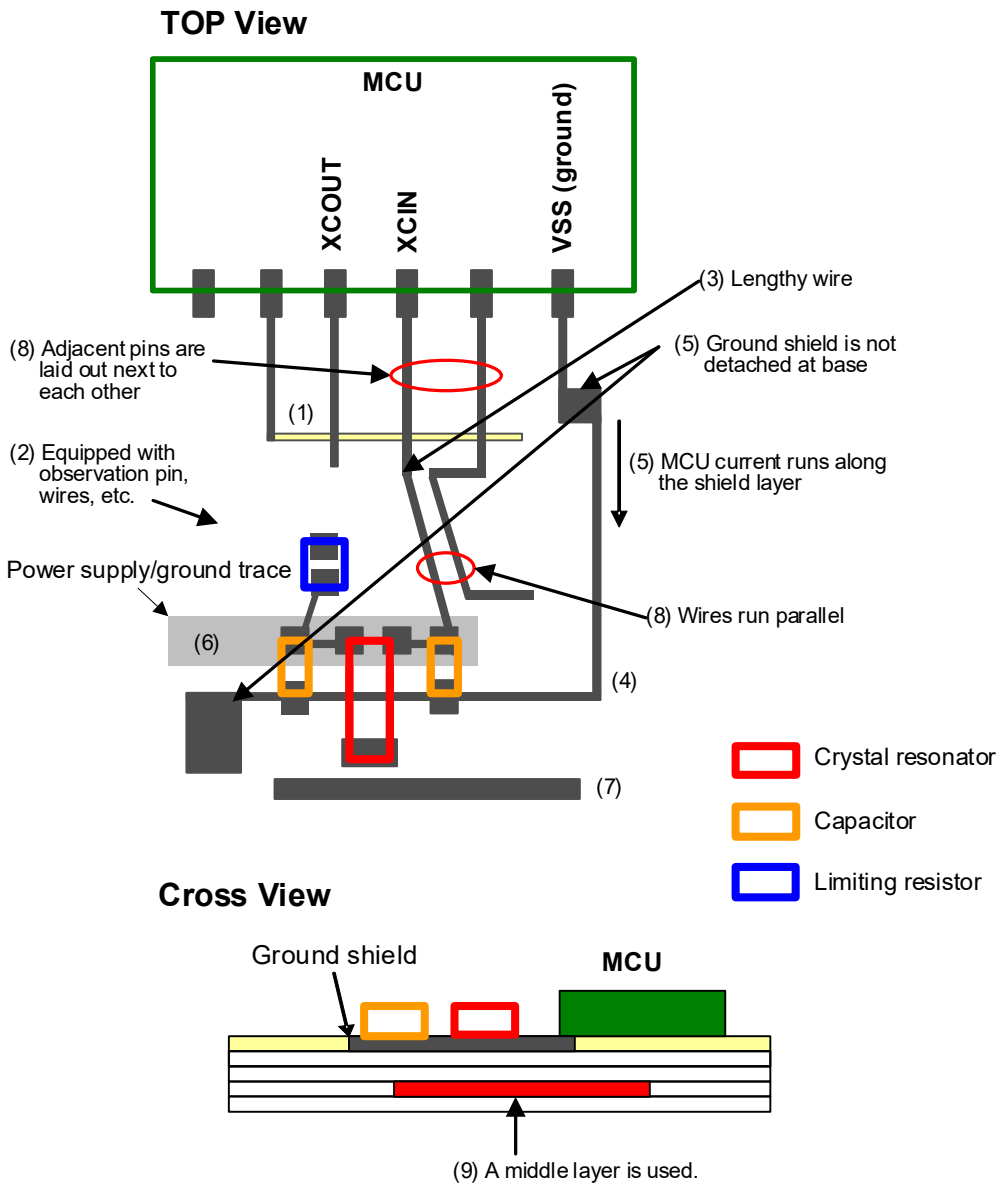


Figure 3.13 Trace Example Showing High Risk of incorrect Operation Due to Noise

3.1.4 Reference Oscillation Circuit Constants and Verified Resonator Operation

Table 3-2 lists the reference oscillation circuit constants for the verified resonator operation, and Figure 3.14 shows a trace example of the verified resonator operation.

Table 3-2 Reference Oscillation Circuit Constants for the Verified Resonator Operation

Manufacturer	Seiko Instruments Inc.
Product	SSP-T7-FL
SMD/With Leads	SMD
Frequency (kHz)	32.768
Sub-clock oscillation mode	Low CL drive capability
Load capacity CL (pF)	3.7
Load capacity Cg (pF) (1)	5.0
Load capacity Cd (pF) (2)	3.0
Oscillation stabilization time (sec)	-
Motional resistance (kΩ)	70 max

Note 1. When using this resonator, contact Seiko Instruments Inc. for details on matching (https://www.sii.co.jp/en/).

Note 2. A low CL resonator is recommended for a sub-clock oscillator.

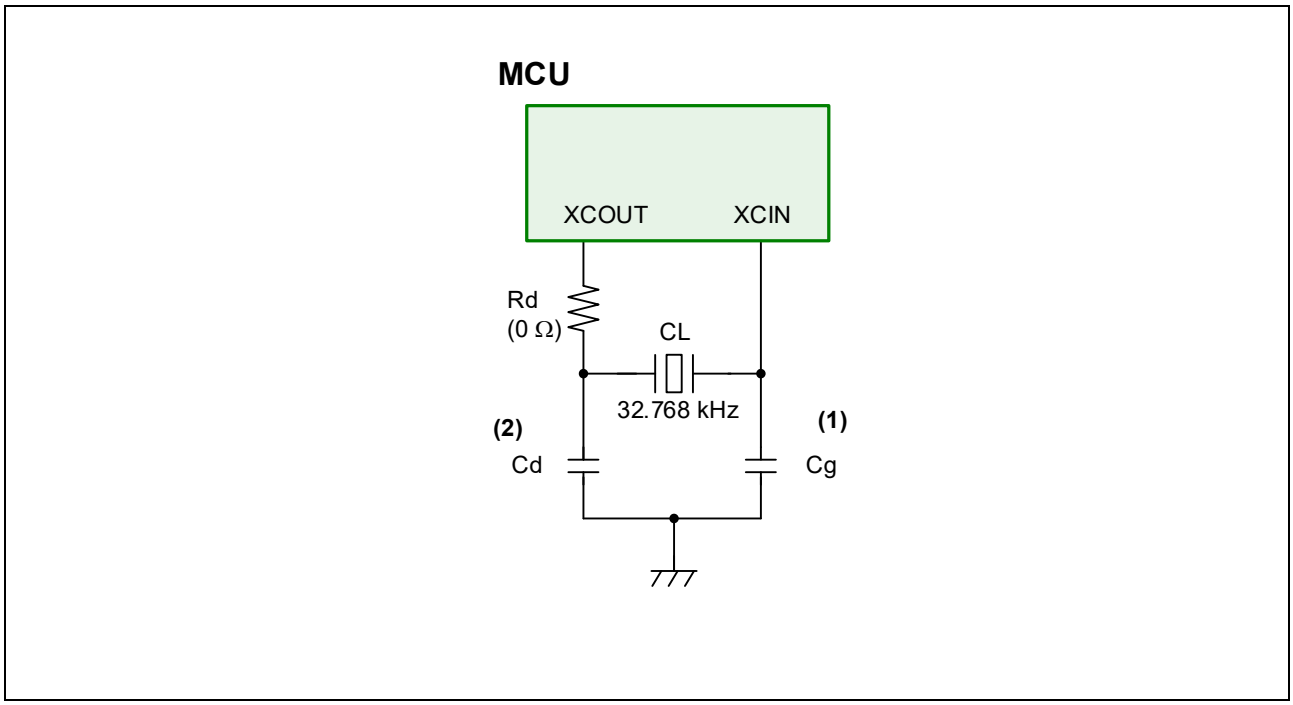


Figure 3.14 Trace Example for Verified Resonator Operation

The verified resonator operation and reference oscillation circuit constants listed here are based on information from the resonator manufacturer and not guaranteed. As reference oscillation circuit constants are measurements surveyed under fixed conditions by the manufacturer, values measured in the user system may vary. To achieve the optimum reference oscillation circuit constants for use in the actual user system, inquire with the resonator manufacturer to perform an evaluation on the actual circuit.

The conditions in the figure are conditions for oscillating the resonator connected to the MCU and are not operating conditions for the MCU itself. Refer to the specifications in the electrical characteristics for details on the MCU operating conditions.

3.2 Reset

This section describes a reset.

3.2.1 Overview of Reset

A reset is enabled using the reset pin. Refer to Tables 6.1 to 6.4 in section 6.1, Overview, in the UMH.

Table 3-3 shows an I/O pin related to the reset function.

Table 3-3 I/O Pin Related to Reset Function

Pin Name	I/O	Function
RES#	Input	Reset pin

3.2.2 POR Reset on Startup

Power-on reset is an internal reset by a power-on reset circuit. It occurs under the following conditions.

- When a power supply is turned on with the RES# pin set to high
- When, with the RES# pin set to high, the VCC/IOVCC voltage falls below the voltage detection level (VPOR) of the power-on reset circuit

When, during power-on reset, the VCC/IOVCC voltage exceeds the VPOR voltage, after a power-on reset time has elapsed, the CPU begins the reset exception processing. The power-on reset time is time for the power supply to stabilize and for this MCU to enter stable operation.

In a state in which RES# is connected to VCC/IOVCC with a resistor interposed, when the power supply is turned on, power-on reset is generated。

When using power-on reset, the RES# pin should be connected to the VCC/IOVCC pin with a resistor interposed both for normal operation and when using EHC. A capacitor need not be connected to the RES# pin, but even when a capacitor is connected to the RES# pin, the voltage at the RES# pin should always be kept at VIH or higher (see Table 3-4). When connecting the board power supply and each of the power supply pins in common, adequate consideration is necessary to ensure that power-on reset occurs upon startup. The circuit configuration is as indicated below. Power-on reset should be used when using EHC.

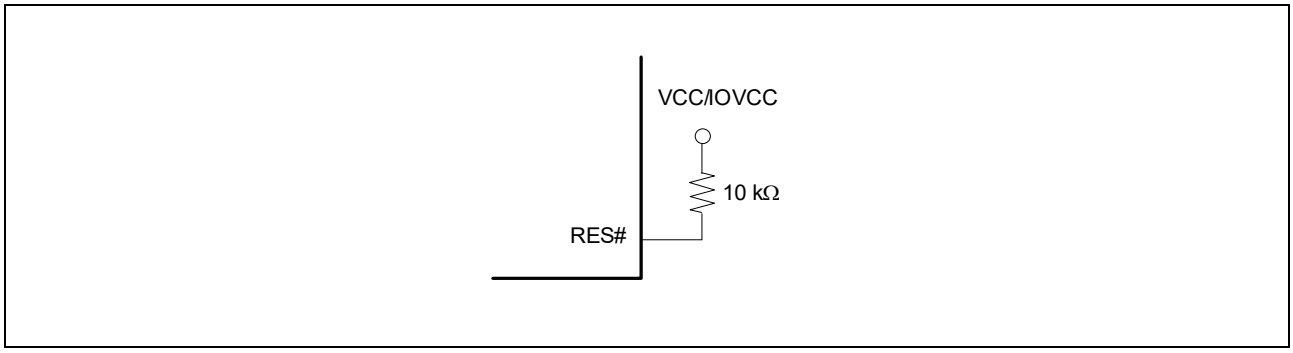


Figure 3.15 Circuit Configuration Example of Power-On Reset

Table 3-4 RES# Reset Detection Level

Pin	Symbol	Min	Typ	Max	Unit	Measurement Condition
RES#	V_{IH}	VCC x 0.8	-	-	V	-

Figure 3.16 shows a circuit configuration example of the reset pin. Figure 3.17 shows a trace example of the reset pin (when using the multilayered board).

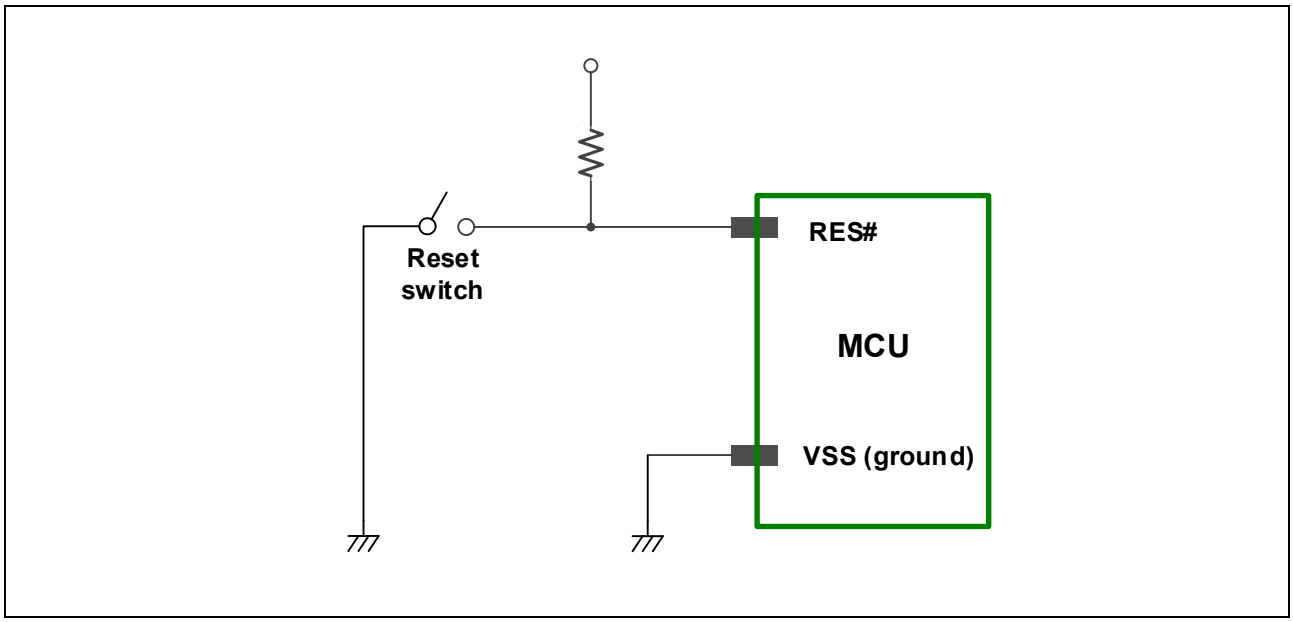


Figure 3.16 Circuit Configuration Example of Reset Pin

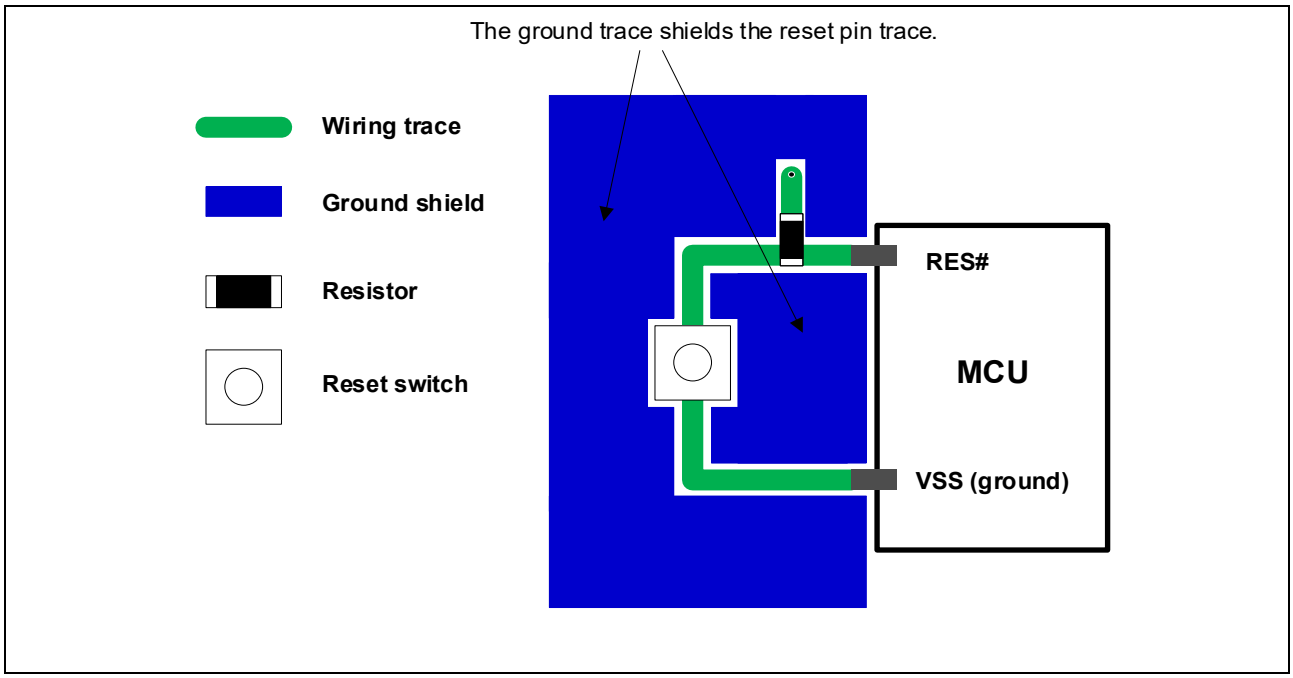


Figure 3.17 Trace Example of Reset Pin (Using Multilayered Board)

3.3 Pin Processing

This section describes the processing method for each pin. Notes on the processing are provided below. For details, refer to section 1.5, Pin Functions, in the UMH.

3.3.1 Pins from Which Initial Value is Output

Table 3-5 indicates pins from which an initial value is output, and the output values. A summary of the I/O ports is given in "22.1 Overview" of the UMH.

Table 3-5 Pins from Which Initial Value is Output

Pin Name	Initial Value
P208	Low output
P209	Low output
P210	High output
P409	Low output
P410	High output

3.3.2 Pull-Up Pin Processing

Pull-up pins should be connected to pins selected from among power supply pins (VCC/IOVCC, IOVCC0/1, and AVCC0) in order to equalize voltage levels. As an example, port 4 may use a pull-up connection to the VCC/IOVCC pin, and port 6 may have a pull-up connection to IOVCC1. For details, refer to the Applicable Power Supply columns in Table 1.15 that describes the corresponding power supply pins in section 1.7, Pin Lists, in the UMH. Moreover, in order that pull-up pins do not become sources of leaks, prior to chip startup the pull-up pins should not be set to high level.

3.3.3 Processing of Unused Pins

In this MCU, there are pins which, if unused, require processing. Refer to section 22.4, Handling of Unused Pins, in the UMH.

Table 3-6 shows how to process unused pins.

Table 3-6 Processing of Unused Pins

Pin Name	Description
P201/MD	(Used as a mode pin)
EHMD	Connected to VSS
RES#	Connected to VCC via a resistor (pull-up)
P200/NMI	Connected to VCC via a resistor (pull-up)
P412/EXTAL	When the main clock oscillator is not used, the MOSCCR.MOSTP bit is set to 1 (the general-purpose port P412). When this pin is not used as the port P412, it is connected to VSS via a resistor (pull-down).
P413/XTAL	When the main clock oscillator is not used, the MOSCCR.MOSTP bit to 1 (the general-purpose port P413). When this pin is not used as the port P413, it is left open.
Ports 0 to 8	When this pin is set to an input (PCNTR1.PDRn = 0), the corresponding pin is connected to VCC via a resistor (pull-up) or to VSS via a resistor (pull-down).(Note 1) When this pin is set to an output (PCNTR1.PDRn = 1), the corresponding pin is left open. (Note 1) (Note 2)
VREFH	Connected to AVCC0 This pin can be left open when power is not supplied to AVCC0.
VREFL	Connected to AVSS0 This pin can be left open when power is not supplied to AVCC0.
BSCANP	When the boundary scan function is not used, this pin is connected to VSS.

Note 1. The PmnPFS.PMR, PmnPFS.ISEL, and PmnPFS.ASEL bits should be set to 0. For details, refer to section 22.2.6 PmnPFS : Port mn Pin Function Select Register (m = 0 to 8; n = 00 to 15), in the UMH.

Note 2. When a pin is set to output and left open, during the interval from reset cancellation until the pin is in the output state, the port is in the input state. Hence while the port is in the input state, the voltage level of the pin is indeterminate, and in some cases the power supply current will increase.

3.3.4 Pin Processing for Serial Communication Interface

For the pin processing when using the smart card interface mode for serial communication interface, refer to section 32.6.1, Example Connection, in the UMH.

4. EHC

This chapter describes the EHC operation, power supply pin connection, power generation element, storage capacitor, and other items.

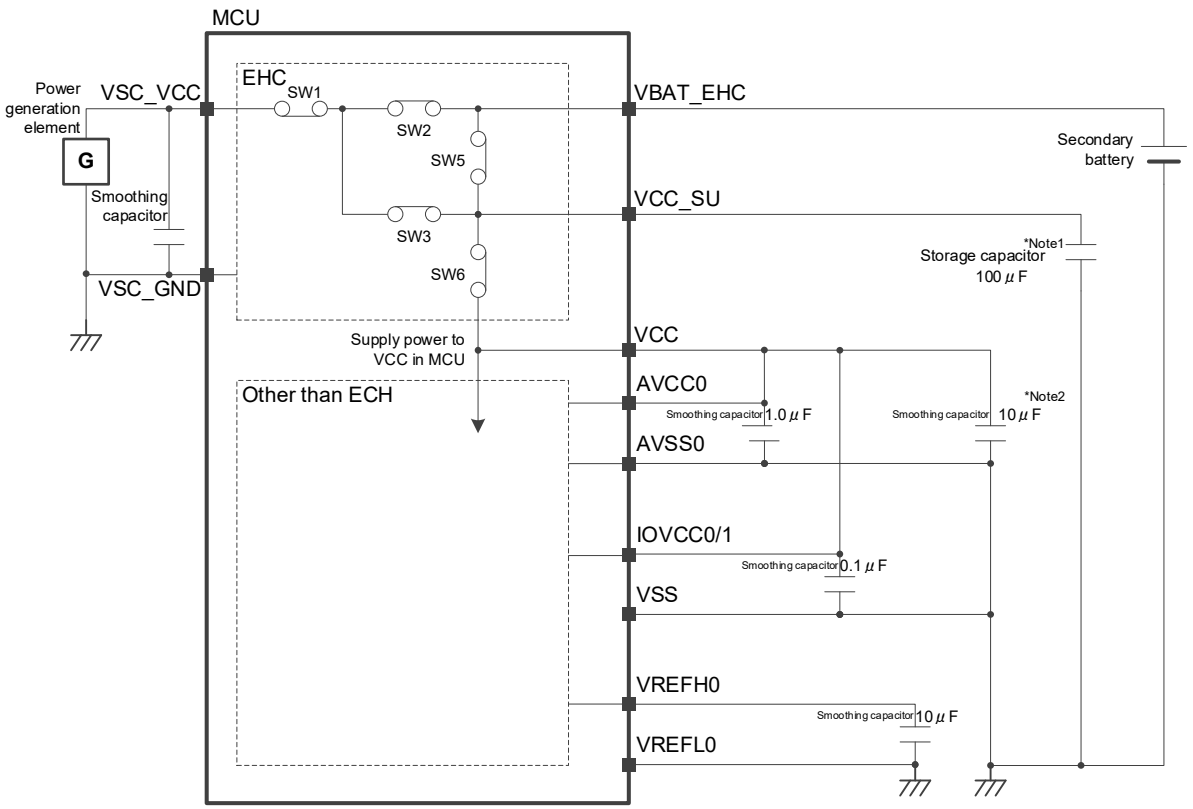
4.1 Explanation of Operation During EHC Use

Upon connection of a power generation element, the EHC begins operation from before reset cancellation, and uses the current generated by the power generation element to charge the storage capacitor and secondary battery, while also supplying power to VCC/IOVCC within the MCU. Even when the amount of power generated by the power generation element is less than the MCU current consumption, operation can be continued using the charged storage capacitor and secondary battery. For details, refer to section 14.3, Operation, in the UMH.

4.2 Connections of Power Supply Pins During EHC Use

During EHC use, power is not supplied from the EHC to the IOVCC0/1 pins, the AVCC0 pin, or the VREFH0 pin. Power should be supplied to the IOVCC0/1 pins, the AVCC0 pin, or the VREFH0 pin from an external power supply or from the VCC/IOVCC pin.

Figure 4.1 shows an example of power supply connection when using EHC (Reference Voltage Generation Circuit is used).



Note. For details of each terminal processing, refer to section 14.5, Usage Notes, in the UMH.

Note1. The required capacitance of the storage capacitor depends on the ambient temperature range. For details, see section 51.9. EHC Characteristics.

Note2. The capacitance should be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.

Figure 4.1 Example for Connecting Power Supply Pins When Using EHC

(Reference Voltage Generation Circuit is used)

4.3 Frequency Settings During Storage Capacitor Charging and Rapid Startup Hardware Function Intervals

During an EHC capacitor charging and rapid startup hardware function interval, the clock frequency should be set to 2 MHz or lower in order to reduce current consumption in the storage capacitor connected to the VCC_SU pin.

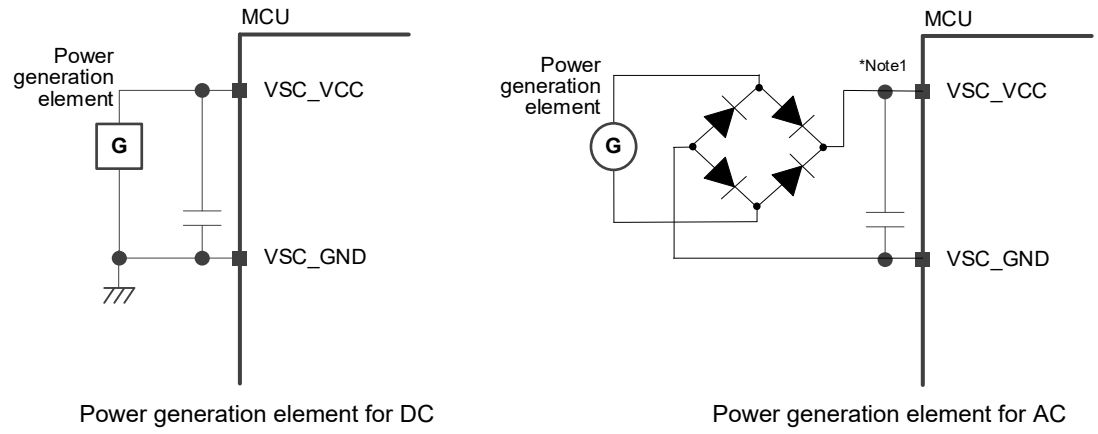
There is no limit on the clock frequency after transition to a normal operation interval. However, depending on the circumstances of internal MCU operation, the amount of power generated and circumstances of power generation of the power generation element connected to the VSC_VCC pin, the discharge capacity of the secondary battery connected to the VBAT_EHC pin, and other factors, there is variation in the time over which the MCU can continue operation, so thorough evaluations should be performed before use.

4.4 Methods of Confirmation of VBAT_EHC Pin Voltage

In order to confirm the voltage of the secondary battery connected to the VBAT_EHC pin, there is a method of measurement using the voltage monitoring battery circuit (LVDBAT), and a method that uses the 14-bit A/D converter (S14AD) and the reference voltage generation circuit (VREF). For details, refer to section 14.3.3, Checking the Voltage on the VBAT_EHC Pin, in the UMH.

4.5 Examples of Power Generation Element Connection

This section describes connections of power generation elements. Figure 4.2 shows examples of connections when the power generation element to be connected to VSC_VCC is a direct voltage and an alternating voltage. In the circuit for use with AC input, a bridge circuit is necessary in order to convert the alternating current to direct current.



Power generation element for DC Power generation element for AC

Note1. Sufficient smoothing is required. Smooth it so that the amplitude is less than 1V.

Figure 4.2 Examples of Connection of AC/DC Power Generation Elements

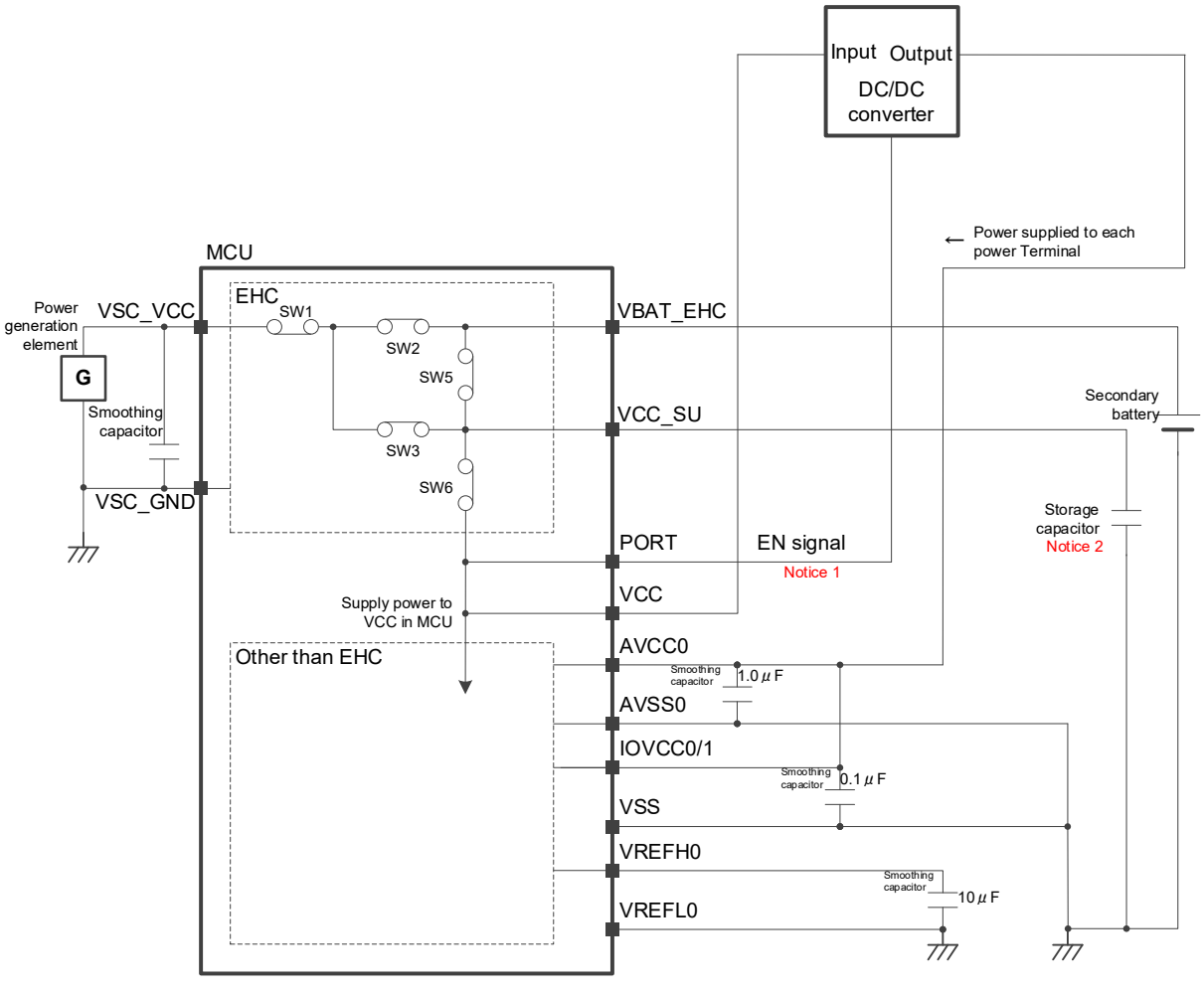
When the power generation element is a constant current source such as a solar cell, the amount of power generated by the power geeration element can be measured by changing the chip internal load resistance at the VSC_VCC pin. There are two methods of detecting the amount of power generated by the power generation element: checking the power generation status flag (EHCCR0.ENOUT) of the power generation element, and directly measuring the voltage of the VSS_VCC pin using the 14-bit A/D converter. For details, refer to section 14.3.7, Level of Charge Detection, in the UMH.

4.6 Supplying Power to Device Outside EHC

This MCU can control power from a power generation element, charge a secondary battery, and supply power to a peripheral circuit.

○ Case of supply from VCC/IOVCC

The power output from this MCU depends on the voltages of the secondary battery, the storage capacitor, and the power generation element. In many cases, the voltage is lower than the operating voltage, and changes with time. A connection example appears in Figure 4.3.



Notice 1: Use VCC/IOVCC domain ports or IOVCCn (n = 0, 1) domain ports that are directly powered from VCC/IOVCC for DCDC converter EN control.

Notice 2: Determine the storage capacitor by considering the capacity connected to the VCC pin. For details, refer to section 14.1 Overview, in the UMH.

Figure 4.3 Connection Example When Power is supplied from VCC/IOVCC

(Reference Voltage Generation Circuit is used)

Because status LEDs such as power indicator LEDs constitute a major load in the EHC, it is recommended that they not be mounted.

4.7 Connection of Power Supply Pins When EHC is Not in Use

When the EHC is not used, the VSC_VCC pin should be connected to the VSC_GND pin. By connecting the VSC_VCC pin to the VSC_GND pin, EHC operation is stopped. The VBAT_EHC pin and VCC_SU pin should be connected to the VCC pin.

Figure 4.4 shows an example for connecting power supply when not using EHC (Reference Voltage Generation Circuit is not used).

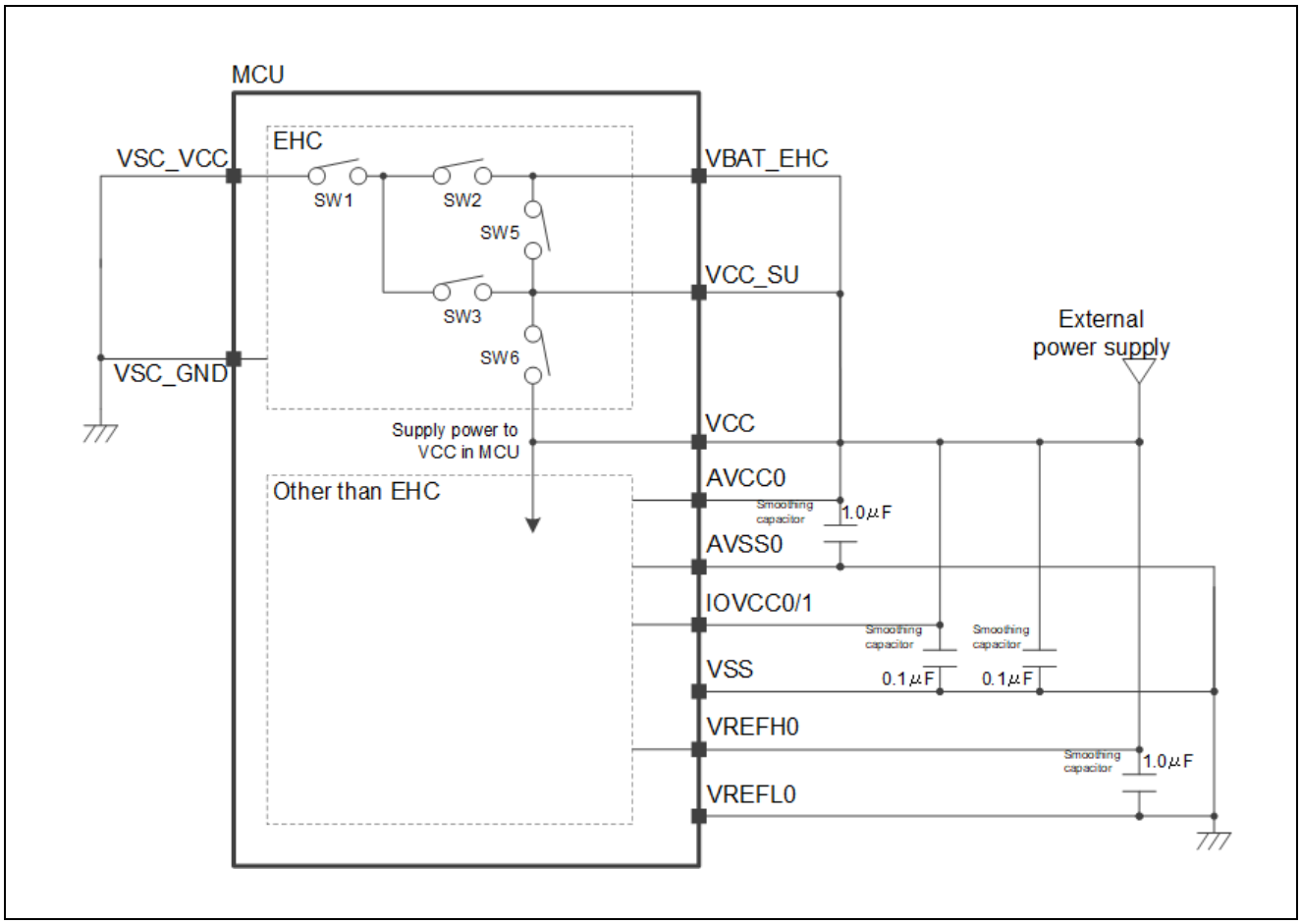


Figure 4.4 Example for Connecting Power Supply Pins When Not Using EHC

(Reference Voltage Generation Circuit is not used)

4.8 Boot Mode

4.8.1 Serial Programming Modes

This MCU incorporates up to 256 Kbytes of code flash memory. Serial programming modes are provided for onboard programming of the flash memory. The serial programming modes include the following.

- SCI boot mode using SCI9

Table 4-1 indicates input/output pins for modules related to flash memory. For details, refer to section 50.5, Serial Programming Mode, in the UMH.

When the RES# pin goes to low, processing in execution is all interrupted, and this MCU enters the reset state; hence the pin should be kept at high level so that reset does not occur. For connection and other details, see section 3.2, Reset.

Table 4-1 Basic Functions

Pin Name	I/O	Applicable Mode	Function
MD	Input	SCI boot mode	Selection of startup mode
RXD9_A (Notes 1, 2)	Input		SCI data reception in the host communication
TXD9_A (Notes 1, 2)	Output		SCI data transmission in the host communication

Note 1. For the ports to which the RXD9_A/TXD9_A pins are assigned, refer to chapter 22, IO Ports, in the UMH.

Note 2. The RXD9_A/TXD9_A pins are recommended to be pulled up. A pull-up resistor of 4.7 k to 10 kΩ should be used.

4.9 Debugging

4.9.1 SWD Interface

This MCU supports a SWD interface as a debugging interface.

Table 4-2 indicates the SWD pins.

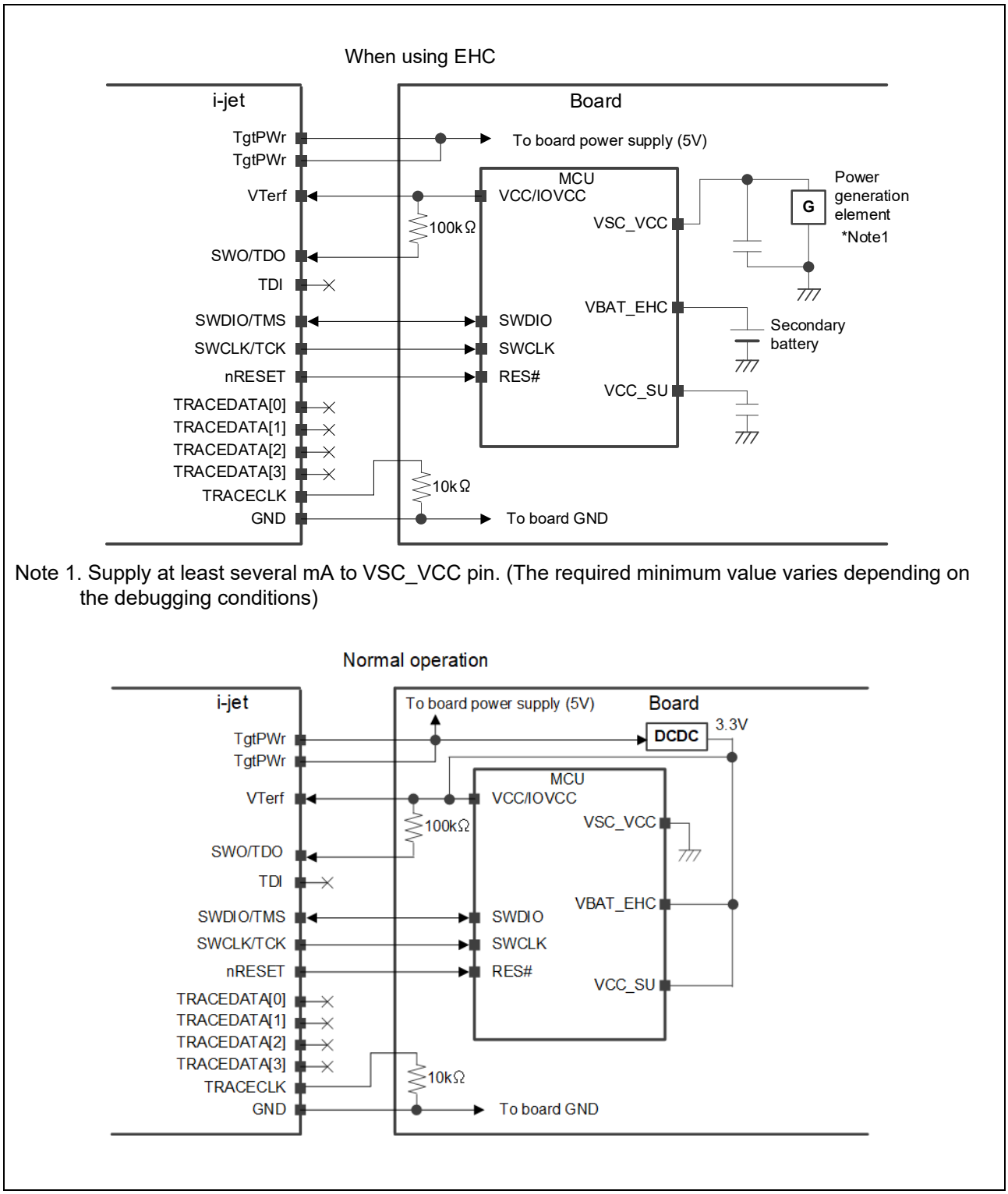
Table 4-2 SWD Pins

Pin Name	I/O	Function	Processing for Not in Use
SWCLK	Input	Serial wire clock input pin	Pull-up
SWDIO	I/O	Serial data input/output pin	Pull-up

4.9.2 Emulator Connection Examples

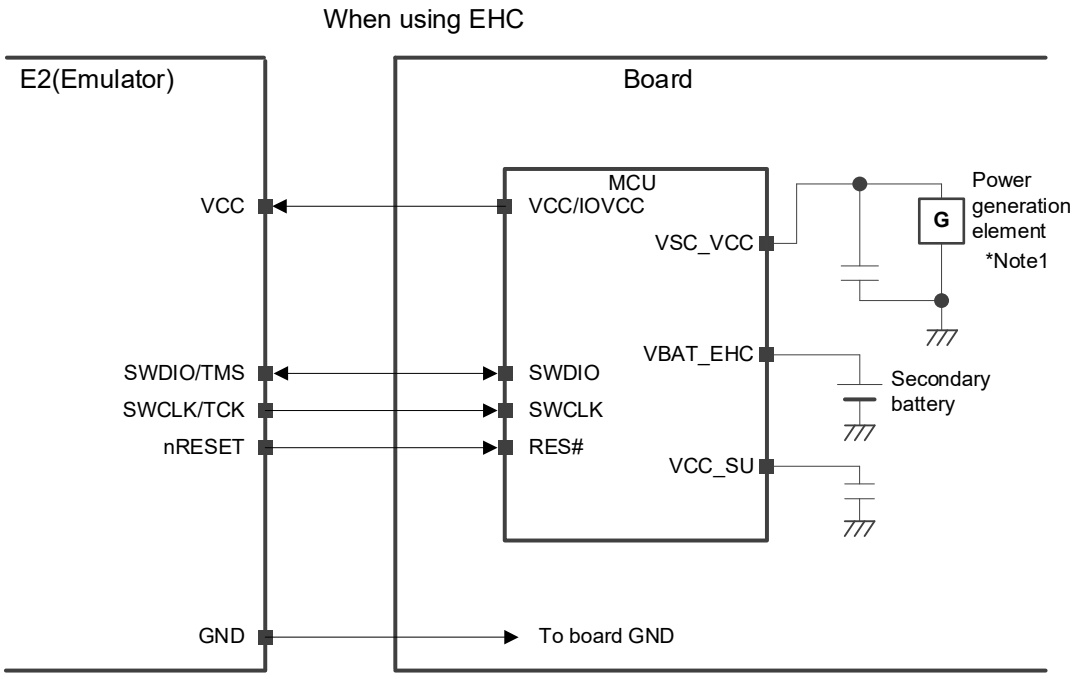
This section describes examples of emulator connection. Figure 4.5 shows an I-jet connection example. Figure 4.6 shows an E2 emulator connection example. Figure 4.7 shows a J-link emulator connection example.

For the power connection of each emulator, when using EHC is an example of supplying power from the user system to the emulator, and in normal operation, power is supplied from the emulator to the user system.

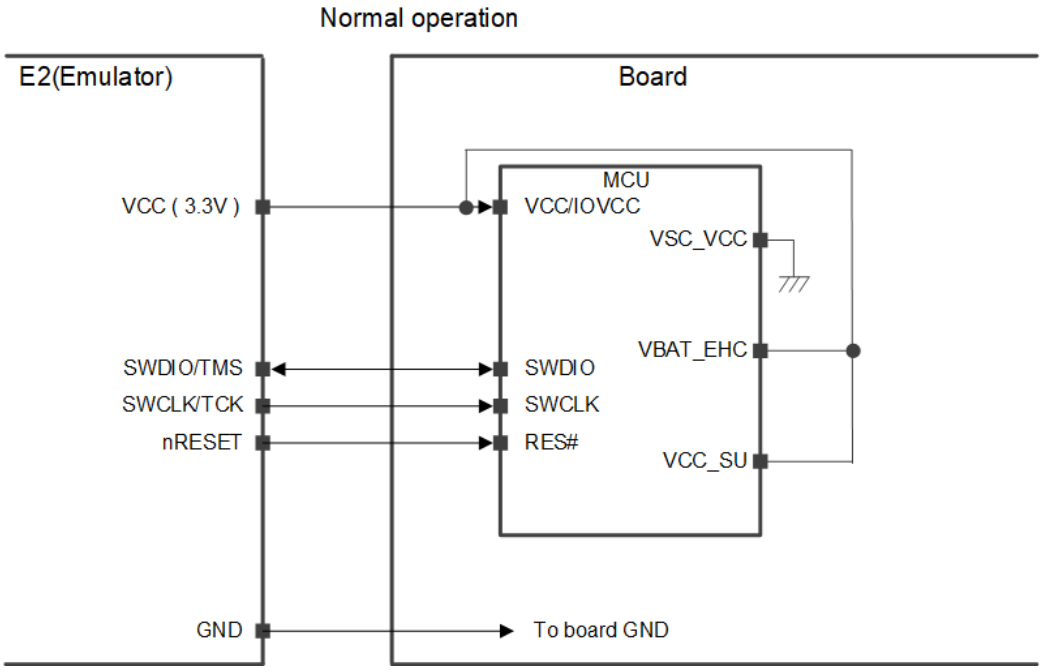


Note 1. Supply at least several mA to VSC_VCC pin. (The required minimum value varies depending on the debugging conditions)

Figure 4.5 I-jet Connection Example

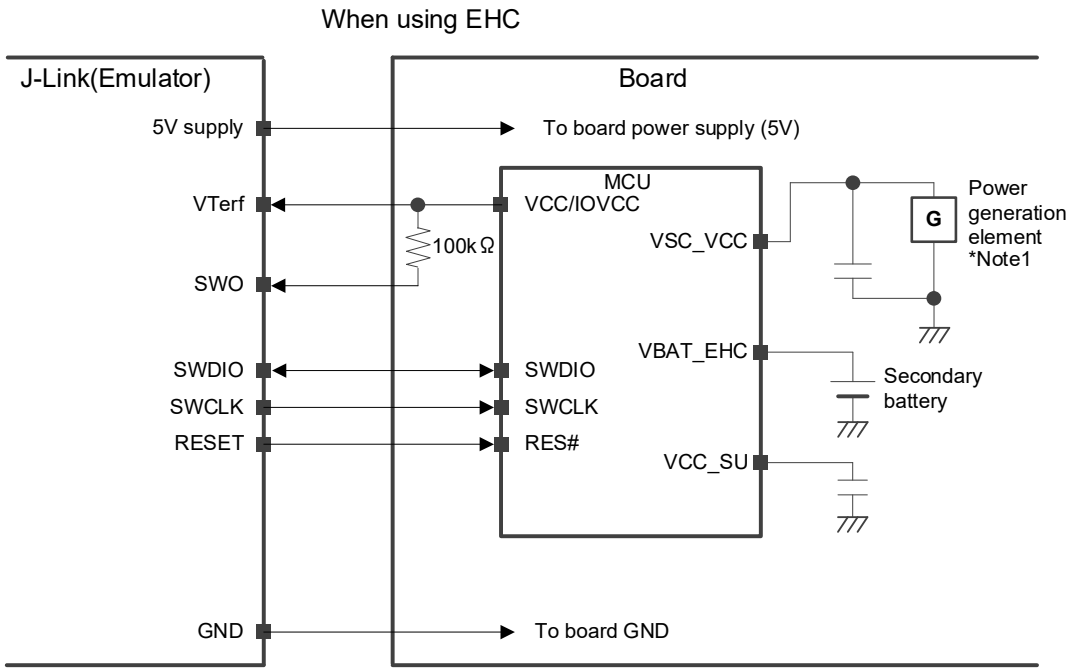


Note 1. Supply at least several mA to VSC_VCC pin. (The required minimum value varies depending on the debugging conditions)

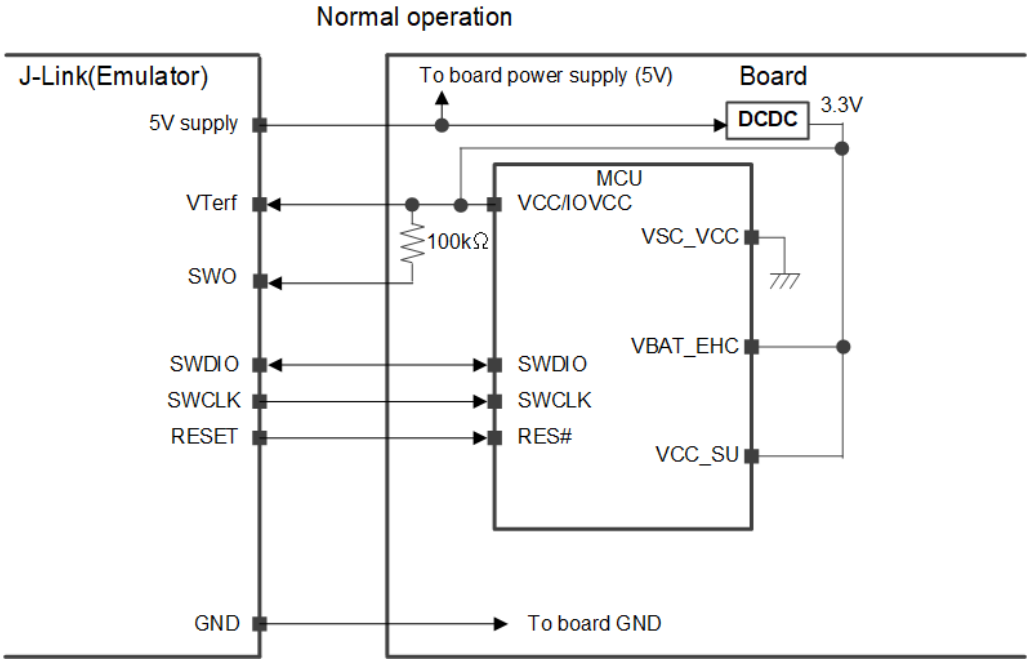


* For details, refer to E2 Emulator, E2 Emulator Lite (R01UT4582), in the UM.

Figure 4.6 E2 Emulator Connection Example



Note 1. Supply at least several mA to VSC_VCC pin. (The required minimum value varies depending on the debugging conditions)



*For details, refer to Segger (https://www.segger.com/).

Figure 4.7 J-link Emulator Connection Example

4.9.3 Notes on when using EHC

Debugging is possible using the circuit configuration when using EHC, but the debugger cannot be connected before EHC startup, and so an emulator is connected to the board in advance.

Supply at least several mA to VSC_VCC pin, and connect the IDE to MCU after starting the EHC. Continuously supply several mA of current during debugging.

5. Electrical Characteristics

5.1 Power Supplies

5.1.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power-supply voltage	Power supply voltage	VCC	-0.3 to 4.6	V
	Input voltage for EHC	VSC_VCC	-0.3 to 4.6	V
	2ndry battery input voltage for EHC	VBAT_EHC	-0.3 to 4.6	V
	Power supply voltage for I/O	IOVCC, IOVCC0 to IOVCC1	-0.3 to 4.6	V
Input voltage		Vin	-0.3 to VCC + 0.3 (max 4.6V)	V
Reference power supply voltage		VREFH0	-0.3 to AVCC0 + 0.3 (max 4.6V)	V
		VREFL0	-0.3 to AVSS0 + 0.3 (max 4.6V)	V
Analog power supply voltage		AVCC0	-0.3 to 4.6	V
Junction temperature		Tj	-40 to +95	°C
Storage temperature		Tstg	-55 to +125	°C

Note on usage: If this MCU is used beyond the absolute maximum ratings, it may be permanently destroyed.

5.1.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Power-supply voltage	VCC	1.62	-	3.6	V
	VSS	-	0	-	V
Input voltage for EHC	VSC_VCC	1.62	-	3.6	V
2ndry battery input voltage for EHC	VBAT_EHC(Note 1)	1.62	-	3.6	V
Analog power supply voltage	AVCC0	1.62	-	3.6	V
	AVSS0	-	0	-	V
	VREFH0	1.62	-	AVCC0	V
	VREFL0	-	0	-	V
Power supply voltage for I/O	IOVCC, IOVCC0, IOVCC1	1.62	-	3.6	V
Operating temperature	Topr	-40	-	85	℃

Note 1. A charging voltage of the secondary battery connected to the VBAT_EHC pin is 2.4 V, 2.5 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V or 3.1 V.

5.1.3 Selection of Power Generation Elements

Power generation elements connected to the VSC_VCC pin should be elements with an open circuit voltage of up to 5.4 V and a short circuit current of up to 10 mA, and should satisfy the following condition.

- The power generation current should be 3 μA or greater when the voltage of the power generation element is equal to the secondary battery charging voltage.

The upper limit to the open circuit voltage of the power generation element is 5.4 V, but a power generation element for which the VSC_VCC pin voltage does not exceed the absolute maximum rating should be used.

Table 5-3 Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Input voltage for EHC	VSC_VCC	-0.3 to 4.6	V

5.1.4 Storage Capacitor

The VCC_SU pin is a power supply pin to which power is supplied from the storage capacitor. When using a solar cell as the power generation element, the capacitance of the connected storage capacitor must be selected according to the operating temperature. At 25°C, a value of 47 µF is necessary; the higher the temperature, the greater the capacitance required.

Please refer to section 51.9, EHC Characteristics, in Electrical Characteristics chapter in the UMH. When using a power generation element other than the above, a 100 µF storage capacitor should be connected. It is recommended that the capacitor to be used has a small leakage current.

5.1.5 Secondary Battery Selection

The secondary battery for connection to the VBAT_EHC pin should have a charging voltage of 2.4 V or 3.1 V. The charging voltage for the secondary battery to be connected should be set using the OFS1.VBATSEL bit of the option setting memory. For details, refer to section 7.2.2 OFS1: Option Function Select Register 1, in the UMH.

Table 5-4 provides information related to connection of the mounted secondary battery. The recommended secondary battery is Nichicon's SLB Series. The included solar panel(note 1) generates a current of 42 µA, and therefore some time is required to charge the recommended secondary battery, although this also depends on the operation settings of this MCU. Charging prior to mounting should be considered, according to the details of evaluations to be performed.

Note 1. Panasonic AM-1815CA: Operating voltage 3.0 V, operating current 42.0 µA (white fluorescent lamp - 200 lx (25°C))

Table 5-4 Secondary Battery (BT2)

Secondary Battery (BT2)							
Pin	Symbol	MCU		Pin	Symbol	MCU	
		Port	Pin			Port	Pin
1	RE-BATTERY_VCC	VBAT_EHC	28	2	GROUND	-	-

5.1.6 Secondary Battery Selection When Using MLCD

A MIP liquid crystal controller (MLCD) requires a MLCD pin output voltage of 2.7 V or higher. The EHC is used to supply power from the secondary battery connected to the VBAT_EHC pin to the VCC region within the MCU, and when an MLCD is used, a secondary battery with a charging voltage of 2.7 V should be connected to the VBAT_EHC pin.

Website and Support

Renesas Electronics Website
http://japan.renesas.com

Inquiries
http://japan.renesas.com/contact/

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun.30.2020	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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