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H8/300H Super Low Power Series

RAM Emulation Function

Introduction

This document explains emulation of flash memory using RAM of the H8/38099 Group.

Target Device

H8/38099F

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1. Specifications

- (1) The RAM emulation function of the H8/38099 Group is used.
- (2) The user program active in the RAM emulation mode is transferred to the on-chip RAM area.
- (3) The RAM overlay area is loaded with the interrupt vector addresses for the interrupts (RTC second interval interrupts) used in the RAM emulation mode.
- (4) After the transfer of the user program is completed, the LED (LED0) connected to the P90 output pin is turned on and off at 0.5 s intervals using the on-chip RTC of the H8/38099 Group.
- (5) When the switch (SW1) connected to the $\overline{\text{IRQ0}}$ input pin is pressed, control is transferred to the user program in the RAM to set the flash memory into the module standby mode.
- (6) The user program running in the RAM turns on and off the LED (LED1) connected to the P91 output pin at one s intervals using the H8/38099 Group on-chip RTC.
- (7) When the switch (SW3) connected to the $\overline{\text{IRQ3}}$ input pin is pressed, the flash memory's module standby mode is canceled. Subsequently, program process is returned to the program in the flash memory, which turns on and off the LED (LED0) connected to the P90 output pin at 0.5 s intervals.
- (8) This program runs on the H8/38099 Group RSK (Renesas Starter Kit). Figure 1 shows the block diagram of the hardware that this program uses.

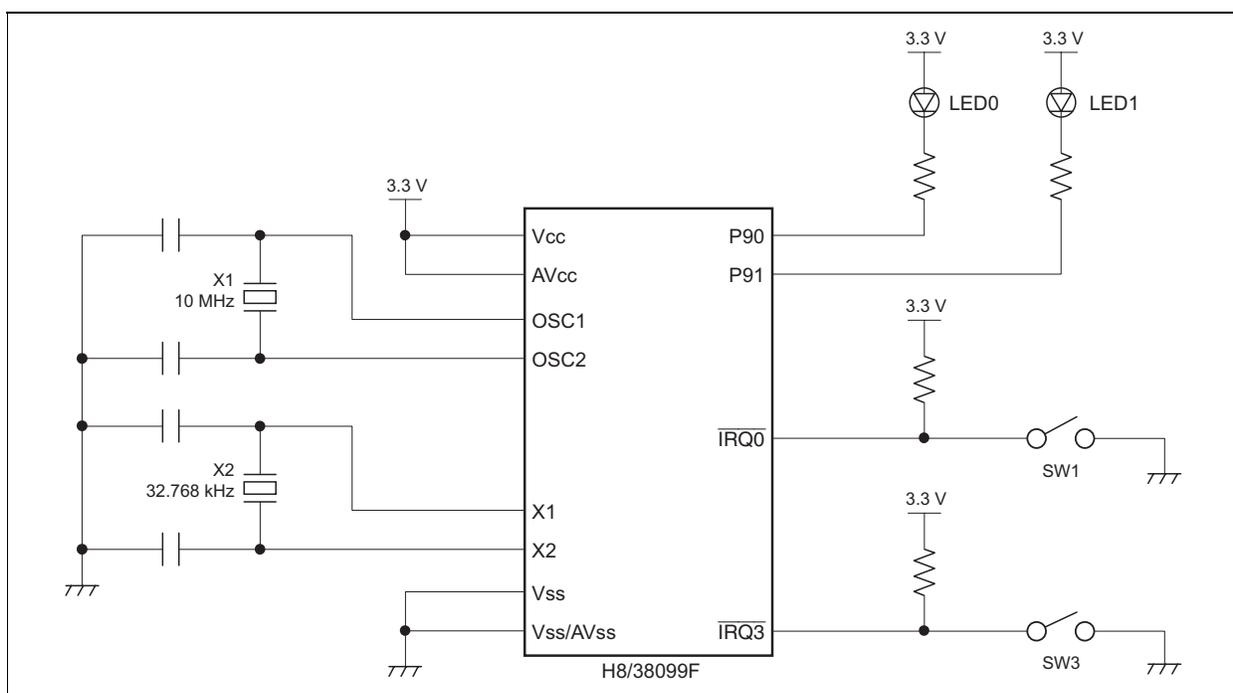


Figure 1 Hardware Block Diagram (Renesas Starter Kit for H8/38099)

2. Applicable Conditions

Table 1 summarizes the H8/38099 Group conditions applied to this task example.

Table 1 Applicable Conditions

| Item | Description |
|------------------------|---|
| System clock frequency | Crystal oscillator frequency: 10 MHz System clock (ϕ): 10 MHz |
| Subclock frequency | Crystal oscillator frequency: 32.768 kHz Subclock (ϕ_{SUB}): 32.768 kHz |
| Supply voltage | Vcc = AVcc = 3.3 V |

3. Functional Description

3.1 RAM Emulation Function

The RAM emulation function can overlay part of the flash memory (emulation area) with the on-chip RAM.

Figure 2 shows the outline of the memory configuration in which the flash memory's emulation area and RAM overlay.

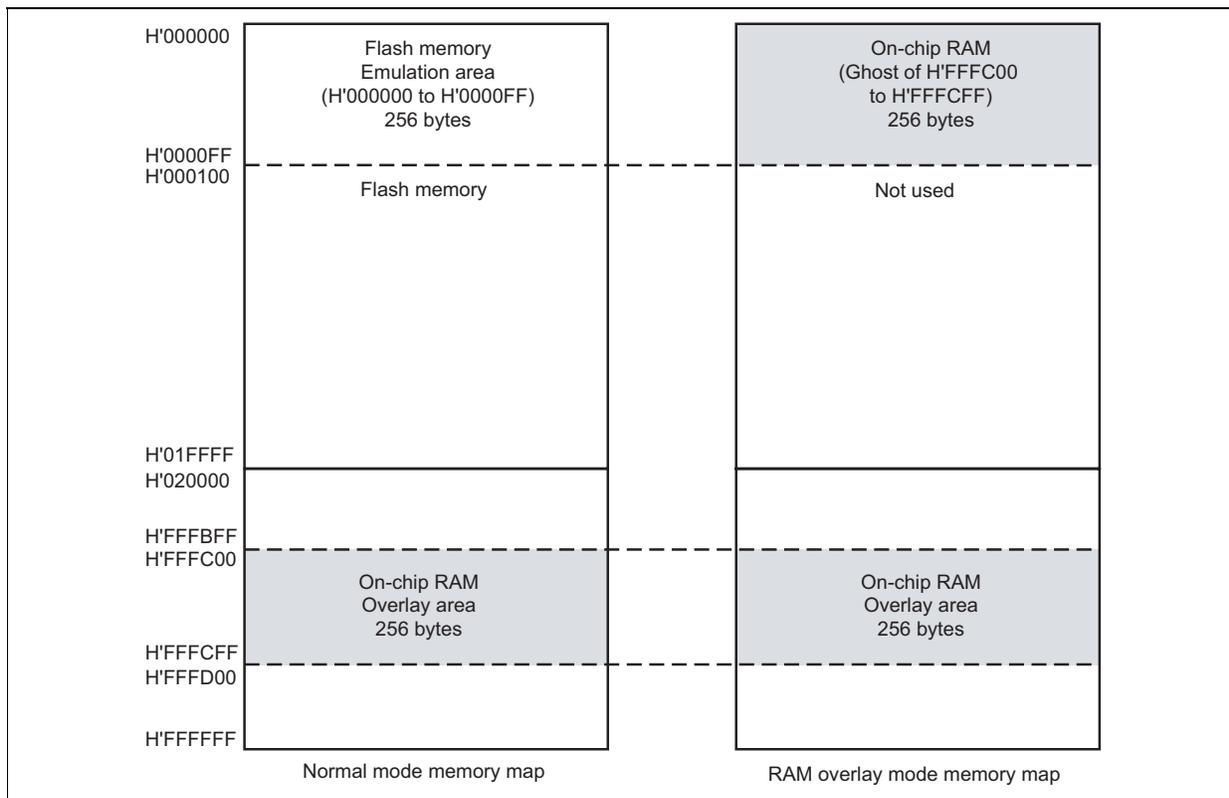


Figure 2 Outline of RAM Overlay Processing

- (1) The size of the overlaid RAM area (RAM overlay area) is fixed at 256 bytes from H'FFFC00 to H'FFFCFF.
- (2) The size of the overlaid flash memory area (emulation area) is 256 bytes from H'000000 to H'0000FF.
- (3) The emulation area is overlaid with the RAM overlay area when the flash memory module standby bit (FROMCKSTP) of the clock stop register 1 (CKSTPR1) is set to 0 to set the flash memory into the standby mode and an access is made to the emulation area.
- (4) The RAM overlay area is accessible from both the addresses in the flash memory and in the original RAM. The RAM overlay area needs to be provided with a vector table when RAM emulation is used.
- (5) The RAM overlay is cancelled by setting the FROMCKSTP bit of CKSTPR1 to 1 and canceling the flash memory's module standby mode.

3.2 Power-down Operation of Flash Memory

The flash memory will operate in one of the following states in the user mode:

- Normal operating state
The flash memory can be read at high speed.
- Power-down state
Part of the power supply circuit for the flash memory can be stopped. This makes it possible to read data from the flash memory with low power consumption.
- Standby state
All circuitry of the flash memory are stopped.

Table 2 shows the relationship between the LSI's operating modes and flash memory states. In subactive mode, the flash memory can be set into power-down mode using the power-down enable bit (PDWND) of the flash memory power control register (FLPWCR). Some operation stabilization time is required for the suspended power supply circuit to restore the flash memory from power-down or standby state. Set the standby timer select bits 3-0 (STS3 to STS0) of the system control registers (SYSCR1 and SYSCR3) so that the wait time required to return to normal operating mode, including the case when an external clock is used, is set to 20 μ s or longer.

Table 2 Flash Memory Operating States

| LSI Operating Mode | Flash Memory State | |
|----------------------|--------------------------------|------------------------|
| | When PDWND = 0 (initial value) | When PDWND = 1 |
| Active mode | Normal operating state | Normal operating state |
| Sleep mode | Normal operating state | Normal operating state |
| Subactive mode | Power-down mode | Normal operating state |
| Subsleep mode | Standby state | Standby state |
| Module stand by mode | Standby state | Standby state |
| Standby mode | Standby state | Standby state |

3.3 Notes on the Setting of Module Standby Mode

When the flash memory is set to enter module standby mode, the system clock supply is stopped to the module, the function is stopped, and the state is the same as that in standby mode. Also program operation is stopped in the flash memory. Therefore operation program should be transferred to the RAM and the program should run in the RAM. Then the flash memory should be set to enter module standby mode.

When the RAM emulation is not in use, if an interrupt is generated in module standby mode, the vector address cannot be fetched. As a result, the program may run away.

Before the flash memory is set to enter module standby mode, the corresponding bit in the interrupt enable register should be cleared to 0 and the I bit in CCR should be set to 1. Then after the flash memory enters module standby mode, NMI and address break interrupt requests should not be generated.

Figure3 shows a module standby mode setting when the RAM emulation is not used.

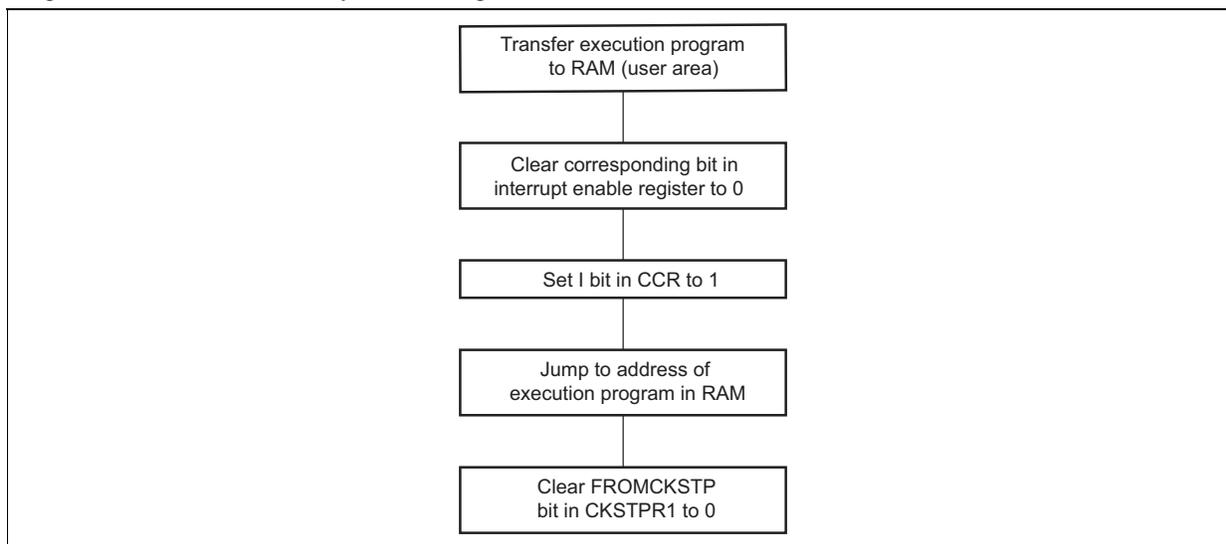


Figure 3 Configuring Module Standby Mode (Without Using the RAM Emulation)

When the RAM emulation is used (an interrupt vector is provided), if an interrupt is generated in module standby mode, the vector address can be set by assigning the interrupt vector to the RAM, and this prevents the program to run away.

4. Principles of Operation

4.1 State Transition Diagram

Figure 4 shows the state transition diagram of this program.

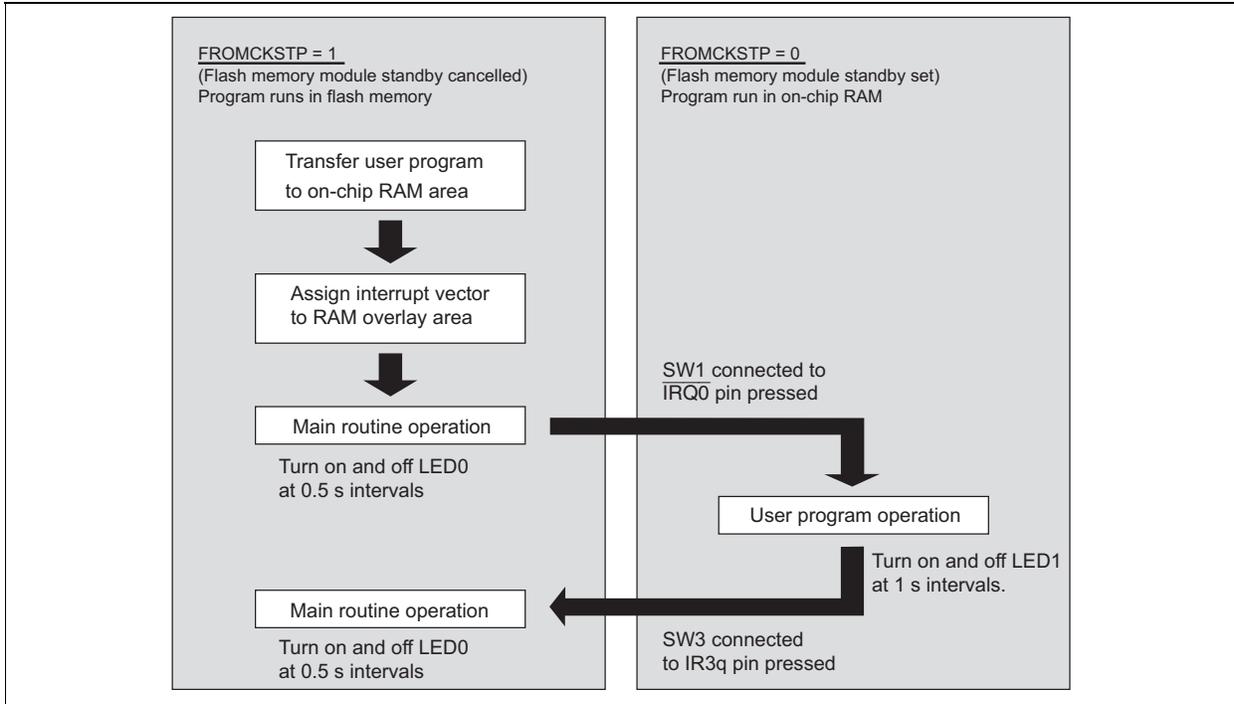


Figure 4 State Transition Diagram

4.2 LED On/Off Operations

Figure 5 illustrates the operations of the main routing running in the flash memory and the user program running in the on-chip RAM.

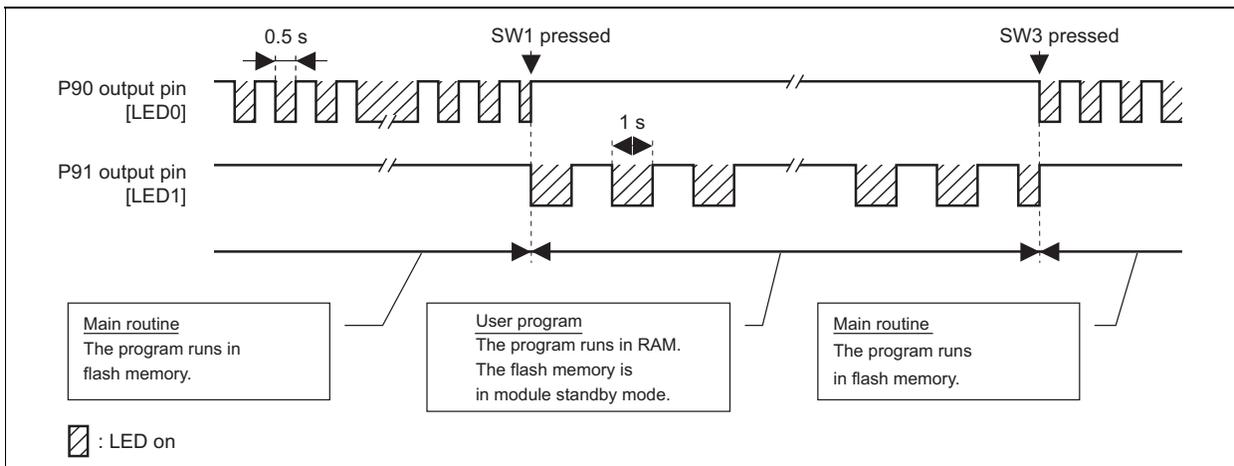


Figure 5 LED On/Off Operations

4.3 Memory Map

Figure 6 shows the H8/38099 Group (flash memory version) memory map for this program.

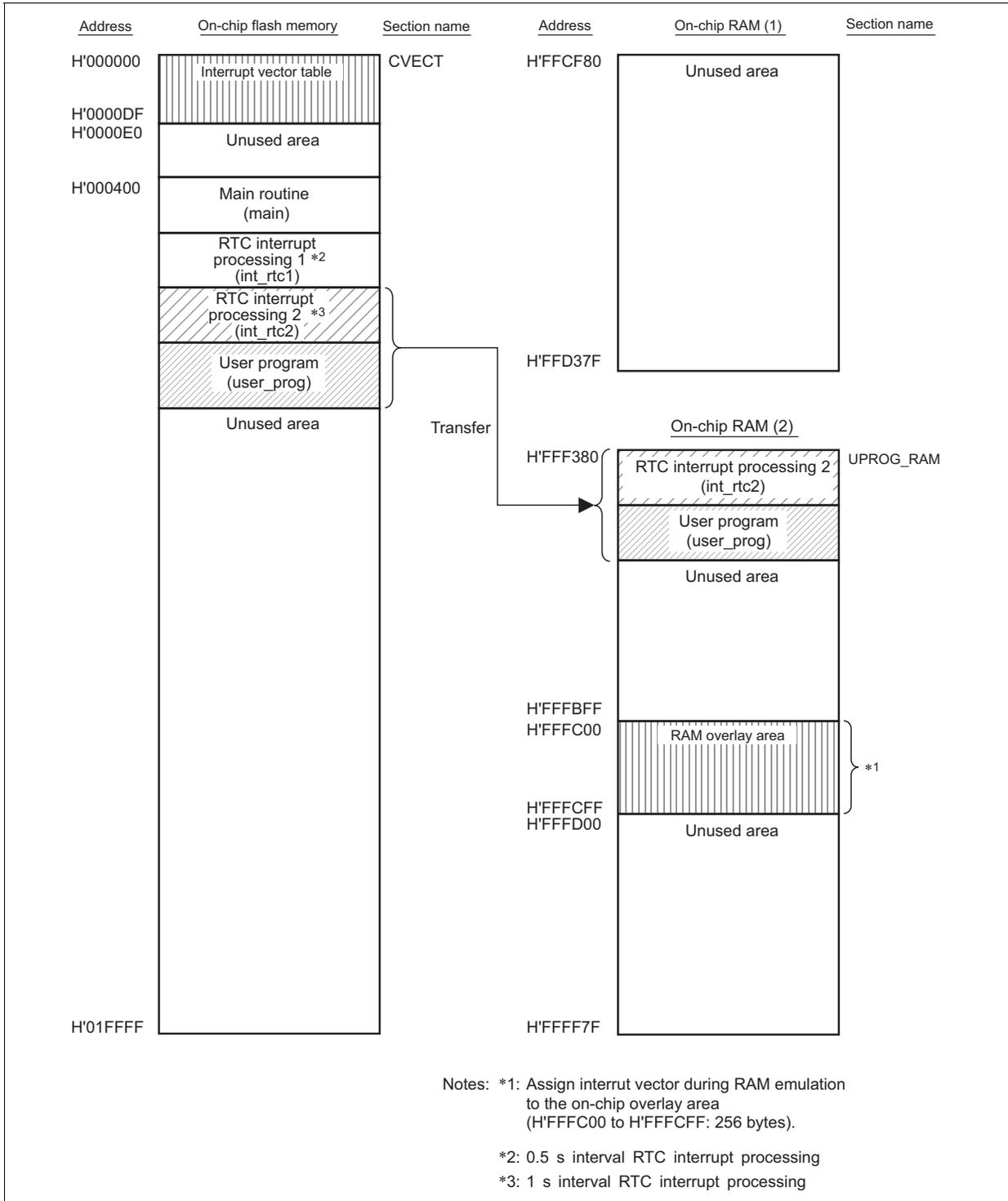


Figure 6 Memory Map

4.4 Program Transfer to RAM

When the H8/38099 Group on-chip flash memory is set in module standby mode, programs operating in the on-chip RAM is transferred to the on-chip RAM.

The program (user_prog) that is to run when the on-chip flash memory is set in module standby mode and the RTC second interval interrupt processing routine (int_rtc2) are transferred from the on-chip flash memory with a section name [PUPROG_ROM] to the on-chip RAM with a section name [UPROG_RAM] (address = H'FFF380).

In this case, it is necessary to set the ROM conversion support option of the Optimizing Linkage Editor. The ROM conversion support option reserves the ROM and RAM areas in the initialized data area and the symbols defined in the ROM section are relocated to addresses in the RAM section. Figure 7 shows the ROM conversion option setting for this program.

ROMization support option setting

```
rom = PUPROG_ROM = UPROG_RAM
```

Legends

PUPROG_ROM : Name of the section in on-chip flash memory of the program that is to run in the on-chip RAM when the on-chip flash memory is set to module standby mode.

UPROG_RAM : Name of Section in On-chip RAM to which PUPROG_ROM Section is transferred

Figure 7 Specifying the Optimized Linkage Editor Option

The function memcpy() in [string.h] is used to transfer the actual program.

4.5 Vector Table in RAM Overlay Area

A vector table needs to be set up in the RAM overlay area (H'FFFC00 to H'FFFCFF) to use the RAM emulation function. In this program, the start address (H'FFF380) of the RTC second interval interrupt processing routine (int_rtc2) is written into the address (H'FFFC54) of the RAM overlay area to make use of RTC interrupts (second interval interrupts) during RAM emulation processing. Table 3 lists the vector table in the RAM overlay area.

Table 3 Vector Table in RAM Overlay Area

| RAM Overlay Area Address | Vector No. | Interrupt Source | Destination Function (Address) |
|--------------------------|------------|---------------------|--------------------------------|
| H'FFFC00 to H'FFFC03 | 0 | Reset | — |
| H'FFFC0C to H'FFFC0F | 3 | NMI | — |
| H'FFFC14 to H'FFFC17 | 5 | Address break | — |
| H'FFFC18 to H'FFFC1B | 6 | External pin IRQ0 | — |
| H'FFFC1C to H'FFFC1F | 7 | External pin IRQ1 | — |
| H'FFFC20 to H'FFFC23 | 8 | External pin IRQAEC | — |
| H'FFFC24 to H'FFFC27 | 9 | External pin IRQ3 | — |
| H'FFFC28 to H'FFFC2B | 10 | External pin IRQ4 | — |
| H'FFFC2C to H'FFFC2F | 11 | External pin WKP0 | — |
| H'FFFC30 to H'FFFC33 | 12 | External pin WKP1 | — |
| H'FFFC34 to H'FFFC37 | 13 | External pin WKP2 | — |
| H'FFFC38 to H'FFFC3B | 14 | External pin WKP3 | — |
| H'FFFC3C to H'FFFC3F | 15 | External pin WKP4 | — |

Table 3 Vector Table in RAM Overlay Area (Continued)

| RAM Overlay Area Address | | | Vector No. | Interrupt Source | Destination Function (Address) |
|--------------------------|----|----------|------------|------------------------------|--------------------------------|
| H'FFFC40 | to | H'FFFC43 | 16 | External pin WKP5 | — |
| H'FFFC44 | to | H'FFFC47 | 17 | External pin WKP6 | — |
| H'FFFC48 | to | H'FFFC4B | 18 | External pin WKP7 | — |
| H'FFFC4C | to | H'FFFC4F | 19 | RTC 0.25 s overflow | — |
| H'FFFC50 | to | H'FFFC53 | 20 | RTC 0.5 s overflow | — |
| H'FFFC54 | to | H'FFFC57 | 21 | RTC second interval overflow | int_rtc2 (H'FFF380) |
| H'FFFC58 | to | H'FFFC5B | 22 | RTC minute interval overflow | — |
| H'FFFC5C | to | H'FFFC5F | 23 | RTC hour interval overflow | — |
| H'FFFC60 | to | H'FFFC63 | 24 | RTC day interval overflow | — |
| H'FFFC64 | to | H'FFFC67 | 25 | RTC week interval overflow | — |
| H'FFFC68 | to | H'FFFC6B | 26 | RTC free-running overflow | — |
| H'FFFC6C | to | H'FFFC6F | 27 | WDT | — |
| H'FFFC70 | to | H'FFFC73 | 28 | AEC | — |
| H'FFFC74 | to | H'FFFC77 | 29 | TPU_1 TG1A | — |
| H'FFFC78 | to | H'FFFC7B | 30 | TPU_1 TG1B | — |
| H'FFFC7C | to | H'FFFC7F | 31 | TPU_1 TCI1V | — |
| H'FFFC80 | to | H'FFFC83 | 32 | TPU_2 TG2A | — |
| H'FFFC84 | to | H'FFFC87 | 33 | TPU_2 TG2B | — |
| H'FFFC88 | to | H'FFFC8B | 34 | TPU_2 TCI2V | — |
| H'FFFC8C | to | H'FFFC8F | 35 | Timer FL | — |
| H'FFFC90 | to | H'FFFC93 | 36 | Timer FH | — |
| H'FFFC94 | to | H'FFFC97 | 37 | SCI4 | — |
| H'FFFC98 | to | H'FFFC9B | 38 | SCI3_1 | — |
| H'FFFC9C | to | H'FFFC9F | 39 | SCI3_2 | — |
| H'FFFCA0 | to | H'FFFCA3 | 40 | IIC2 | — |
| H'FFFCA8 | to | H'FFFCAB | 42 | 10-bit A/D converter | — |
| H'FFFCAC | to | H'FFFCAF | 43 | Direct transition | — |
| H'FFFCD4 | to | H'FFFCD7 | 53 | Timer C | — |
| H'FFFCD8 | to | H'FFFCDB | 54 | Timer G | — |
| H'FFFCDC | to | H'FFFCDF | 55 | SCI3_3 | — |

Note: It is presumed that neither NMI nor address break interrupts can occur.

5. Software Description

5.1 Operating Environment

Table 4 Operating Environment

| Item | Details |
|---------------------------|--|
| Development tool | High Performance Embedded Workshop (HEW) Version 4.03.00.001 |
| C/C++ compiler | H8S,H8/300 SERIES C/C++ Compiler V.6.01.02 |
| Compiler options | <ul style="list-style-type: none"> -cpu=300HA:24 -object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -nolist -chgincpath -nologo |
| Optimizing Linkage Editor | Optimizing Linkage Editor V.9.02.00 |
| Linkage editor options | <ul style="list-style-type: none"> -noprelink -rom=PUPROG_ROM=UPROG_RAM -nomessage -list="\$(CONFIGDIR)\\$(PROJECTNAME).map" -nooptimize -start=CVECT/00,P,PUPROG_ROM/0400,UPROG_RAM/0FFF380 -nologo -output="\$(CONFIGDIR)\\$(PROJECTNAME).abs" -end -input="\$(CONFIGDIR)\\$(PROJECTNAME).abs" -form=stype -output="\$(CONFIGDIR)\\$(PROJECTNAME).mot" -exit |

Table 5 Section Settings

| Address | Section Name | Description |
|----------|--------------|---|
| H'000000 | CVECT | Vector table area (constant area) |
| H'000400 | P | Program area Programs running in on-chip flash memory |
| | PUPROG_ROM | Program area Program area in on-chip flash memory for programs running in on-chip RAM area |
| H'FFF380 | UPROG_RAM | On-chip RAM area (initialized data area) Destination initialized data area in on-chip RAM to which contents of PURPOG_ROM section in on-chip flash memory are copied |

Table 6 Interrupt Exception Processing Vector Table

| Source of Exception Processing | Name | Vector No. | Vector Address | Destination Function |
|--------------------------------|---------------------------|------------|----------------|----------------------|
| RES, WDT | Reset | 0 | H'000000 | main |
| NMI | NMI | 3 | H'00000C | main |
| Address break | Break condition satisfied | 5 | H'000014 | main |
| External pin | IRQ0 | 6 | H'000018 | main |
| | IRQ1 | 7 | H'00001C | main |
| | IRQAEC | 8 | H'000020 | main |
| | IRQ3 | 9 | H'000024 | main |
| | IRQ4 | 10 | H'000028 | main |
| | WKP0 | 11 | H'00002C | main |
| | WKP1 | 12 | H'000030 | main |
| | WKP2 | 13 | H'000034 | main |
| | WKP3 | 14 | H'000038 | main |
| | WKP4 | 15 | H'00003C | main |
| | WKP5 | 16 | H'000040 | main |
| | WKP6 | 17 | H'000044 | main |
| | WKP7 | 18 | H'000048 | main |

Table 6 Interrupt Exception Processing Vector Table (Continued)

| Source of Exception Processing | Name | Vector No. | Vector Address | Destination Function |
|--------------------------------|---|------------|----------------|----------------------|
| RTC | 0.25 s overflow | 19 | H'00004C | main |
| | 0.5 s overflow | 20 | H'000050 | int_rtc1 |
| | Second interval overflow | 21 | H'000054 | int_rtc2 |
| | Minute interval overflow | 22 | H'000058 | main |
| | Hour interval overflow | 23 | H'00005C | main |
| | Day interval overflow | 24 | H'000060 | main |
| | Week interval overflow | 25 | H'000064 | main |
| | Free-running overflow | 26 | H'000068 | main |
| WDT | WDT overflow (Interval timer) | 27 | H'00006C | main |
| AEC | AEC overflow | 28 | H'000070 | main |
| TPU_1 | TG1A (TG1A input capture/compare match) | 29 | H'000074 | main |
| | TG1B (TG1B input capture/compare match) | 30 | H'000078 | main |
| | TC11V (overflow 1) | 31 | H'00007C | main |
| TPU_2 | TG2A (TG2A input capture/compare match) | 32 | H'000080 | main |
| | TG2B (TG2B input capture/compare match) | 33 | H'000084 | main |
| | TC12V (overflow 2) | 34 | H'000088 | main |
| Timer F | Timer FL compare match | 35 | H'00008C | main |
| | Timer FL overflow | | | |
| | Timer FH compare match | 36 | H'000090 | main |
| | Timer FH overflow | | | |
| SCI4 | Receive data full/transmit data empty/ transmit end/receive error | 37 | H'000094 | main |
| SCI3_1 | Transmission completion/transmit data empty/receive data full/overrun error/framing error/parity error | 38 | H'000098 | main |
| SCI3_2 | Transmission completion /transmit data empty/receive data full/overrun error/framing error/parity error | 39 | H'00009C | main |
| IIC2 | Transmit data empty/transmit end/ receive data full/stop condition detected/NACK detected/arbitration/overrun error | 40 | H'0000A0 | main |
| 10-bit A/D converter | A/D conversion end | 42 | H'0000A8 | main |
| (SLEEP instruction executed) | Direct transition | 43 | H'0000AC | main |
| Timer C | Timer C overflow/underflow | 53 | H'0000D4 | main |
| Timer G | Timer G input capture | 54 | H'0000D8 | main |
| | Timer G overflow | | | |
| SCI3_3 | Transmission completion /transmit data empty/receive data full/overrun error/framing error/parity error | 55 | H'0000DC | main |

5.2 Variable Description (in On-chip RAM Area)

This program has no on-chip RAM area that is used to store variables.

5.3 List of Functions

Table 7 Function List

| Function Name | Function |
|---------------|---|
| main | <u>Main routine</u> Sets up the stack pointer, stops the watchdog timer, sets up the module standby mode, copies the user program to RAM, setups up interrupt vector addresses in RAM overlay area, initializes port 9, RTC, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ3}}$ interrupt pins, and jump to the user program. |
| rtc_int1 | <u>RTC 0.5 s interval overflow interrupt processing routine</u> Clears the interrupt request flag and controls the P90 pin output. |
| rtc_int2 | <u>RTC second interval interrupt processing routine</u> Clears the interrupt request flag and controls the P91 pin output. |
| user_prog | <u>User program subroutine</u> Controls the on-chip flash memory module standby mode and interrupts. |

5.4 Function Description

5.4.1 main Function (Main Routine)

(1) Function overview

Sets up the stack pointer, stops the watchdog timer, sets up module standby mode, transfers the user program that is to run in RAM emulation mode to on-chip RAM, sets up an interrupt vector table in the RAM overlay area, sets up the P90 and P91 output pins to which the LEDs are connected, sets up RTC, sets up the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ3}}$ input pins to which switches are connected, enables or disables interrupts, waits until the switch (SW1) connected to the $\overline{\text{IRQ0}}$ input pin is pressed, and jumps to the user program that has been transferred n RAM.

(2) Argument

None

(3) Return value

None

(4) Flowchart

The flowchart of the main function (main routine) is shown in figure 8.

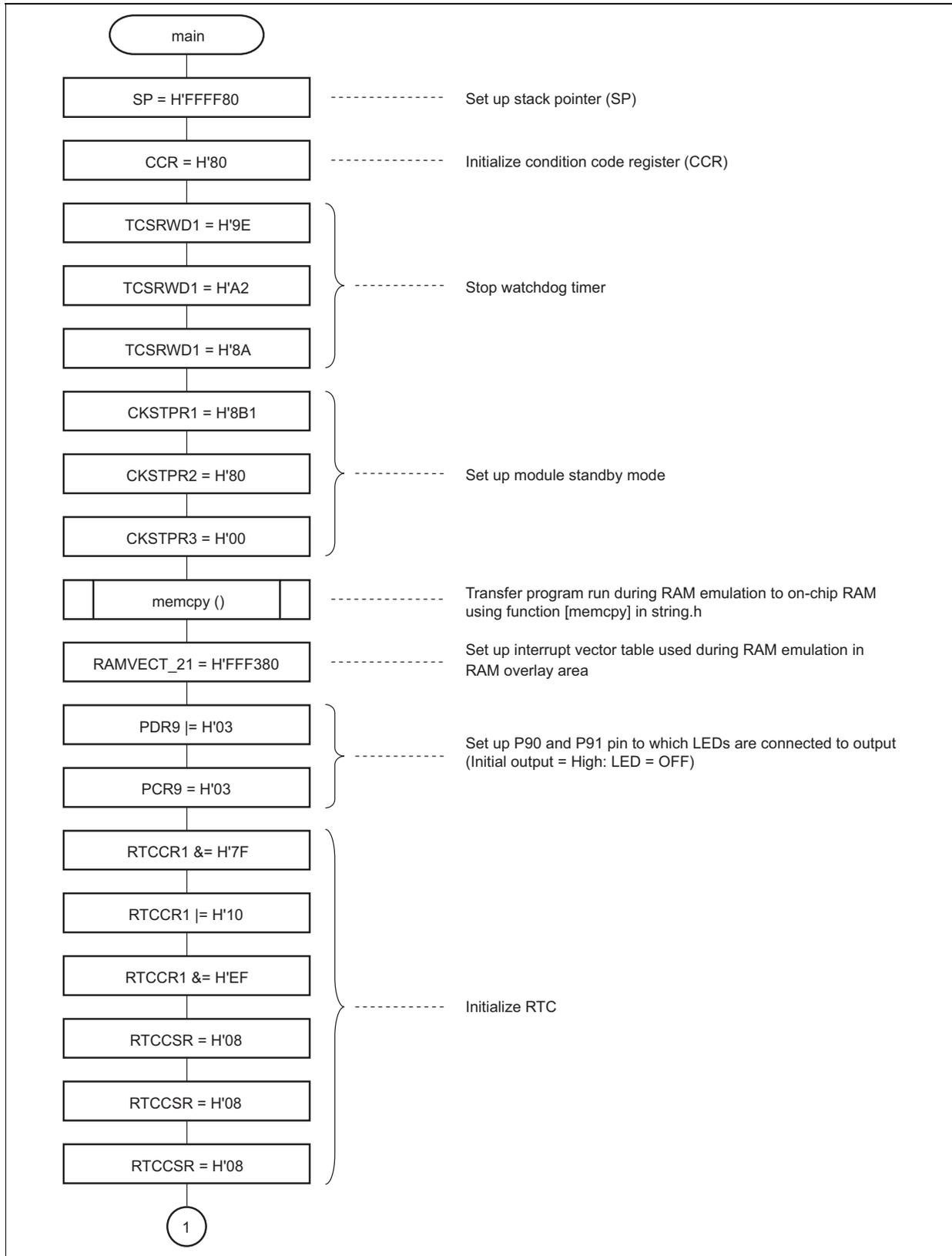


Figure 8 main Function (Main Routine) Flowchart

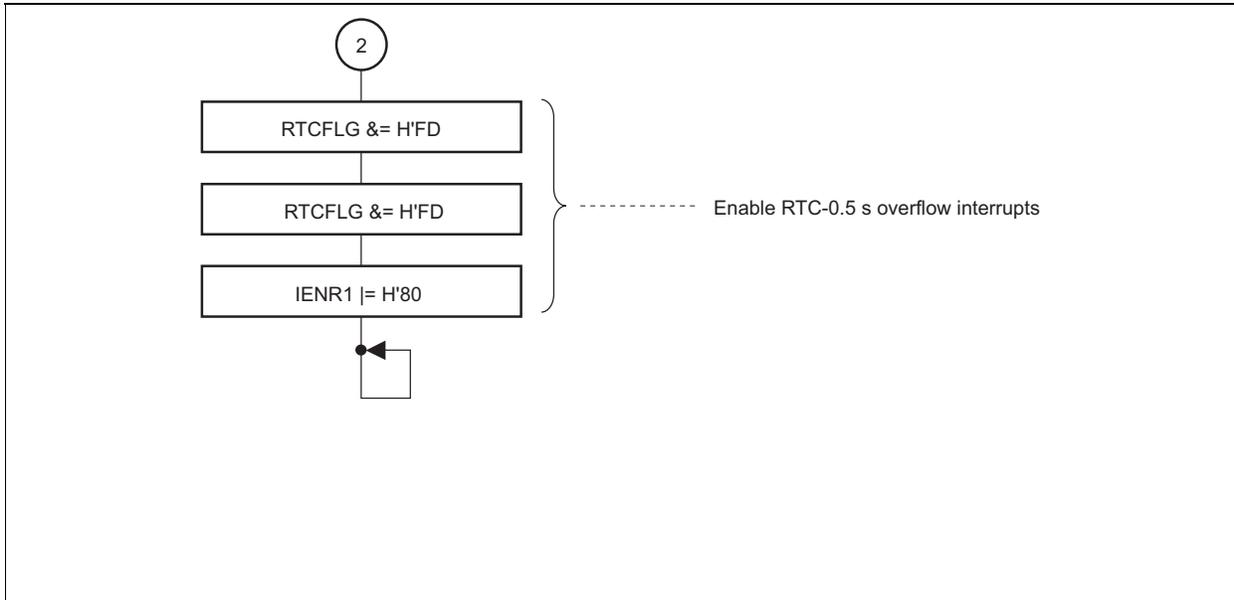


Figure 8 main Function (Main Routine) Flowchart (Continued)

5.4.2 int_rtc1 Function (RTC 0.5 s Overflow Interrupt Processing Routine)

(1) Function overview

Clears the interrupt request flag and inverts the output at the P90 pin.

(2) Argument

None

(3) Return value

None

(4) Flowchart

The flowchart of the int_rtc1 function (RTC 0.5 s overflow interrupt processing routine) is shown in figure 9.

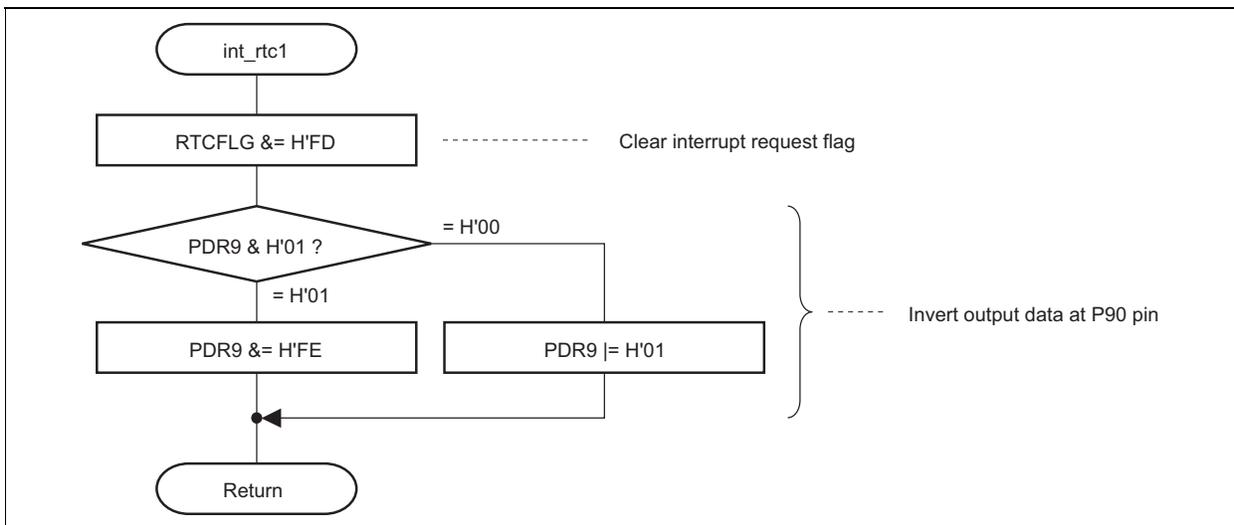


Figure 9 int_rtc1 Function (RTC 0.5 s Overflow Interrupt Processing Routine) Flowchart

5.4.3 int_rtc2 Function (RTC Second Interval Interrupt Processing Routine)

- (1) Function overview
Clears the interrupt request flag and inverts the output at the P91 pin.
- (2) Argument
None
- (3) Return value
None
- (4) Flowchart

The flowchart of the int_rtc2 function (RTC second interval interrupt processing routine) is shown in figure 10.

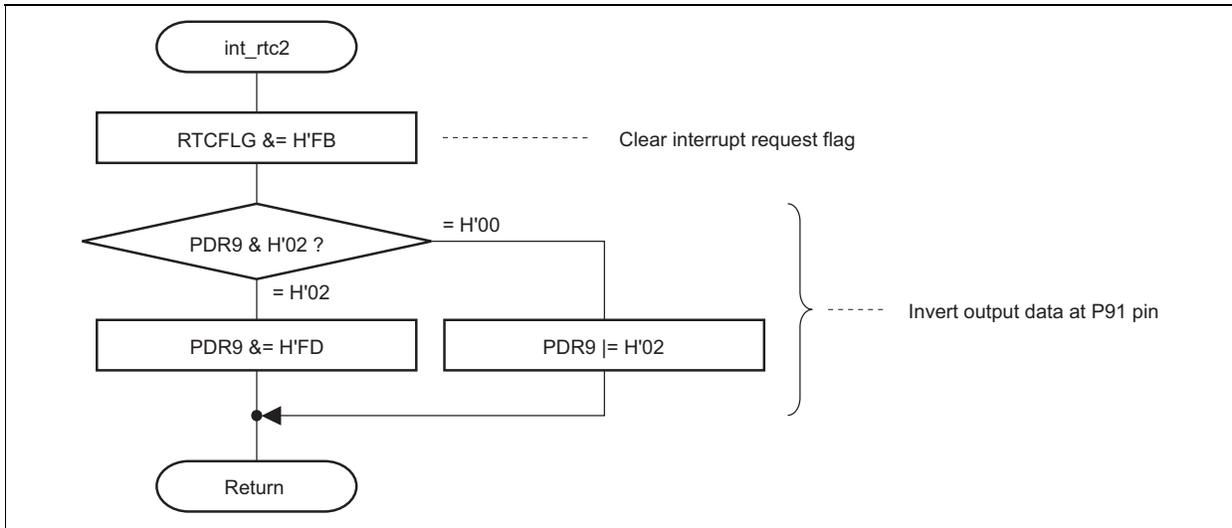


Figure 10 int_rtc2 Function (RTC Second Interval Interrupt Processing Routine) Flowchart

5.4.4 user_prog Function (User Program Subroutine)

- (1) Function overview
Sets up module standby mode for the on-chip flash memory, enables RTC interrupts (second interval interrupts), waits for the press of the switch (SW3) connected to the $\overline{\text{IRQ3}}$ input pin, disables RTC interrupts (second interval interrupts), turns off the LED connected to the P91 output pin, releases the on-chip flash memory from module standby state, and waits for the time required for the on-chip flash memory to restore from standby state to normal operating state.
- (2) Argument
None
- (3) Return value
None
- (4) Flowchart

The flowchart of the user_prog function (user program subroutine) is shown in figure 11.

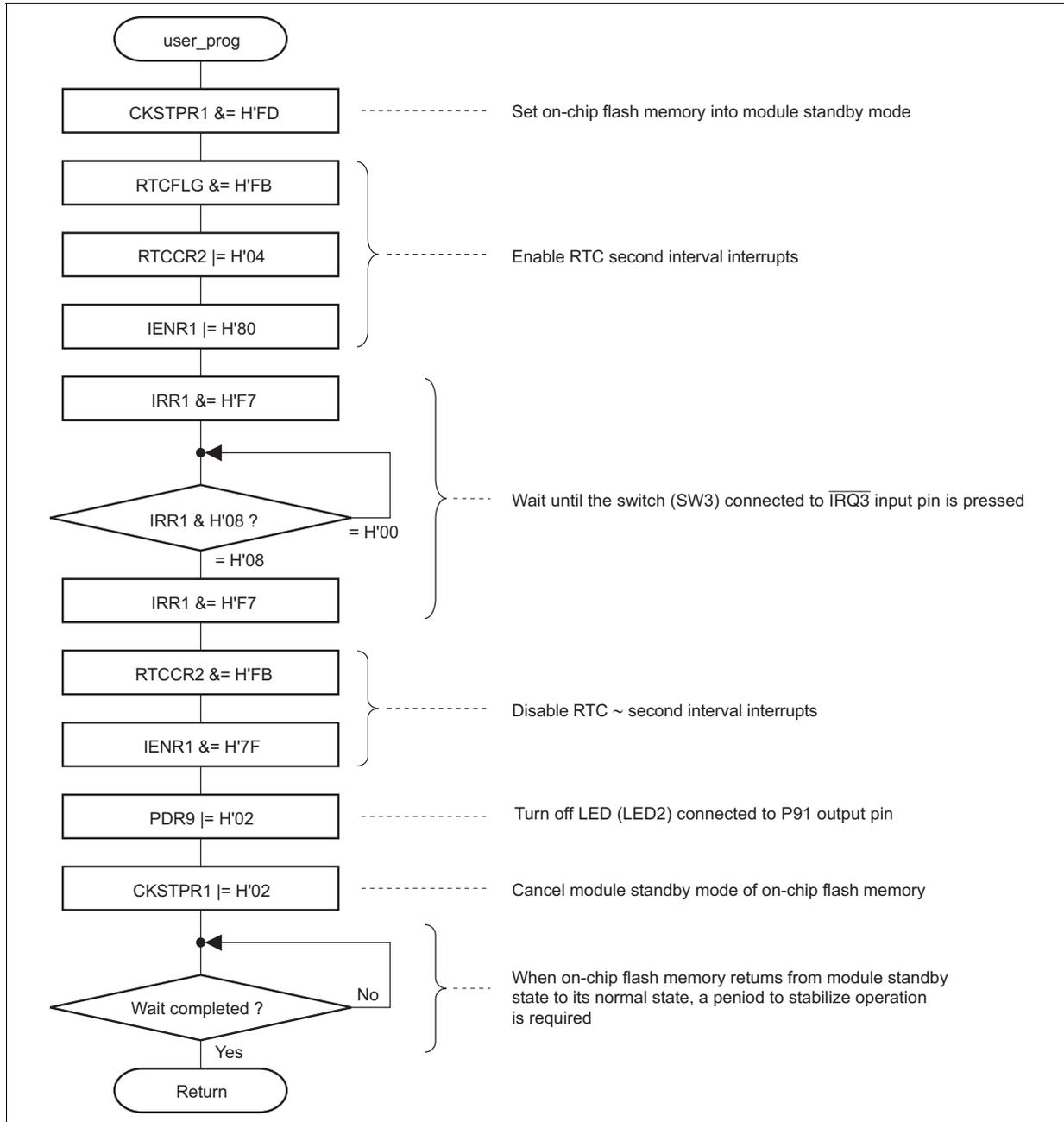


Figure 11 user_prog Function (User Program Subroutine) Flowchart

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