Renesas RA Family

Design Guide for Sub-Clock Circuits

Introduction

The sub-clock oscillation circuit has low gain to reduce power consumption. Due to the low gain, there is a risk that noise may cause the MCU to operate erroneously. This document describes how to minimize this risk when using a low capacitive load (CL) resonator.

Target Devices

RA MCU Series

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1. Component Selection

Component selection is critical to ensure correct operation of the sub-clock circuit with RA MCU devices. The following sections provide guidance to aid in component selection.

1.1 External Crystal Resonator selection

An external crystal resonator may be used as the sub-clock oscillator source. The external crystal resonator is connected across the XCIN and XCOUT pins of the MCU. The frequency of the external crystal resonator for the sub-clock oscillator must be exactly 32.768 kHz . Refer to the Electrical Characteristics section of the MCU Hardware User's Manual for specific details.

For most RA microcontrollers, an external crystal resonator may be used as the main clock source. The external crystal resonator is connected across the EXTAL and XTAL pins of the MCU. The frequency of the main clock external crystal resonator must be in the frequency range of the main clock oscillator. This document focuses on the sub-clock oscillator, but these selection and design guidelines can also apply to design of the main clock source using an external crystal resonator.

Selection of a crystal resonator will be largely dependent on each unique board design. Due to the large selection of crystal resonators available that may be suitable for use with RA MCU devices, carefully evaluate the electrical characteristics of the selected crystal resonator to determine the specific implementation requirements.

Figure 1 shows a typical example of a crystal resonator connection for the sub-clock source.

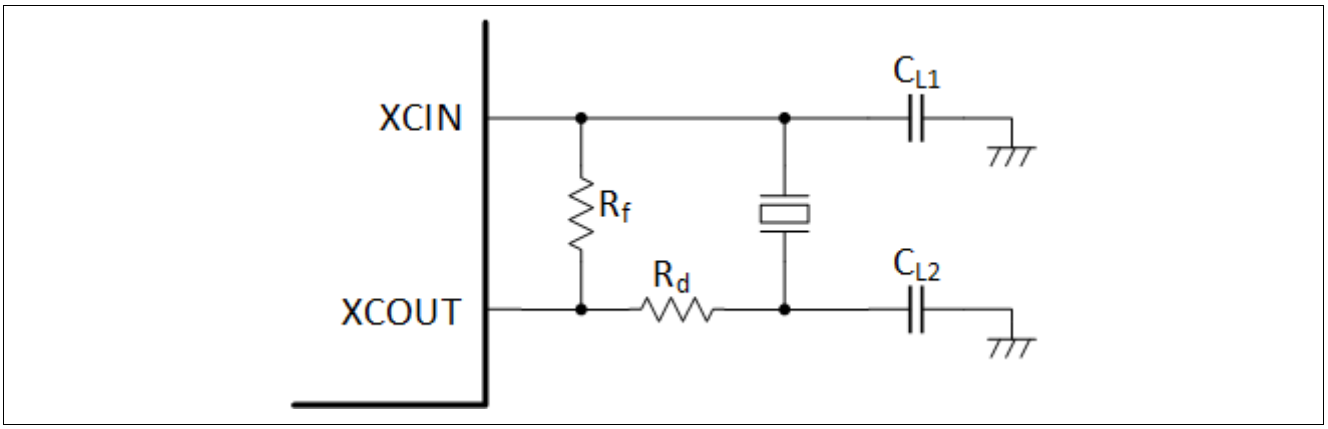

Figure 1. Example Crystal Resonator Connection for the Sub-clock

Figure 2 shows an equivalent circuit for the crystal resonator on the sub-clock circuit.

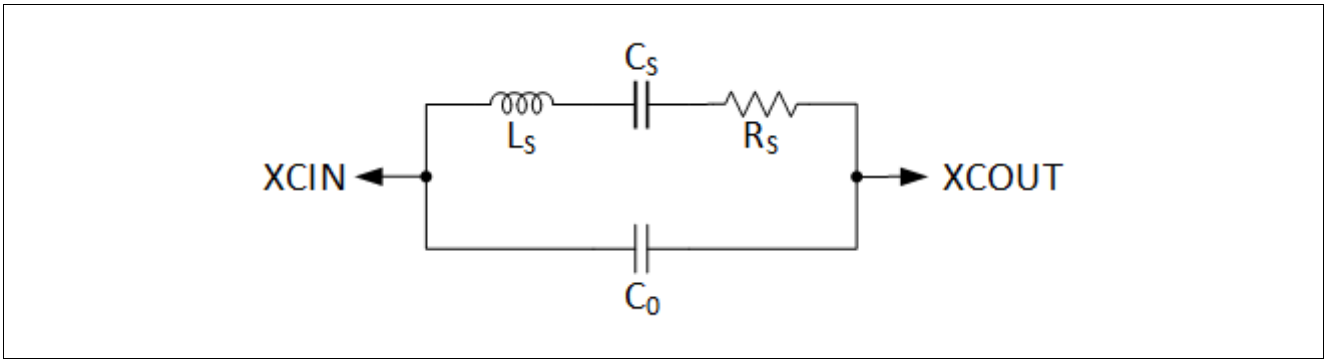

Figure 2. Equivalent Circuit for the Sub-clock Crystal Resonator

Figure 3 shows a typical example of a crystal resonator connection for the main clock source.

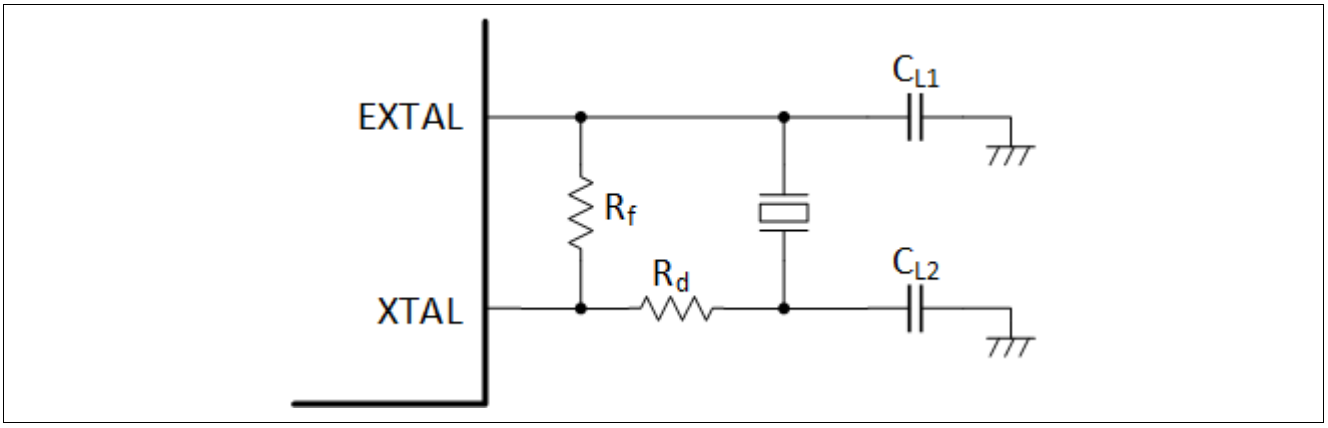

Figure 3. Example Crystal Resonator Connection for the Main Clock

Figure 4 shows an equivalent circuit for the crystal resonator on the main clock circuit.

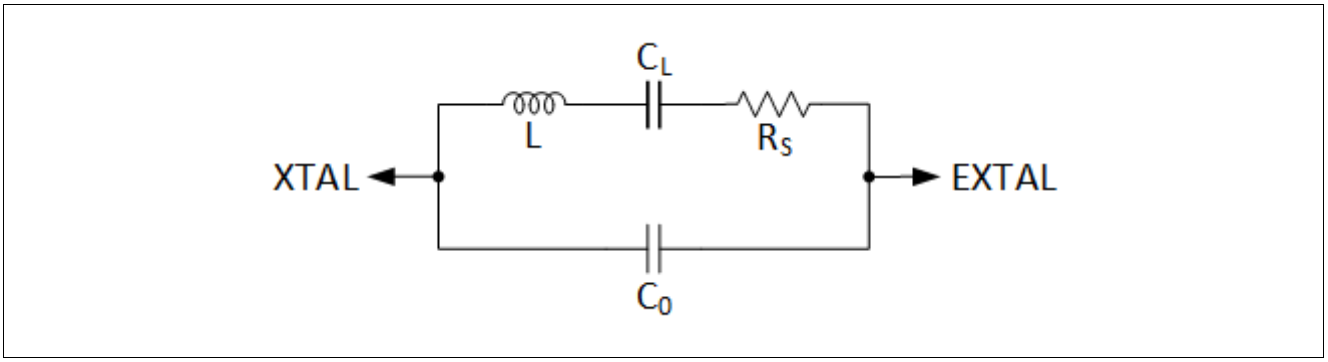

Figure 4. Equivalent Circuit of the Main Clock Crystal Resonator

Careful evaluation must be used when selecting the crystal resonator and the associated capacitors. The external feedback resistor (R_f) and damping resistor (R_d) may be added if recommended by the crystal resonator manufacturer.

Selection of the capacitor values for C_{L1} and C_{L2} will affect the accuracy of the internal clock. To understand the impact of the values for C_{L1} and C_{L2}, the circuit should be simulated using the equivalent circuit of the crystal resonator in the figures above. For more accurate results, also take in to account the stray capacitance associated with the routing between the crystal resonator components.

Some crystal resonators may have limits on the maximum current provided by the MCU. If the current provided to these crystal resonators is too high, the crystal may be damaged. A damping resistor (R_d) may be added to limit the current to the crystal resonator. Refer to the crystal resonator manufacturer to determine the value of this resistor.

1.2 Load Capacitor Selection

Crystal resonator manufacturers will typically provide a load capacitance (C_L) rating for each crystal resonator. For proper operation of the crystal resonator circuit, the board design must match the C_L value of the crystal.

There are several methods to calculate the correct values for the load capacitors C_{L1} and C_{L2}. These calculations take into account the values of the load capacitors and the stray capacitance (C_S) of the board design, which includes the capacitance of the copper traces and the device pins of the MCU.

One equation to calculate C_L is:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_S$$

As an example, if the crystal manufacturer specifies C_L = 14 pF, and the board design has a C_S of 5 pF, the resulting C_{L1} and C_{L2} would be 18 pF. Section 2.4 in this document provides details for some verified resonator selections and the associated circuit constants for proper operation.

There are other factors that will affect the performance of the crystal. Temperature, component aging, and other environmental factors may change the performance of a crystal over time and should be accounted for in each specific design.

To ensure proper operation, each circuit should be tested under the expected environmental conditions to guarantee correct performance.

2. Board Design

2.1 Component Placement

Placement of the crystal oscillator, load capacitors, and optional resistors can have a significant impact on the performance of the clock circuit.

For reference within this document, “component side” refers to same side of the PCB design as the MCU, and “solder side” refers to the opposite side of the PCB design from the MCU.

It is recommended to place the crystal resonator circuit as close as possible to the MCU pins on the component side of the PCB. The load capacitors and optional resistors should also be placed on the component side and should be placed between the crystal resonator and the MCU. An alternate placement is to place the crystal resonator between the MCU pins and the load capacitors, but additional ground routing will need to be considered.

Low C_L crystal oscillators are sensitive to fluctuations in temperature, which can affect the stability of the sub-clock circuit. To reduce the influence of temperature on the sub-clock circuit, keep other components which may produce excessive heat away from the crystal oscillator. If copper areas are used as a heat sink for other components, keep the copper heat sink away from the crystal oscillator.

2.2 Routing – Best Practices

This section describes key points on proper layout of a crystal resonator circuit for RA MCU devices.

2.2.1 XCIN and XCOUT Routing

The following list describes points on routing for XCIN and XCOUT. Figure 5, Figure 6, and Figure 7 show examples of preferred trace routing for XCIN and XCOUT. Figure 8 shows an alternate example of trace routing for XCIN and XCOUT. Identification numbers in the Figures refer to this list.

1. Do not cross the XCIN and XCOUT traces with other signal traces.
2. Do not add an observation pin or test point to XCIN or XCOUT traces.
3. Make the XCIN and XCOUT trace width between 0.1 mm and 0.3 mm. The trace length from the MCU pins to the crystal resonator pins should be less than 10 mm. If 10 mm is not possible, make the trace length as short as possible.
4. The trace connected to the XCIN pin and the trace connected to the XCOUT pin should have as much space between them (at least 0.3 mm) as possible.
5. Connect external capacitors as close together as possible. Connect the traces for the capacitors to the ground trace (hereinafter referred to as the “ground shield”) on the component side. For details on the ground shield, refer to section 2.2.2. When the capacitors cannot be placed using the preferred placement, use the placement shown in Figure 8.
6. In order to decrease the parasitic capacitance between XCIN and XCOUT, include a ground trace between the resonator and the MCU.

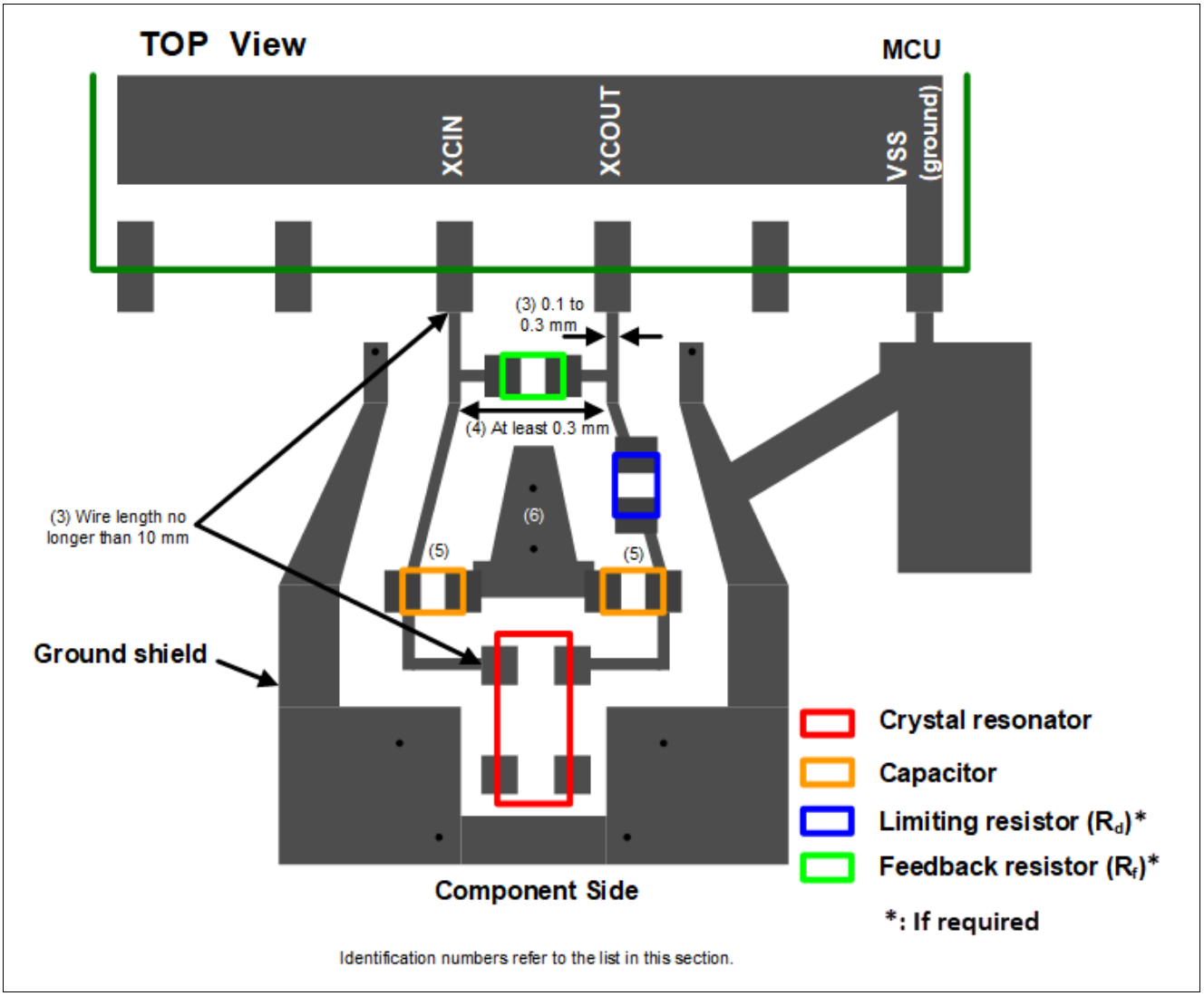

Figure 5. Example of Preferred Placement and Routing for XCIN and XCOUT, LQFP Packages

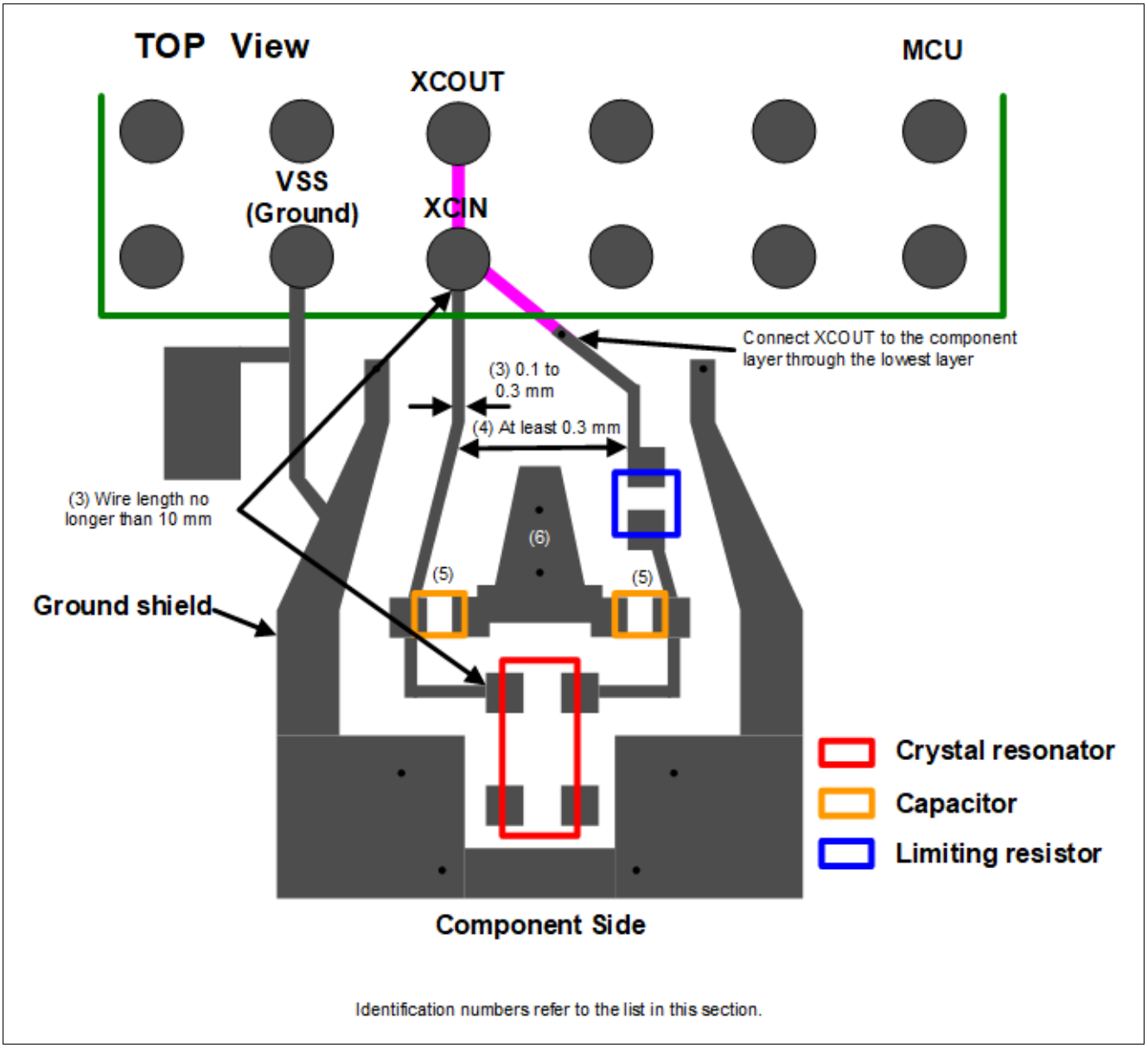

Figure 6. Example of Preferred Placement and Routing for XCIN and XCOUT, LGA Packages

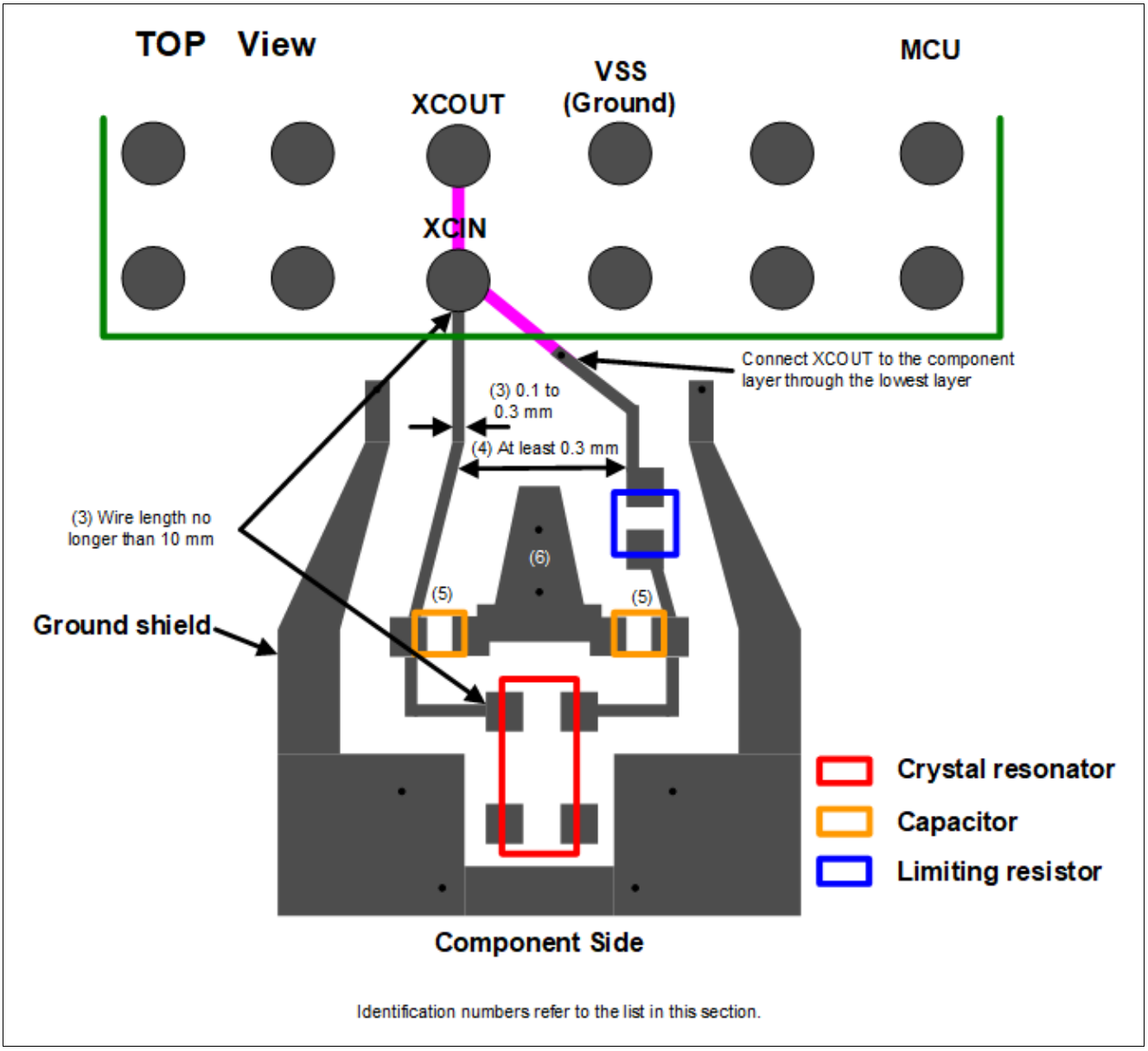

Figure 7. Example of Preferred Placement and Routing for XCIN and XCOUT, BGA Packages

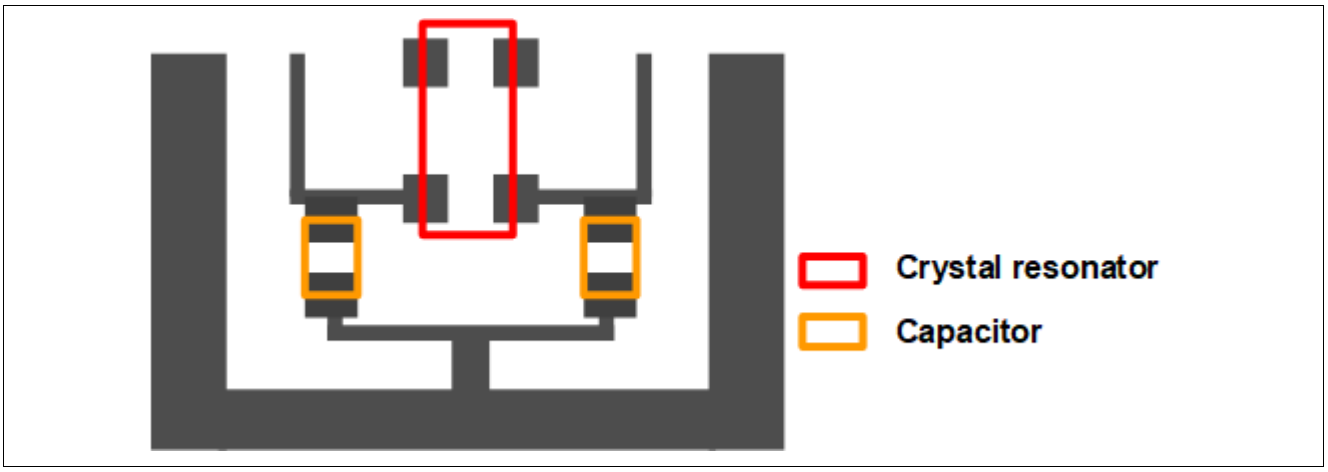

Figure 8. Example of Alternate Placement and Routing for XCIN and XCOUT

2.2.2 Ground Shield

Shield the crystal resonator with a ground trace. The following list describes the points regarding the ground shield. Figure 9, Figure 10, and Figure 11 show routing examples for each package. Identification numbers in each figure refer to this list.

1. Lay out the ground shield on the same layer as the crystal resonator trace routing.
2. Make the ground shield trace width at least 0.3 mm and leave a 0.3 to 2.0 mm gap between the ground shield and other traces.
3. Route the ground shield as close to the VSS pin on the MCU as possible and ensure that the trace width is at least 0.3 mm.
4. To prevent current through the ground shield, branch the ground shield and the ground on the board near the VSS pin on the board.

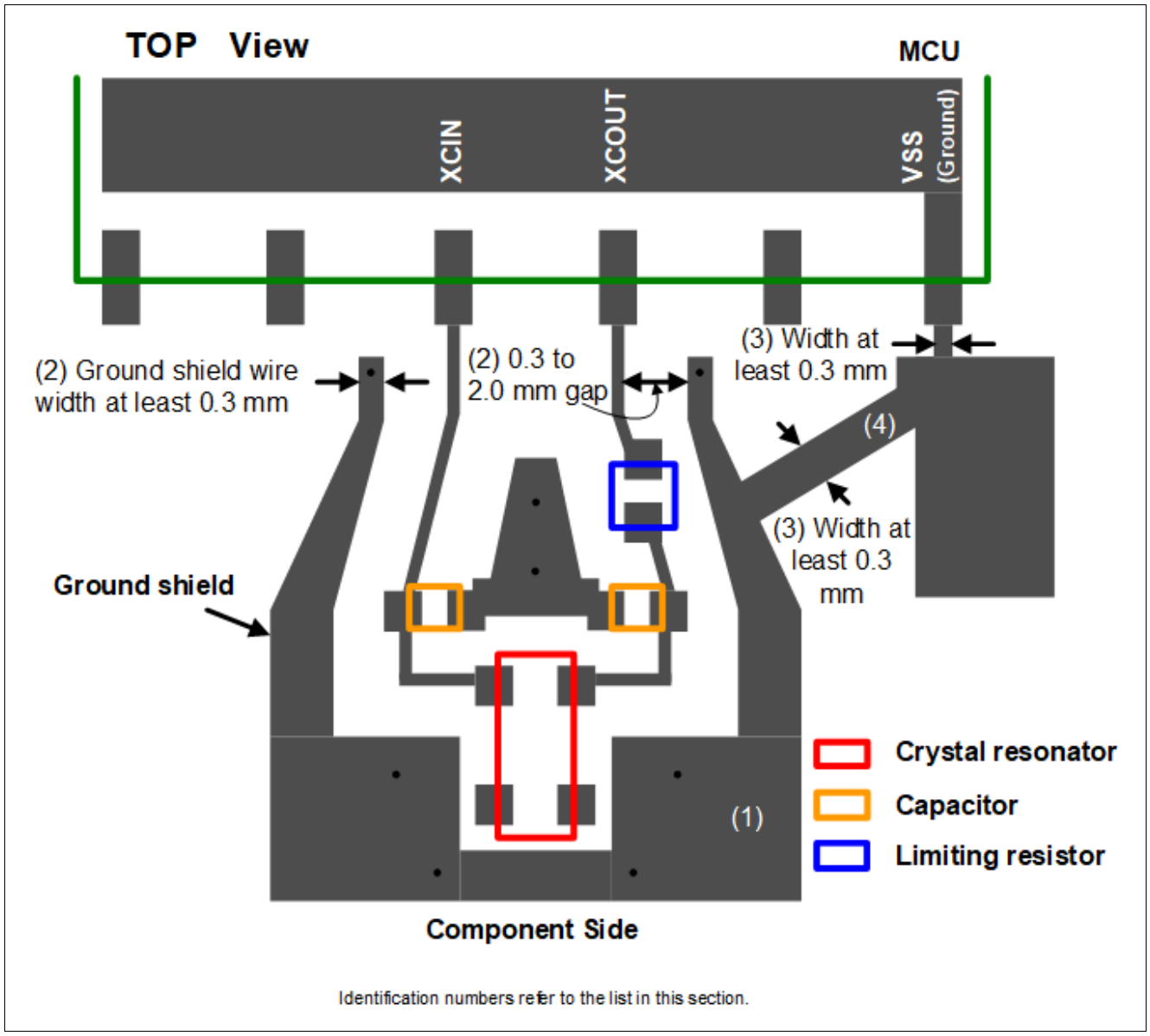

Figure 9. Trace Example for the Ground Shield, LQFP Packages

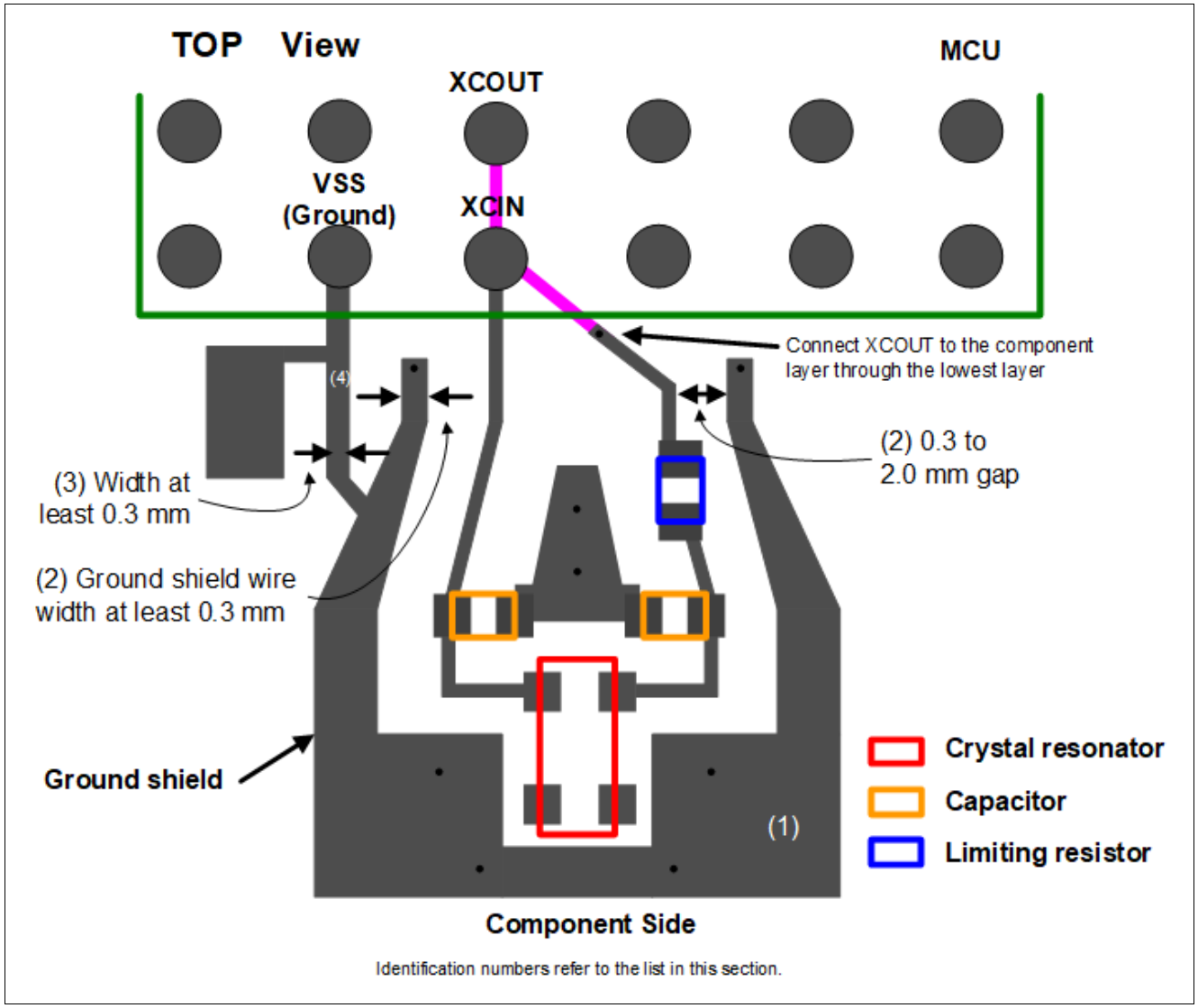

Figure 10. Trace Example for the Ground Shield, LGA Packages

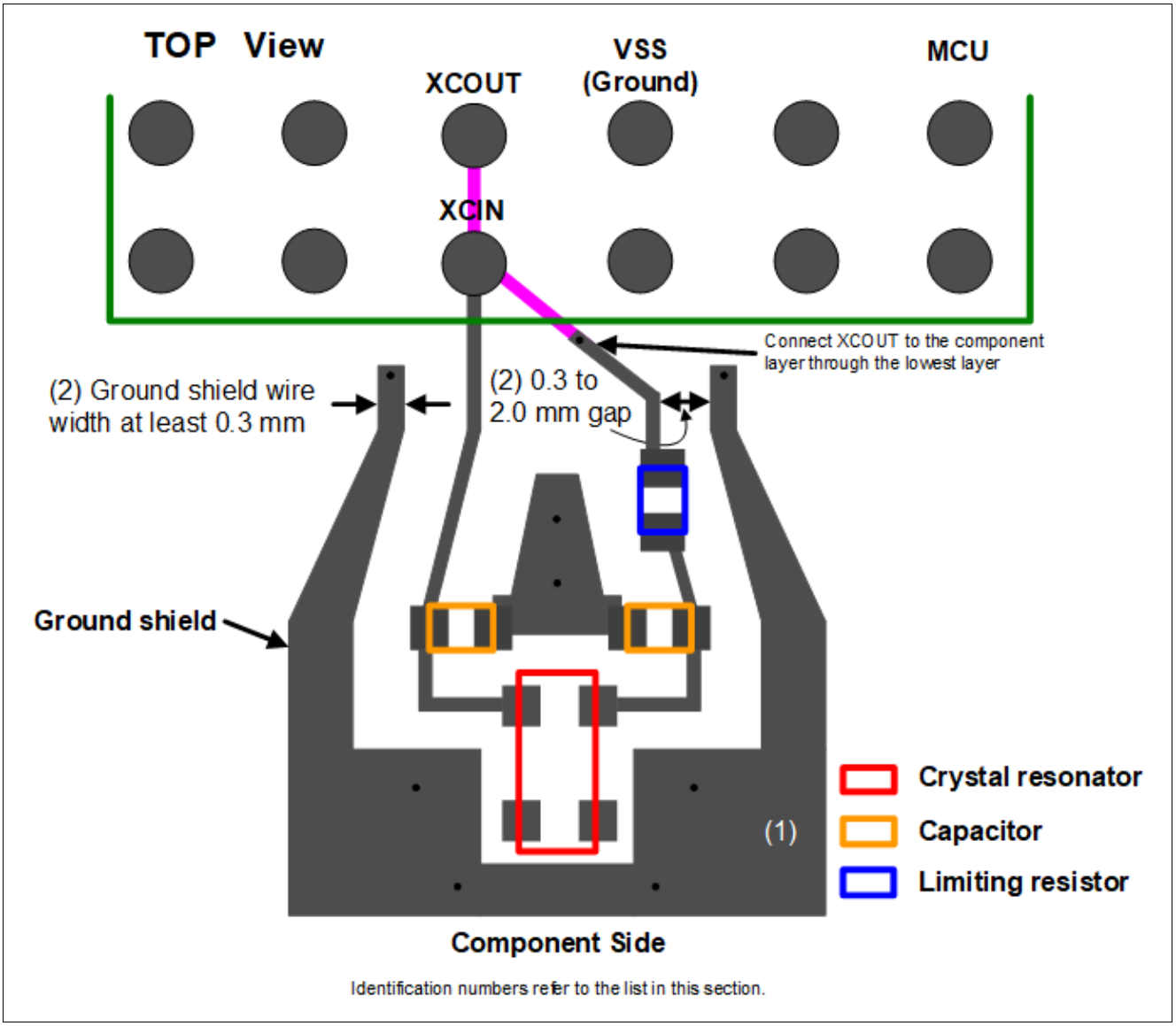

Figure 11. Trace Example for the Ground Shield, BGA Packages

2.2.3 Bottom Ground

2.2.3.1 Multilayered Boards at Least 1.2 mm Thick

For boards that are at least 1.2 mm thick, lay out a ground trace on the solder side (hereinafter referred to as bottom ground) of the crystal resonator area.

The following list describes points when making a multilayered board that is at least 1.2 mm thick. Figure 12, Figure 13, and Figure 14 show routing examples for each package type. Identification numbers in each figure refer to this list.

1. Do not lay out any traces in the middle layers of the crystal resonator area. Do not lay out power supply or ground traces in this area. Do not pass signal traces through this area.
2. Make the bottom ground at least 0.1 mm bigger than the ground shield.
3. Connect the bottom ground on the solder side only to the ground shield on the component side before connecting it to the VSS pin.

Additional notes:

- For LQFP and TFLGA packages, only connect the ground shield to the bottom ground of the component side of the board. Connect the bottom ground to the VSS pin through the ground shield. Do not connect the bottom ground or the ground shield to a ground other than the VSS pin.

- For LFBGA packages, connect the bottom ground directly to the VSS pin. Do not connect the bottom ground or the ground shield to a ground other than the VSS pin.

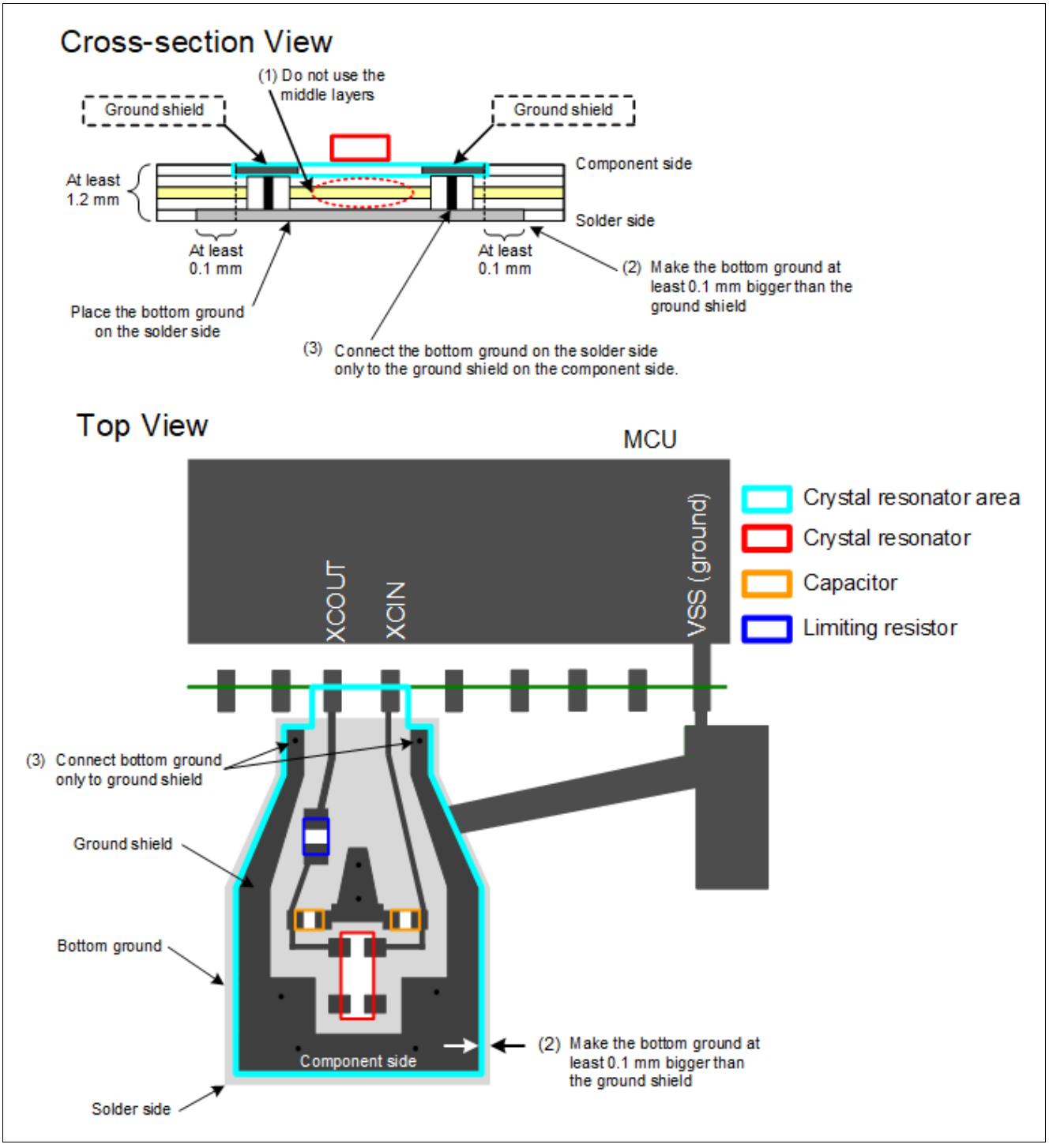

Figure 12. Routing Example When a Multilayered Board is at Least 1.2 mm Thick, LQFP Packages

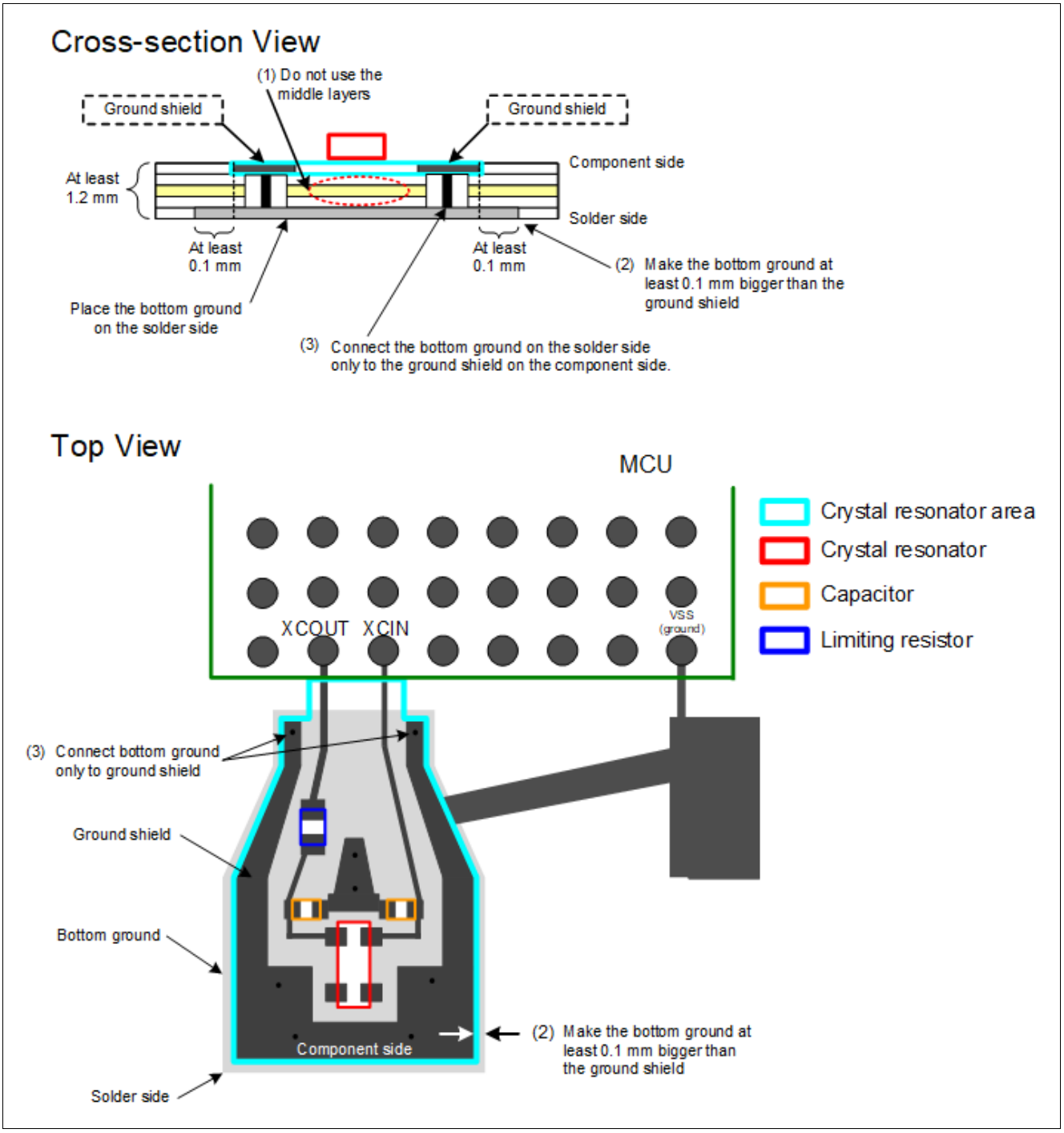

Figure 13. Routing Example When a Multilayered Board is at Least 1.2 mm Thick, LGA Packages

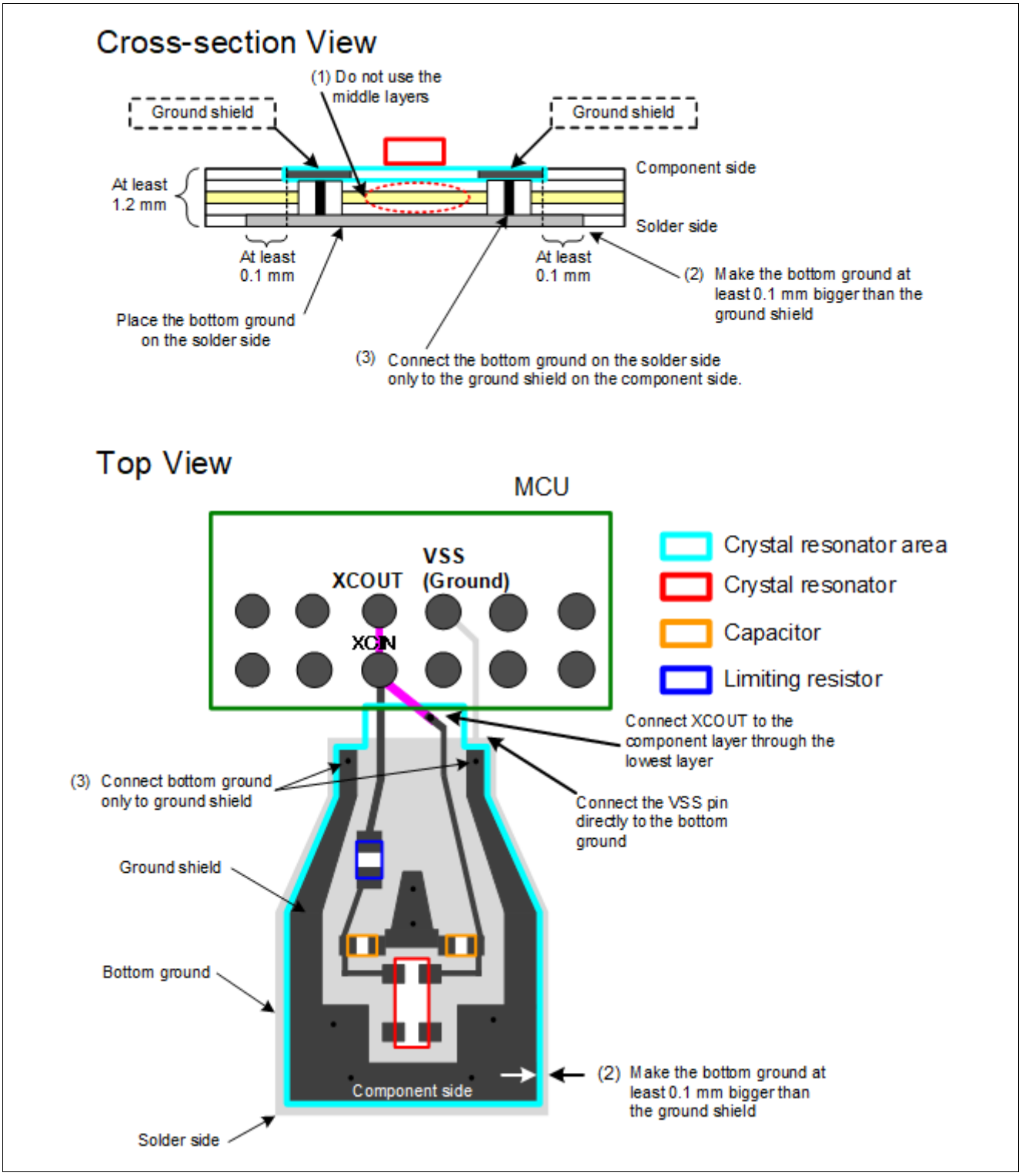

Figure 14. Routing Example When a Multilayered Board is at Least 1.2 mm Thick, BGA Packages

2.2.3.2 Multilayered Boards Less than 1.2 mm Thick

The following describes points when making a multilayered board that is less than 1.2 mm thick. Figure 15 shows a routing example.

- Do not lay out any traces to layers other than the component side for the crystal resonator area. Do not lay out power supply and ground traces in this area. Do not pass signal traces through this area.

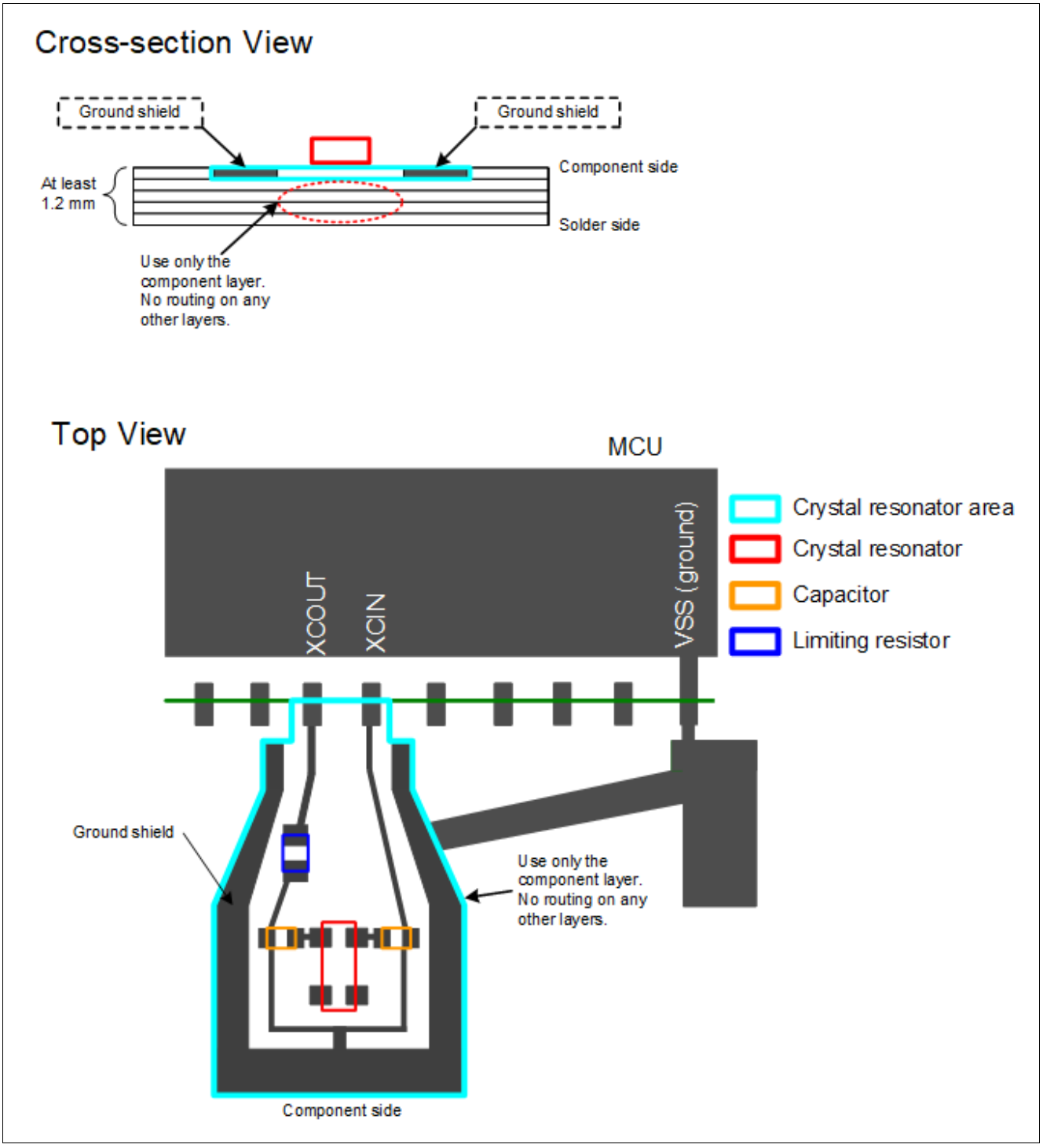

Figure 15. Routing Example When a Multilayered Board is Less Than 1.2 mm Thick, LQFP Packages

2.2.4 Other Points

The following list describes other points to consider, and Figure 16 shows a routing example when using an LQFP package. The same points apply to any package type. Identification numbers in the figure refer to this list.

1. Do not place the XCIN and XCOUT traces near traces that have big changes in current.
2. Do not route the XCIN and XCOUT traces parallel to other signal traces, such as those for adjacent pins.
3. Traces for pins that are adjacent to the XCIN and XCOUT pins should be routed away from the XCIN and XCOUT pins. Route the traces toward the center of the MCU first, then route the traces away from the XCIN and XCOUT pins. This is recommended to avoid routing of traces parallel to the XCIN and XCOUT traces.

4. Lay out as much of the ground trace on the bottom side of the MCU as possible.

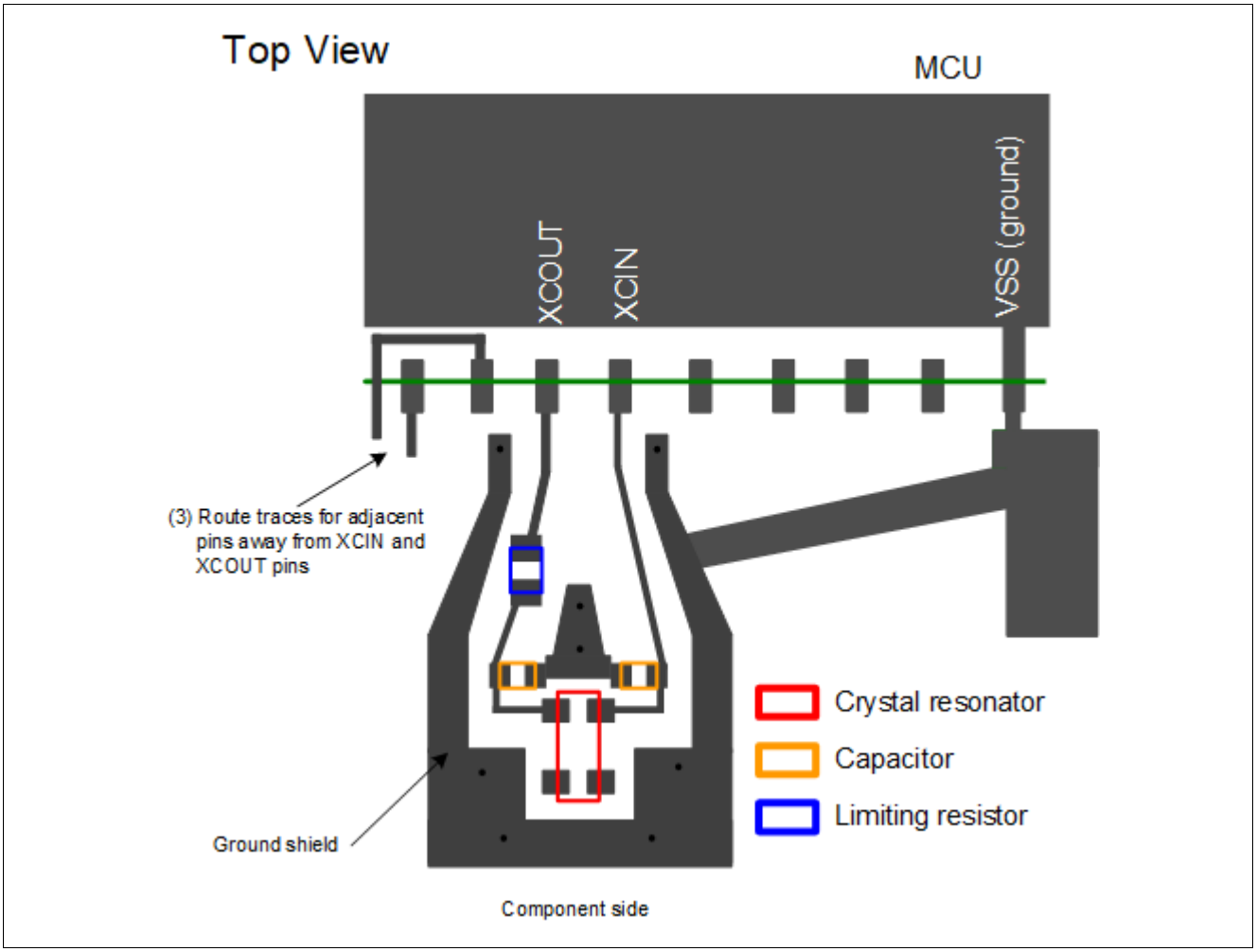

Figure 16. Routing Example for Other Points, LQFP Package Example

2.2.5 Main Clock Resonator

This section describes points on routing the main clock resonator. Figure 17 shows a routing example.

- Shield the main clock resonator with a ground.
- Do not connect the ground shield for the main clock resonator to the ground shield for the sub-clock. If the main clock ground shield is connected directly to the sub-clock ground shield, there is a possibility that noise from the main clock resonator may transfer through and affect the sub-clock.
- When placing and routing the main clock resonator, follow the same guidelines as explained for the sub-clock oscillator.

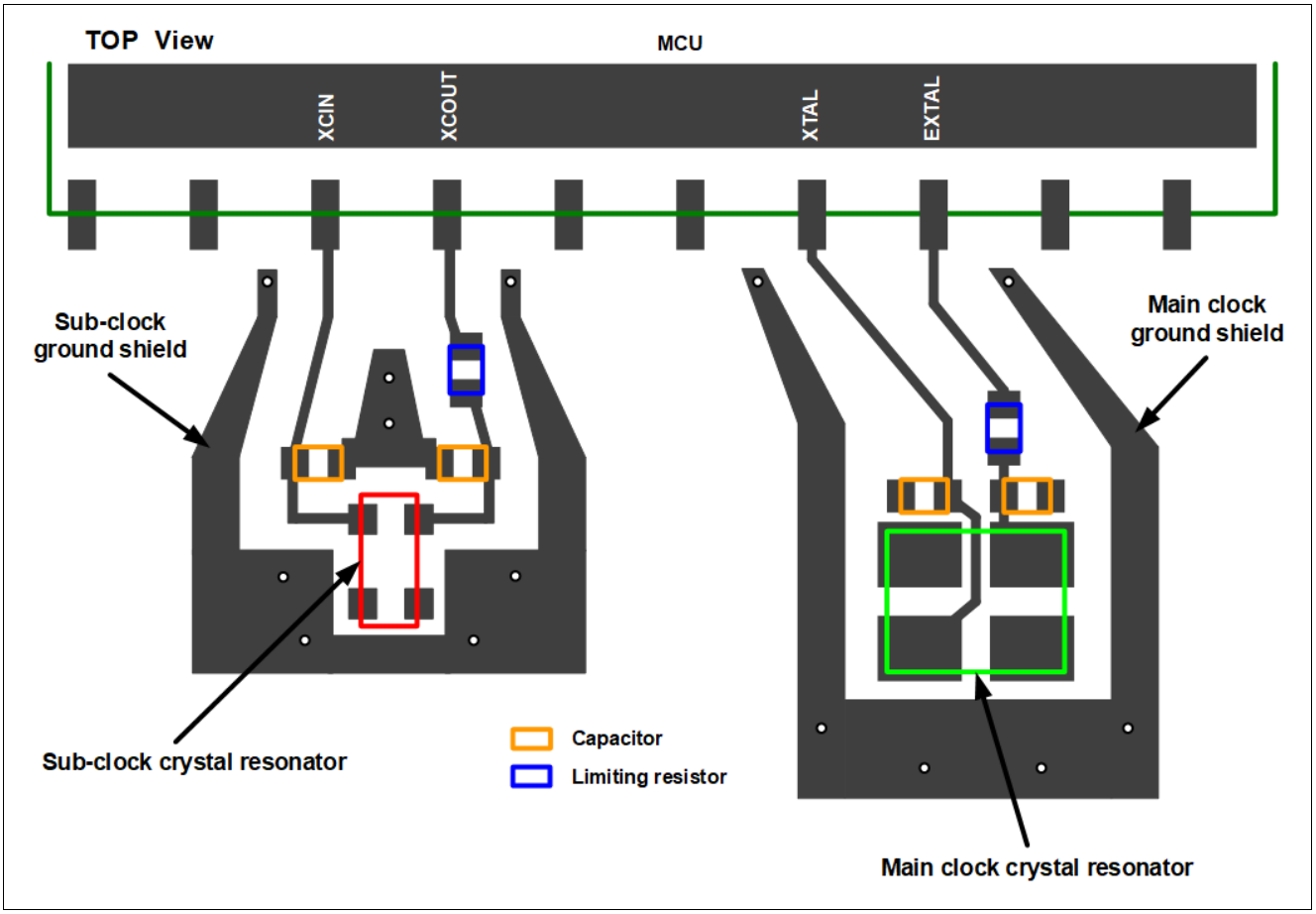

Figure 17. Routing Example When Shielding the Main Clock Resonator with a Ground Shield

2.3 Routing – Errors to Avoid

When routing the sub-clock circuit, be cautious to avoid any of the following points. Routing the traces with any of these issues may cause the low C_L resonator to not oscillate correctly. Figure 18 shows a routing example and points out the routing errors. Identification numbers in the figure refer to this list.

1. XCIN and XCOUT traces cross other signal traces. (Risk of erroneous operation.)
2. Observation pins (test points) are attached to XCIN and XCOUT. (Risk of oscillation stopping.)
3. XCIN and XCOUT wires are long. (Risk of erroneous operation or decreased accuracy.)
4. The ground shield does not cover the entire area, and where there is a ground shield, the routing is long and narrow. (Easily affected by noise, and there is a risk that accuracy will decrease from the ground potential difference generated by the MCU and external capacitor.)
5. Ground shield has multiple VSS connections in addition to the VSS pin. (Risk of erroneous operation from MCU current flowing through the ground shield.)
6. Power supply or ground traces are under the XCIN and XCOUT traces. (Risk of losing the clock or oscillation stopping.)
7. A trace with a large current is routed nearby. (Risk of erroneous operation.)
8. Parallel traces for adjacent pins are close and long. (Risk of losing the clock or oscillation stopping.)
9. The middle layers are used for routing. (Risk of oscillation characteristics decreasing or signals operating erroneously.)

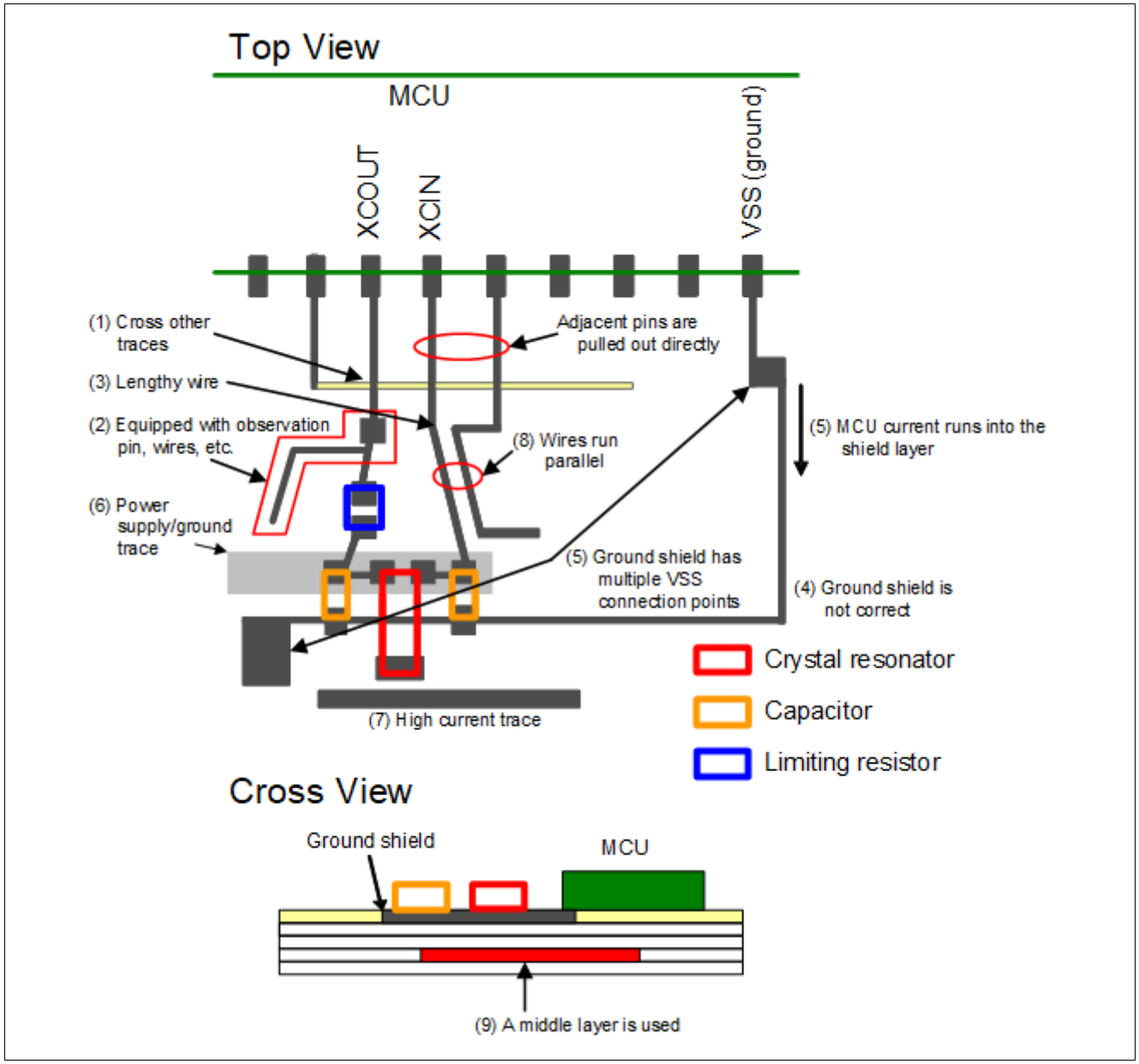

Figure 18. Routing Example Showing a High Risk of Erroneous Operation Due to Noise

2.4 Reference Oscillation Circuit Constants and Verified Resonator Operation

Table 1 lists the reference oscillation circuit constants for the verified crystal resonator operation. Figure 1 at the beginning of this document shows an example circuit for the verified resonator operation.

Table 1. Reference Oscillation Circuit Constants for Verified Resonator Operation

Manufacturer	Series	SMD/ Leaded	Frequency (kHz)	C_L (pF)	C_{L1}(pF)	C_{L2}(pF)	R_d(kΩ)
Kyocera	ST3215SB	SMD	32.768	12.5	22	22	0
				9	15	15	0
				6	9	9	0
				7	10	10	0
				4	1.8	1.8	0

Note that not all RA MCU devices are listed on the Kyocera website, and sub-clock oscillator recommendations are not listed for most RA MCU devices. Data in this table includes recommendations for other comparable Renesas MCU devices.

The verified resonator operation and reference oscillation circuit constants listed here are based on information from the resonator manufacturer and are not guaranteed. As reference oscillation circuit constants are measurements surveyed under fixed conditions by the manufacturer, values measured in the user system may vary. To achieve optimum reference oscillation circuit constants for use in the actual user system, inquire with the resonator manufacturer to perform an evaluation on the actual circuit.

The conditions in the figure are conditions for oscillating the resonator connected to the MCU and are not operating conditions for the MCU itself. Refer to the specifications in the electrical characteristics for details on the MCU operating conditions.

Website and Support

Visit the following URLs to learn about key elements of the RA family, download components and related documentation, and get support.

RA Product Information	www.renesas.com/ra
RA Product Support Forum	www.renesas.com/ra/forum
RA Flexible Software Package	www.renesas.com/FSP
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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan.7.2022	—	Initial release

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(Rev.4.0-1 November 2017)

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