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## R8C/M12A Group

Output Compare Function of Timer RC

R01AN0105EJ0111

Rev.1.11

Mar. 31, 2011

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### 1. Abstract

This document describes a setting method and an application example of toggle output using timer RC timer mode (output compare function) in the R8C/M12A Group.

### 2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/M12A Group
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

### 3. Application Example

#### 3.1 Program Outline

Toggle output is performed from the TRCIOA pin every 100  $\mu\text{s}$  using timer RC timer mode (output compare function).

##### Settings

- Use timer mode.
- Do not use the TRCGRC register as the buffer register of the TRCGRA register.
- Select the initial output level of the TRCIOA pin as low level.
- Select f1 (20 MHz) as the count source.
- Clear the TRCCNT counter at compare match A.
- Perform toggle output to the TRCIOA pin at compare match A.
- Use the output compare function.
- Continue incrementing for the TRCCNT register at compare match A.
- Enable TRCIOA output.
- Do not disable TRCIOA output by low input to the  $\overline{\text{INT0}}$  pin.
- Disable the A/D conversion start trigger.
- Disable waveform output manipulation.
- Do not use the timer RC interrupt.

##### Calculating the setting time

$$\begin{aligned} 100 \mu\text{s} &= 1/f1 \times (\text{TRCGRA} + 1) \\ &= 1/20 \text{ MHz} \times (1999 + 1) \\ &= 50 \text{ ns} \times 2000 \end{aligned}$$

Figure 3.1 shows a Block Diagram and Figure 3.2 shows a Timing Diagram. Table 3.1 lists the pin used and its function.

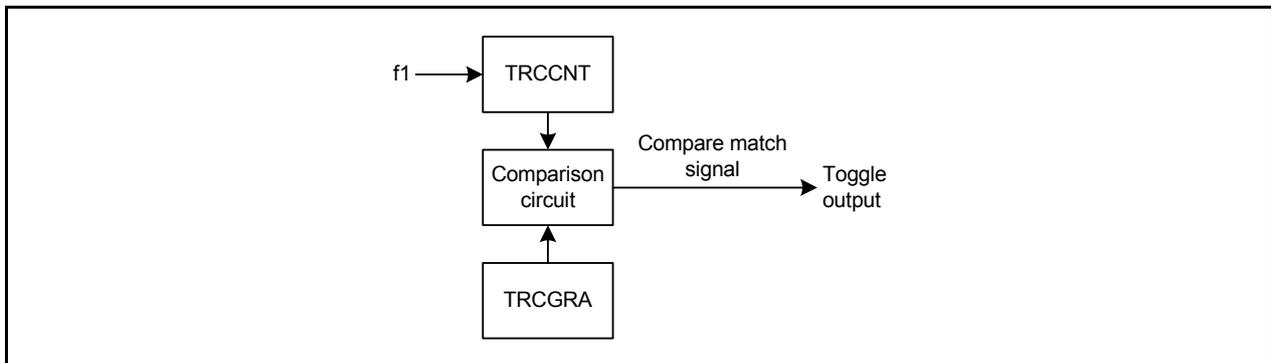


Figure 3.1 Block Diagram

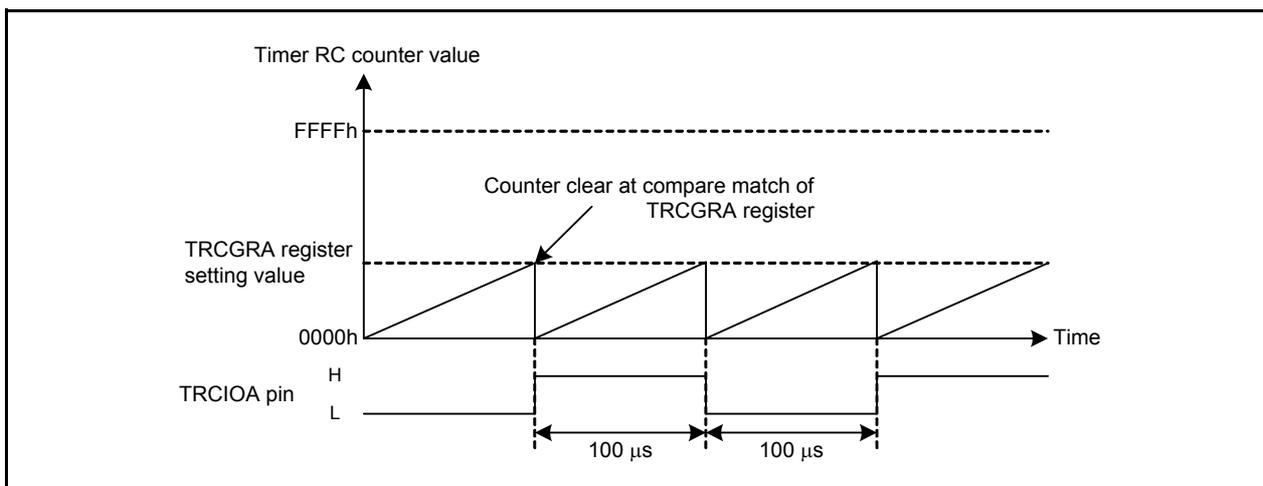


Figure 3.2 Timing Diagram

Table 3.1 Pin Used and Its Function

| Pin Name    | I/O    | Function                     |
|-------------|--------|------------------------------|
| P1_1/TRCIOA | Output | TRCGRA output compare output |

### 3.2 Memory

Table 3.2 Memory

| Memory                  | Size      | Remarks                       |
|-------------------------|-----------|-------------------------------|
| ROM                     | 159 bytes | In the r01an0105_src.c module |
| RAM                     | 0 bytes   | In the r01an0105_src.c module |
| Maximum user stack      | 10 bytes  |                               |
| Maximum interrupt stack | 0 bytes   |                               |

Memory size varies depending on the C compiler version and compile options.

The above applies to the following conditions:

C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01

Compile options: -c -finfo -dir "\${CONFIGDIR}" -R8C

## 4. Software

This section shows the initial setting procedures and values to set the example described in section 3. **Application Example.** Refer to the latest **R8C/M12A Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

### 4.1 Function Tables

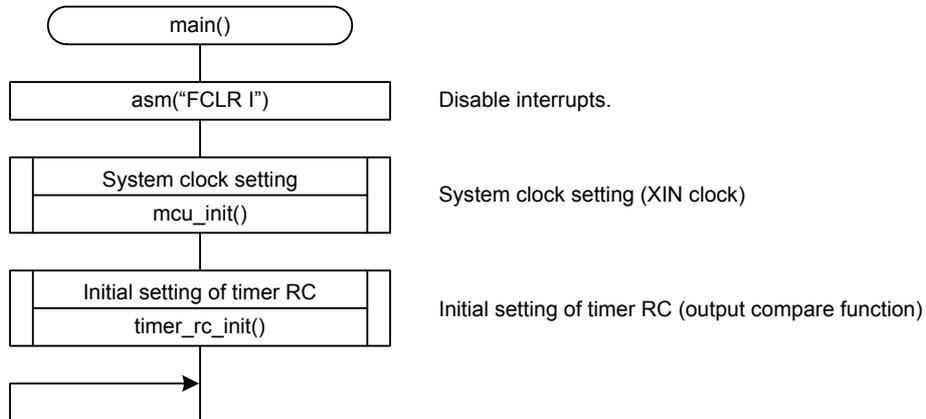
|                   |   |       |          |
|-------------------|---|-------|----------|
| Declaration       | void main (void)                          |       |          |
| Outline           | Main function                             |       |          |
| Argument          | Argument name                             |       | Meaning  |
|                   | None                                      |       | —        |
| Variable (global) | Variable name                             |       | Contents |
|                   | None                                      |       | —        |
| Returned value    | Type                                      | Value | Meaning  |
|                   | None                                      | —     | —        |
| Function          | Initialize the system clock and timer RC. |       |          |

|                   |                                   |       |          |
|-------------------|-----------------------------------|-------|----------|
| Declaration       | void mcu_init (void)              |       |          |
| Outline           | System clock setting              |       |          |
| Argument          | Argument name                     |       | Meaning  |
|                   | None                              |       | —        |
| Variable (global) | Variable name                     |       | Contents |
|                   | None                              |       | —        |
| Returned value    | Type                              | Value | Meaning  |
|                   | None                              | —     | —        |
| Function          | Set the system clock (XIN clock). |       |          |

|                   |  |       |          |
|-------------------|--|-------|----------|
| Declaration       | void timer_rc_init (void)  |       |          |
| Outline           | Initial setting of timer RC  |       |          |
| Argument          | Argument name  |       | Meaning  |
|                   | None   |       | —        |
| Variable (global) | Variable name  |       | Contents |
|                   | None   |       | —        |
| Returned value    | Type   | Value | Meaning  |
|                   | None   | —     | —        |
| Function          | Initialize SFRs to use timer RC in timer mode (output compare function). |       |          |

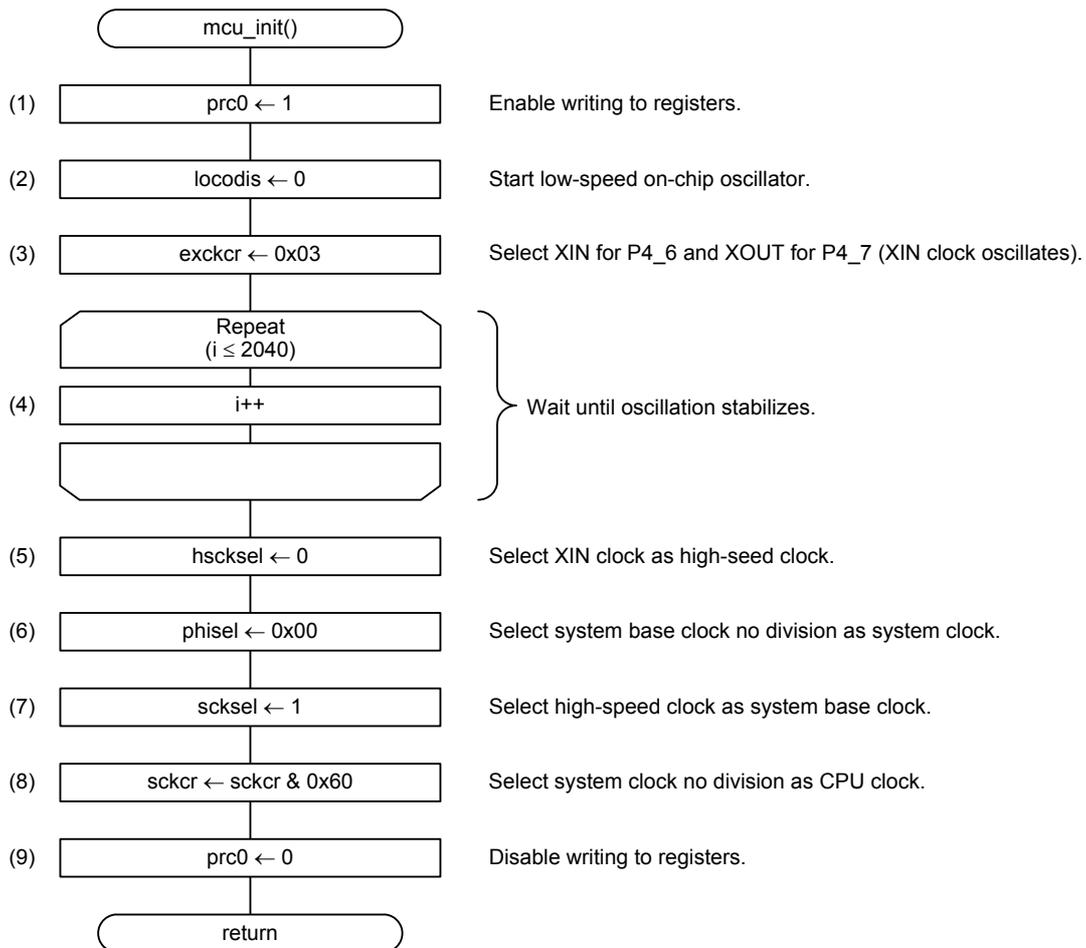
### 4.2 Main Function

• Flowchart



### 4.3 System Clock Setting

• Flowchart



- Register settings

- (1) Enable writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2.

## Protect Register (PRCR)

|               |    |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|----|
| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Setting Value | —  | —  | —  | x  | x  | —  | x  | 1  |

| Bit | Symbol | Bit Name      | Function   | R/W |
|-----|--------|---------------|--|-----|
| b0  | PRC0   | Protect bit 0 | Enables writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2<br>1: Enabled | R/W |

- (2) Start the low-speed on-chip oscillator.

## High-Speed/Low-Speed On-Chip Oscillator Control Register (OCOCR)

|               |    |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|----|
| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Setting Value | —  | —  | —  | —  | —  | —  | 0  | x  |

| Bit | Symbol  | Bit Name  | Function                           | R/W |
|-----|---------|---|------------------------------------|-----|
| b1  | LOCODIS | Low-speed on-chip oscillator oscillation stop bit | 0: Low-speed on-chip oscillator on | R/W |

- (3) Oscillate the XIN clock.

## External Clock Control Register (EXCKCR)

|               |    |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|----|
| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Setting Value | —  | x  | —  | —  | —  | —  | 1  | 1  |

| Bit | Symbol | Bit Name                                    | Function          | R/W |
|-----|--------|---|-------------------|-----|
| b0  | CKPT0  | Port P4_6 and P4_7 pin function select bits | P4_6 pin<br>b1 b0 | R/W |
| b1  | CKPT1  |   | 1 1: XIN          | R/W |
|     |        |   | P4_7 pin<br>b1 b0 |     |
|     |        |   | 1 1: XOUT         |     |

- (4) Wait until the XIN clock oscillation stabilizes.

- (5) Set the XIN clock as the high-speed clock.

## System Clock f Control Register (SCKCR)

|               |    |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|----|
| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Setting Value | —  | 0  | x  | —  | —  |    |    |    |

| Bit | Symbol  | Bit Name   | Function     | R/W |
|-----|---------|--|--------------|-----|
| b6  | HSCKSEL | High-speed on-chip oscillator/XIN clock select bit | 0: XIN clock | R/W |

- (6) Set the system base clock with no division as the system clock.

## System Clock f Select Register (PHISEL)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit | Symbol  | Bit Name                          | Function  | R/W |
|-----|---------|-----------------------------------|---|-----|
| b0  | PHISEL0 | System clock division select bits | These bits used to set the division ratio of the system base clock (fBASE) to generate the system clock (f).<br>$f = fBASE/(n + 1)$<br>n: Binary value set by the PHISEL register | R/W |
| b1  | PHISEL1 |                                   |   | R/W |
| b2  | PHISEL2 |                                   |   | R/W |
| b3  | PHISEL3 |                                   |   | R/W |
| b4  | PHISEL4 |                                   |   | R/W |
| b5  | PHISEL5 |                                   |   | R/W |
| b6  | PHISEL6 |                                   |   | R/W |
| b7  | PHISEL7 |                                   |   | R/W |

- (7) Set the high-speed clock as the system base clock.

## Clock Stop Control Register (CKSTPR)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | 1  | —  | —  | —  | —  | x  | x  | x  |

| Bit | Symbol | Bit Name                     | Function | R/W |
|-----|--------|------------------------------|----------|-----|
| b7  | SCKSEL | System base clock select bit | 1: fHSCK | R/W |

- (8) Set the system clock with no division as the CPU clock.

## System Clock f Control Register (SCKCR)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | —  | —  | x  | —  | —  | 0  | 0  | 0  |

| Bit | Symbol   | Bit Name                       | Function  | R/W |
|-----|----------|--------------------------------|---|-----|
| b0  | PHISSEL0 | CPU clock division select bits | $b2 b1 b0$<br>0 0 0: fs = System clock with no division | R/W |
| b1  | PHISSEL1 |                                |   | R/W |
| b2  | PHISSEL2 |                                |   | R/W |

- (9) Disable writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2.

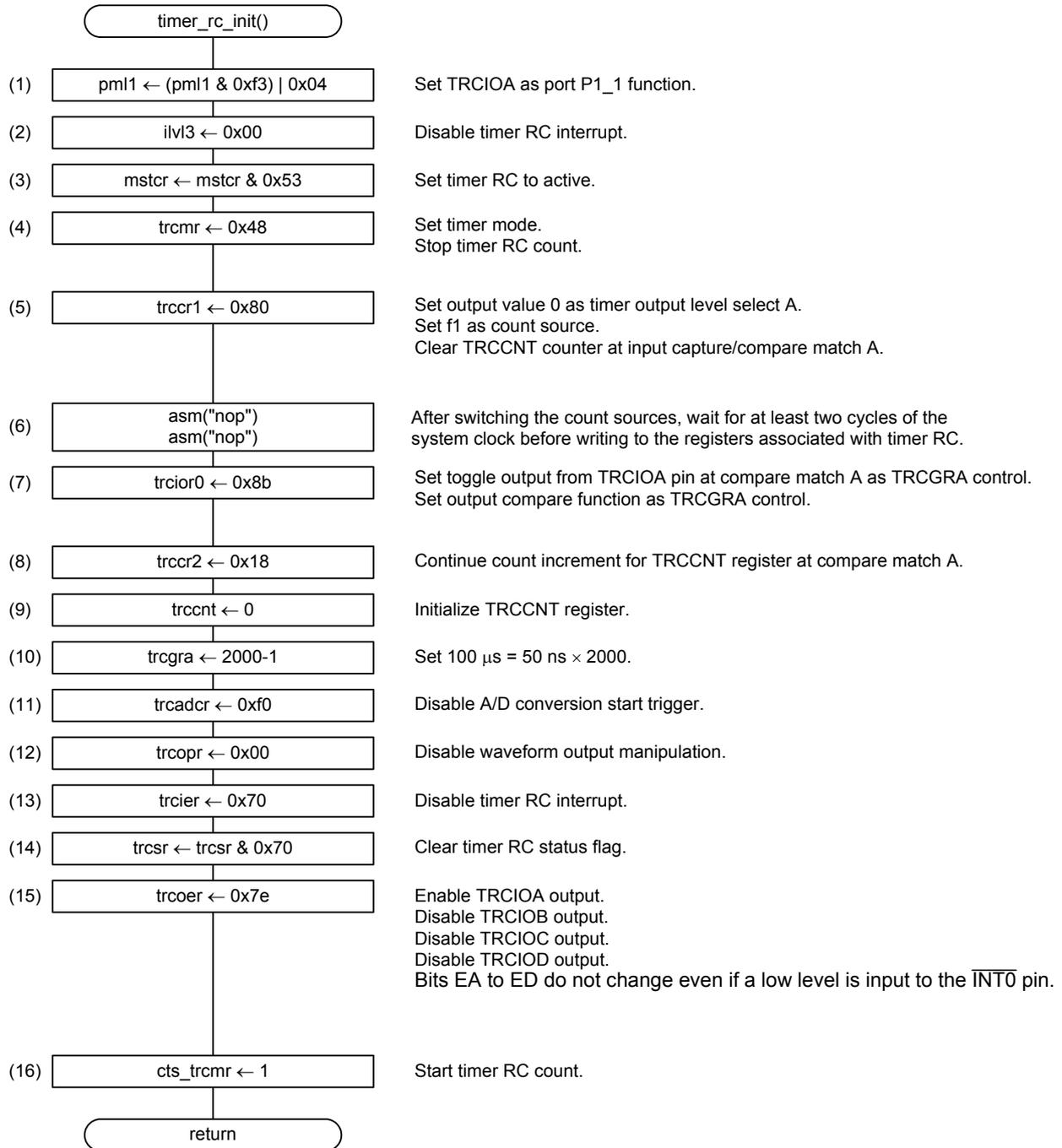
## Protect Register (PRCR)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | —  | —  | —  | x  | x  | —  | x  | 0  |

| Bit | Symbol | Bit Name      | Function  | R/W |
|-----|--------|---------------|---|-----|
| b0  | PRC0   | Protect bit 0 | Enables writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2<br>0: Disabled | R/W |

## 4.4 Initial Setting of Timer RC

### • Flowchart



- Register settings

(1) Set TRCIOA as the port P1\_1 function.

## Port 1 Function Mapping Register 0 (PML1)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | x  | x  | x  | x  | 0  | 1  | x  | x  |

| Bit | Symbol  | Bit Name                       | Function             | R/W |
|-----|---------|--------------------------------|----------------------|-----|
| b2  | P11SEL0 | Port P1_1 function select bits | b1 b0<br>0 1: TRCIOA | R/W |
| b3  | P11SEL1 |                                |                      | R/W |

(2) Disable the timer RC interrupt.

## Interrupt Priority Level Register 3 (ILVL3)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | —  | —  | 0  | 0  | —  | —  | —  | —  |

| Bit | Symbol | Bit Name                              | Function                                   | R/W |
|-----|--------|---------------------------------------|--|-----|
| b4  | ILVL34 | Interrupt priority level setting bits | b5 b4<br>0 0: Level 0 (interrupt disabled) | R/W |
| b5  | ILVL35 |                                       |  | R/W |

(3) Set timer RC to active.

## Module Standby Control Register (MSTCR)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | —  | x  | 0  | x  | —  | —  | x  | x  |

| Bit | Symbol | Bit Name             | Function  | R/W |
|-----|--------|----------------------|-----------|-----|
| b5  | MSTTRC | Timer RC standby bit | 0: Active | R/W |

(4) Set the timer RC mode register.

## Timer RC Mode Register (TRCMR)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | 0  | —  | x  | x  | 1  | x  | x  | x  |

| Bit | Symbol | Bit Name               | Function                  | R/W |
|-----|--------|------------------------|---------------------------|-----|
| b3  | PWM2   | PWM2 mode select bit   | 1: Timer mode or PWM mode | R/W |
| b7  | CTS    | TRCCNT count start bit | 0: Count is stopped       | R/W |

(5) Set timer RC control register 1.

#### Timer RC Control Register 1 (TRCCR1)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | 1  | 0  | 0  | 0  | x  | x  | x  | 0  |

| Bit | Symbol | Bit Name                        | Function  | R/W |
|-----|--------|---------------------------------|---|-----|
| b0  | TOA    | Timer output level select A bit | 0: Output value 0   | R/W |
| b4  | CKS0   | Count source select bits        | b6 b5 b4<br>0 0 0: f1   | R/W |
| b5  | CKS1   |                                 |   | R/W |
| b6  | CKS2   |                                 |   | R/W |
| b7  | CCLR   | TRCCNT counter clear select bit | 1: TRCCNT counter is cleared by input capture/compare match A | R/W |

(6) Wait for at least two cycles of the system clock.

(7) Set timer RC I/O control register 0.

#### Timer RC I/O Control Register 0 (TRCIOR0)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | —  | x  | x  | x  | —  | 0  | 1  | 1  |

| Bit | Symbol | Bit Name              | Function   | R/W |
|-----|--------|-----------------------|--|-----|
| b0  | IOA0   | TRCGRA control A0 bit | b1 b0<br>1 1: Toggle output from TRCIOA pin at compare match A | R/W |
| b1  | IOA1   | TRCGRA control A1 bit |  | R/W |
| b2  | IOA2   | TRCGRA control A2 bit | 0: Output compare function                                     | R/W |

(8) Set timer RC control register 2.

#### Timer RC Control Register 2 (TRCCR2)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | x  | x  | 0  | —  | —  | x  | x  | x  |

| Bit | Symbol | Bit Name       | Function                  | R/W |
|-----|--------|----------------|---------------------------|-----|
| b5  | CSTP   | Count stop bit | 0: Increment is continued | R/W |

- (9) Initialize the timer RC counter to 0000h.

## Timer RB Counter (TRCCNT)

|               |     |     |     |     |     |     |    |    |
|---------------|-----|-----|-----|-----|-----|-----|----|----|
| Bit           | b7  | b6  | b5  | b4  | b3  | b2  | b1 | b0 |
| Setting Value | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  |
| Bit           | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
| Setting Value | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  |

| Bit    | Function                             | Setting Range  | R/W |
|--------|--------------------------------------|----------------|-----|
| b15-b0 | 16-bit readable/writable up counter. | 0000h to FFFFh | R/W |

- (10) Set compare value 2000-1 (07CFh) with the timer RC counter to timer RC general register A.

## Timer RC General Register A (TRCGRA)

|               |     |     |     |     |     |     |    |    |
|---------------|-----|-----|-----|-----|-----|-----|----|----|
| Bit           | b7  | b6  | b5  | b4  | b3  | b2  | b1 | b0 |
| Setting Value | 1   | 1   | 0   | 0   | 1   | 1   | 1  | 1  |
| Bit           | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
| Setting Value | 0   | 0   | 0   | 0   | 0   | 1   | 1  | 1  |

| Bit    | Function   | R/W |
|--------|--|-----|
| b15-b0 | Set compare value: 100 $\mu$ s = 50 ns $\times$ 2000 | R/W |

- (11) Set the timer RC A/D conversion trigger control register.

## Timer RC A/D Conversion Trigger Control Register (TRCADCR)

|               |    |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|----|
| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Setting Value | —  | —  | —  | —  | 0  | 0  | 0  | 0  |

| Bit | Symbol  | Bit Name                                       | Function   | R/W |
|-----|---------|--|--|-----|
| b0  | ADTRGAE | TRCGRA A/D conversion start trigger enable bit | 0: No A/D conversion start trigger occurs at compare match A | R/W |
| b1  | ADTRGBE | TRCGRB A/D conversion start trigger enable bit | 0: No A/D conversion start trigger occurs at compare match B | R/W |
| b2  | ADTRGCE | TRCGRC A/D conversion start trigger enable bit | 0: No A/D conversion start trigger occurs at compare match C | R/W |
| b3  | ADTRGDE | TRCGRD A/D conversion start trigger enable bit | 0: No A/D conversion start trigger occurs at compare match D | R/W |

(12) Set the timer RC waveform output manipulation register.

#### Timer RC Waveform Output Manipulation Register (TRCOPR)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | —  | —  | 0  | x  | x  | x  | x  | x  |

| Bit | Symbol | Bit Name                                | Function                                 | R/W |
|-----|--------|---|--|-----|
| b5  | OPE    | Waveform output manipulation enable bit | 0: Waveform output manipulation disabled | R/W |

(13) Set the timer RC interrupt enable register.

#### Timer RC Interrupt Enable Register (TRCIER)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | 0  | —  | —  | —  | 0  | 0  | 0  | 0  |

| Bit | Symbol | Bit Name   | Function  | R/W |
|-----|--------|--|---|-----|
| b0  | IMIEA  | Input capture/compare match A interrupt enable bit | 0: Interrupt request (IMIA) by IMFA bit in TRCSR register is disabled | R/W |
| b1  | IMIEB  | Input capture/compare match B interrupt enable bit | 0: Interrupt request (IMIB) by IMFB bit in TRCSR register is disabled | R/W |
| b2  | IMIEC  | Input capture/compare match C interrupt enable bit | 0: Interrupt request (IMIC) by IMFC bit in TRCSR register is disabled | R/W |
| b3  | IMIED  | Input capture/compare match D interrupt enable bit | 0: Interrupt request (IMID) by IMFD bit in TRCSR register is disabled | R/W |
| b7  | OVIE   | Timer overflow interrupt enable bit                | 0: Interrupt request (FOVI) by OVF bit in TRCSR register is disabled  | R/W |

(14) Initialize the timer RC status register.

#### Timer RC Status Register (TRCSR)

| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---------------|----|----|----|----|----|----|----|----|
| Setting Value | 0  | —  | —  | —  | 0  | 0  | 0  | 0  |

| Bit | Symbol | Bit Name                           | Function   | R/W |
|-----|--------|------------------------------------|--|-----|
| b0  | IMFA   | Input capture/compare match A flag | [Condition for setting to 0]<br>When 0 is written to this bit after reading it as 1. | R/W |
| b1  | IMFB   | Input capture/compare match B flag |  | R/W |
| b2  | IMFC   | Input capture/compare match C flag |  | R/W |
| b3  | IMFD   | Input capture/compare match D flag |  | R/W |
| b7  | OVF    | Timer overflow flag                |  | R/W |

(15) Set the timer RC output enable register.

#### Timer RC Output Enable Register (TRCOER)

|               |    |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|----|
| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Setting Value | 0  | —  | —  | —  | 1  | 1  | 1  | 0  |

| Bit | Symbol | Bit Name                  | Function   | R/W |
|-----|--------|---------------------------|--|-----|
| b0  | EA     | TRCIOA output disable bit | 0: Output enabled<br>(dependent on settings of registers TRCMR and TRCIOR0)    | R/W |
| b1  | EB     | TRCIOB output disable bit | 1: Output disabled<br>(independent of settings of registers TRCMR and TRCIOR0) | R/W |
| b2  | EC     | TRCIOC output disable bit | 1: Output disabled<br>(independent of settings of registers TRCMR and TRCIOR1) | R/W |
| b3  | ED     | TRCIOD output disable bit | 1: Output disabled<br>(independent of settings of registers TRCMR and TRCIOR1) | R/W |
| b7  | PTO    | Timer output disable bit  | 0: Bits EA to ED do not change even if a low level is input to the INT0 pin    | R/W |

(16) Start the timer RC count.

#### Timer RC Mode Register (TRCMR)

|               |    |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|----|
| Bit           | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Setting Value | 1  | —  | x  | x  |    | x  | x  | x  |

| Bit | Symbol | Bit Name              | Function            | R/W |
|-----|--------|-----------------------|---------------------|-----|
| b7  | CTS    | TRCNT count start bit | 1: Count is started | R/W |

## 5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

## 6. Reference Documents

R8C/M12A Group User’s Manual: Hardware Rev.1.00

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

## Website and Support

Renesas Electronics website

<http://www.renesas.com/>

Inquiries

<http://www.renesas.com/inquiry>

|                  |   |
|------------------|---|
| Revision History | R8C/M12A Group<br>Output Compare Function of Timer RC |
|------------------|---|

| Rev. | Date          | Description |  |
|------|---------------|-------------|--|
|      |               | Page        | Summary  |
| 1.00 | Jan. 26, 2011 | —           | First edition issued   |
| 1.10 | Mar. 10, 2011 | —           | R8C/M12A Group hardware user's manual Rev.1.00 reviewed  |
|      |               | 6           | External clock control register (EXCKCR) revised   |
|      |               | 7           | System clock f select register (PHISEL) revised<br>System clock f control register (SCKCR) revised |
|      |               | 8, 10       | (6) CPU revised as system  |
| 1.11 | Mar. 31, 2011 | 6           | High-speed/low-speed on-chip oscillator control register (OCOOCR) revised                          |

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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