R8C/LA8A Group

Timer RJ in Timer Mode

R01AN0380EJ0101
Rev. 1.01
Sep. 29, 2011

Abstract

This document describes timer RJ in timer mode in the R8C/LA8A Group.

Product

R8C/LA8A Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Generate a timer RJ0 interrupt each millisecond using timer RJ in timer mode.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows a Block Diagram.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Timer RJ	Measure 1 ms.

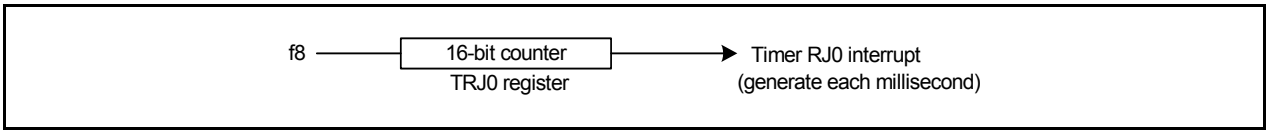


Figure 1.1 Block Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R8C/LA8A Group
Operating frequencies	• XIN clock: 20 MHz • System clock: 20 MHz • CPU clock: 20 MHz
Operating voltage	5.0 V (2.7 to 5.5 V)
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation M16C Series, R8C Family C Compiler V.5.45 Release 01
	Compile options -D__UART0__ -c -finfo -dir "$(CONFIGDIR)" -R8C (Default setting is used in the integrated development environment.)

3. Software

3.1 Operation Overview

Use timer RJ in timer mode to generate a timer RJ0 interrupt each millisecond and count the number of timer RJ0 interrupts.

Settings

- Use timer RJ0.
- Use timer mode.
- Use f8 for the count source of timer RJ0.
- Use the timer RJ0 interrupt.

Calculating the setup time

1 ms = (1 ÷ f8) × (TRJ0 + 1)
= {1 ÷ (20 MHz ÷ 8)} × 2500
= 400 ns × 2500

(1) Initial setting
Perform an initial setting of timer RJ0.
(2) Timer RJ0 count start
Set the TSTART bit in the TRJ0CR register to 1 to start the timer RJ0 count.
(3) Timer RJ0 interrupt occurs (first to ninth times)
When timer RJ0 underflows, a timer RJ0 interrupt occurs and the timer RJ0 interrupt counter is incremented in the timer RJ0 interrupt handling.
(4) Timer RJ0 interrupt occurs (10th time)
When timer RJ0 underflows, a timer RJ0 interrupt occurs and the timer RJ0 interrupt counter is incremented in the timer RJ0 interrupt handling. When the counter value is larger than nine, the counter value is initialized.

Figure 3.1 shows the Timing Diagram.

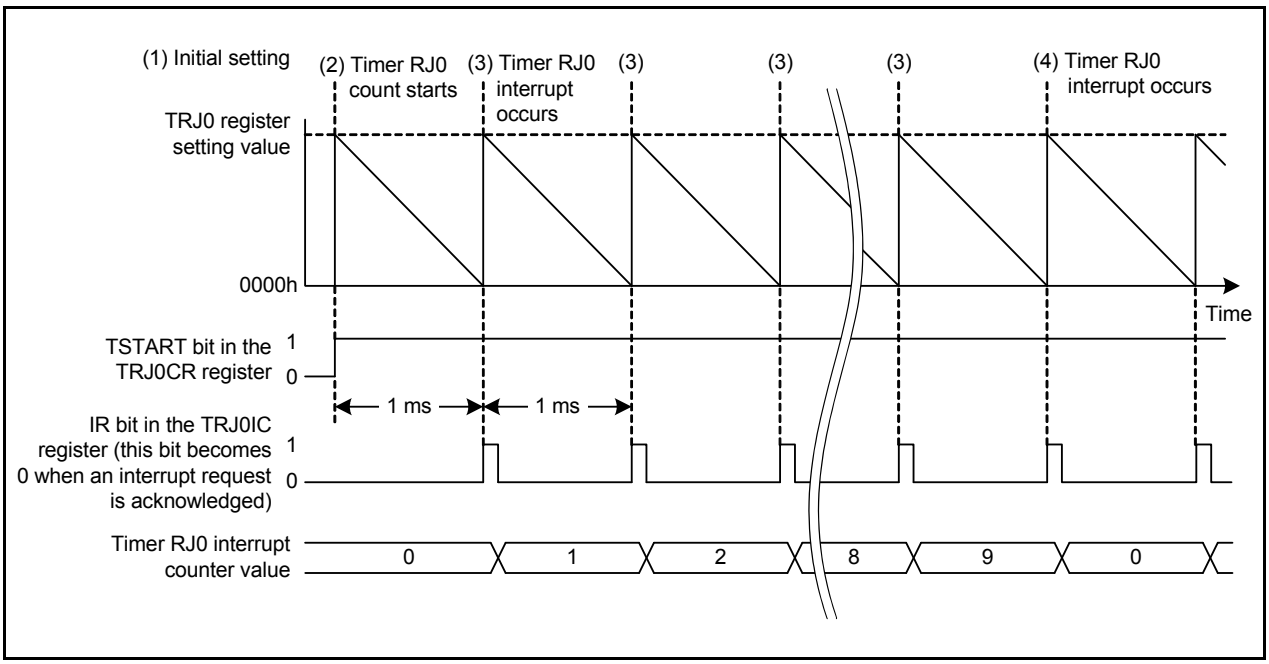


Figure 3.1 Timing Diagram

3.2 Required Memory Size

Table 3.1 lists the Required Memory Size.

Table 3.1 Required Memory Size

Memory Used	Size	Remarks
ROM	151 bytes	In the r01an0380_src.c module
RAM	1 byte	In the r01an0380_src.c module
Maximum user stack usage	10 bytes	
Maximum interrupt stack usage	3 bytes	

The required memory size varies depending on the C compiler version and compile options.

3.3 Variable

Table 3.2 lists the Global Variable.

Table 3.2 Global Variable

Type	Variable Name	Contents	Function Used
unsigned char	cnt_tmrj_int	Timer RJ0 interrupt counter	_timer_rj_ch0

3.4 Functions

Table 3.3 lists the Functions.

Table 3.3 Functions

Function Name	Outline
mcu_init	System clock setting
timer_rj_init	Initial setting of timer RJ0
_timer_rj_ch0	Timer RJ0 interrupt handling

3.5 Function Specifications

The following tables list the sample code function specifications.

mcu_init	
Outline	System clock setting
Header	None
Declaration	void mcu_init(void)
Description	Set the system clock.
Argument	None
Returned value	None
Remark	—

timer_rj_init	
Outline	Initial setting of timer RJ0
Header	None
Declaration	void timer_rj_init(void)
Description	Perform initial setting to use timer RJ0 in timer mode.
Argument	None
Returned value	None
Remark	—

_timer_rj_ch0	
Outline	Timer RJ0 interrupt handling
Header	None
Declaration	void _timer_rj_ch0(void)
Description	Perform timer RJ0 interrupt handling.
Argument	None
Returned value	None
Remark	—

3.6 Flowcharts

3.6.1 Main Processing

Figure 3.2 shows the Main Processing.

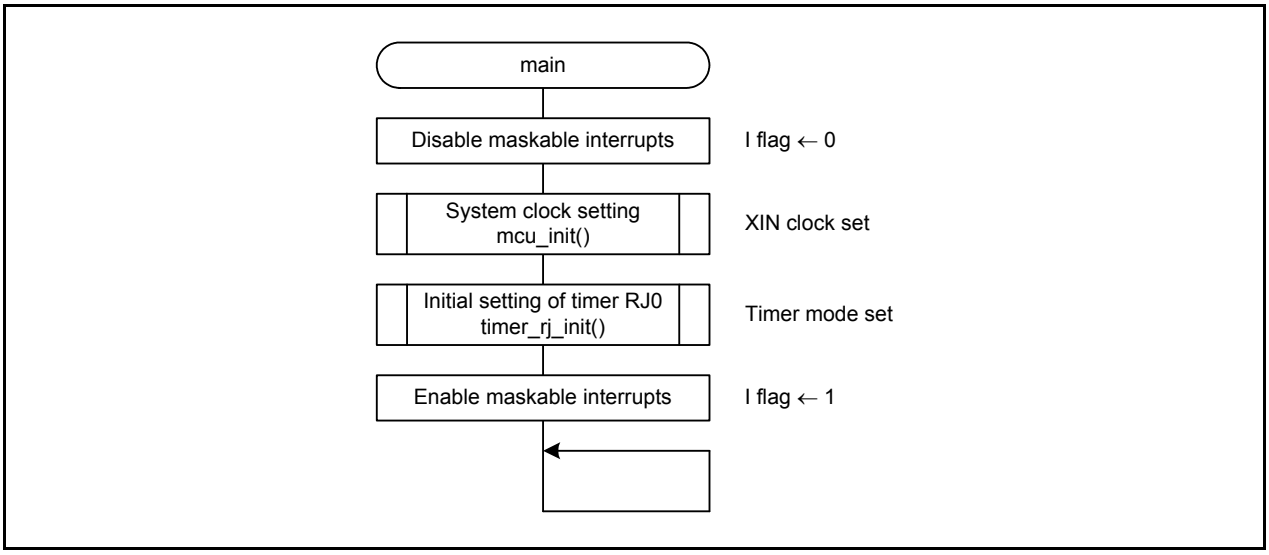


Figure 3.2 Main Processing

3.6.2 System Clock Setting

Figure 3.3 shows the System Clock Setting.

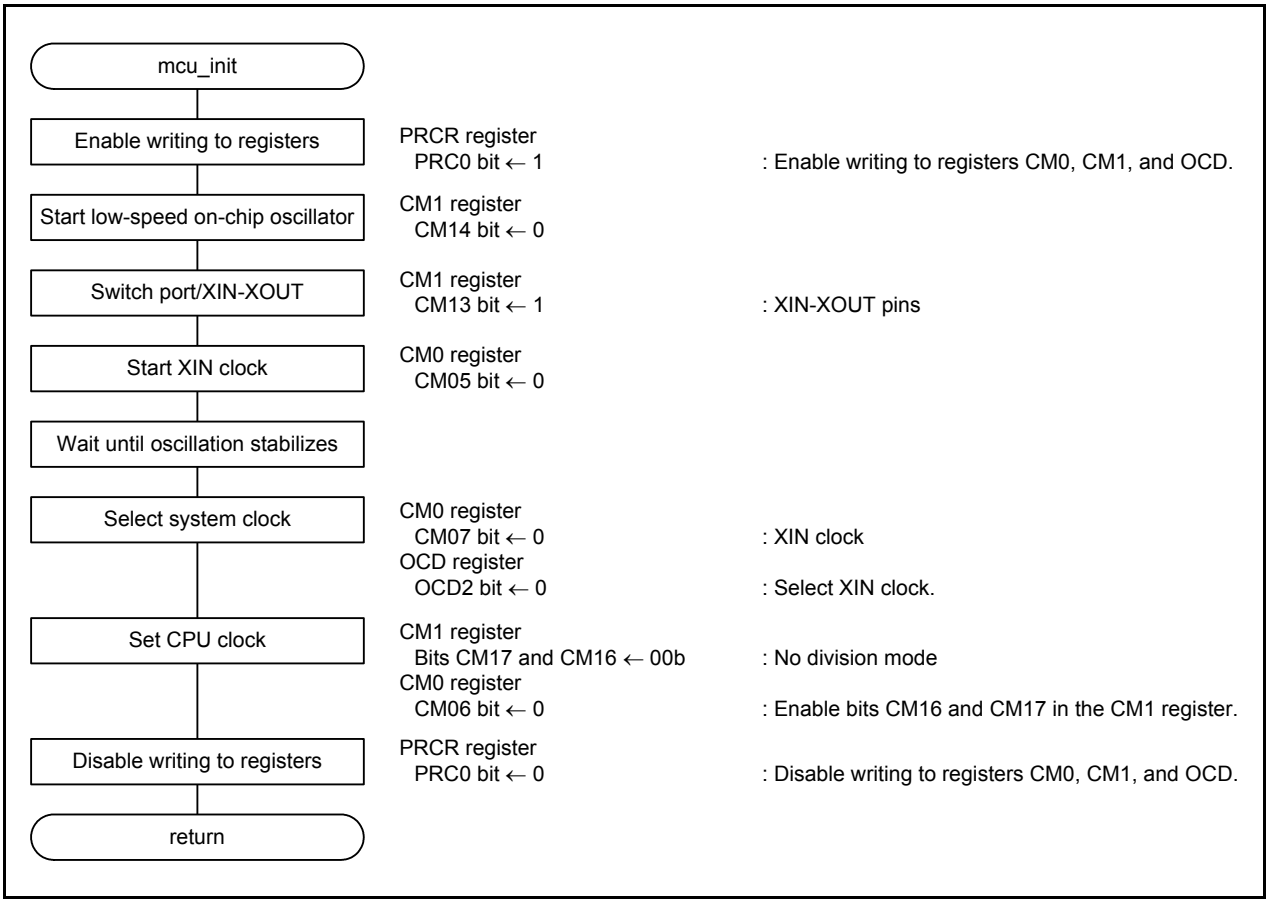
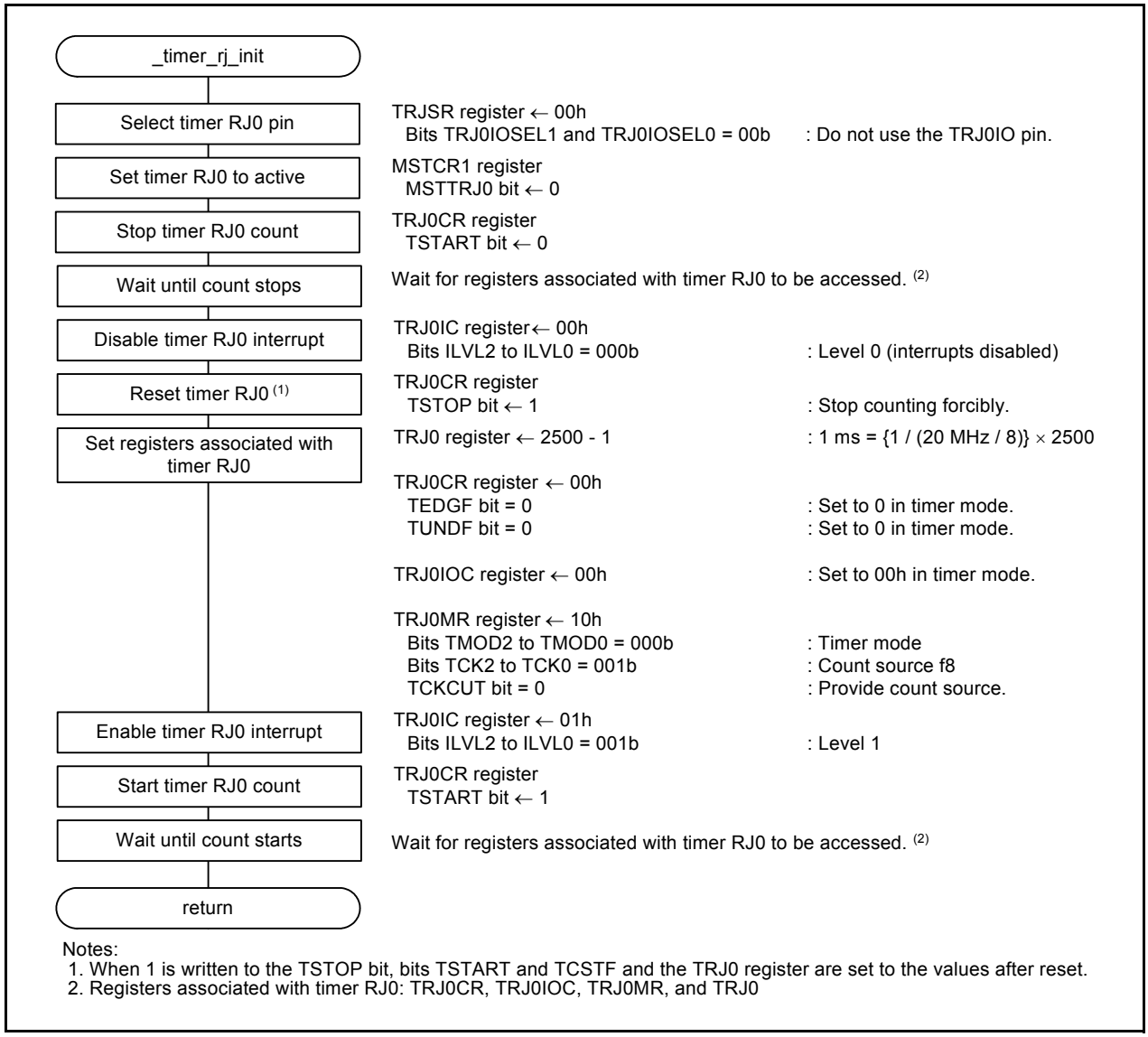


Figure 3.3 System Clock Setting

3.6.3 Initial Setting of Timer RJ0

Figure 3.4 shows the Initial Setting of Timer RJ0.



Notes:
1. When 1 is written to the TSTOP bit, bits TSTART and TCSTF and the TRJ0 register are set to the values after reset.
2. Registers associated with timer RJ0: TRJ0CR, TRJ0IOC, TRJ0MR, and TRJ0

Figure 3.4 Initial Setting of Timer RJ0

3.6.4 Timer RJ0 Interrupt Handling

Figure 3.5 shows the Timer RJ0 Interrupt Handling.

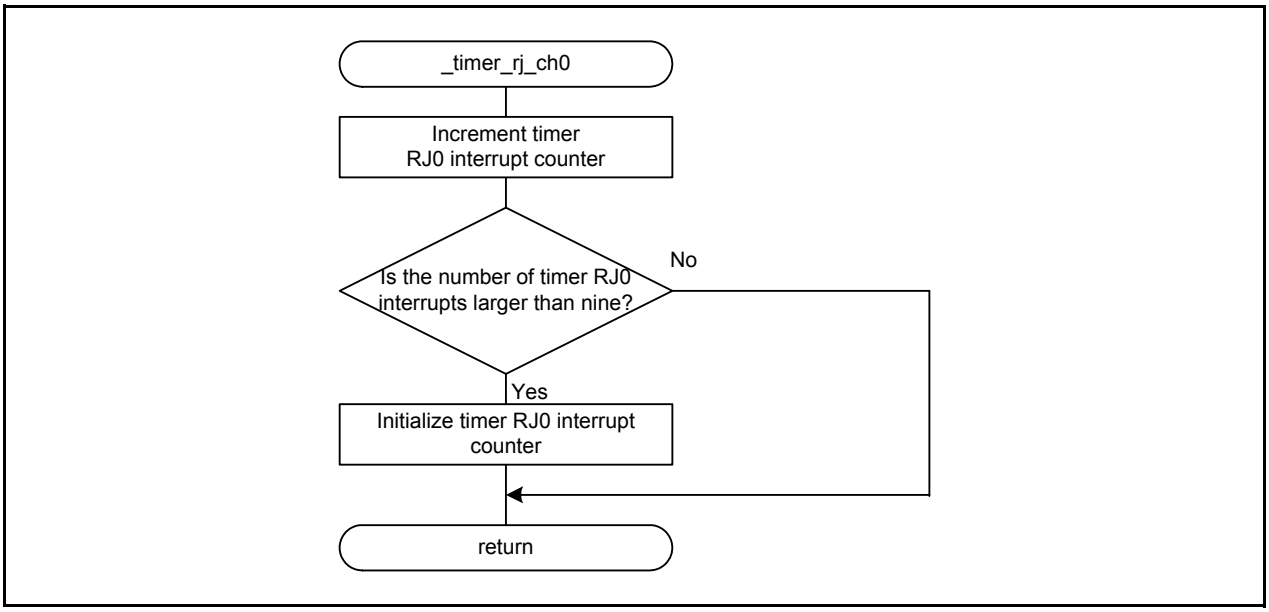


Figure 3.5 Timer RJ0 Interrupt Handling

4. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

5. Reference Documents

R8C/LA8A Group User's Manual: Hardware Rev.1.02
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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Revision History	R8C/LA8A Group Timer RJ in Timer Mode

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 31, 2011	—	First edition issued
1.01	Sep. 29, 2011	3	Table 2.1 errors revised

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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