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R8C/L3AC Group

LCD Drive Control Circuit (External Voltage Multiplier Reference Power, Blink Function)

1. Abstract

This document describes the setting method and an application example of the LCD drive control circuit (when using external voltage multiplier reference power, blink function) for the R8C/L3AC Group.

2. Introduction

The application example described in this document applies to the following MCU:

- MCU: R8C/L3AC Group

The sample program in this application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the sample program described in this application note.

3. Application Example

3.1 LCD Display

Outline: Use the LCD drive control circuit to display the LCD.

Specifications:

- Use segment pins SEG0 to SEG23 and common pins COM0 to COM3.
- Duty = 1/4, bias value = 1/3
- Frame frequency = 76 Hz

$$f(\text{FR}) = \frac{f(\text{LCDCK}) \times \text{duty}}{2}$$

$$f(\text{LCDCK}) = \frac{\text{LCD clock source frequency}}{n \times \text{division ratio}}$$

Notes:
 n = 32 when f32 is selected
 n = 4 when fC-LCD is selected

LCD clock source frequency = f32 = (high-speed on-chip oscillator divided by 2) / 32

n = 32

Division ratio = divide by 32

- Use the voltage multiplier. VL1: 1.5 V (external input)
- Wait time for the voltage multiplier = f(FR) x 64 counts = 0.84 seconds
- Data display control interval = f(FR) x 32 counts = 0.42 seconds
- Enable LCD display control and display LCD blink.
- Display as R8C/LX.

Figure 3.1 shows a Segment Layout. Figure 3.2 shows a Circuit Example When Using External Power. Figure 3.3 shows the LCD Display Data Register Settings.

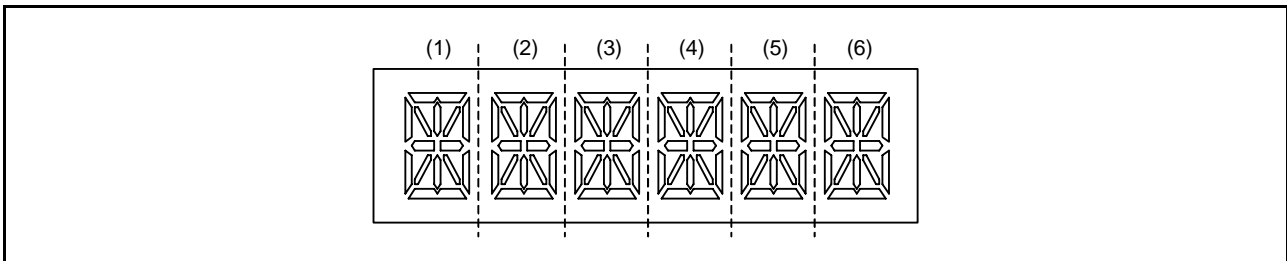


Figure 3.1 Segment Layout

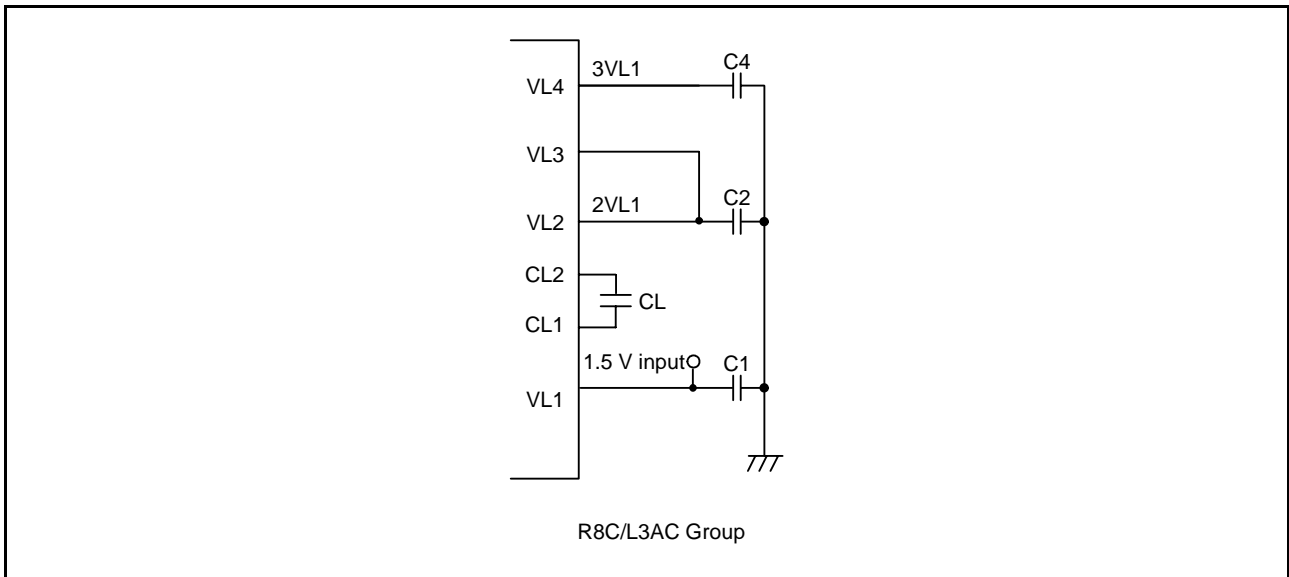


Figure 3.2 Circuit Example When Using External Power

Address	Bit									Digit
		7	6	5	4	3	2	1	0	
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	
0210h	LRA0L					d	c	b	a	→(1)
0211h	LRA1L					h	g	f	e	→(1)
0212h	LRA2L					k	j		i	→(1)
0213h	LRA3L					n	m		l	→(1)
0214h	LRA4L					d	c	b	a	→(2)
0215h	LRA5L					h	g	f	e	→(2)
0216h	LRA6L					k	j		i	→(2)
0217h	LRA7L					n	m		l	→(2)
0218h	LRA8L					d	c	b	a	→(3)
0219h	LRA9L					h	g	f	e	→(3)
021Ah	LRA10L					k	j		i	→(3)
021Bh	LRA11L					n	m		l	→(3)
021Ch	LRA12L					d	c	b	a	→(4)
021Dh	LRA13L					h	g	f	e	→(4)
021Eh	LRA14L					k	j		i	→(4)
021Fh	LRA15L					n	m		l	→(4)
0220h	LRA16L					d	c	b	a	→(5)
0221h	LRA17L					h	g	f	e	→(5)
0222h	LRA18L					k	j		i	→(5)
0223h	LRA19L					n	m		l	→(5)
0224h	LRA20L					d	c	b	a	→(6)
0225h	LRA21L					h	g	f	e	→(6)
0226h	LRA22L					k	j		i	→(6)
0227h	LRA23L					n	m		l	→(6)

These bits are not used in this application note (they can be used as RAM).

Figure 3.3 LCD Display Data Register Settings

3.2 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	272 bytes	In the rej05b1165_src.c module
RAM	0 bytes	In the rej05b1165_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options.

The above applies to the following conditions:

- C compiler: M16C/60, 30, 20, 10, and Tiny, and R8C/Tiny Series Compiler V.5.45 Release 00
- Compile option: -c -finfo -dir "\$(CONFIGDIR)" -R8CE

4. Software Outline

This section shows the setting procedures and values to set the example described in section 3. Application Example. Refer to the latest R8C/L3AC Group Hardware Manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the hyphen represents reserved bits or bits that have nothing assigned.

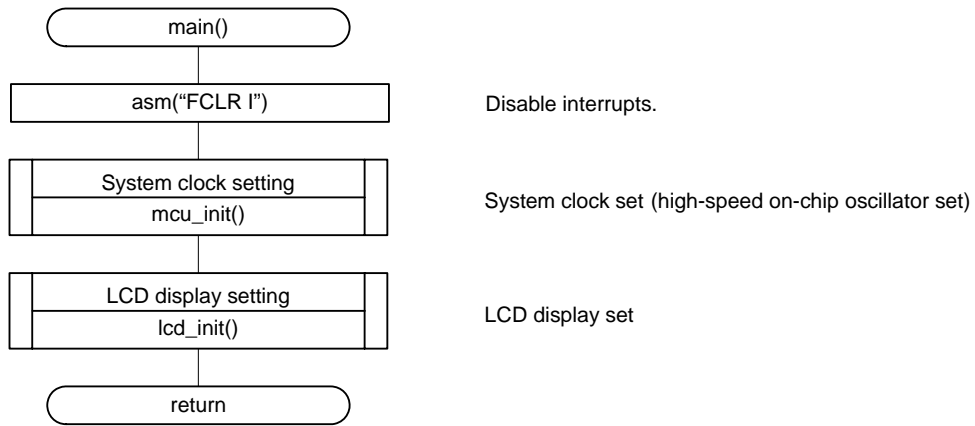
4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (high-speed on-chip oscillator).		

Declaration	void lcd_init(void)		
Outline	LCD display setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set registers associated with the LCD.		

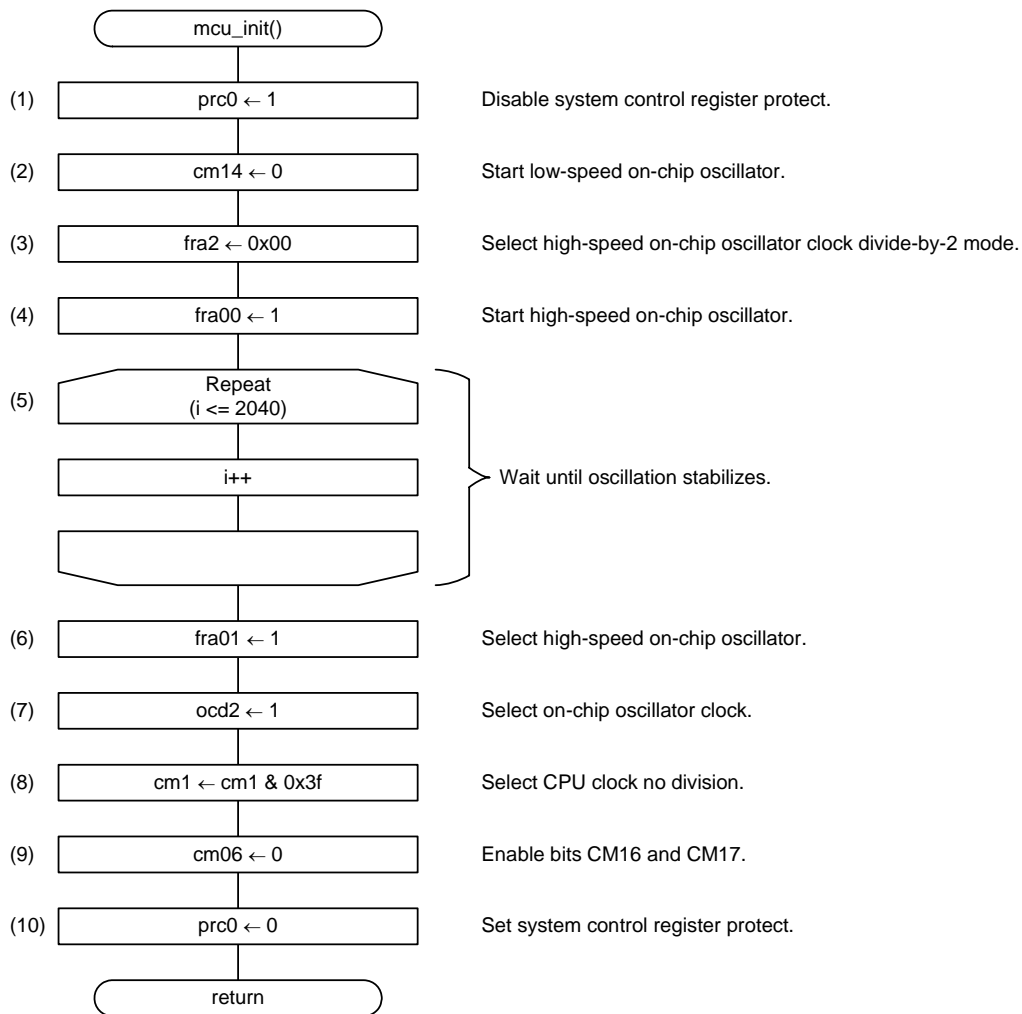
4.2 Main Function

- Flowchart



4.3 System Clock Setting

• Flowchart



• Register Settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Oscillate the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the division ratio for the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switch bit	Division ratio selection	R/W
b1	FRA21		These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b2	FRA22			R/W

(4) Oscillate the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	×	—	1	—

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator on	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	×	1	×	×

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	On-chip oscillator clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	—	—	×	×	×	×

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	×	0	×	×	×	×	×	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

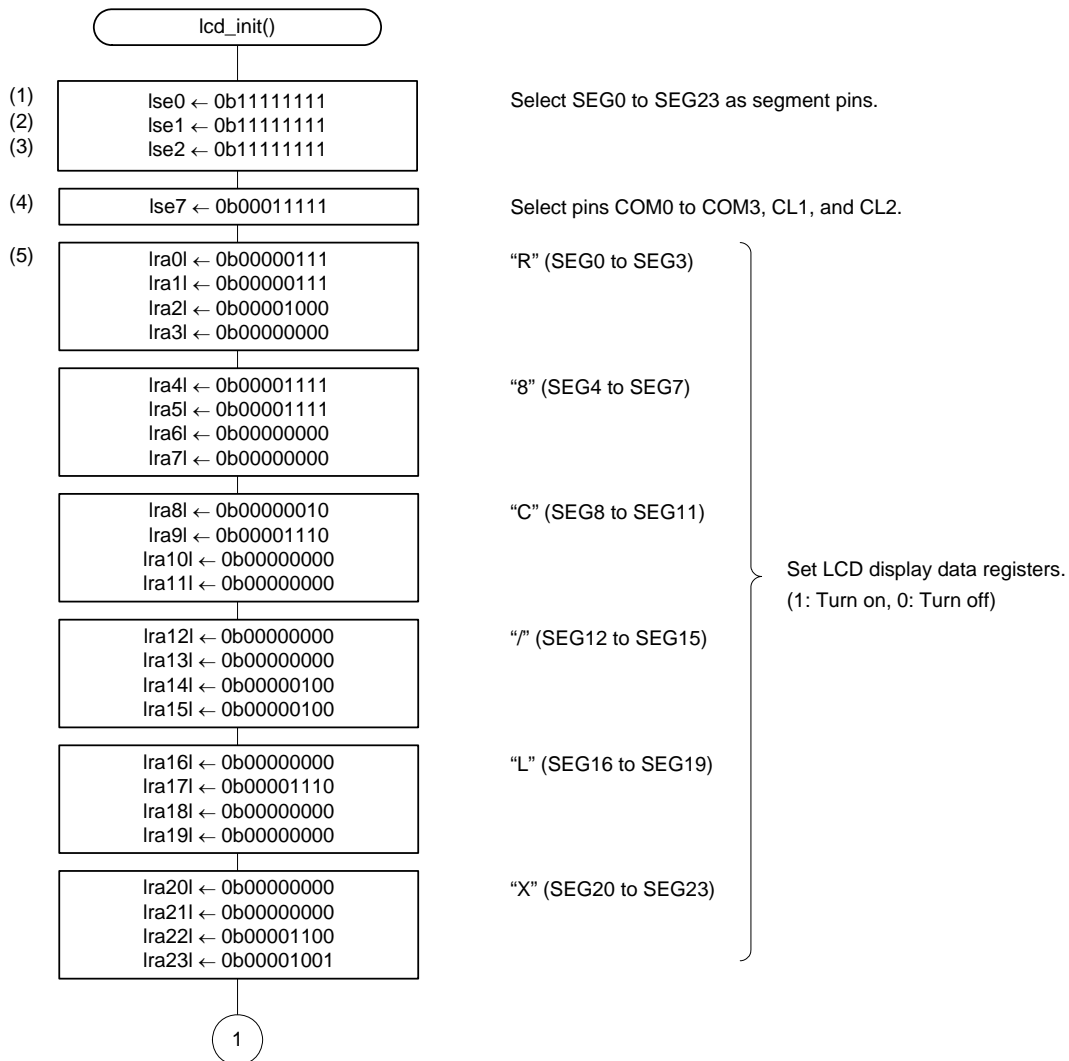
Protect Register (PRCR)

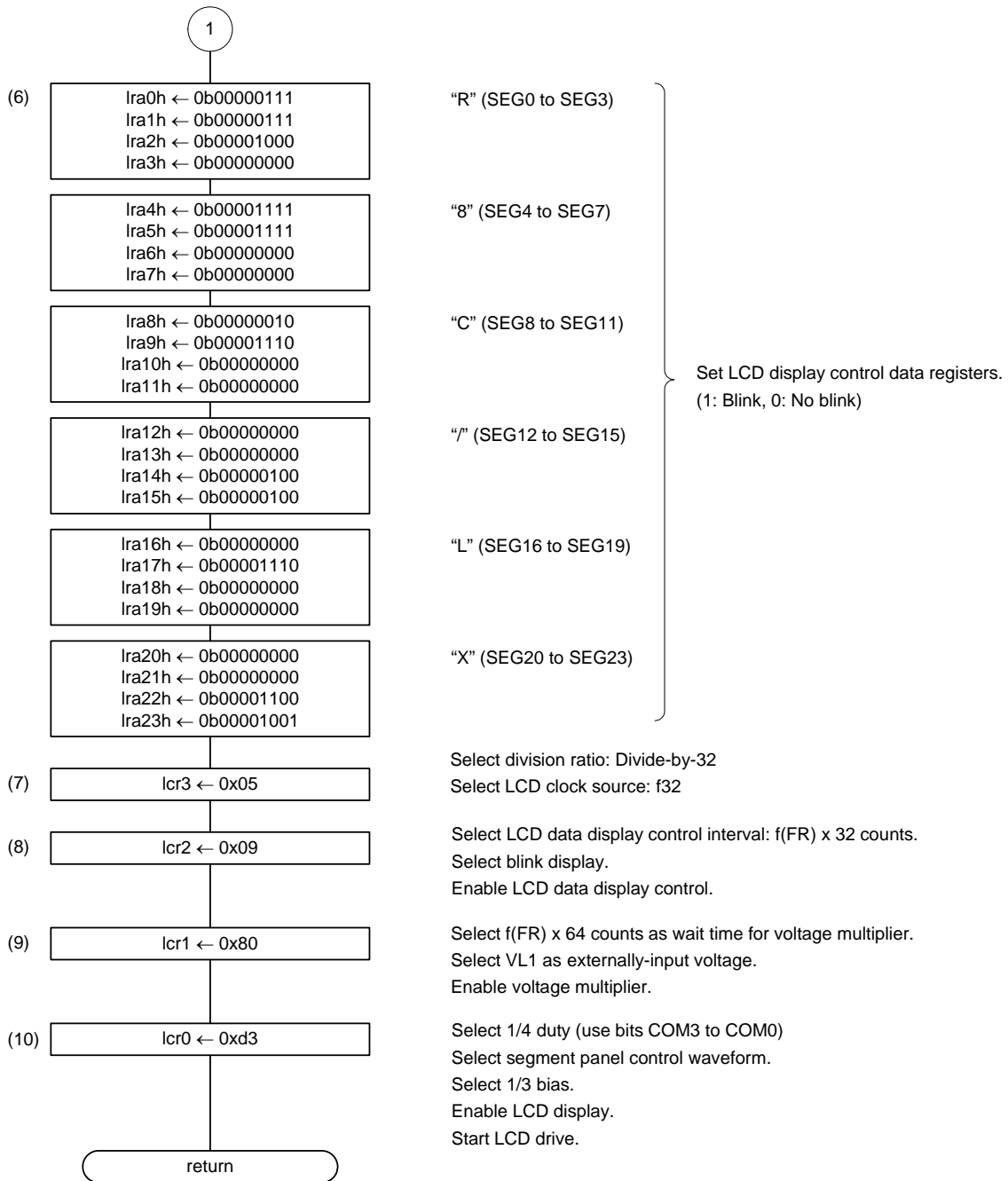
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	×	—	×	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 LCD Display Setting

• Flowchart





• Register Settings

(1) Set port P0 as a segment pin.

LCD Port Select Register 0 (LSE0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	LSE00	LCD port select bit 0	1: SEG0	R/W
b1	LSE01	LCD port select bit 1	1: SEG1	R/W
b2	LSE02	LCD port select bit 2	1: SEG2	R/W
b3	LSE03	LCD port select bit 3	1: SEG3	R/W
b4	LSE04	LCD port select bit 4	1: SEG4	R/W
b5	LSE05	LCD port select bit 5	1: SEG5	R/W
b6	LSE06	LCD port select bit 6	1: SEG6	R/W
b7	LSE07	LCD port select bit 7	1: SEG7	R/W

(2) Set port P1 as a segment pin.

LCD Port Select Register 1 (LSE1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	LSE08	LCD port select bit 8	1: SEG8	R/W
b1	LSE09	LCD port select bit 9	1: SEG9	R/W
b2	LSE10	LCD port select bit 10	1: SEG10	R/W
b3	LSE11	LCD port select bit 11	1: SEG11	R/W
b4	LSE12	LCD port select bit 12	1: SEG12	R/W
b5	LSE13	LCD port select bit 13	1: SEG13	R/W
b6	LSE14	LCD port select bit 14	1: SEG14	R/W
b7	LSE15	LCD port select bit 15	1: SEG15	R/W

(3) Set port P2 as a segment pin.

LCD Port Select Register 2 (LSE2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	LSE16	LCD port select bit 16	1: SEG16	R/W
b1	LSE17	LCD port select bit 17	1: SEG17	R/W
b2	LSE18	LCD port select bit 18	1: SEG18	R/W
b3	LSE19	LCD port select bit 19	1: SEG19	R/W
b4	LSE20	LCD port select bit 20	1: SEG20	R/W
b5	LSE21	LCD port select bit 21	1: SEG21	R/W
b6	LSE22	LCD port select bit 22	1: SEG22	R/W
b7	LSE23	LCD port select bit 23	1: SEG23	R/W

(4) Set ports P7_4 to P7_7 as COM pins and ports P12_2 and P12_3 to the CL pin.

LCD Port Select Register 7 (LSE7)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	LSE56	LCD port select bit 56	1: COM3	R/W
b1	LSE57	LCD port select bit 57	1: COM2	R/W
b2	LSE58	LCD port select bit 58	1: COM1	R/W
b3	LSE59	LCD port select bit 59	1: COM0	R/W
b4	LSE60	LCD port select bit 60	1: CL1 and CL2	R/W

(5) Set the LCD display data register.

When 1 is written to a bit in the LCD display data register (LRA), the corresponding segment of the LCD panel is turned on, when a bit is set to 0, the corresponding segment is turned off.

Symbol	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
LRA0L	0210h	SEG0							
LRA1L	0211h	SEG1							
LRA2L	0212h	SEG2							
LRA3L	0213h	SEG3							
LRA4L	0214h	SEG4							
LRA5L	0215h	SEG5							
LRA6L	0216h	SEG6							
LRA7L	0217h	SEG7							
LRA8L	0218h	SEG8							
LRA9L	0219h	SEG9							
LRA10L	021Ah	SEG10							
LRA11L	021Bh	SEG11							
LRA12L	021Ch	SEG12							
LRA13L	021Dh	SEG13							
LRA14L	021Eh	SEG14							
LRA15L	021Fh	SEG15							
LRA16L	0220h	SEG16							
LRA17L	0221h	SEG17							
LRA18L	0222h	SEG18							
LRA19L	0223h	SEG19							
LRA20L	0224h	SEG20							
LRA21L	0225h	SEG21							
LRA22L	0226h	SEG22							
LRA23L	0227h	SEG23							

(6) Set the LCD display control data register.

When 1 is written to a bit in the LCD display control data register (LRAH), the corresponding segment of the LCD is blinked for the interval selected by bits LDFR0 to LDFR2.

Symbol	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
LRA0H	0270h	SEG0							
LRA1H	0271h	SEG1							
LRA2H	0272h	SEG2							
LRA3H	0273h	SEG3							
LRA4H	0274h	SEG4							
LRA5H	0275h	SEG5							
LRA6H	0276h	SEG6							
LRA7H	0277h	SEG7							
LRA8H	0278h	SEG8							
LRA9H	0279h	SEG9							
LRA10H	027Ah	SEG10							
LRA11H	027Bh	SEG11							
LRA12H	027Ch	SEG12							
LRA13H	027Dh	SEG13							
LRA14H	027Eh	SEG14							
LRA15H	027Fh	SEG15							
LRA16H	0280h	SEG16							
LRA17H	0281h	SEG17							
LRA18H	0282h	SEG18							
LRA19H	0283h	SEG19							
LRA20H	0284h	SEG20							
LRA21H	0285h	SEG21							
LRA22H	0286h	SEG22							
LRA23H	0287h	SEG23							

(7) Set the division ratio and LCD clock source.

LCD Clock Control Register (LCR3)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	—	—	—	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	LPSC0	Division ratio select bit	b2 b1 b0 1 0 1: Divide-by-32	R/W
b1	LPSC1			R/W
b2	LPSC2			R/W
b6	LCKS0	LCD clock source select bit	b7 b6 0 0: f32	R/W
b7	LCKS1			R/W

- (8) Select the LCD data display control interval, enable the data display control, and select the display control mode.

LCD Display Control Register (LCR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	0	0	0	1	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	LDFR0	LCD data display control interval select bit 1 (counts the frame frequency)	$b_2 b_1 b_0$ 0 0 1: Display control interval = $f(FR)$ Other than LDTY2 to LDTY0 = 010b (other than 1/3 duty) x 32 counts	R/W
b1	LDFR1			R/W
b2	LDFR2			R/W
b3	LDSPC	LCD data display control enable bit	1: Data display control enabled	R/W
b4	LRVRS	LCD display control mode select bit	0: On/off display	R/W
b5	LDFR20	LCD data display control interval select bit 2 (synchronized with timer RE)	$b_6 b_5$ 0 0 : Settings of bits LDER0 to LDER2 enabled	R/W
b6	LDFR21			R/W

- (9) Select the voltage multiplier wait time and voltage multiplier reference voltage source, and enable the voltage multiplier.

LCD Bias Control Register (LCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	0	0	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	LVWT0	Voltage multiplier wait time select bit	$b_5 b_4$ 0 0 : Wait time = $f(FR)$ Other than LDTY2 to LDTY0 = 010b (other than 1/3 duty) x 64 counts	R/W
b5	LVWT1			R/W
b6	LVURS	Voltage multiplier reference voltage source select bit	0: VL1 externally-input voltage	R/W
b7	LVUPE	Voltage multiplier enable bit	1: Voltage multiplier enabled	R/W

(10) Select the duty, waveform control, and bias. Turn on the LCD display and start the LCD drive.

LCD Control Register (LCR0)

	Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value		1	1	0	1	0	0	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	LDTY0	Duty select Bit	^{b2 b1 b0} 0 1 1: 1/4 duty (COM0 to COM3 used)	R/W
b1	LDTY1			R/W
b2	LDTY2			R/W
b3	LWAV	LCD waveform control select bit	0: Segment panel control waveform	R/W
b4	LBAS0	Bias select bit	^{b5 b4} 0 1: 1/3 bias	R/W
b5	LBAS1			R/W
b6	LDSPE	LCD display enable bit	1: LCD on	R/W
b7	LSTAT	LCD drive start bit	1: Drive starts	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

Hardware Manual

R8C/L3AC Group Hardware Manual Rev.0.10

The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Technology website.

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<http://www.renesas.com/>

Inquiries
<http://www.renesas.com/inquiry>
csc@renesas.com

REVISION HISTORY	R8C/L3AC Group LCD Drive Control Circuit (External Voltage Multiplier Reference Power, Blink Function)
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