R8C/38C Group

Timer RG Timer Mode (Periodic Timer)

REJ05B1155-0110
Rev.1.10
Mar. 10, 2011

1. Abstract

This document describes the setting method and an application example for the periodic timer using timer mode (output compare function) in timer RG.

2. Introduction

The application example described in this document applies to the following MCU:

- MCU: R8C/38C Group

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

When the values of the timer RG counter (TRG) and timer RG general register A (TRGGRA) match (compare match), an interrupt is generated in a 1 ms period. When an interrupt is generated, the interrupt counter increments by one.

Main settings

- The TRG register is cleared by a compare match with the TRGGRA register.
- P5_6/TRGIOA pin output from a compare match is disabled.
- Timer RG general resister C (TRGGRC) is not used as a buffer register for the TRGGRA register.

Formula for setting time

1 ms = 1 ÷ fOCO40M × (TRGGRA register value + 1)
= 1 ÷ 40 MHz × (39999 + 1)
= 25 ns × 40000

Figure 3.1 shows the block diagram and Figure 3.2 shows the timing chart.

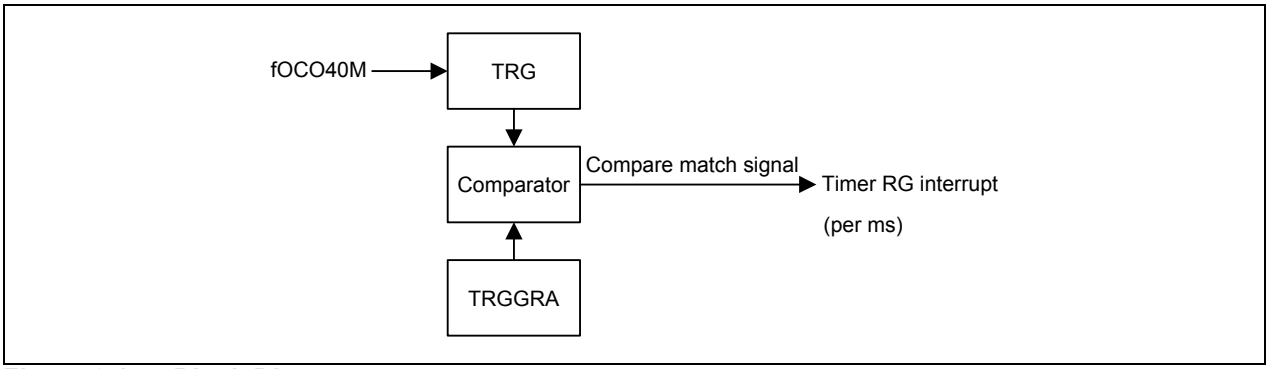


Figure 3.1 Block Diagram

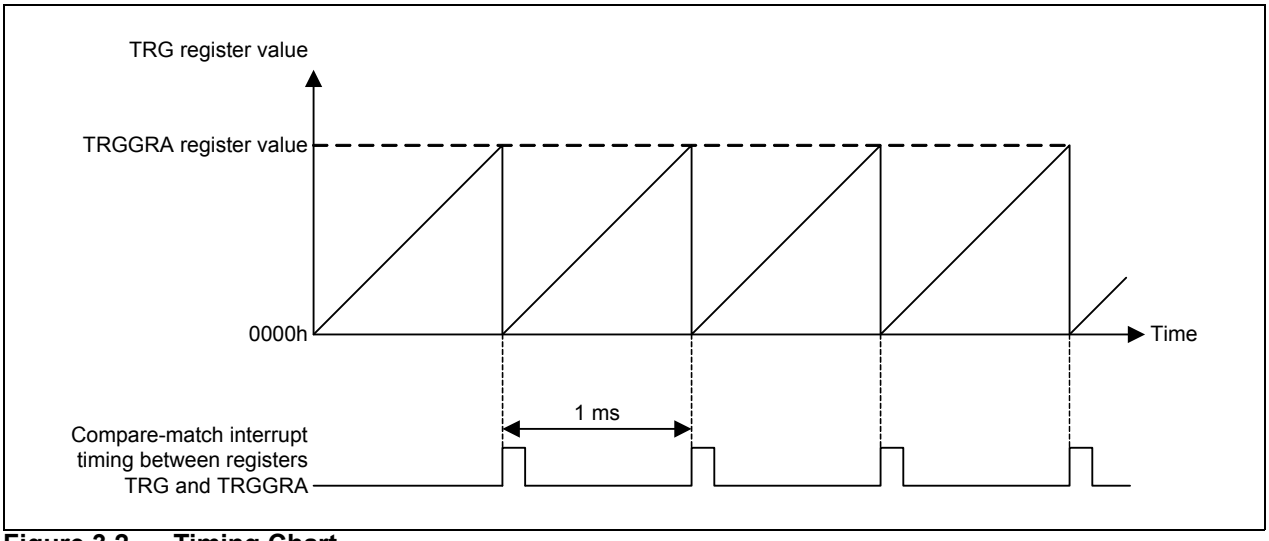


Figure 3.2 Timing Chart

3.2 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	213 bytes	In the rej05b1155_src.c module
RAM	2 bytes	In the rej05b1155_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	19 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software Outline

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/38C Group hardware user's manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

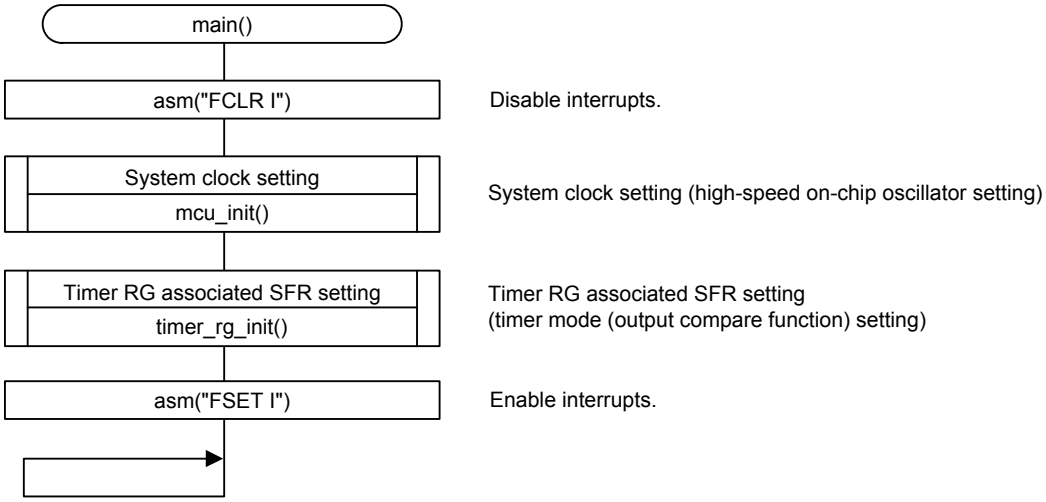
Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The system clock (high-speed on-chip oscillator) is set.		

Declaration	void timer_rg_init(void)		
Outline	Timer RG associated SFR setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The SFR register is set to use timer RG in timer mode.		

Declaration	void timer_rg_interrupt(void)		
Outline	Timer RG interrupt		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	An interrupt process in a 1 ms period which is generated by a compare match between the TRG register and the TRGGRA register. The interrupt counter increments by 1.		

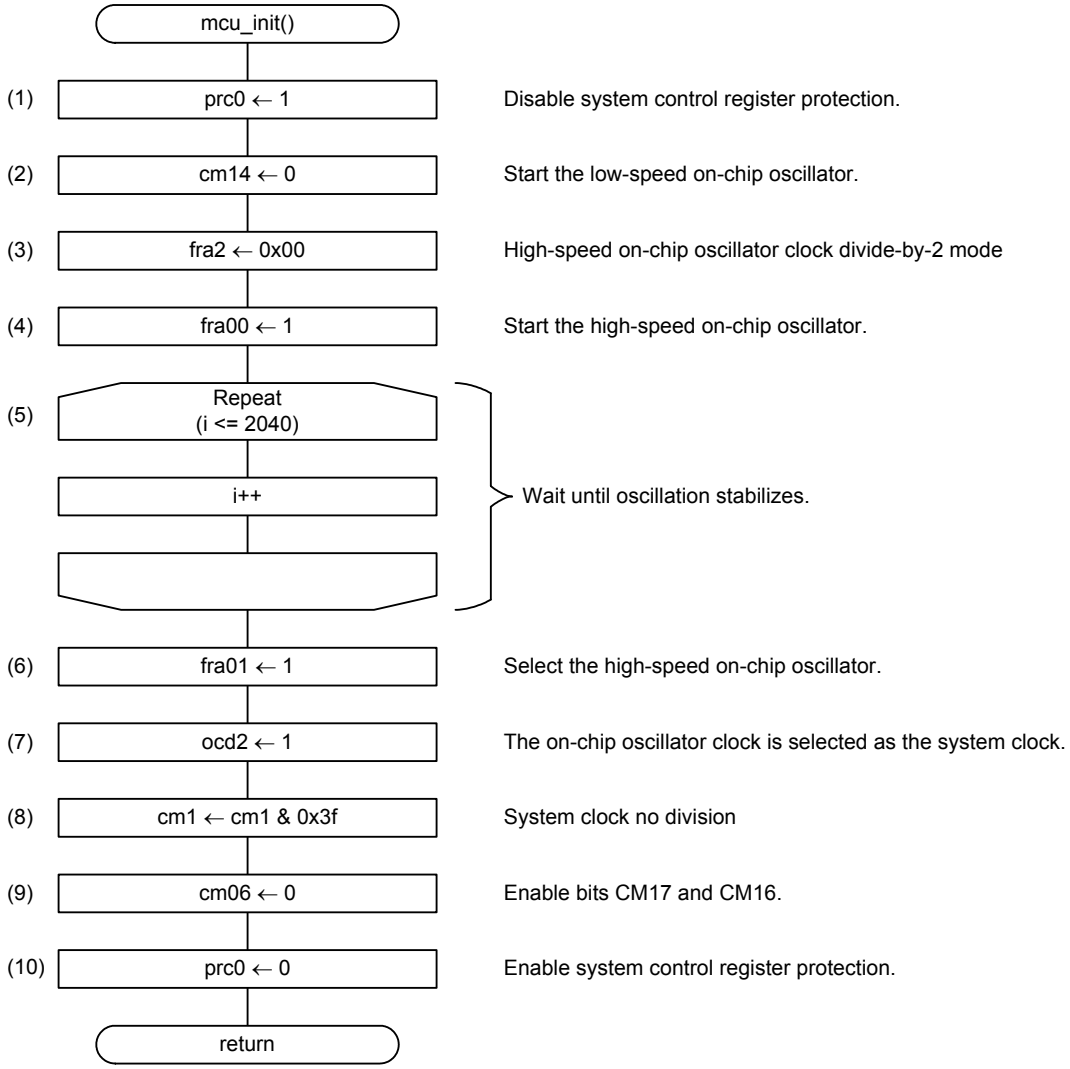
4.2 Main Function

- Flowchart



4.3 System Clock Setting

- Flowchart



• Register Setting

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set system clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

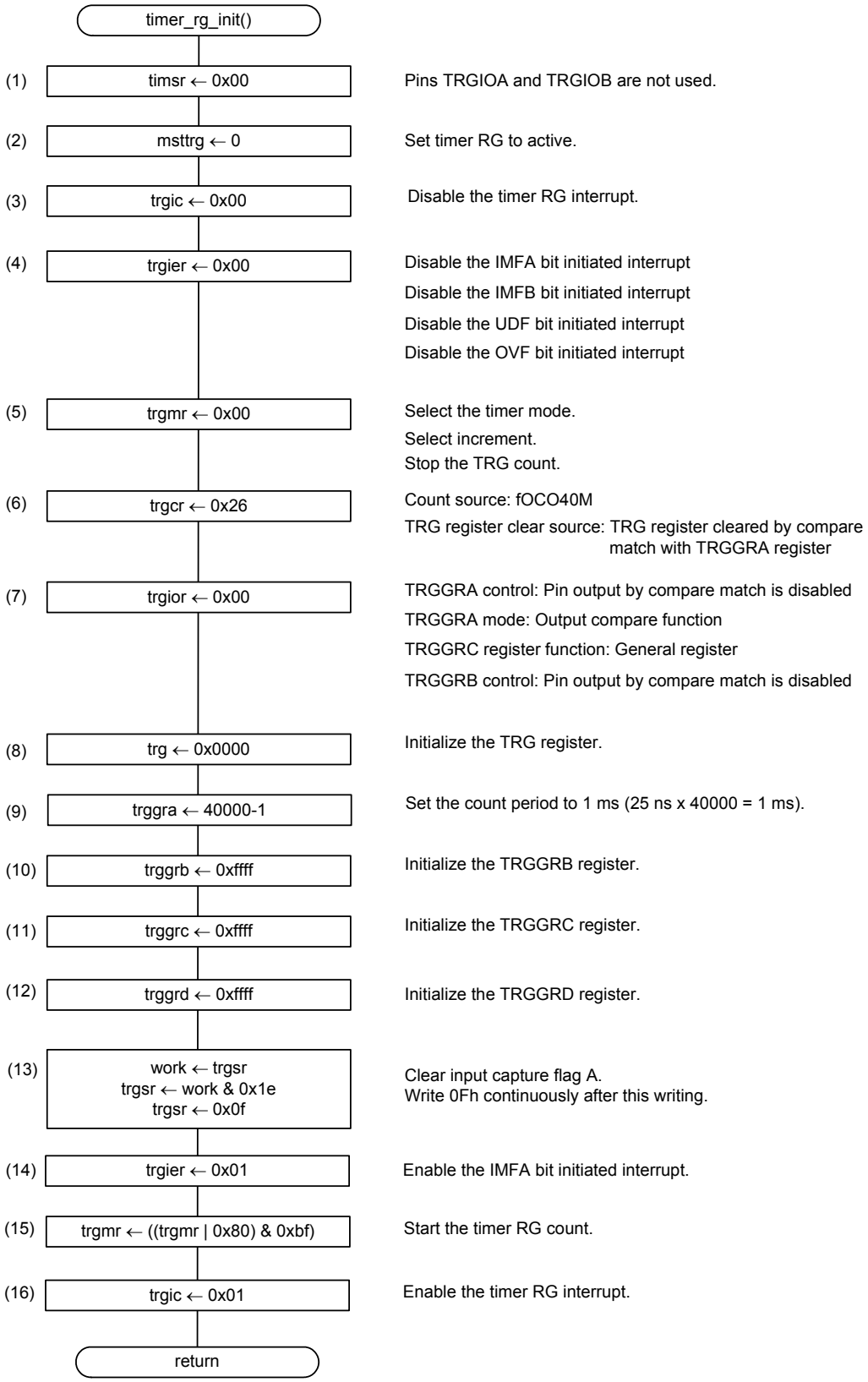
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Timer RG Associated SFR Setting

- Flowchart



• Register Setting

(1) Set the TIMSR register.

Timer Pin Select Register (TIMSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0	0	—	x	—	x

Bit	Symbol	Bit Name	Function	R/W
b4	TRGIOASEL	TRGIOA pin select bit	0: TRGIOA pin not used	R/W
b5	TRGIOBSEL	TRGIOB pin select bit	0: TRGIOB pin not used	R/W

(2) Set timer RG to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	x	x	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	MSTTRG	Timer RG standby bit	0: Active	R/W

(3) Disable the timer RG interrupt.

Interrupt Control Register (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(4) Disable all interrupt sources for timer RG.

Timer RG Interrupt Enable Register (TRGIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt by IMFA flag disabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt by IMFB flag disabled	R/W
b2	UDIE	Underflow interrupt enable bit	0: Interrupt by UDF flag disabled	R/W
b3	OVIE	Overflow interrupt enable bit	0: Interrupt by OVF flag disabled	R/W

(5) Select the timer RG mode register.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	x	x	x	x	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWM	PWM mode select bit	0: Timer Mode	R/W
b1	MDF	Phase counting mode select bit	0: Increment	R/W
b7	TSTART	TRG count start bit	0: Count stops	R/W

(6) Set the count source to fOCO40M, and the TRG register clear source to the compare match of TRGGRA.

Timer RG Control Register (TRGCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	1	x	x	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 1 1 0: fOCO40M	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b5	CCLR0	TRG register clear source select bit	b6 b5 0 1: TRG register cleared by input capture or compare match with TRGGRA register	R/W
b6	CCLR1			R/W

(7) Set the TRGIOR register.

Timer RG I/O Control Register (TRGIOR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	b1 b0 0 0: Pin output by compare match disabled (TRGIOA pin is programmable I/O port)	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit	0: Output compare function	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register	R/W

(8) Initialize the timer RG counter to 0000h.

Timer RG Counter (TRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count operation is increment.	0000h to FFFFh	R/W

(9) Set 40000-1 (9C3Fh) which is the compare value with the TRG register to the TRGGRA register.

Timer RG General Register A (TRGGRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	1	0	0	1	1	1	0	0

Bit	Function	R/W
b15 to b0	Compare value with TRG register.	R/W

(10) Initialize the TRGGRB register to FFFFh.

Timer RG General Register B (TRGGRB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	The value larger than setting value in timer RG general register A (TRGGRA).	R/W

(11) Initialize the TRGGRC register to FFFFh.

Timer RG General Register C (TRGGRC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	The value larger than setting value in timer RG general register A (TRGGRA).	R/W

(12) Initialize the TRGGRD register to FFFFh.

Timer RG General Register D (TRGGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	The value larger than setting value in timer RG general register A (TRGGRA).	R/W

(13) Clear the compare match flag A. Then write 0Fh continuously after this writing.

Timer RG Status Register (TRGSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading.	R/W

(14) Enable a compare match interrupt between registers TRG and TRGGRA.

Timer RG Interrupt Enable Register (TRGIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	1: Interrupt by IMFA flag enabled	R/W

(15) Start the timer RG counter.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	—	x	x	x	x	x	

Bit	Symbol	Bit Name	Function	R/W
b7	TSTART	TRG count start bit	1: Count starts	R/W

(16) Enable the timer RG interrupt.

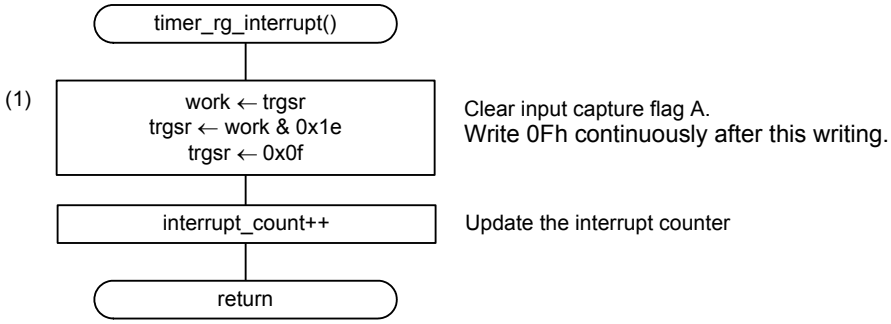
Interrupt Control Register (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R

4.5 Timer RG Interrupt

• Flowchart



• Register Setting

(1) Clear input-capture/compare match flag A. Then write 0Fh continuously after this writing.

Timer RG Status Register (TRGSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—		x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading.	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/38C Group User’s Manual: Hardware Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
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Revision History	R8C/38C Group Timer RG Timer Mode (Periodic Timer)

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 29, 2009	—	First edition issued
1.10	Mar. 20, 2011	—	R8C/38C Group hardware user's manual Rev.1.10 reviewed
		3	Table 3.1 revised, C compiler revised
		10, 15	Processing for TRGSR regsiter setting revised

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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