R8C/38C Group

Timer RG Timer Mode (Input Capture Function)

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Rev.1.10
Mar. 10, 2011

1. Abstract

This document describes the setting method and an application example for timer RG's timer mode (input capture function) in the R8C/38C Group.

2. Introduction

The application example described in this document applies to the following MCU:

- MCU: R8C/38C Group

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

The pulse width is measured by detecting both edges of an external signal input to the TRGIOA pin using the input capture function.

A timer RG interrupt is generated when an active edge is detected or when timer RG counter overflows. When an interrupt is triggered by overflow (OVF is 1), the number of overflows is counted. When an interrupt is triggered by detecting an active edge (IMFA is 1), the content of the TRGGRA register is read as the current value, and the content of the TRGGRC buffer register is read as the previous value.

The pulse width is calculated by the values read from the main process and number of overflows.

Main settings

- Use both edges to detect the input capture to the TRGIOA pin.
- Use the digital filter function.
- Enable an interrupt when timer RG counter overflows.
- Enable an interrupt when an active edge is detected.

See Figure 3.2 for the formula to calculate pulse width.

Figure 3.1 shows the block diagram, Figure 3.2 shows the timing chart, and Table 3.1 shows the pin used and its function.

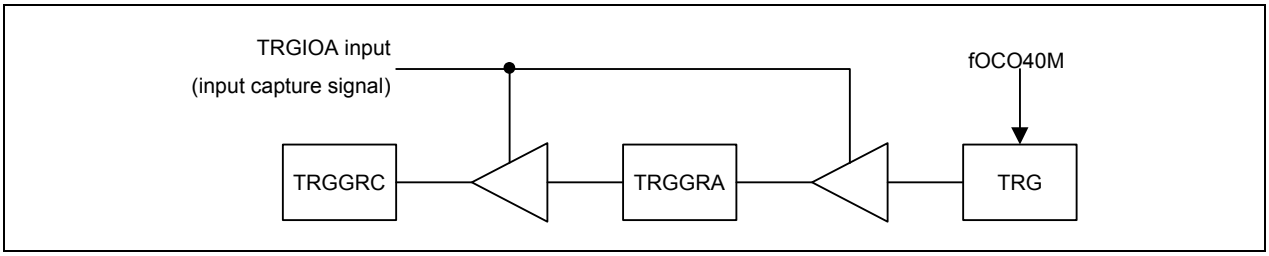


Figure 3.1 Block Diagram

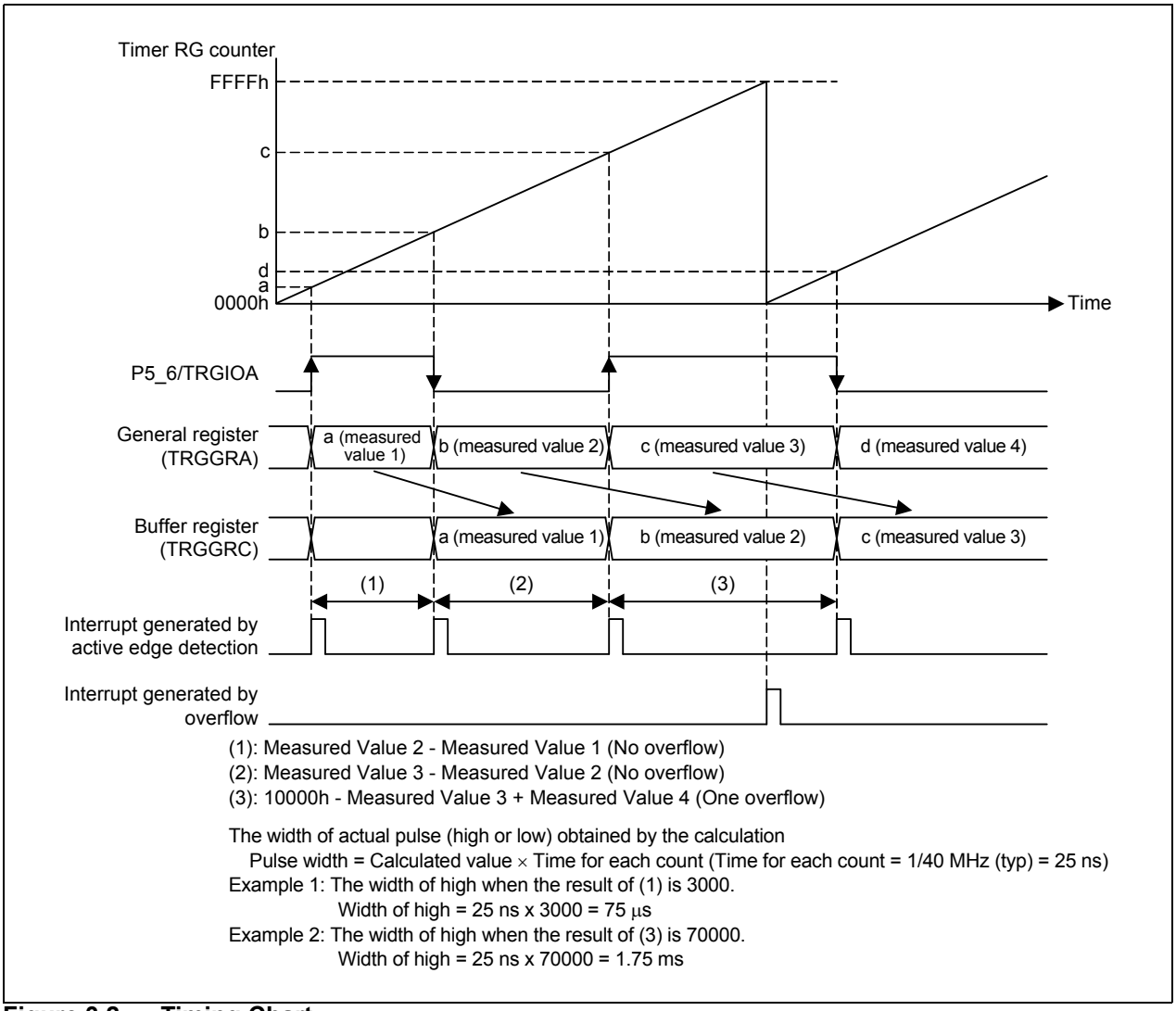


Figure 3.2 Timing Chart

Table 3.1 Pin and Function

Pin Name	I/O	Function
P5_6/TRGIOA	Input	External signal input

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	330 bytes	In the rej05b1156_src.c module
RAM	11 bytes	In the rej05b1156_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	19 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software Outline

This section shows the setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/38C Group Hardware Manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the hyphen represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The system clock (high-speed on-chip oscillator) is set.		

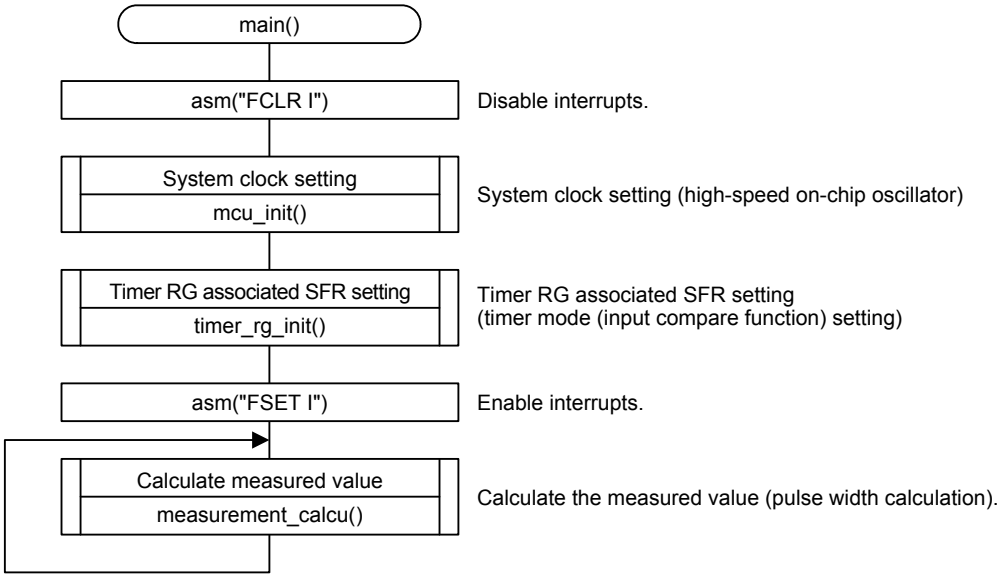
Declaration	void timer_rg_init(void)		
Outline	Timer RG associated SFR setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The SFR register is set to use the timer RG in input capture function.		

Declaration	void measurement_calcu(void)		
Outline	Measured value calculation result		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Content
	unsigned char f_capture		Capture flag
	unsigned short ovf_cnt		Overflow counter
	unsigned short present_value		RAM to hold TRGGRA register value
	unsigned short last_value		RAM to hold TRGGRC register value
	unsigned long measurement_value		RAM to hold measured value
Returned value	Type	Value	Meaning
	None	—	—
Function	Calculate the pulse width by the number of overflows and values read from registers TRGGRA and TRGGRC.		

Declaration	void timer_rg_interrupt(void)		
Outline	Timer RG interrupt		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char f_capture		Capture flag
	unsigned short ovf_cnt		Overflow counter
	unsigned short present_value		RAM to hold TRGGRA register value
	unsigned short last_value		RAM to hold TRGGRC register value
Returned value	Type	Value	Meaning
	None	—	—
Function	Count the number of overflows when an interrupt is triggered by overflow. When an interrupt is triggered by input capture, read the values in registers TRGGRA and TRGGRC.		

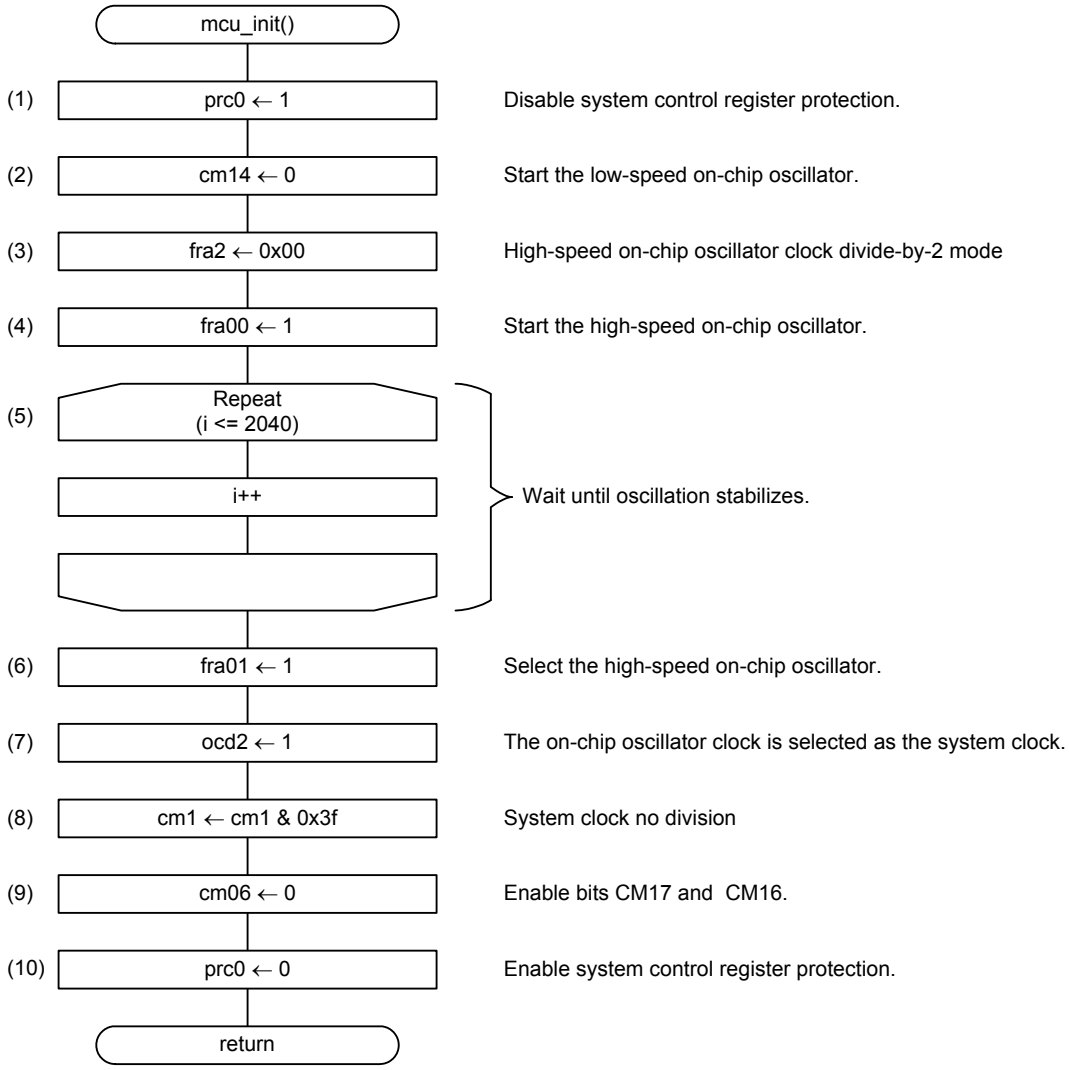
4.2 Main Function

- Flowchart



4.3 System Clock Setting

- Flowchart



• Register Settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set system clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

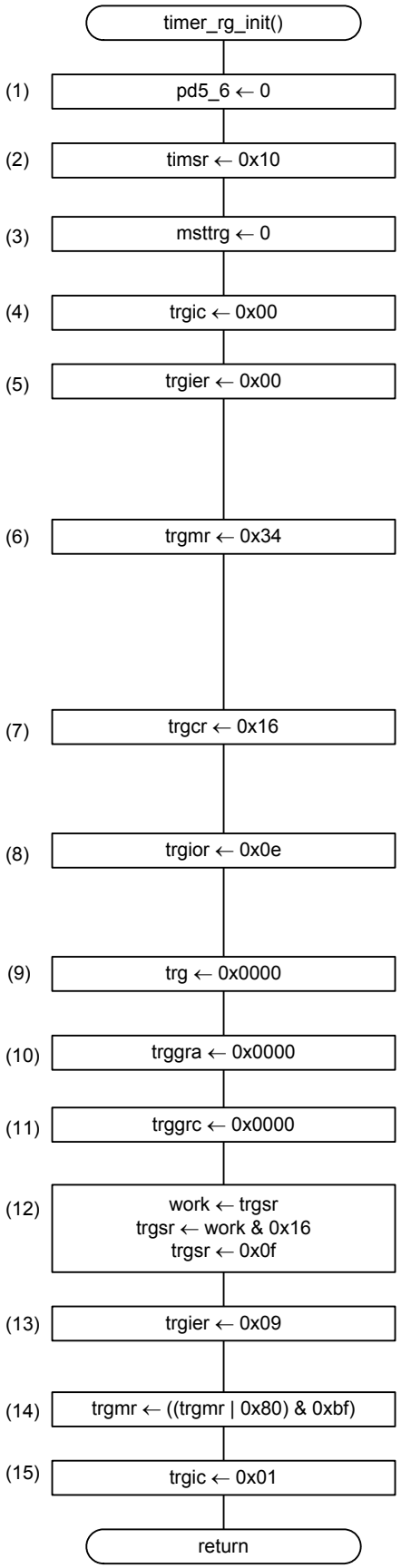
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write Disabled	R/W

4.4 Timer RG Associated SFR Setting

- Flowchart



Set the P5_6/TRGIOA pin as an input port.

The TRGIOA pin is assigned to P5_6.

Set timer RG to active.

Disable the timer RG interrupt.

Disable the IMFA bit initiated interrupt.
Disable the IMFB bit initiated interrupt.
Disable the UDF bit initiated interrupt.
Disable the OVF bit initiated interrupt.

Select the timer mode.
Select increment.
The digital filter function is used for the TRGIOA pin.
The digital filter function clock is selected by bits TCK0 to TCK2 in TRGCR register.
Stop the timer RG count.

Count source: fOCO40M
External clock active edge: Count at both the rising/falling edges
TRG register clear source: Clear disabled

TRGGRA control: Input capture to TRGGRA on both edge
TRGGRA mode: Input capture function
TRGGRC register function: Used as the buffer register of the TRGGRA register

Initialize the TRG register.

Initialize the TRGGRA register.

Initialize the TRGGRC register.

Clear input capture flag A.
Clear the overflow flag.
Write 0Fh continuously after this writing.

Enable IMFA bit initiated interrupts.
Enable OVF bit initiated interrupts.

Start the timer RG count.

Enable the timer RG interrupt.

• Register Settings

(1) Set the P5_6/TRGIOA pin as an input port.

Port P5 Direction Register (PD5)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	x	0	x	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	PD5_6	Port P5_6 direction bit	0: Input mode (functions as an input port)	R/W

(2) Assign the TRGIOA pin to P5_6.

Timer Pin Select Register (TIMSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	x	x	x	1	—	x	—	x

Bit	Symbol	Bit Name	Function	R/W
b4	TRGIOASEL	TRGIOA pin select bit	1: P5_6 pin assigned	R/W

(3) Set timer RG to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	x	x	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	MSTTRG	Timer RG standby bit	0: Active	R/W

(4) Disable the timer RG interrupt.

Interrupt Control Register (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R

(5) Disable all interrupt sources to timer RG.

Timer RG Interrupt Enable Register (TRGIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt by IMFA flag disabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt by IMFB flag disabled	R/W
b2	UDIE	Underflow interrupt enable bit	0: Interrupt by UDF flag disabled	R/W
b3	OVIE	Overflow interrupt enable bit	0: Interrupt by OVF flag disabled	R/W

(6) Set the TRGMR register.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	—	1	1	x	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWM	PWM mode select bit	0: Timer Mode	R/W
b1	MDF	Phase counting mode select bit	0: Increment	R/W
b2	DFA	Digital filer function select bit for TRGIOA pin	1: Digital filter function used	R/W
b4	DFCK0	Digital filter function clock select bit	b5 b4 1 1: Clock selected by bits TCK0 to TCK2 in TRGCR register	R/W
b5	DFCK1			R/W
b7	TSTART	TRG count start bit	0: Count stops	R/W

(7) Set the TRGCR register.

Timer RG Control Register (TRGCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	0	0	1	0	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 1 1 0: fOCO40M	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock active edge select bit	b4 b3 1 0: Count at both the rising/falling edges	R/W
b4	CKEG1			R/W
b5	CCLR0	TRG register clear source select bit	b6 b5 0 0: Clear disabled	R/W
b6	CCLR1			R/W

(8) Set the TRGIOR register.

Timer RG I/O Control Register (TRGIOR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	x	x	x	x	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	b1 b0 1 0: Input capture to TRGGRA register on both edges	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit	1: Input capture function	R/W
b3	BUFA	TRGGRC register function select bit	1: Used as the buffer register of the TRGGRA register	R/W

(9) Initialize the TRG counter to 0000h.

Timer RG Counter (TRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count operation is increment.	0000h to FFFFh	R/W

(10) Initialize the TRGGRA register to 0000h.

Timer RG General Register A (TRGGRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting value	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	These bits store the values in the timer RG counter when detecting an external input capture signal.	R/W

(11) Initialize the TRGGRC register to 0000h.

Timer RG General Register C (TRGGRC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting value	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	These bits are used as a buffer register of timer RG general register A.	R/W

(12) Clear the overflow flag and input capture flag A. Then write 0Fh continuously after this writing.

Timer RG Status Register (TRGSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—		0	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading	R/W
b3	OVF	Overflow flag		R/W

(13) Set the IMFA and OVF bits to enable the interrupt.

Timer RG Interrupt Enable Register (TRGIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	1	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	1: Interrupt by IMFA flag enabled	R/W
b3	OVIE	Overflow interrupt enable bit	1: Interrupt by OVF flag enabled	R/W

(14) Start the timer RG counter.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	—			x		x	

Bit	Symbol	Bit Name	Function	R/W
b7	TSTART	TRG count start bit	1: Count starts	R/W

(15) Enable the timer RG interrupt.

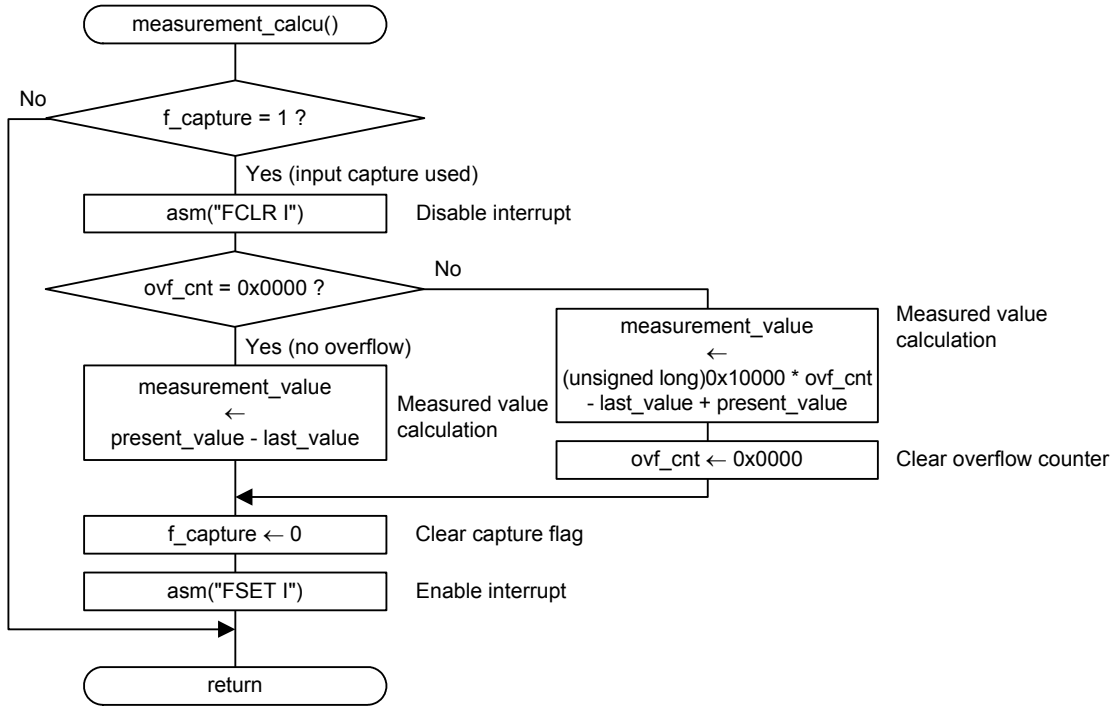
Interrupt Control Register (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R

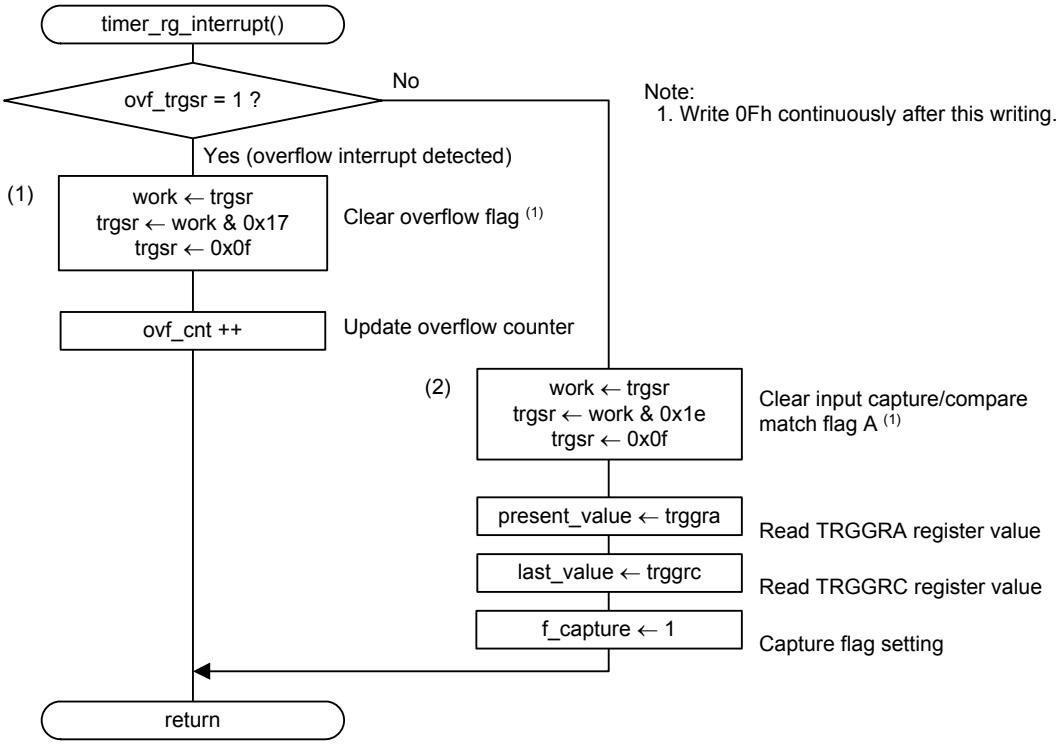
4.5 Measured Value Calculation

• Flowchart



4.6 Timer RG Interrupt

• Flowchart



• Register Settings

(1) Clear the overflow flag. Then write 0Fh continuously after this writing.

Timer RG Status Register (TRGSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—		0	x	x	

Bit	Symbol	Bit Name	Function	R/W
b3	OVF	Overflow flag	[Condition for setting to 0] Write 0 after reading.	R/W

(2) Clear input capture/compare match flag A. Then write 0Fh continuously after this writing.

Timer RG Status Register (TRGSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—			x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/38C Group User’s Manual: Hardware Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
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Inquiries

Revision History	R8C/38C Group Timer RG Timer Mode (Input Capture Function)

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 29, 2009	—	First edition issued
1.10	Mar. 10, 2011	—	R8C/38C Group hardware user's manual Rev.1.10 reviewed
		3	Table 3.2 revised, C compiler revised
		11, 17	Processing for TRGSR regsiter setting revised

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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