R8C/38C Group

Timer RC (PWM2 Mode)

R01AN0081EJ0100
Rev.1.00
Aug. 31, 2010

1. Abstract

This document describes a setting method and an application example for timer RC in PWM2 mode in the R8C/38C Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/38C Group
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

A PWM waveform with a 200 µs period is output. The PWM period is generated at a compare match of the timer RC counter (TRC) and general register A (TRCGRA). PWM change points for each are generated at the compare match of the TRC register and general registers TRCGRB and TRCGRC. An interrupt is generated at the compare match of registers TRC and TRCGRA. Output signals are as follows:

TRCIOB pin: Active high level 100 µs = 1/20 MHz × (TRCGRB – TRCGRC)
= 50 ns × (3000 – 1000) = 50 ns × 2000
Wait time: 50 µs = 1/20 MHz × TRCGRC
= 50 ns × 1000
The 200 µs PWM period is set to the TRCGRA register.
200 µs = 1/20 MHz × (TRCGRA + 1) = 50 ns × 4000

Settings

- Use f1 (XIN clock: 20 MHz) as the count source.
- Clear the TRC register at the compare match of the TRCGRA register.
- Select the TRCIOB pin output level as active high and the initial output level as inactive low.
- Output an active high level from the TRCIOB output pin at the compare match of registers TRC and TRCGRC.
- Output an active high level from the TRCIOB output pin at the compare match of registers TRC and TRCGRB.
- Do not use buffer operation (BFD).
- Disable trigger input from the TRCTRG pin.
- Do not use the pulse output forced cutoff input function.
- Do not use A/D triggers.
- Use the timer RC interrupt.

Figure 3.1 shows a Block Diagram and Figure 3.2 shows a Timing Diagram. Table 3.1 lists the pin used and its function.

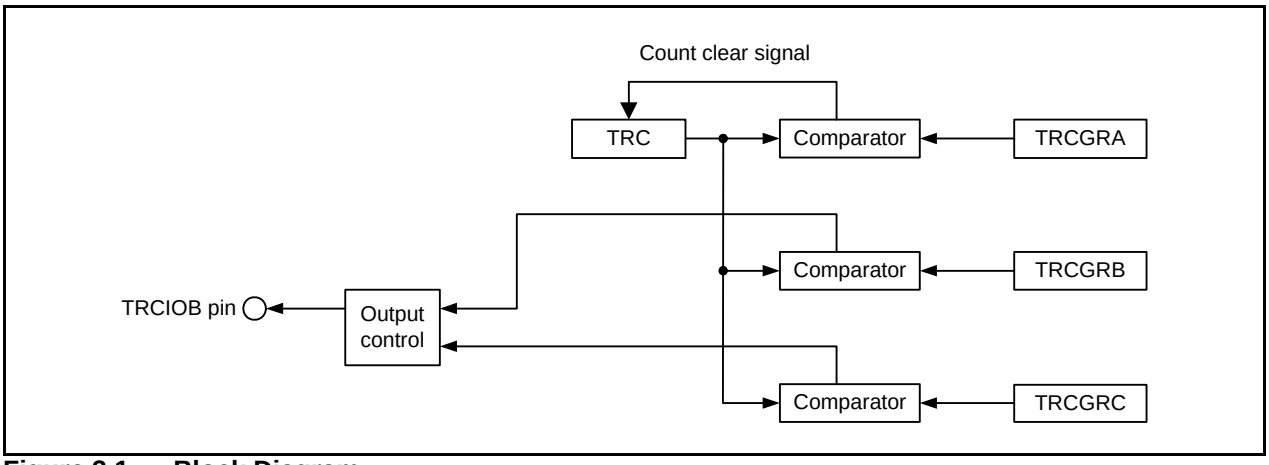


Figure 3.1 Block Diagram

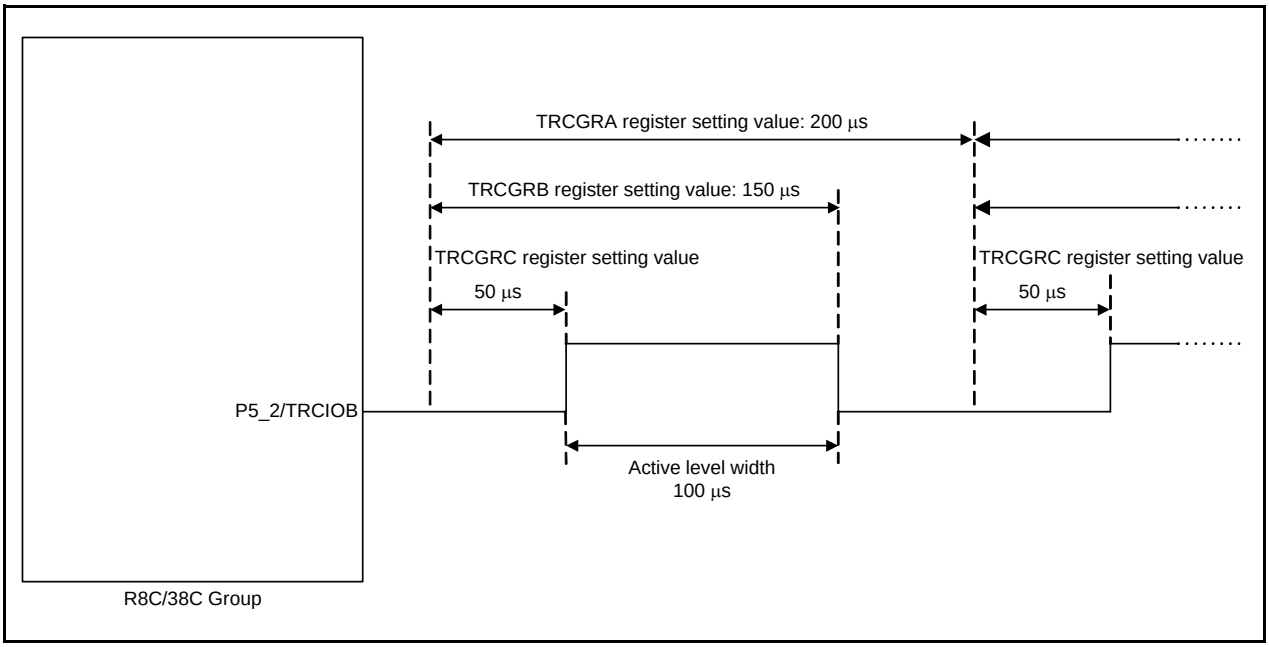


Figure 3.2 Timing Diagram

Table 3.1 Pin and Its Function

Pin Name	I/O	Function
P5_2/TRCIOB	Output	PWM output

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	192 bytes	In the r01an0081_src.c module
RAM	0 bytes	In the r01an0081_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/38C Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

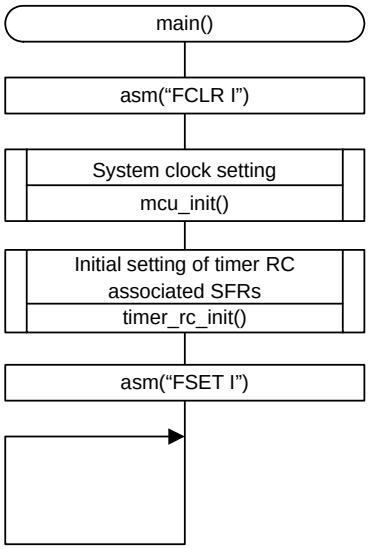
Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (XIN clock).		

Declaration	void timer_rc_init(void)		
Outline	Initial setting of timer RC associated SFRs		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Initialize timer RC associated SFRs to use timer RC in PWM2 mode.		

Declaration	void _timer_rc(void)		
Outline	Timer RC interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform timer RC interrupt handling.		

4.2 Main Function

• Flowchart



Disable interrupts.

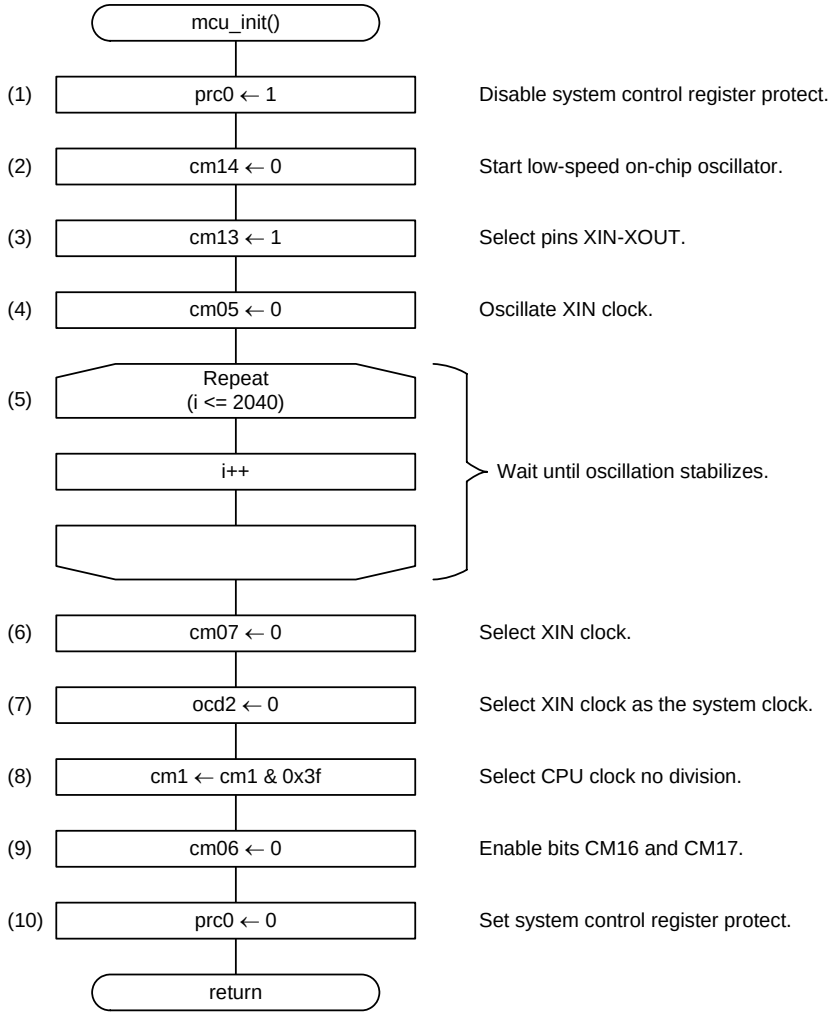
System clock setting (XIN clock set)

Initial setting of timer RC associated SFRs (PWM2 mode set)

Enable interrupts.

4.3 System Clock Setting

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0		x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set system clock control register 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—		1	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port/XIN-XOUT switch bit	1: XIN-XOUT pin	R/W

(4) Set system clock control register 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(5) Wait until oscillation stabilizes.

(6) Select the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	0: XIN clock	R/W

(7) Select the XIN clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	0: XIN clock selected	R/W

(8) Set system clock register 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—			x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock control register 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

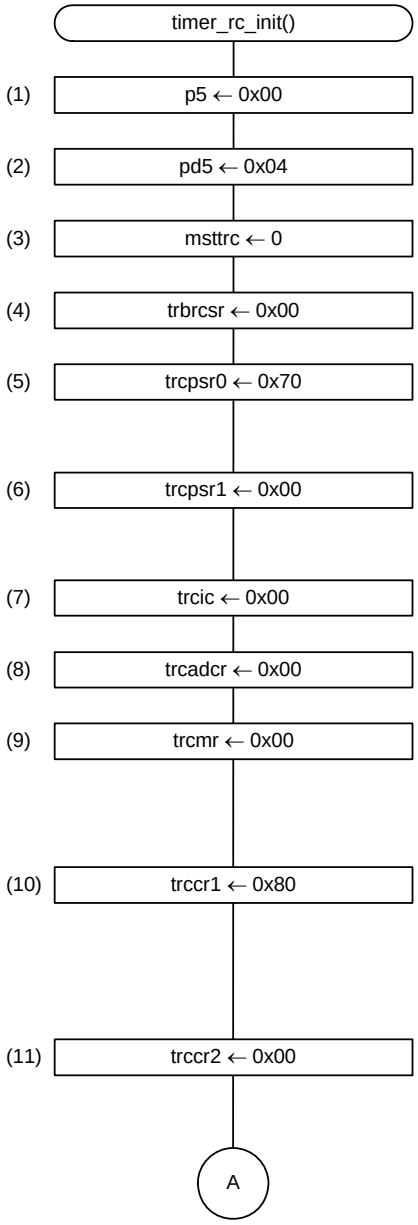
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Initial Setting of Timer RC Associated SFRs

• Flowchart



Initialize port P5.

Set port P5_2 to output mode.

Set timer RC to active.

Do not use TRCCLK pin.

Do not use TRCIOA/TRCTRG pin.
Assign TRCIOB pin to port P5_2.

Do not use TRCIOC pin.
Do not use TRCIOD pin.

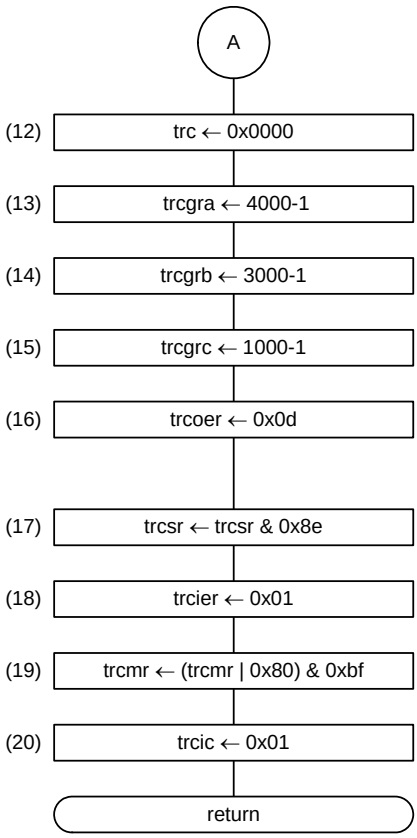
Disable timer RC interrupt.

Disable A/D triggers.

Stop timer RC count.
Select PWM mode for PWM2 mode select bit.
Select general register for TRCGRC register function.

Set TRCIOB pin to active high level (low for initial output, high output at compare match with TRCGRC register, and low output at compare match with TRCGRB register).
Select f1 as count source.
Clear TRC counter at compare match with TRCGRA register.

Continue counting after compare match with TRCGRA register.
Disable trigger input from TRCTRG pin.



Initialize TRC register count value to 0000h.

Set 200 μs for PWM period (50 ns × 4000 = 200 μs)

Set 150 μs (50 ns × 3000 = 150 μs) for active level complete time from count start.

Set 50 μs (50 ns × 1000 = 50 μs) for wait time from count start.

Enable TRCIOB0 output.
Disable pulse output forced cutoff input.

Clear input capture/compare match flag A.

Set IMFA bit to enable IMIA interrupt.

Start timer RC count.

Enable timer RC interrupt (level 1).

• Register settings

(1) Initialize port P5.

Port P5 Register (P5)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	P5_2	Port P5_2 bit	0: “L” level	R/W

(2) Set port P5_2 to output mode.

Port P5 Direction Register (PD5)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	PD5_2	Port P5_2 direction bit	1: Output mode (functions as an output port)	R/W

(3) Set timer RC to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	0	x	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	MSTTRC	Timer RC standby bit	0: Active	R/W

(4) Set the timer RB/RC pin select register.

Timer RB/RC Pin Select Register (TRBRCSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	0	0	—	—	—	x

Bit	Symbol	Bit Name	Function	R/W
b4	TRCCLKSEL0	TRCCLK pin select bit	b6 b5 b4 0 0 0: TRCCLK pin not used	R/W
b5	TRCCLKSEL1			R/W
b6	TRCCLKSEL2			R/W

(5) Set timer RC pin select register 0.

Timer RC Pin Select Register 0 (TRCPSR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	1	1	1	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b4	TRCIOBSEL0	TRCIOB pin select bit	b6 b5 b4 1 1 1: P5_2 assigned	R/W
b5	TRCIOBSEL1			R/W
b6	TRCIOBSEL2			R/W

(6) Set timer RC pin select register 1.

Timer RC Pin Select Register 1 (TRCPSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	0	0	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b2 b1 b0 0 0 0: TRCIOC pin not used	R/W
b1	TRCIOCSEL1			R/W
b2	TRCIOCSEL2			R/W
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W

(7) Disable the timer RC interrupt.

Interrupt Control Register (TRCIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

(8) Set to A/D trigger disabled.

Timer RC Trigger Control Register (TRCADCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGAE	A/D trigger A enable bit	0: A/D trigger disabled	R/W
b1	ADTRGBE	A/D trigger B enable bit	0: A/D trigger disabled	R/W
b2	ADTRGCE	A/D trigger C enable bit	0: A/D trigger disabled	R/W

(9) Stop the timer RC count and set PWM2 mode and TRCGRC register function select bit.

Timer RC Mode Register (TRCMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	x	0	0	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	PWM2	PWM2 mode select bit	0: PWM 2 mode	R/W
b4	BFC	TRCGRC register function select bit	0: General register	R/W
b7	TSTART	TRC count start bit	0: Count stops	R/W

(10) Set timer RC control register 1.

Timer RC Control Register 1 (TRCCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	0	x	x	0	x

Bit	Symbol	Bit Name	Function	R/W
b1	TOB	TRCIOB output level select bit	0: Active level “H” (Initial output “L”, “H” output by compare match in the TRCGRC register “L” output by compare match in the TRCGRB register)	R/W
b4	TCK0	Count source select bit	b6 b5 b4 0 0 0: f1	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	1: Clear by compare match in the TRCGRA register	R/W

(11) Set timer RC control register 2.

Timer RC Control Register 2 (TRCCR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	—	—	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b5	CSEL	TRC count operation select bit	0: Count continues at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit	b7 b6 0 0: Disable the trigger input from the TRCTRG pin	R/W
b7	TCEG1			R/W

(12) Initialize the timer RC counter to 0000h.

Timer RC Counter (TRC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15-b0	Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

(13) Set compare value 4000 - 1 (F9Fh) with the timer RC counter to timer RC general register A.

Timer RC General Register A (TRCGRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	1	1	1	1

Bit	Function	R/W
b15-b0	General register. Set the PWM period.	R/W

(14) Set compare value 3000 - 1 (BB7h) with the timer RC counter to timer RC general register B.

Timer RC General Register B (TRCGRB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	1	1	0	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	1	0	1	1

Bit	Function	R/W
b15-b0	General register. Set the PWM output change point.	R/W

(15) Set compare value 1000 - 1 (3E7h) with the timer RC counter to timer RC general register C.

Timer RC General Register C (TRCGRC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	0	0	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	1	1

Bit	Function	R/W
b15-b0	General register. Set the PWM output change point (wait time after trigger).	R/W

(16) Set the timer RC output master enable register.

Timer RC Output Master Enable Register (TRCOER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	—	—	x	x	0	x

Bit	Symbol	Bit Name	Function	R/W
b1	EB	TRCIOB output disable bit	0: Enable output	R/W
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled	R/W

(17) Initialize input capture/compare match flag A.

Timer RC Status Register (TRCSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.	R/W

(18) Set the IMFA bit to enable the IMIA interrupt.

Timer RC Interrupt Enable Register (TRCIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	1: Enable interrupt (IMIA) by the IMFA bit	R/W

(19) Start the timer RC count.

Timer RC Mode Register (TRCMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	—	x			x	x	x

Bit	Symbol	Bit Name	Function	R/W
b7	TSTART	TRC count start bit	1: Count starts	R/W

(20) Enable the timer RC interrupt (level 1).

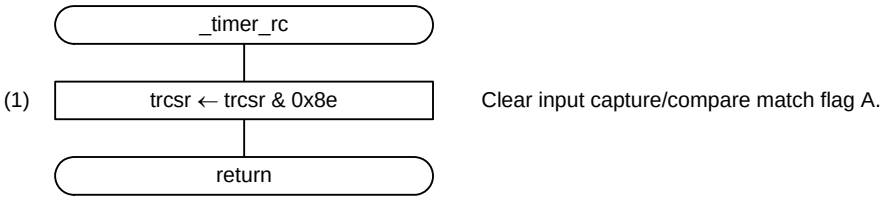
Interrupt Control Register (TRCIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

4.5 Timer RC Interrupt Handling

• Flowchart



• Register setting

(1) Initialize input capture/compare match flag A.

Timer RC Status Register (TRCSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/38C Group User’s Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	R8C/38C Group Timer RC (PWM2 Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 31, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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