

1. Abstract

This documents describes the UART version program downloader for the R8C/35C Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/35C Group
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Program Downloader Overview

3.1 Downloader Specifications

- The system program (including program downloader process) is allocated to block 0.
- The program downloader erases and writes mainly to user programs other than the user program in block 0. The program downloader ignores rewrite operations to block 0.
- EW0 mode is used by the program downloader for rewriting the CPU.
- In a reset start, the program downloader checks the state of port P1_5 and selects either to use the program downloader or the user program. The program downloader operates when port P1_5 is high, and the user program operates when port P1_5 is low.
- The virtual fixed vector table is allocated to block 1 to use the fixed vector table interrupt in the user program.
- UART0 clock asynchronous serial I/O (UART) is used to communicate with a programmer.
- CMOS output is selected for the TXD0 pin.
- The communication format is as follows:
 Bit rate: approximately 9600 bps Transfer data length: 8 bits
 Stop bit: 1 bit Parity bit: None
- Refer to 4. Downloader Communication Protocol for the communication protocol.

Figure 3.1 shows an example of a Connection, Figure 3.2 shows the Transfer Format, Figure 3.3 shows the Memory Map (32 Kbyte ROM MCU), and Figure 3.4 shows an example of the System Interrupt Operation (Overflow Interrupt).

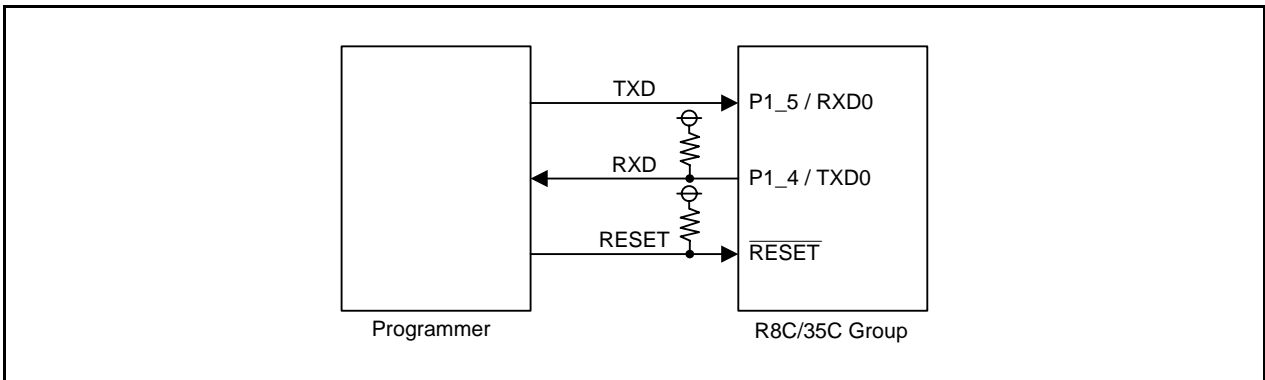


Figure 3.1 Connection

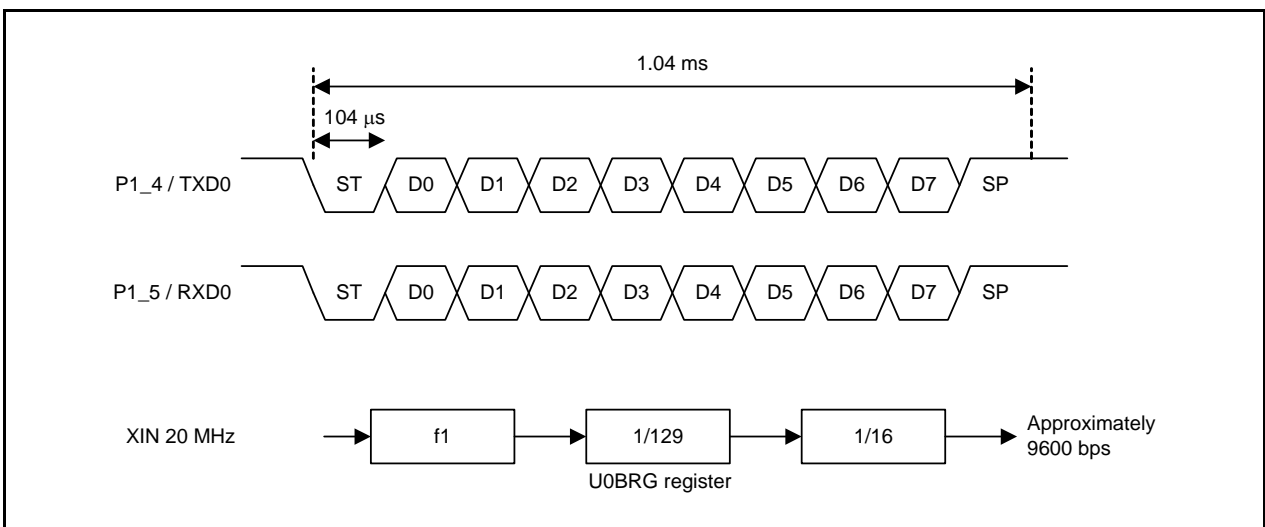


Figure 3.2 Transfer Format

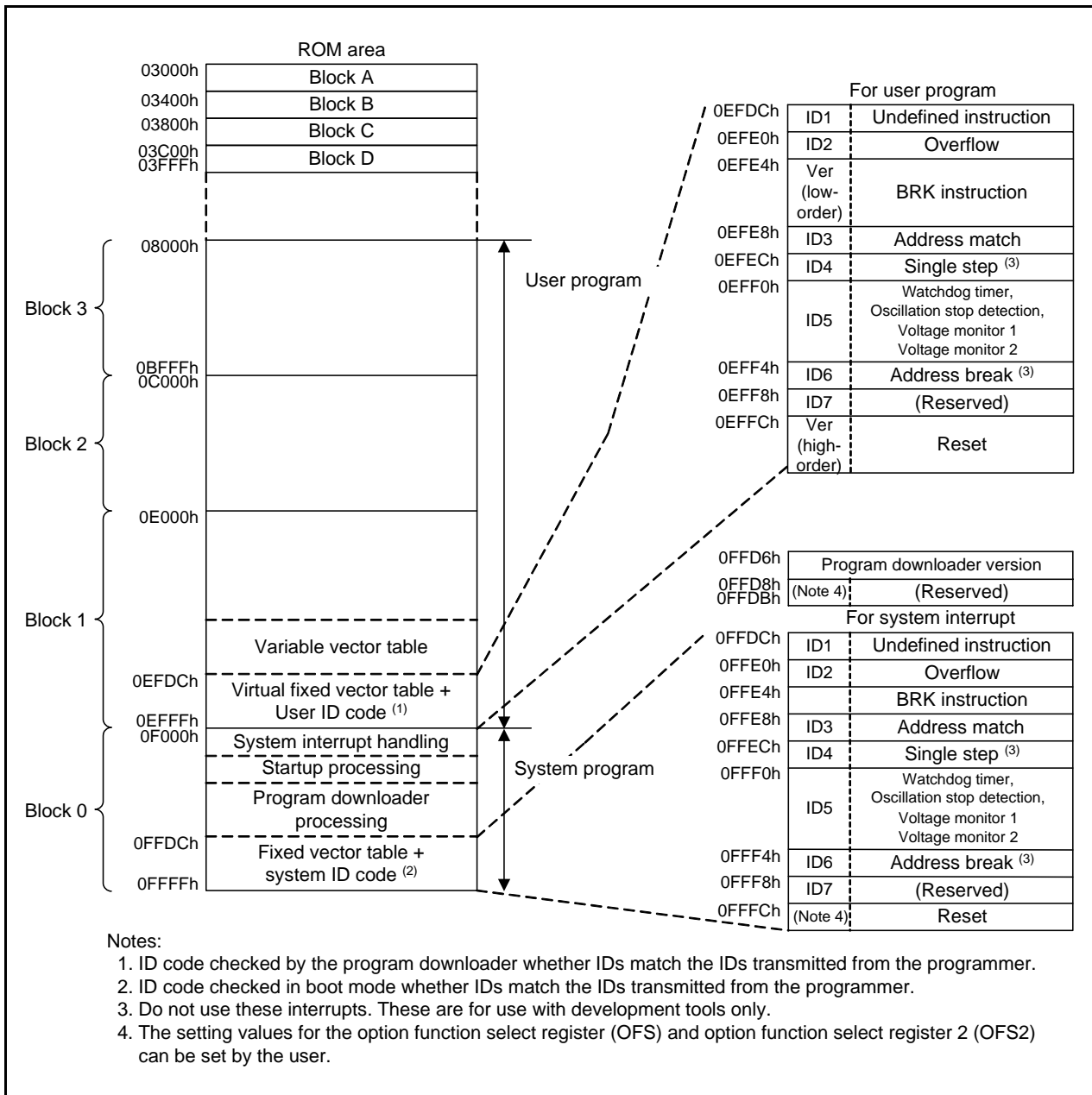


Figure 3.3 Memory Map (32 Kbyte ROM MCU)

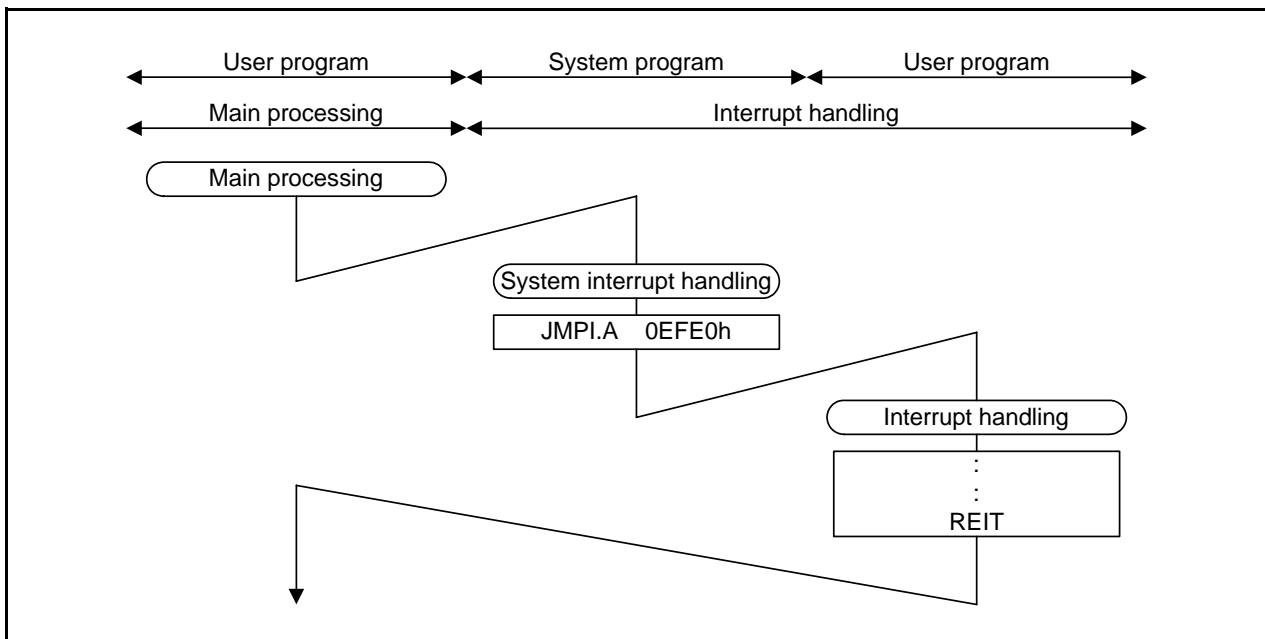


Figure 3.4 System Interrupt Operation (Overflow Interrupt)

3.2 Timing after Reset

The operating program after reset chooses either the program downloader or the user program. The MCU enters either program according to the P1_5/RXD0 pin level applied to the MCU during (1). Before reset is deasserted, a programmer must determine the input level of the P1_5/RXD0 pin, and hold that level during (1).

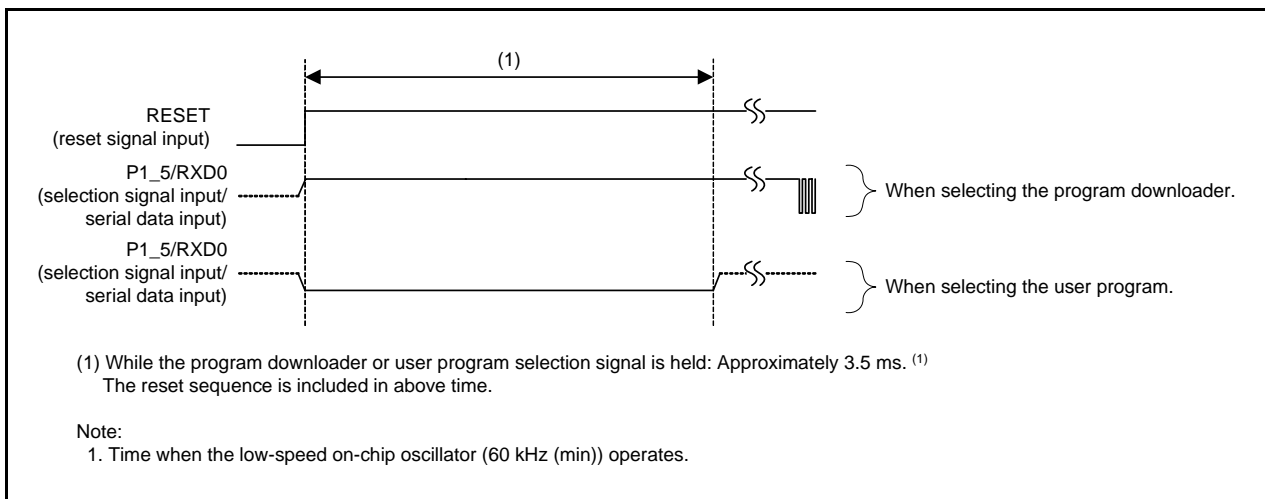


Figure 3.5 Signal Control Timing after Reset

3.3 Initial Settings

(1) Option function select register (OFS)

The OFS register is assigned to the highest-order address 0FFFFh in the fixed vector table. Set the OFS register by a program of the program downloader.

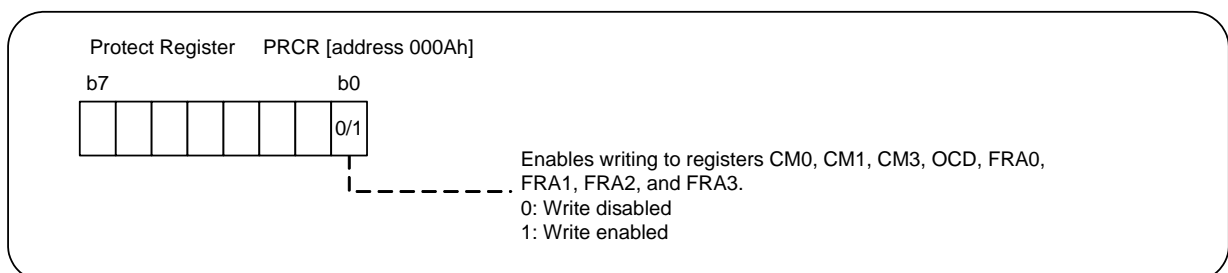
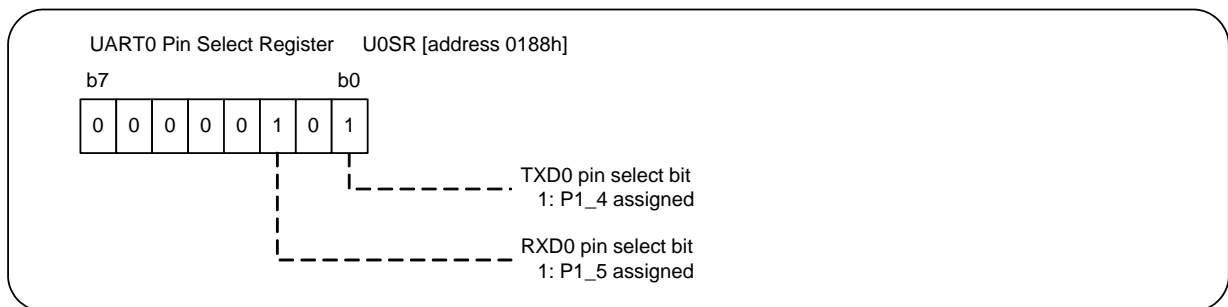
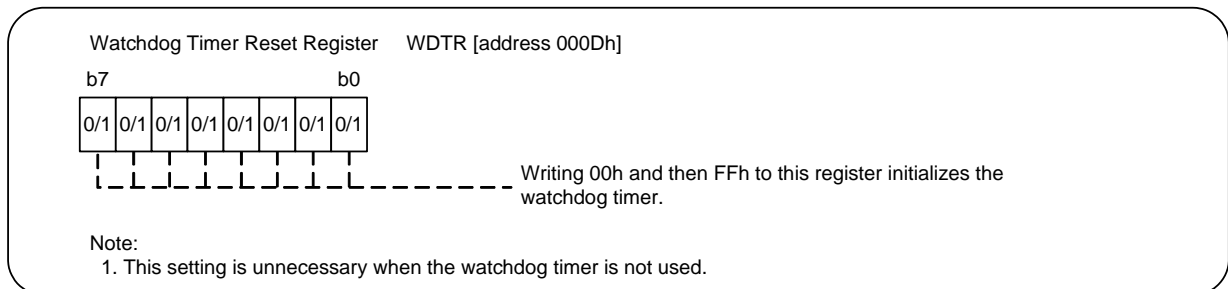
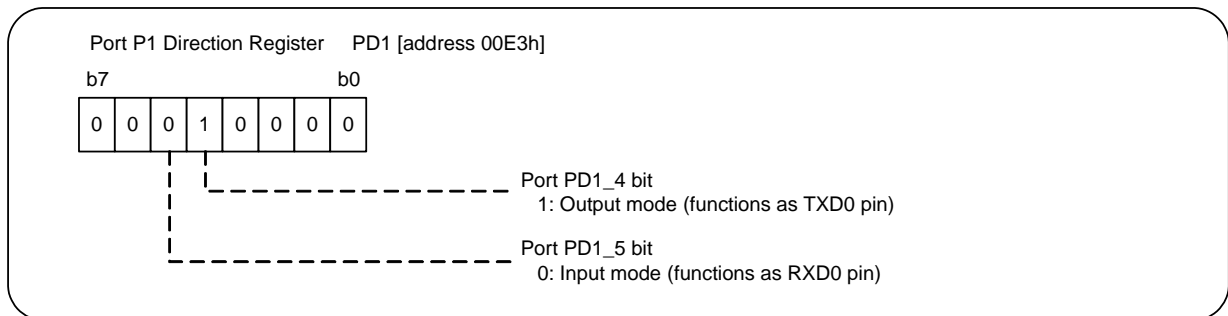
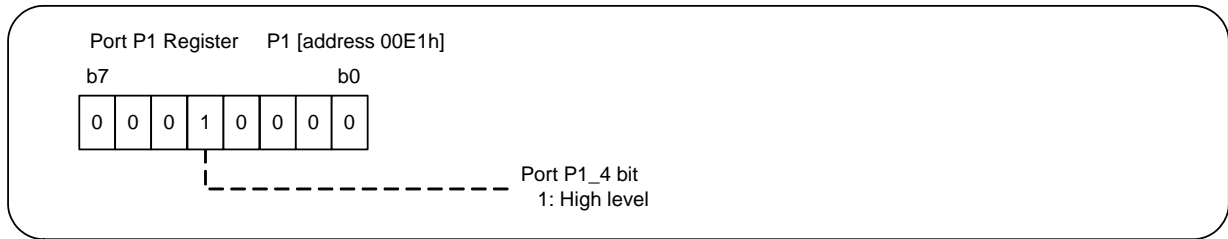
(2) Option function select register 2 (OFS2)

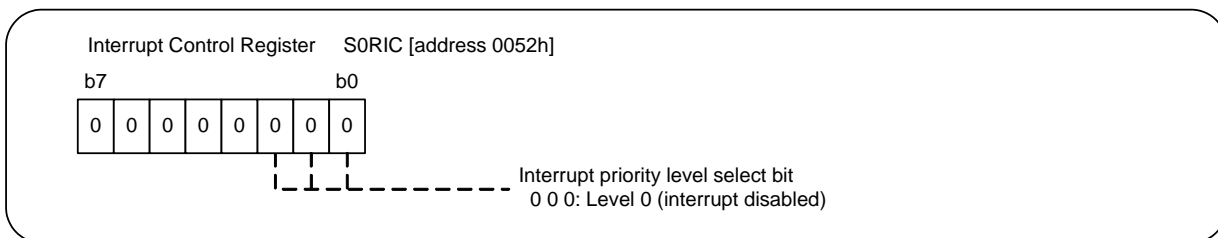
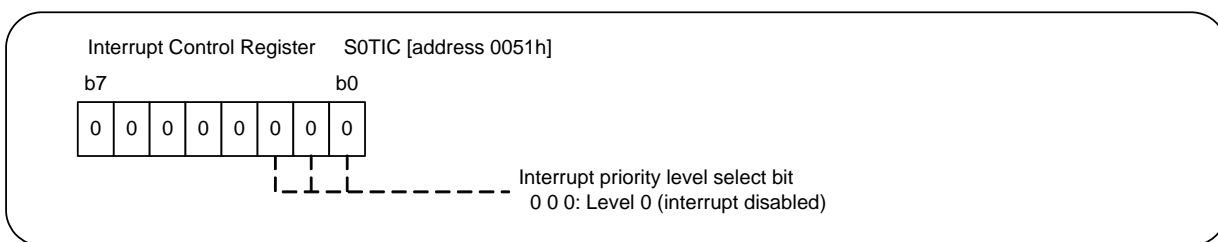
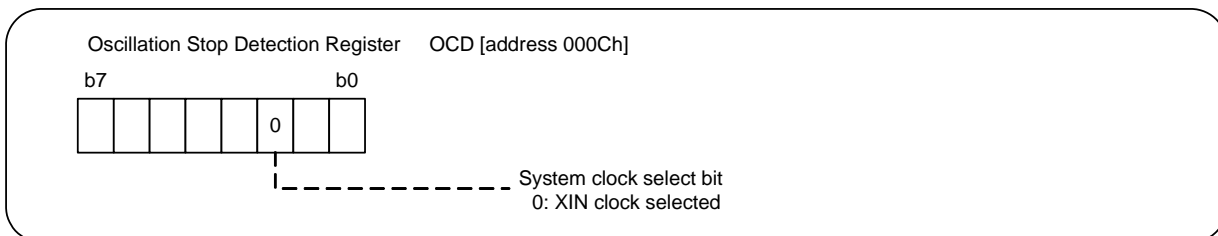
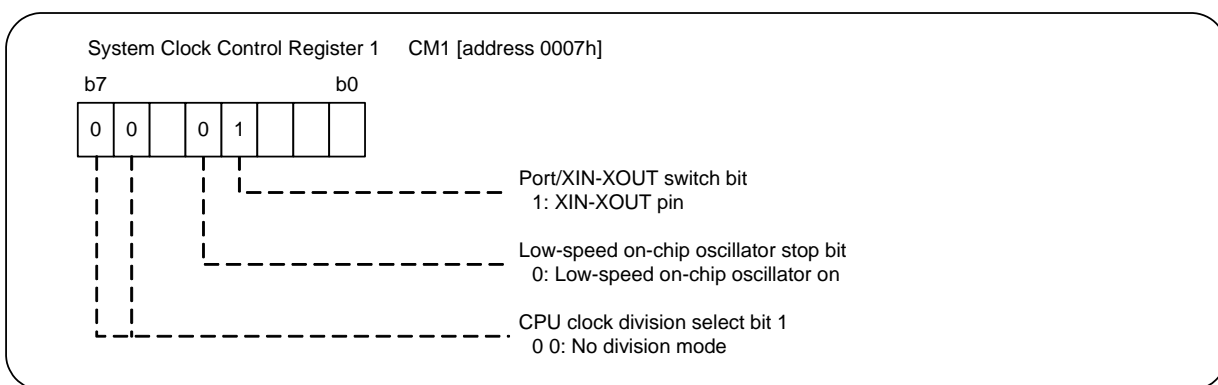
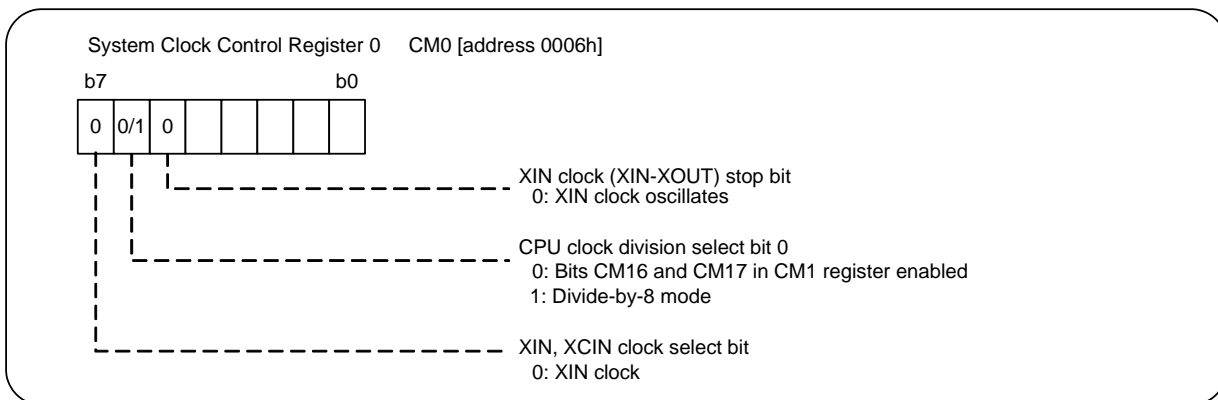
The OFS2 register is assigned to 0FFDBh in the reserved area. Set the OFS2 register by a program of the program downloader.

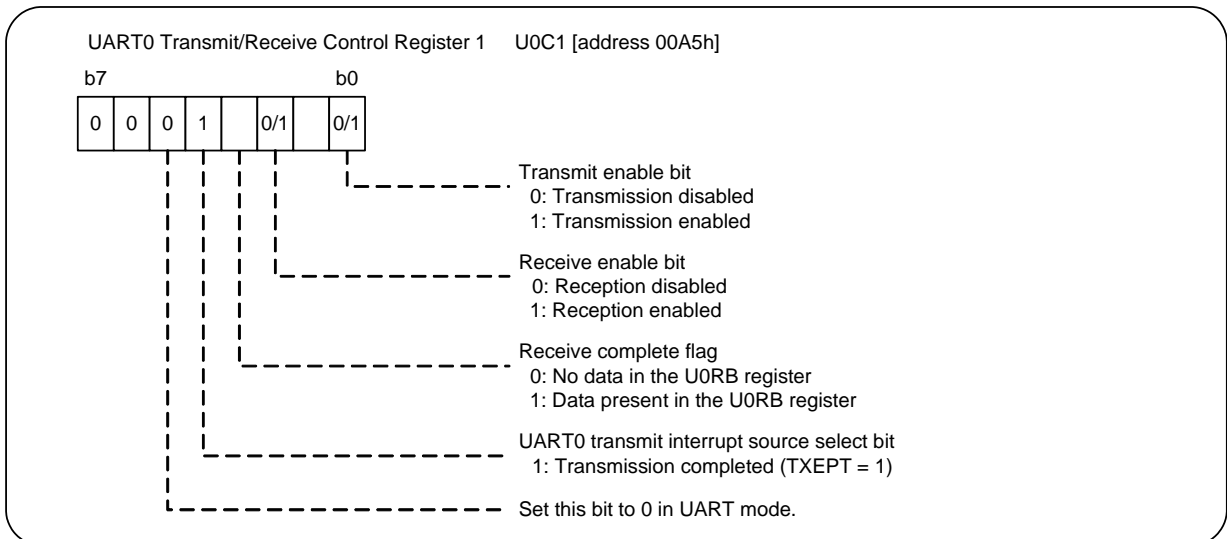
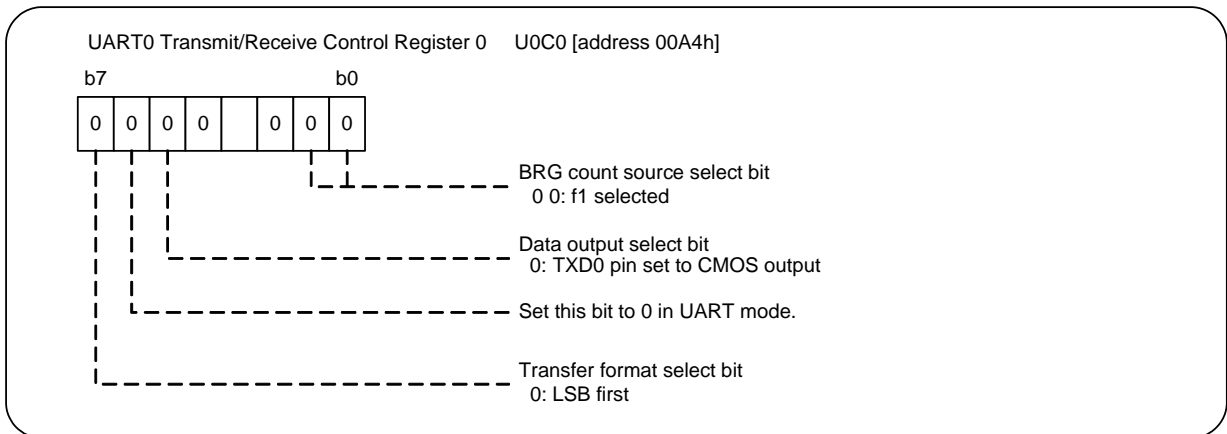
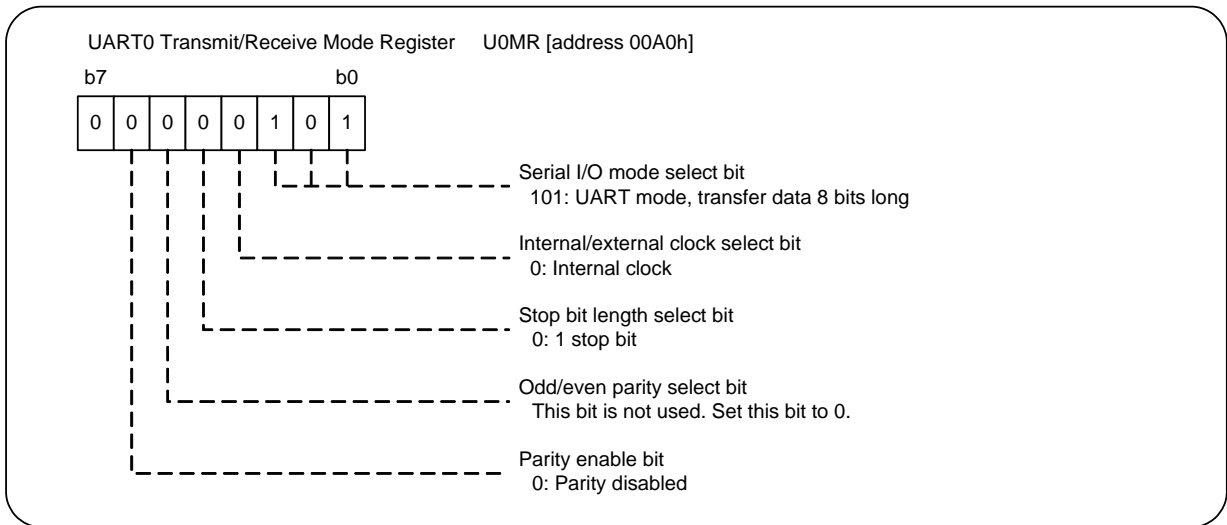
(3) Watchdog timer

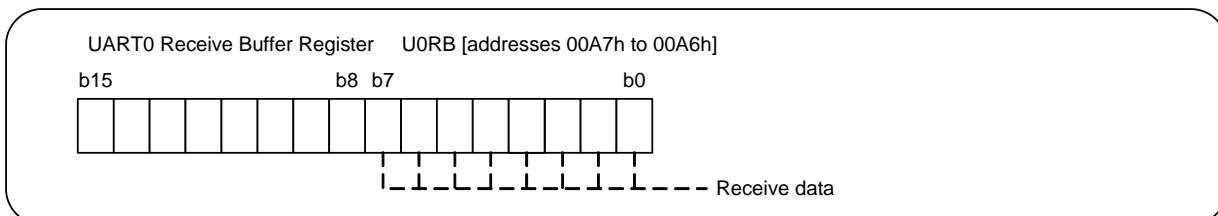
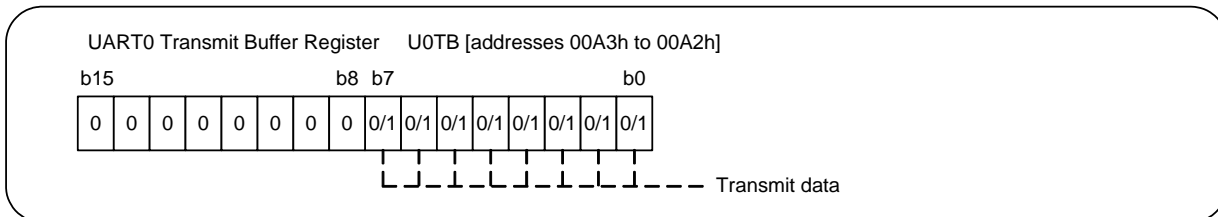
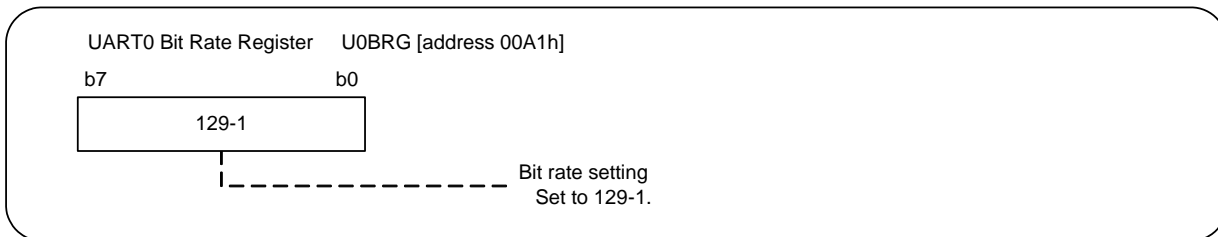
When using the watchdog timer, enable the WDT_USE definition in the fla_r835c.inc file.

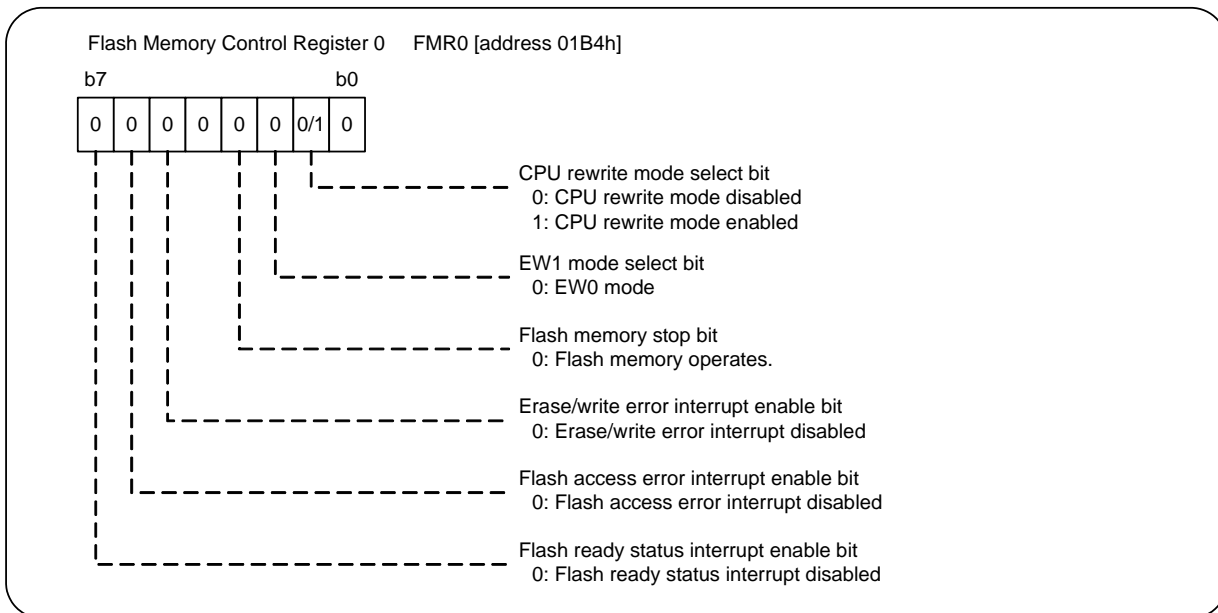
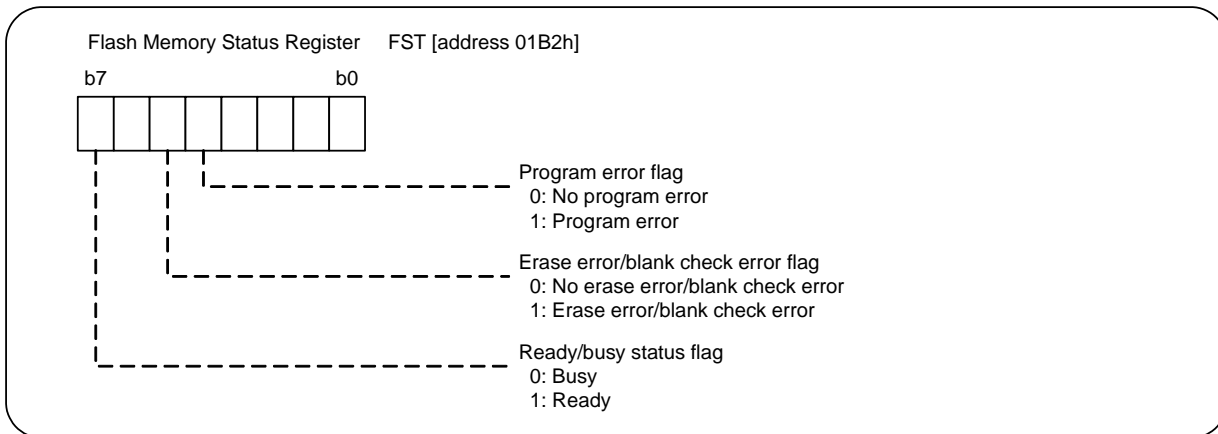
3.4 Registers

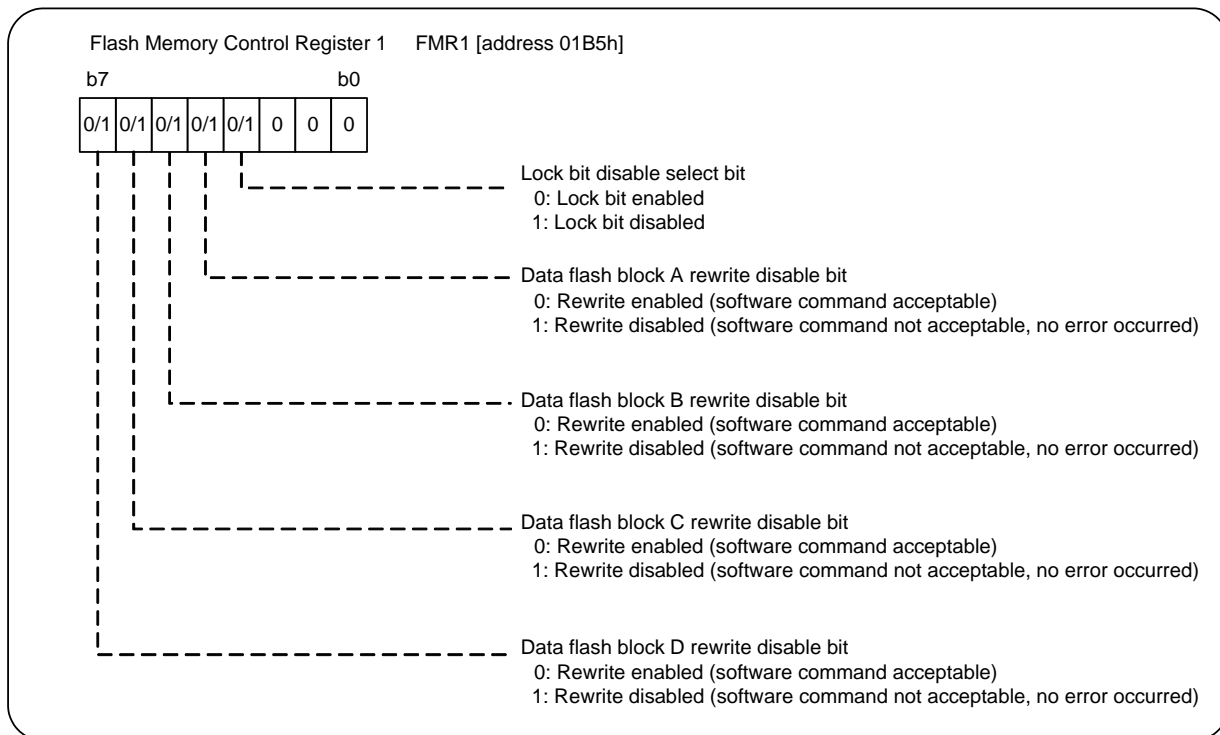












3.5 Memory

Table 3.1 Memory

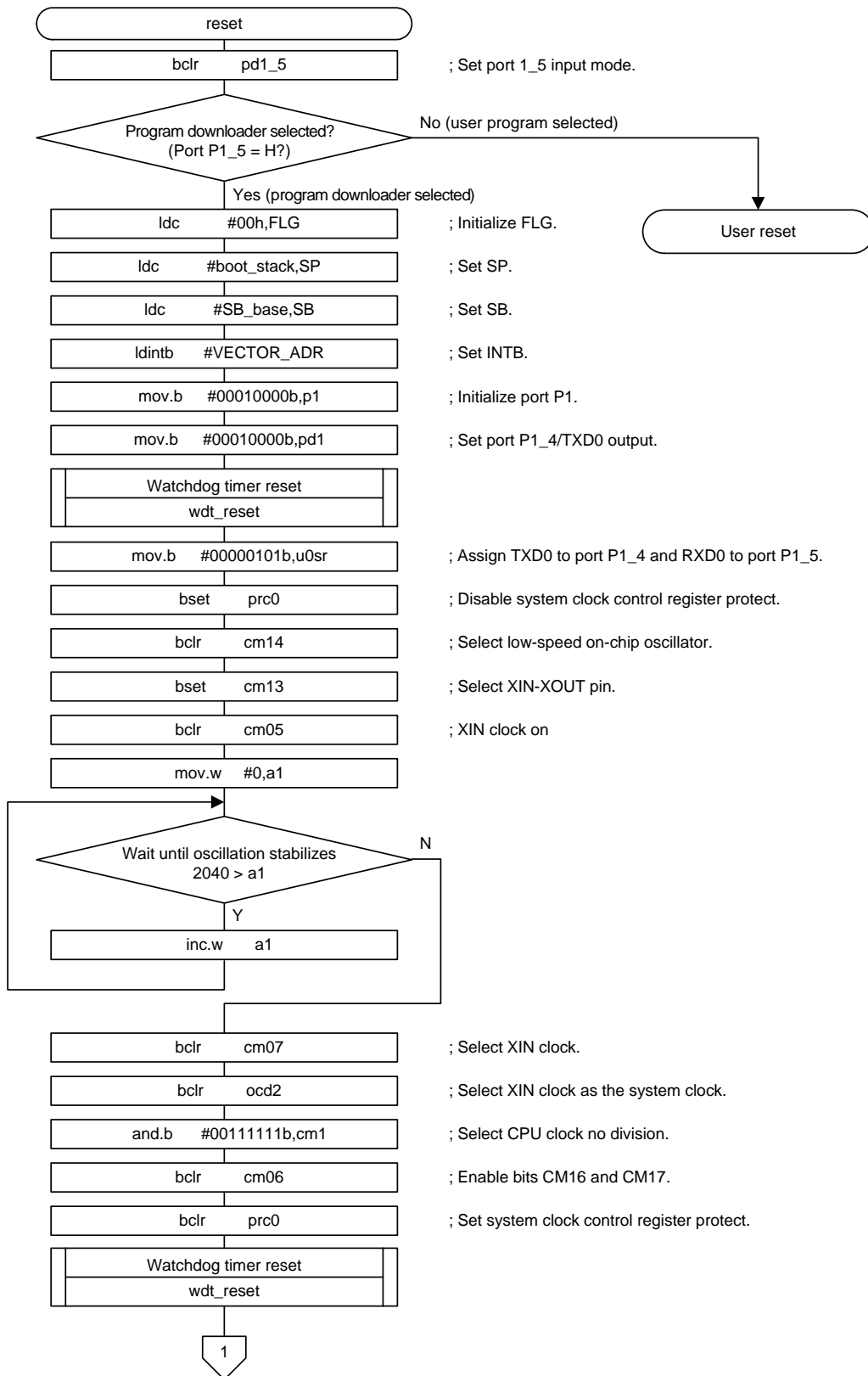
Assigned Memory	Size	Remarks
ROM	1226 bytes	System program only (including fixed vector and variable vector table)
RAM	427 bytes	System program only

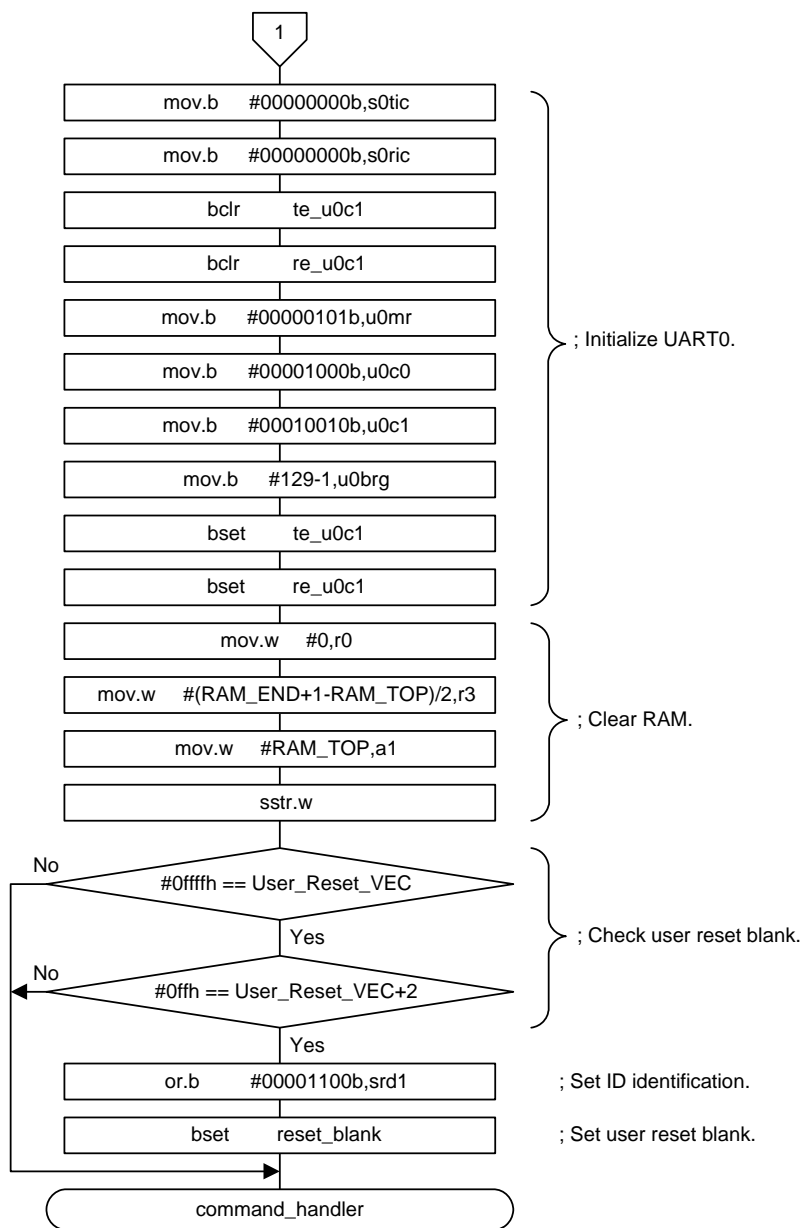
Table 3.2 RAM and Definitions

Symbol	Size	Description
ram_execute	128 bytes	EW0 mode program area
status_flags	1 byte	Serial flag area
reset_blank	–	User program blank flag
srd1	1 byte	SRD1 register
srd08	–	SR8 bit
srd09	–	SR9 bit
srd10	–	SR10 bit
srd11	–	SR11 bit
srd12	–	SR12 bit
srd13	–	SR13 bit
srd14	–	SR14 bit
srd15	–	SR15 bit
srd	1 byte	SRD register
address	4 bytes	Address data
temp	32 bytes	Temporary (used with the stack area)
rx_data	2 bytes	Receive data
tx_data	1 byte	Transmit data
page_buffer	256 bytes	Page buffer

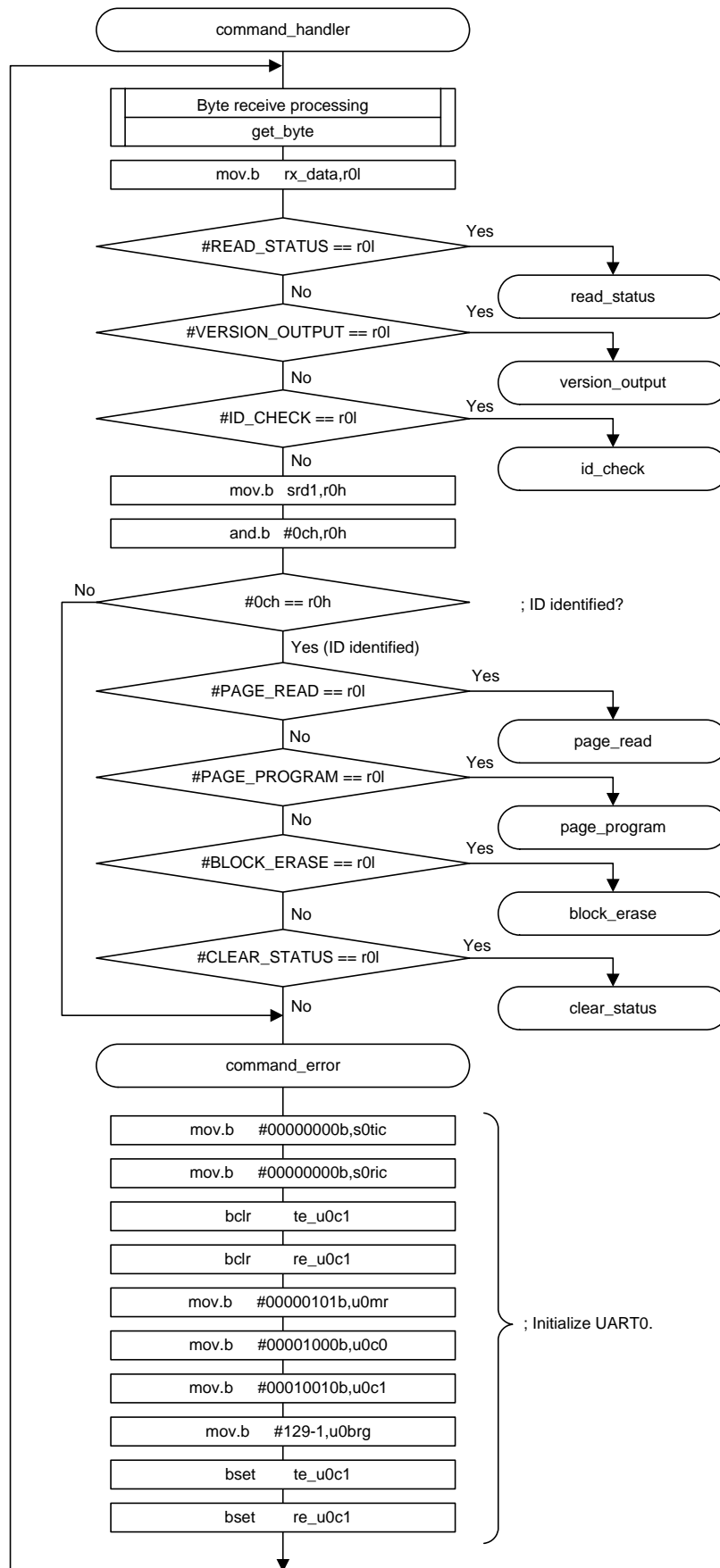
3.6 Flowchart

(1) Startup processing

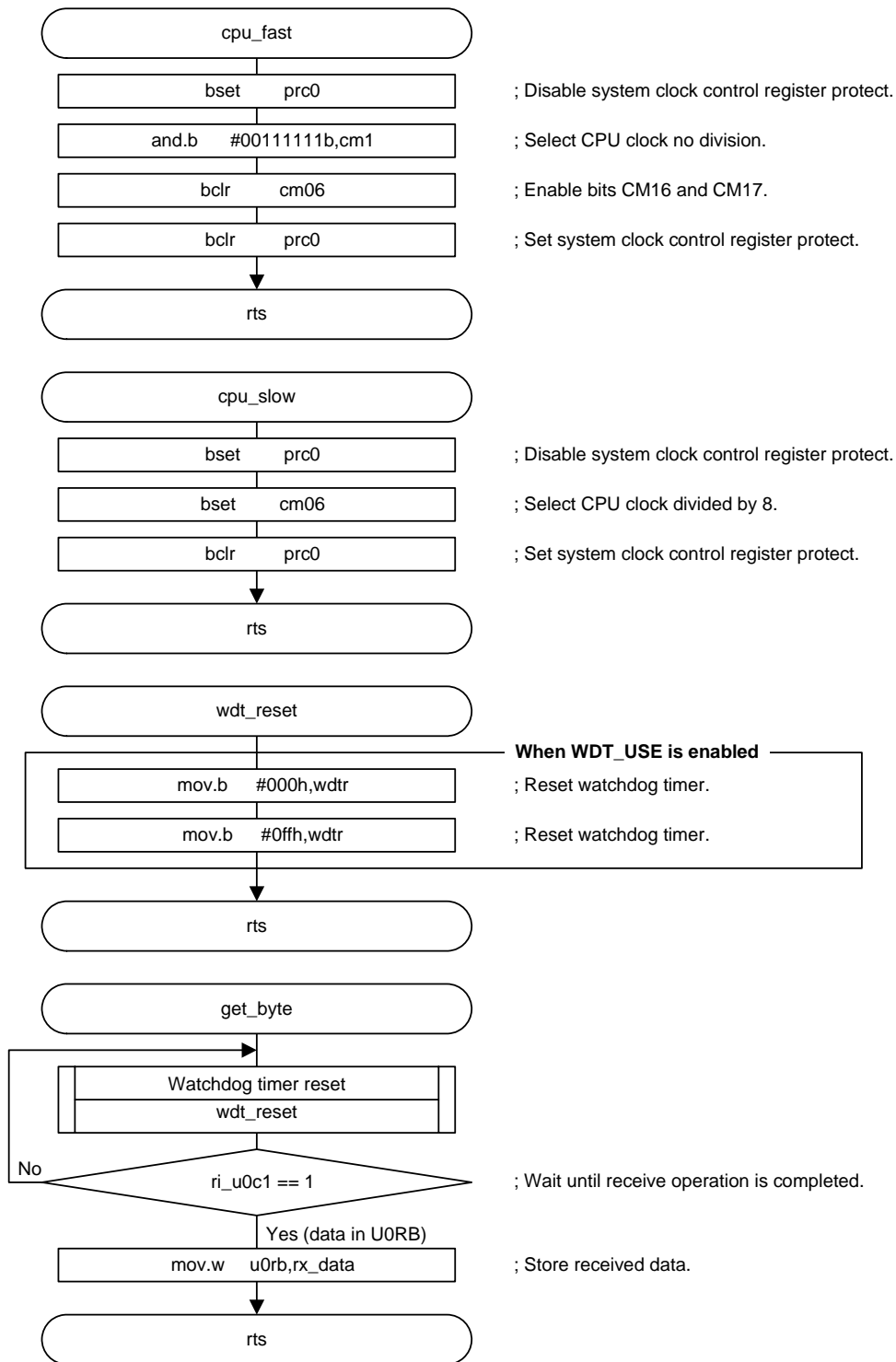




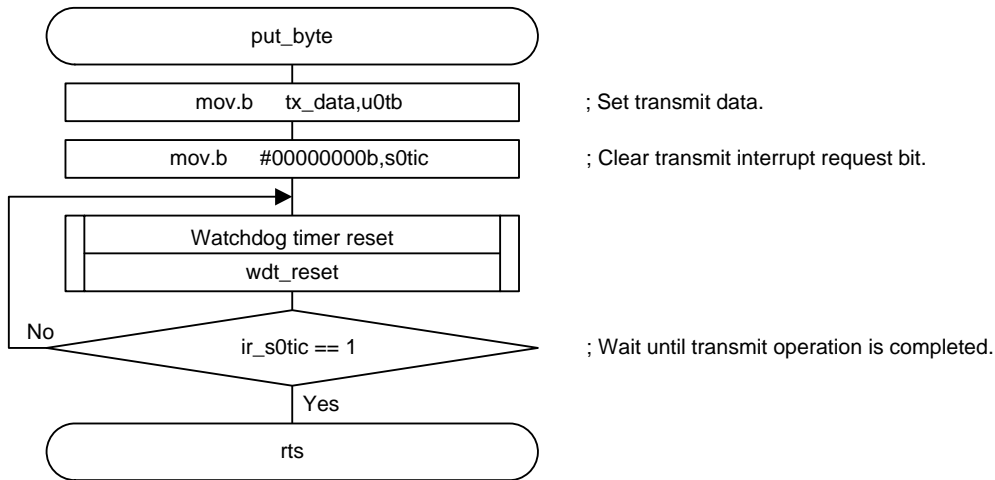
(2) Command handler



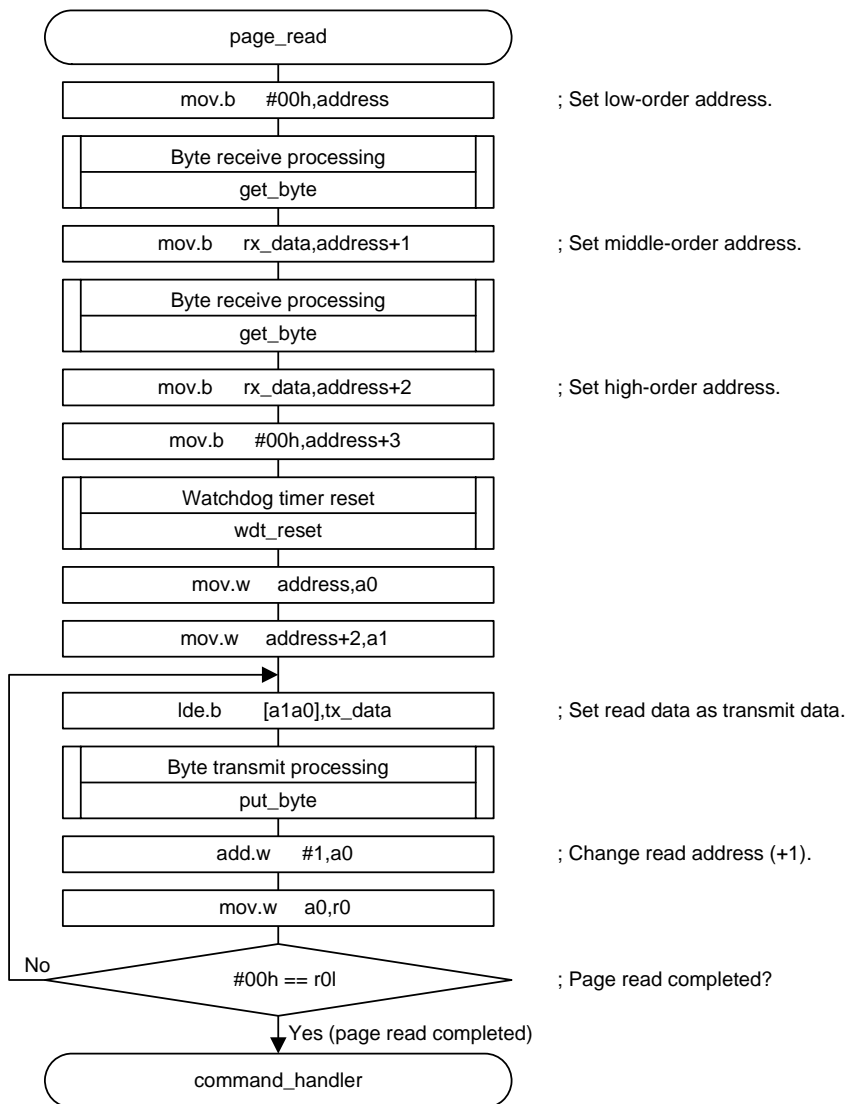
(3) Subroutine 1



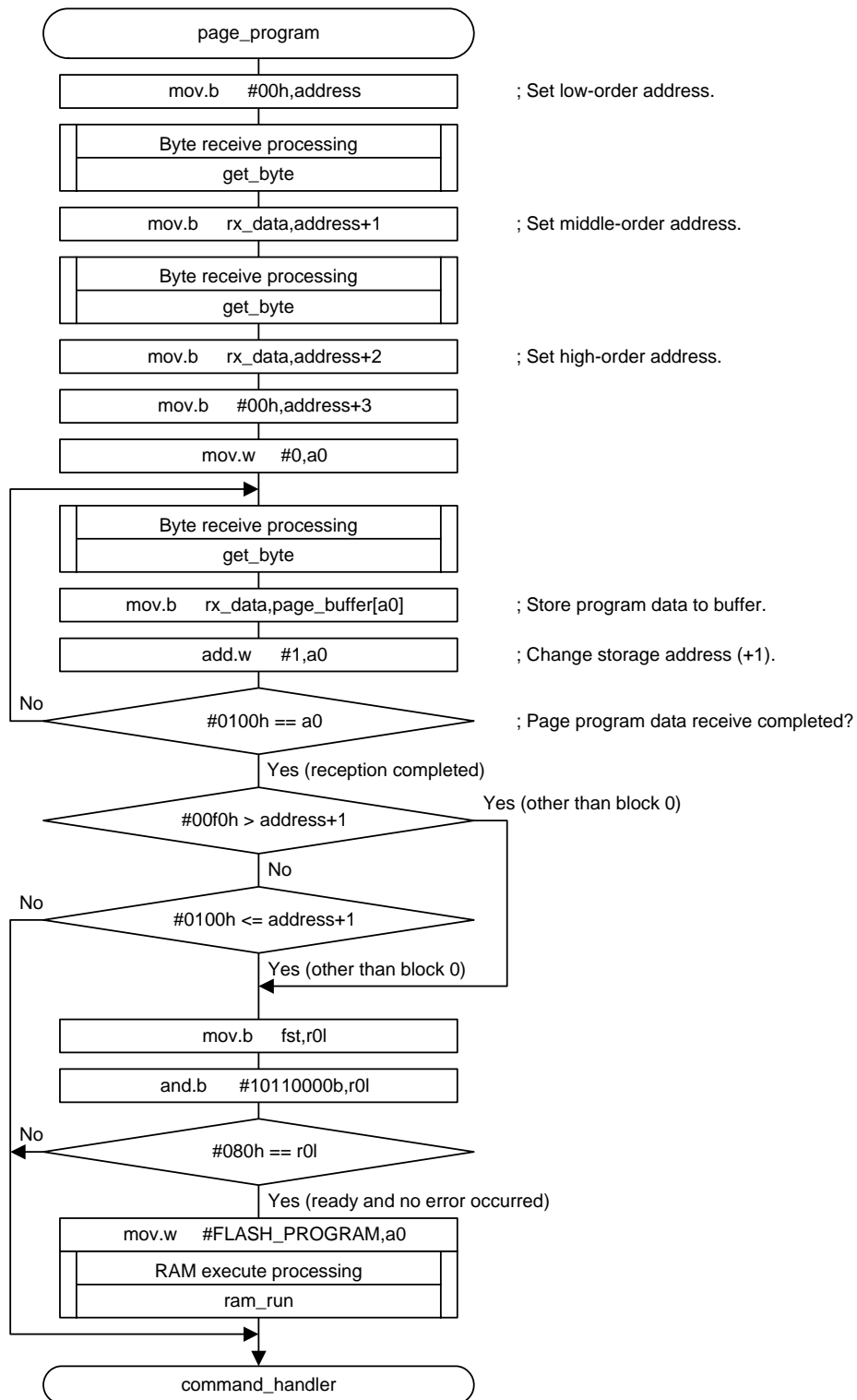
(4) Subroutine 2



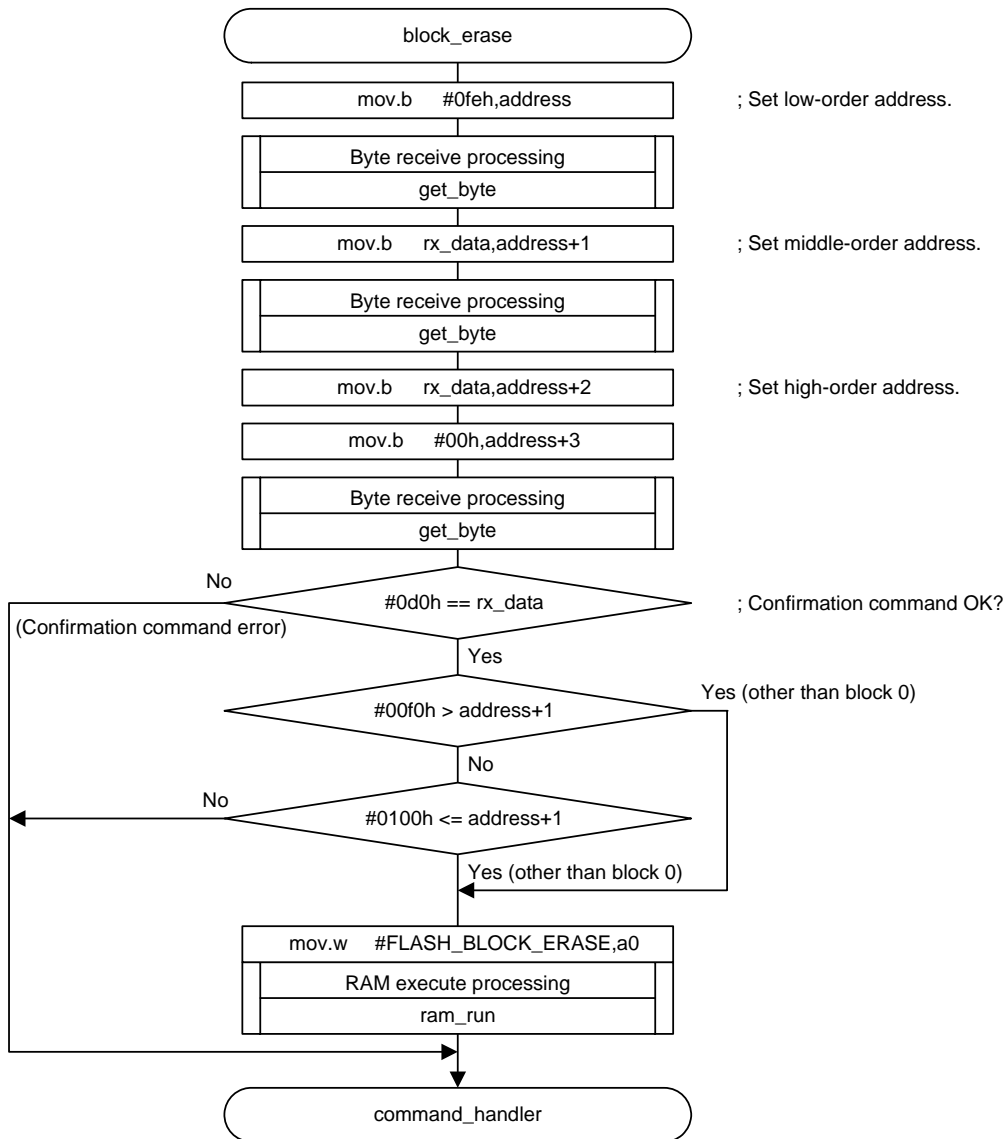
(5) Page read



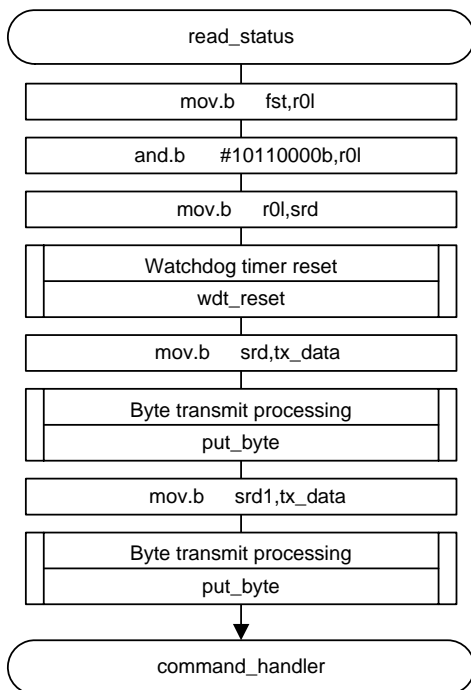
(6) Page program



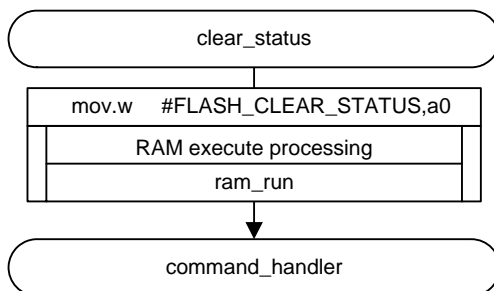
(7) Block erase



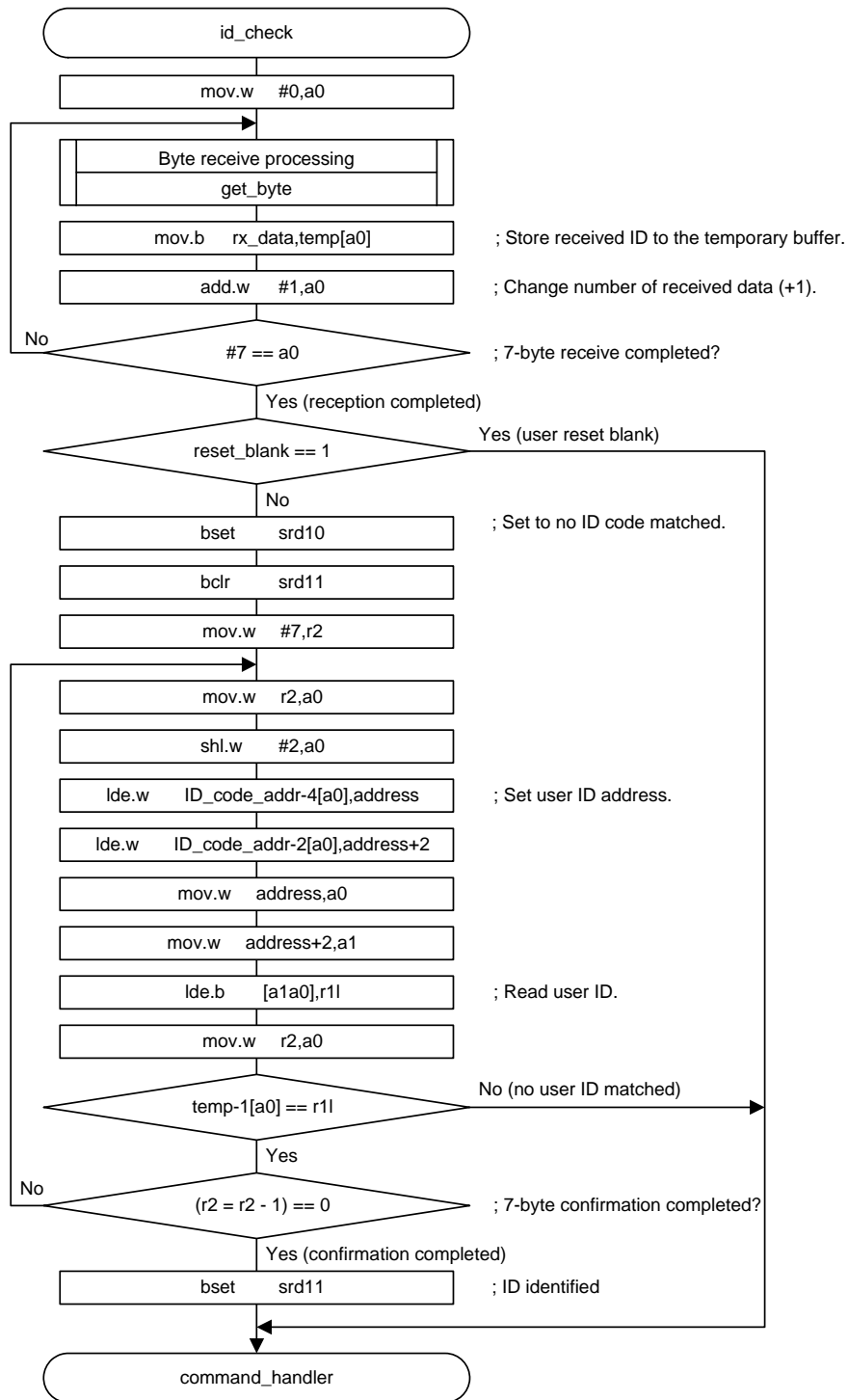
(8) Read status register



(9) Clear status register



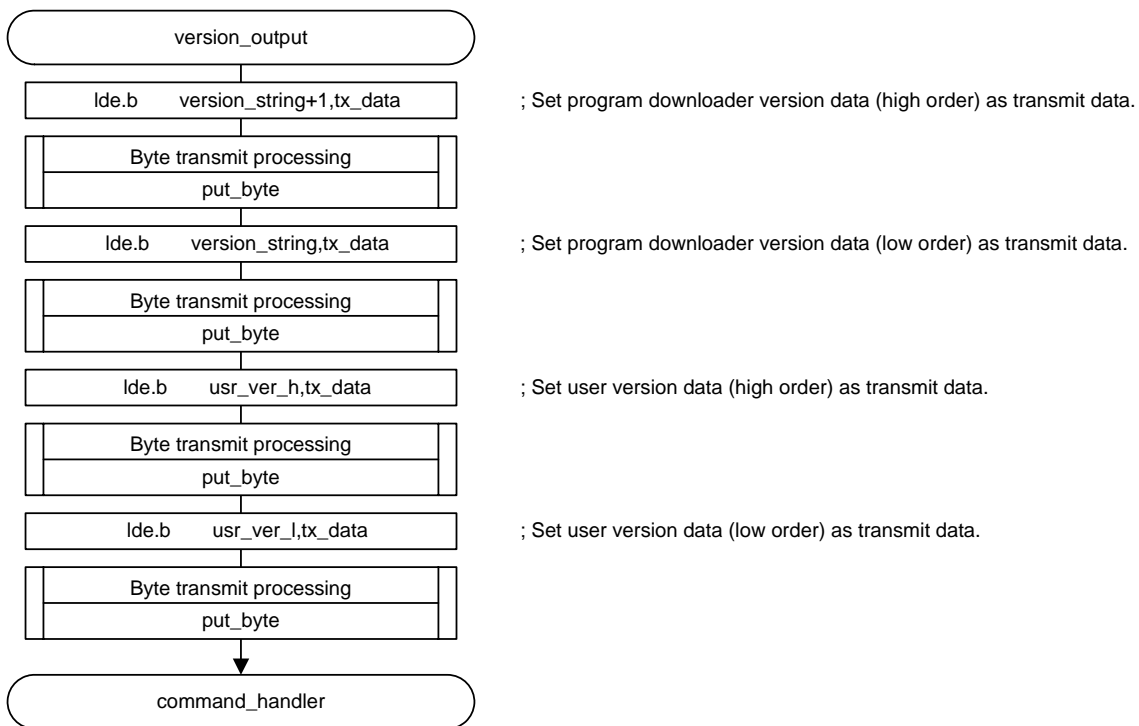
(10)ID check



```

ID_code_addr:
;
.word 0efd3h ; ID1
.word 0efe3h ; ID2
.word 0efebh ; ID3
.word 0efefh ; ID4
.word 0eff3h ; ID5
.word 0eff7h ; ID6
.word 0effbh ; ID7
  
```

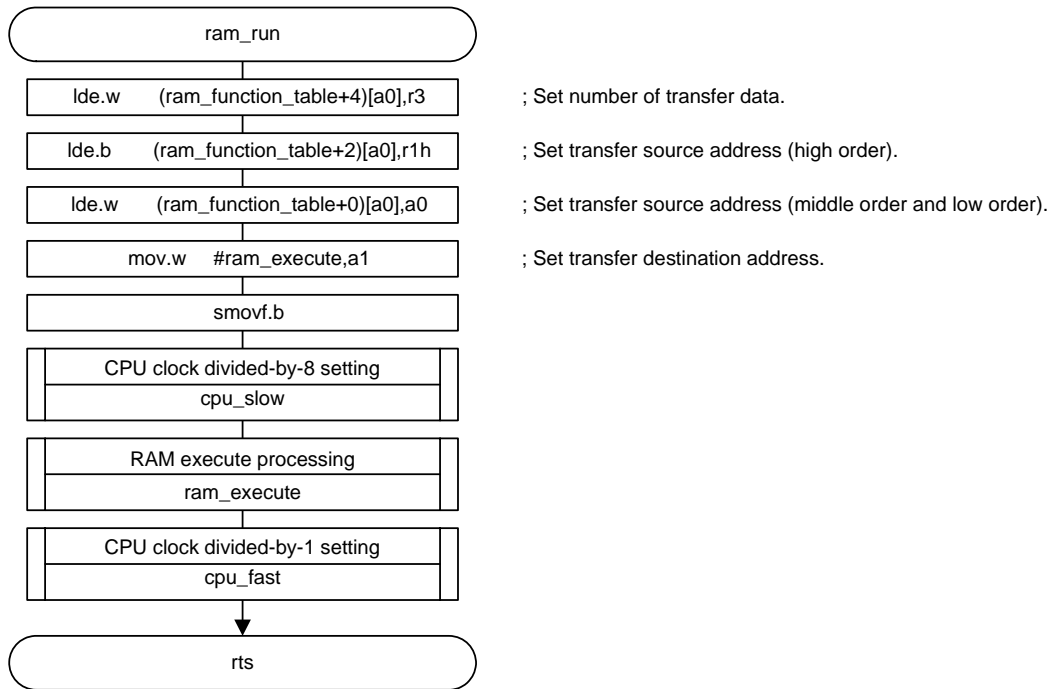
(11) Version output function



```

    .section version_area,ROMDATA
    .org    version_string
    .word 0100h
  
```

(12)RAM execute routine



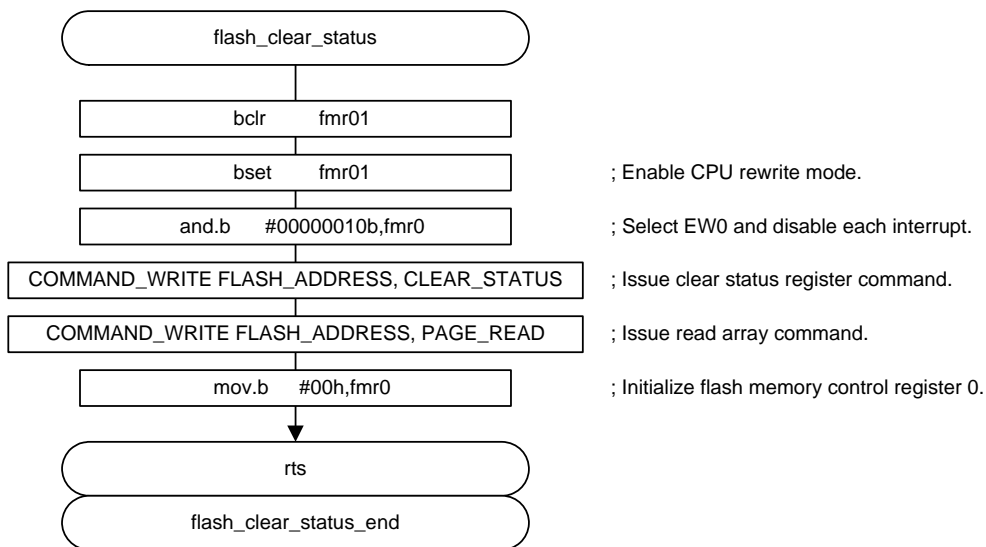
```

ram_function_table:
;
.word flash_clear_status
.word flash_clear_status_end - flash_clear_status

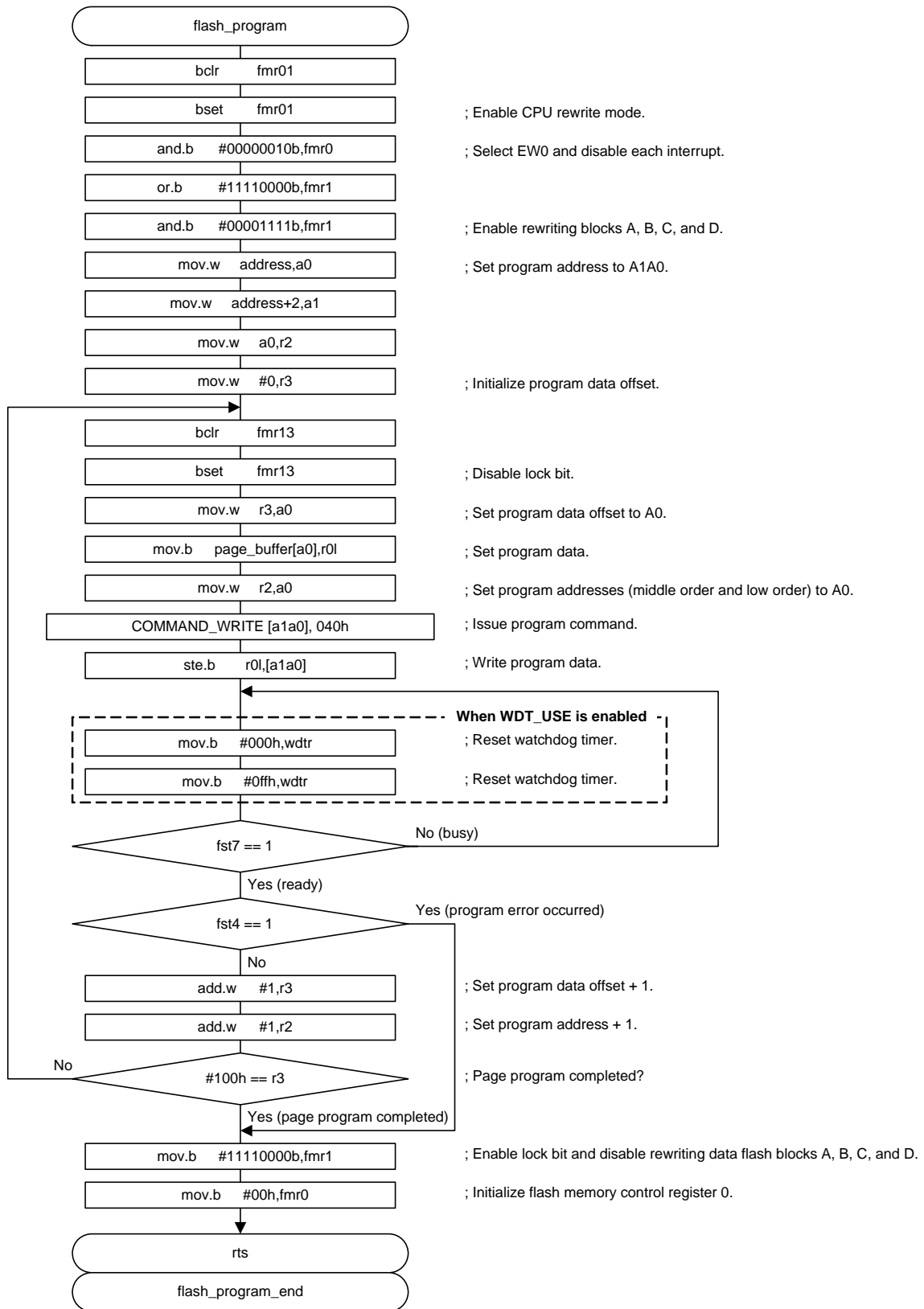
.word flash_program
.word flash_program_end - flash_program

.word flash_block_erase
.word flash_block_erase_end - flash_block_erase
    
```

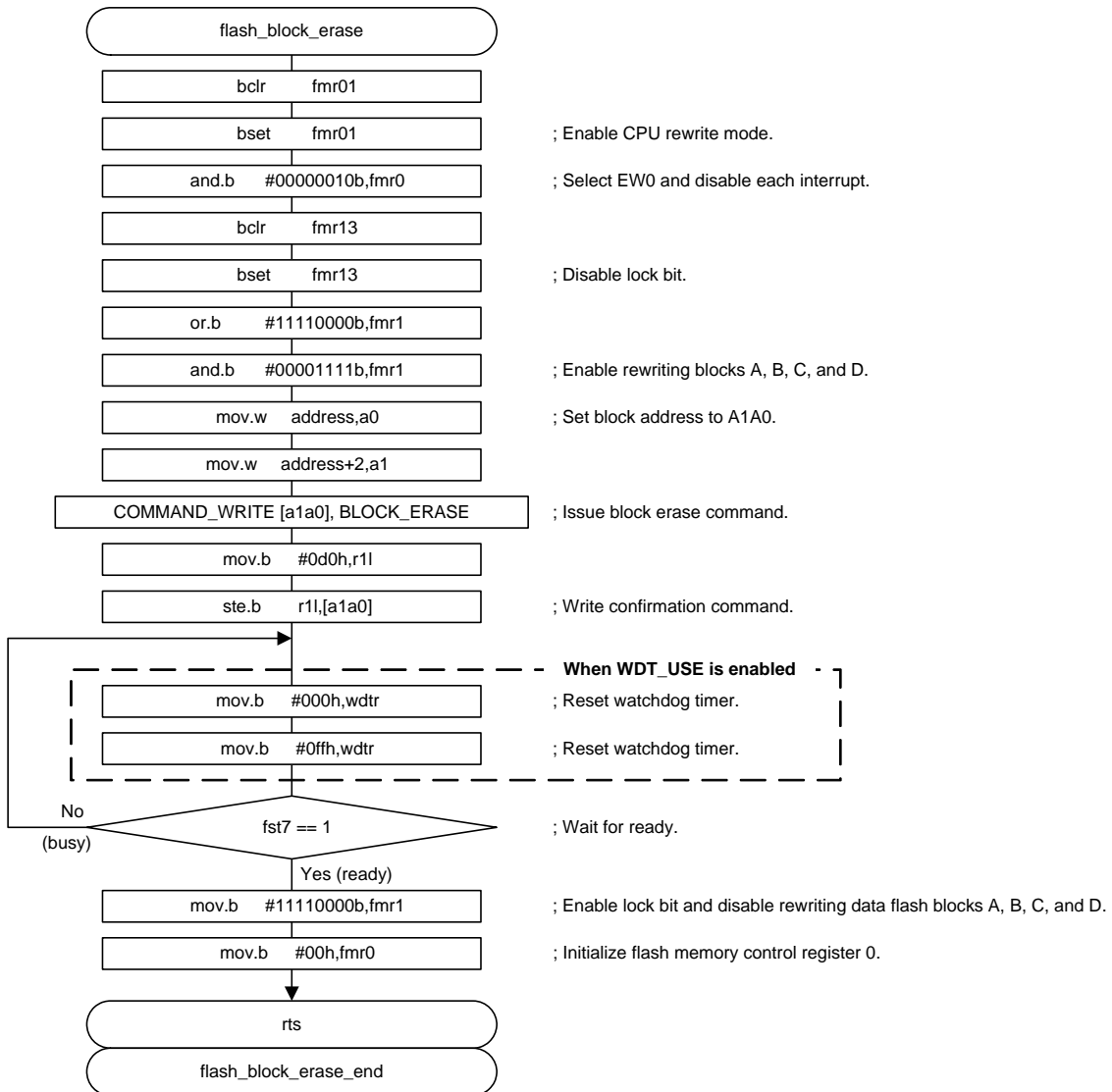
(13)Clear status register to flash memory (execute in RAM)



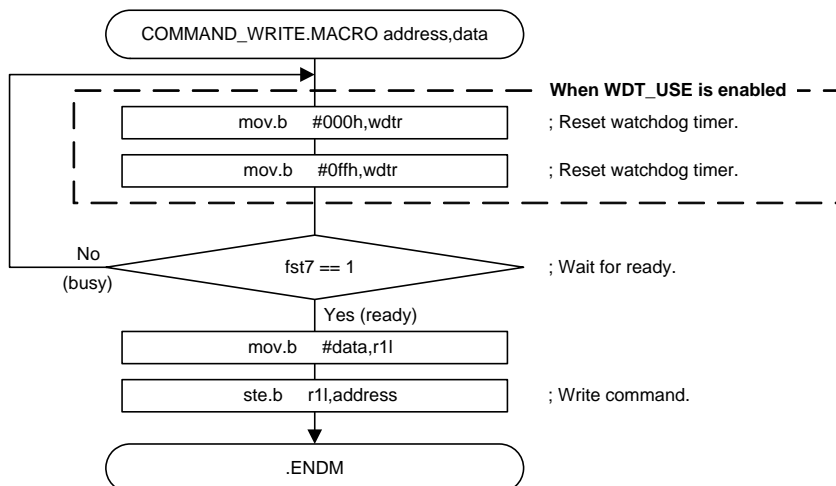
(14) Page program to flash memory (execute in RAM)



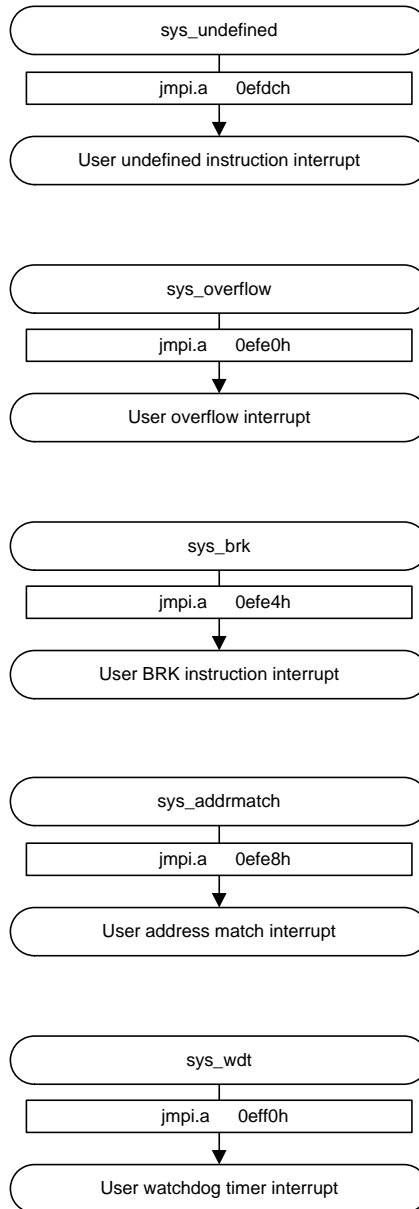
(15)Block erase to flash memory (execute in RAM)



(16)Command write macro



(17) System interrupt handling



4. Downloader Communication Protocol

4.1 Commands

4.1.1 Control Command List

Control commands are listed below.

Control Command	1 Byte	2 Bytes	3 Bytes	4 Bytes	5 Bytes	6 Bytes	7 Bytes or More	ID Unchecked
Page read	FFH	Middle-order address	High-order address	Data	Data	Data	Up to data	Not acceptable
Page program	41H	Middle-order address	High-order address	Data	Data	Data	Up to data	Not acceptable
Block erase	20H	Middle-order address	High-order address	D0H				Not acceptable
Read status register	70H	SRD	SRD1					Acceptable
Clear status register	50H							Not acceptable
ID check function	F5H	ID1	ID2	ID3	ID4	ID5	Up to ID7	Acceptable
Version information output function	FBH	Program downloader version		User version				Acceptable

SRD: Status register data

SRD1: Status register data 1

Notes:

1. The shadowed areas show a transfer from the MCU (program downloader) to a programmer, the rest show a transfer from a programmer to the MCU (program downloader).
2. User program area blank product IDs are identified and all commands can be accepted.
3. The number of receive data is not checked and the timeout error is not processed in the downloader. When transmitting a command, make sure there is no excess or shortage of data.

4.2 Page Read

4.2.1 Operation

The page read command reads the specified user ROM area in the flash memory in units of 256 bytes. Specify the area to be read by the high-order addresses (A16 to A23) and middle-order addresses (A8 to A15). The target bytes are the 256 bytes from addresses xxxx00h to xxxxFFh.

4.2.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command	Address		Data	Up to data
Programmer to MCU	FFh	Middle-order address	High-order address		
MCU to Programmer				Data 0	Up to Data 255

Data 0: Low-order address is 00h

Data 255: Low-order address is FFh

4.2.3 Procedure

- (1) The page read command FFh is received at the first byte.
- (2) The middle-order address is received at the second byte and the high-order address is received at the third byte.
- (3) The content in the low-order address 00h is sequentially transmitted from the fourth byte.

4.3 Page Program

4.3.1 Operation

The page program command programs the data to the specified user ROM area in the flash memory in units of 256 bytes. Specify the area to be programmed by the high-order addresses (A16 to A23) and middle-order addresses (A8 to A15). The target bytes are the 256 bytes from addresses xxxx00h to xxxxFFh.

4.3.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command	Address		Data	Up to data
Programmer to MCU	41h	Middle-order address	High-order address	Data 0	Up to Data 255
MCU to Programmer					

Data 0: Low-order address is 00h

Data 255: Low-order address is FFh

4.3.3 Procedure

- (1) The page program command 41h is received at the first byte.
- (2) The middle-order address is received at the second byte and the high-order address is received at the third byte.
- (3) The programming data to the low-order address 00h is received from the fourth byte.

When the programming data is less than 256 bytes, transmit FFh for the shortage. When programming data is more than 257 bytes, the data at the 257th byte is considered to be the data in the next command. If an error occurs during programming, SR4 becomes 1 (program status ends in error).

After executing this command, confirm the status of the flash memory with the read status register command.

4.4 Block Erase

4.4.1 Operation

The block erase command erases a specified block area in the user ROM area of the flash memory. Specify a block area by the eight high-order bits (A16 to A23) and eight middle-order bits (A8 to A15) at a given address of the block to be erased.

4.4.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command	Block address		Confirmation command	
Programmer to MCU	20h	Middle-order address	High-order address	D0h	
MCU to Programmer					

4.4.3 Procedure

- (1) The block erase command 20h is received at the first byte.
- (2) The middle-order address is received at the second byte and the high-order address is received at the third byte.
- (3) The confirmation command D0h is received at the fourth byte.

After receiving the confirmation command D0h, erasing to the specified block starts. The erase operation sets the contents of the flash memory to FFh. If an error occurs, SR5 becomes 1 (erase status ends in error).

After executing this command, confirm the status of the flash memory with the read status register command.

4.5 Read Status Register

4.5.1 Operation

The read status register command confirms the operating status of the flash memory.

4.5.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command	SRD			
Programmer to MCU	70h				
MCU to Programmer		SRD output	SRD1 output		

SRD: Status register data

SRD1: Status register data 1

4.5.3 Procedure

- (1) The read status register command 70h is received at the first byte.
- (2) SRD is transmitted at the second byte.
- (3) SRD1 is transmitted at the third byte.

4.5.4 SRD Register

Each Bit of SRD	Status Name	Definition	
		1	0
SR7 (bit 7)	Sequencer status	Ready	Busy
SR6 (bit 6)	Reserved		
SR5 (bit 5)	Erase status	Error	Completed normally
SR4 (bit 4)	Program status	Error	Completed normally
SR3 (bit 3)	Reserved		
SR2 (bit 2)	Reserved		
SR1 (bit 1)	Reserved		
SR0 (bit 0)	Reserved		

(1) Sequencer status

The sequencer status shows the operating status of the flash memory. This bit becomes 0 (busy) during auto-programming or auto-erasing. This bit becomes 1 (ready) during auto-programming or auto-erasing.

(2) Erase status

The erase status shows the erase operating status. If an error occurs, this bit becomes 1. This bit is set to 0 when the clear status register command is executed.

(3) Program status

The program status shows the programming status. If an error occurs, this bit becomes 1. This bit is set to 0 when the clear status register command is executed.

Both SR5 and SR4 become 1 in the following cases:

- The defined command is not written correctly.
- Data other than values which can be written to the second bus cycle data of the block erase command (D0h or FFh) is written in the cycle to input the block erase confirmation command. When FFh is written, the MCU enters read array mode and the command is canceled.

(4) Reserved bit

When read, the content is undefined.

4.5.5 SRD1 Register

Each Bit of SRD1	Status Name	Definition	
		1	0
SR15 (bit 7)		Reserved	
SR14 (bit 6)		Reserved	
SR13 (bit 5)		Reserved	
SR12 (bit 4)		Reserved	
SR11 (bit 3)	ID check	00: Not checked	
SR10 (bit 2)		01: ID Not matched	
		10: Reserved	
		11: Checked	
SR9 (bit 1)		Reserved	
SR8 (bit 0)		Reserved	

(1) ID check

These bits indicate the ID check results.

(2) Reserved bit

When read, the content is undefined.

4.6 Clear Status Register

4.6.1 Operation

The clear status register command initializes a status register. Initialize the status register before executing the erase or the page program to the flash memory.

4.6.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command				
Programmer to MCU	50h				
MCU to Programmer					

4.6.3 Procedure

- (1) The clear status register command 50h is received at the first byte.

4.7 ID Check Function

4.7.1 Operation

This function compares the ID received from the programmer and the user ID code stored in the virtual fixed vector address. The ID check results are stored in SR11 to SR10 in the SRD1 register.

4.7.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 8th Byte
	Command	ID			
Programmer to MCU	F5h	ID1	ID2	ID3	Up to ID7
MCU to Programmer					

4.7.3 Procedure

- (1) The ID check function command F5h is received at the first byte.
- (2) ID1 to ID7 are received from the second byte to the eighth byte, respectively.

After receiving the ID, the ID check starts. However, a user program area blank product returns the wait state for the control command from the programmer without performing ID check. When ID1 to ID7 all match, SR11 to SR10 become 11b (verified). If any of the IDs do not match, SR11 to SR10 become 01b (verify not matched).

4.8 Version Information Output Function

4.8.1 Operation

This function transmits version information of the program downloader and user program.

4.8.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	Up to 259th Byte
	Command	Version				
Programmer to MCU	FBh					
MCU to Programmer		Program downloader		User		

4.8.3 Procedure

- (1) The version information output function command FBh is received at the first byte.
- (2) The program downloader version is transmitted at the high-order second byte first and then the low-order third byte.
- (3) The user program version is transmitted at the high-order fourth byte first and then low-order fifth byte.

4.8.4 Version Data

For the example shown below, the program download version is transmitted after 01h is set to the high order and 00h to the low order of the program downloader version, and 00h is set to the high order and 10h to the low order of the user version.

When the program downloader version is Ver.1.00 and the user version is Ver.0.10:

Program downloader version data
(in the bt_r835c.a30 file)

```
.org      version_string
.word     0100h          ; Program Downloader version (Ver.1.00)
```

User version data
(in the sect30.inc file for 5. User Program Example)

```
User_Ver .equ      0010h    ; User version (Ver.0.10)
```

5. User Program Example

The program downloader rewrites the user programs other than the user program in block 0 according to the programmer. An example of the user program is shown below.

5.1 Function

The LEDs connected to I/O ports P3_1, P3_3, P3_4, and P3_6 light.

5.2 Memory Map

Figure 5.1 shows a User Program Memory Map.

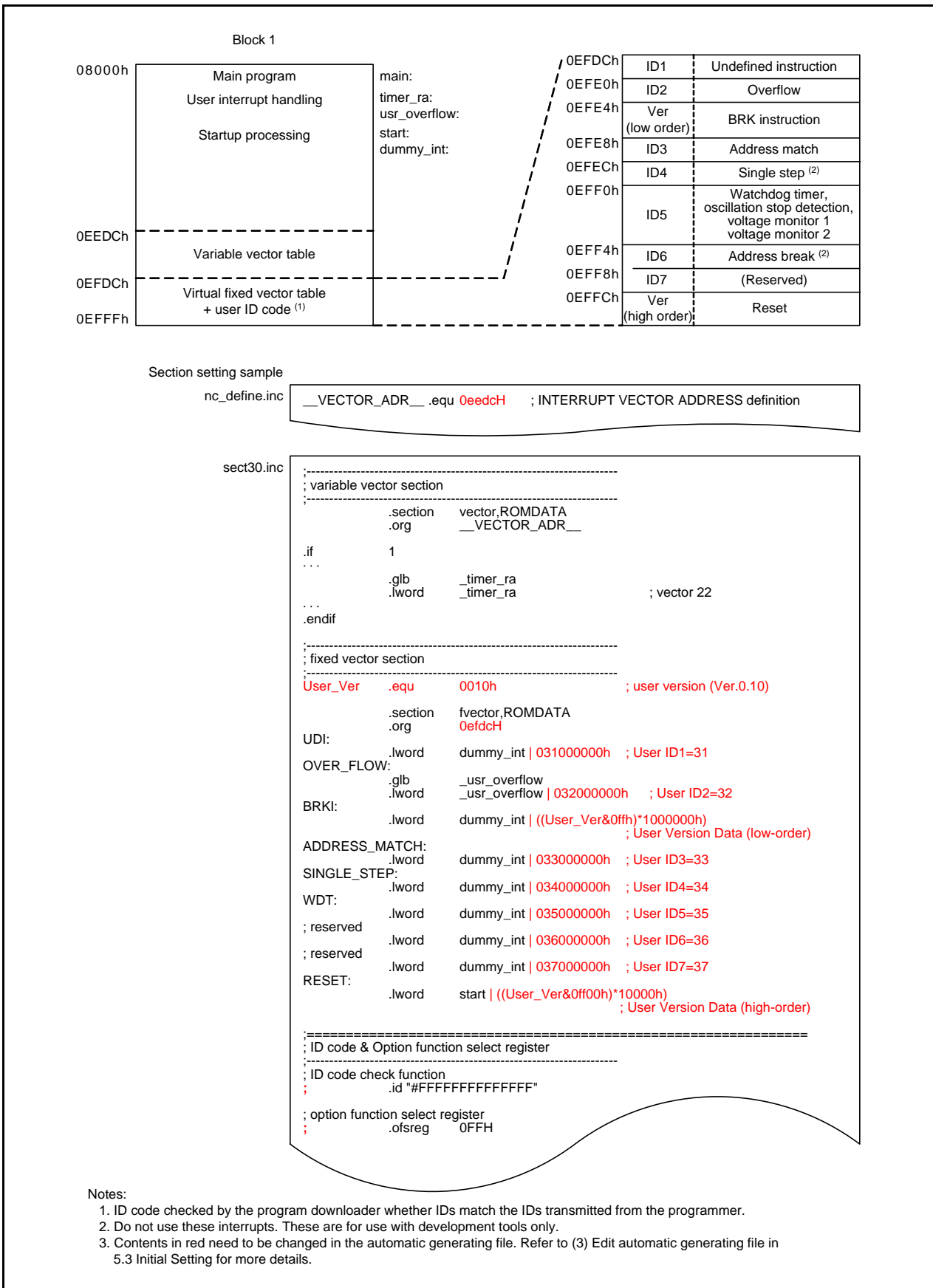


Figure 5.1 User Program Memory Map

5.3 Initial Settings

(1) Vector table

Allocate the virtual fixed vector table to block 1 to use an interrupt by the user program.

(2) ID code

Set an ID code in the virtual fixed vector table. Do not opt to generate an ID code file when compiling.

(3) Edit automatic generating file

When the project type is made in the Application and the initial setting file is automatically generated by the High-performance Embedded Workshop (HEW), change the sect30.inc file and nc_define.inc file as follows (see Figure 5.1):

- Change the allocation address of the locatable table to 0EEDCh, and the virtual fixed vector table to 0EFDCh.
- Set an additional ID code to the virtual fixed vector table.
- Add the symbol definition of the user version data and user version data setting to the virtual fixed vector table.
- Comment out the assembler expansion function direction instructions “.ID” (set an ID code) and “.OFSREG” (set a value to the OFS register).

6. Programmer Example

6.1 Control Pins

- (1) Pins TXD and RXD

These pins are for transmitting and receiving in UART mode.

- (2) $\overline{\text{RESET}}$ pin

This pin controls an MCU reset from the programmer.

- (3) Pins VCC and VSS

Adjust high level from the programmer to the MCU's VCC level and low level from the programmer to the MCU's VSS level, respectively.

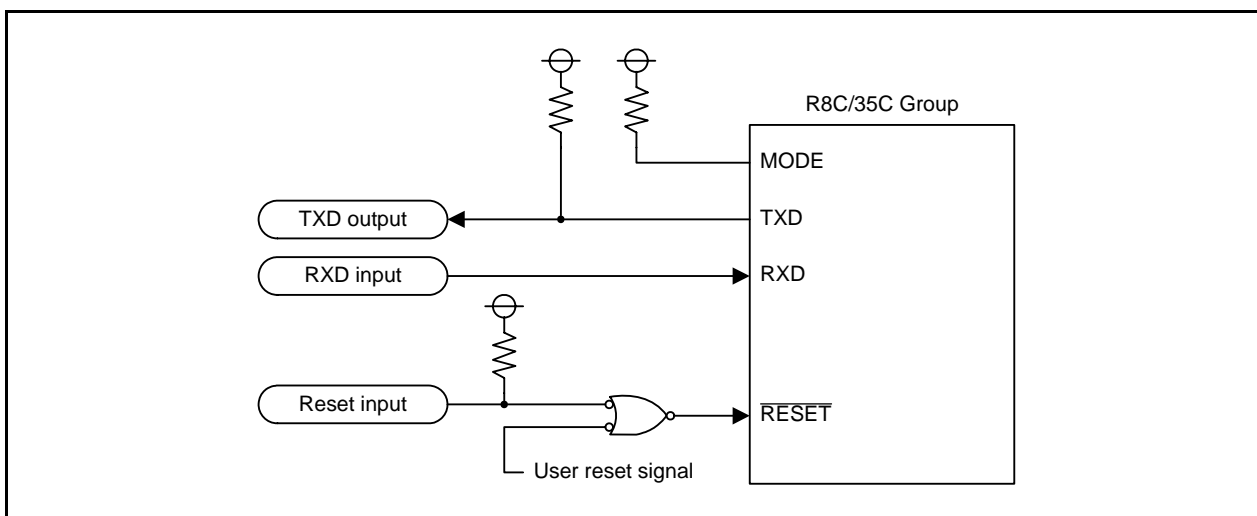


Figure 6.1 Programmer Configuration

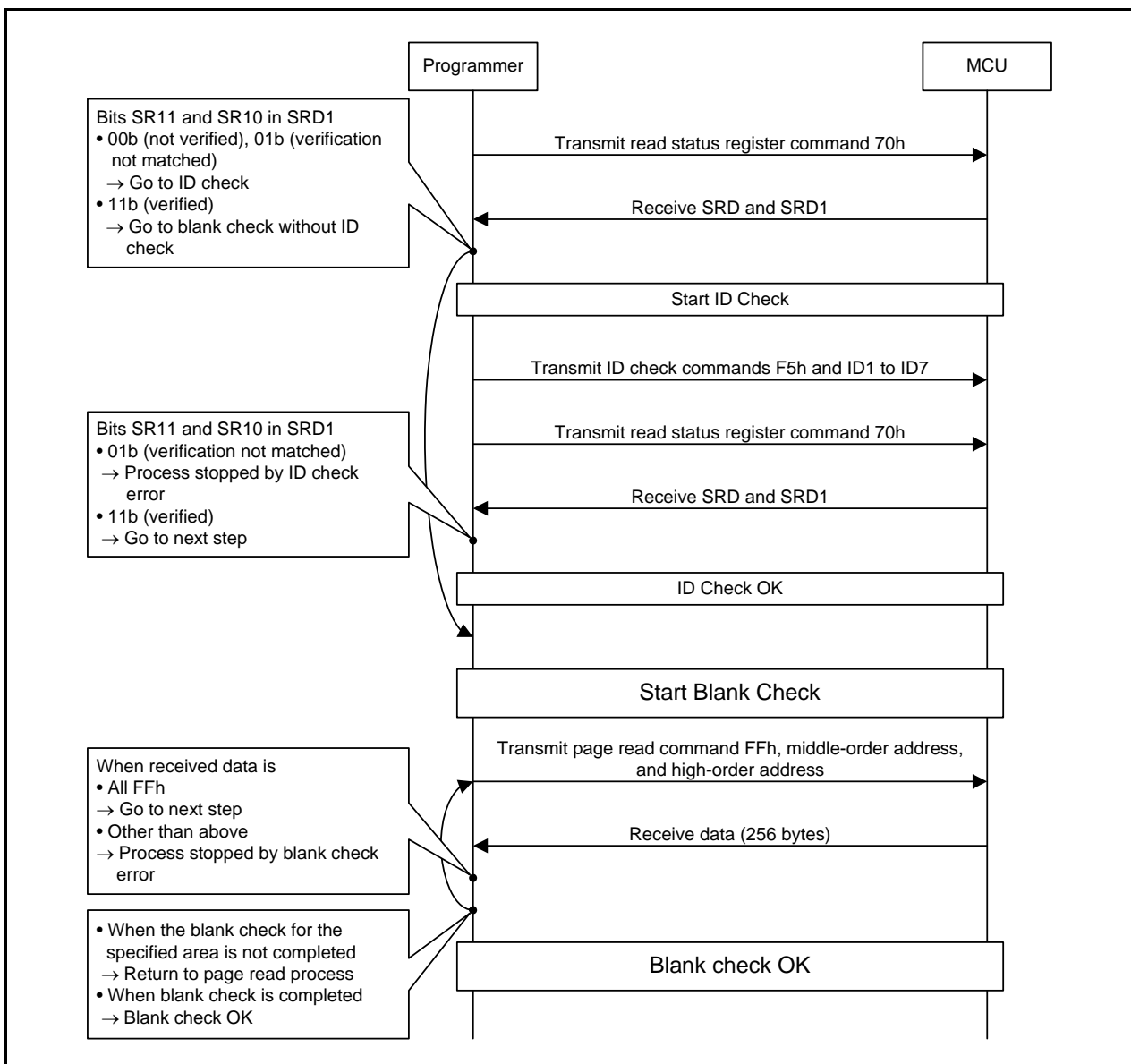
6.2 Programmer Functions

The following are the functions necessary for the programmer:

- Blank Check
- Erase
- Program
- Verify
- Read

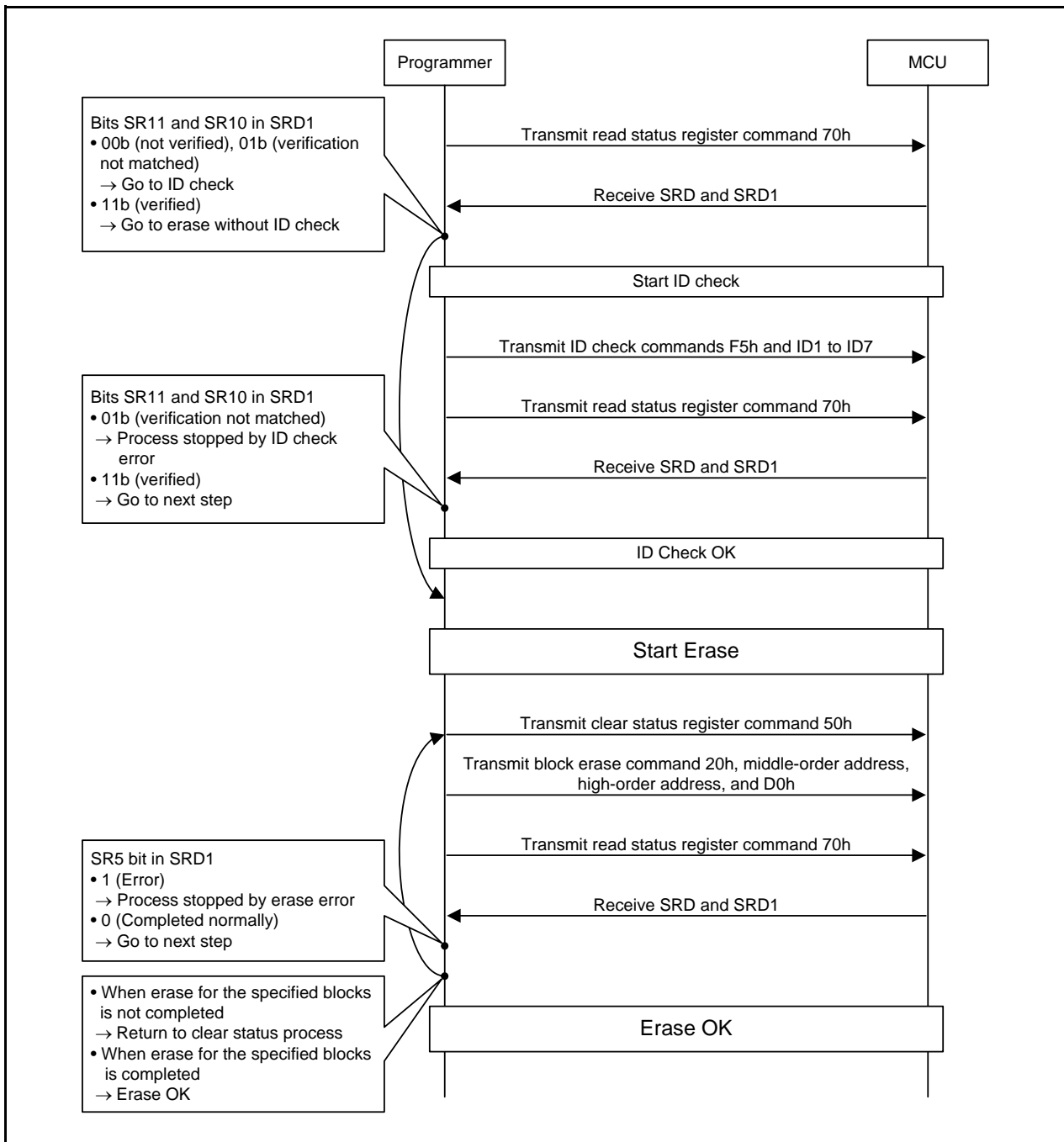
6.3 Blank Check

Data (program) in the specified area automatically or manually is read from the MCU's on-chip flash memory. The programmer confirms that all read data is blank (FFh).



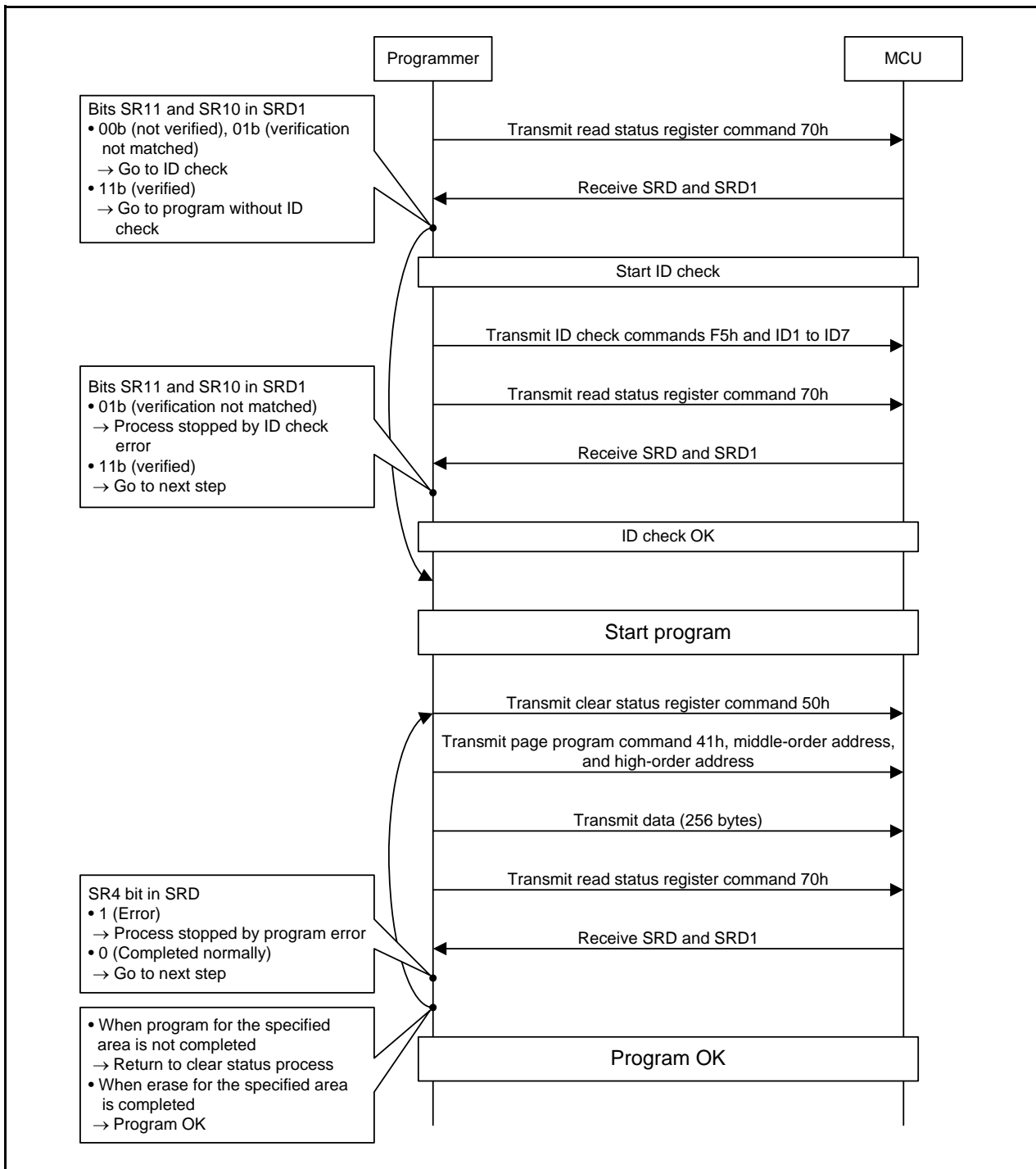
6.4 Erase

Data (program) in the MCU's specified on-chip flash memory blocks automatically or manually is erased.



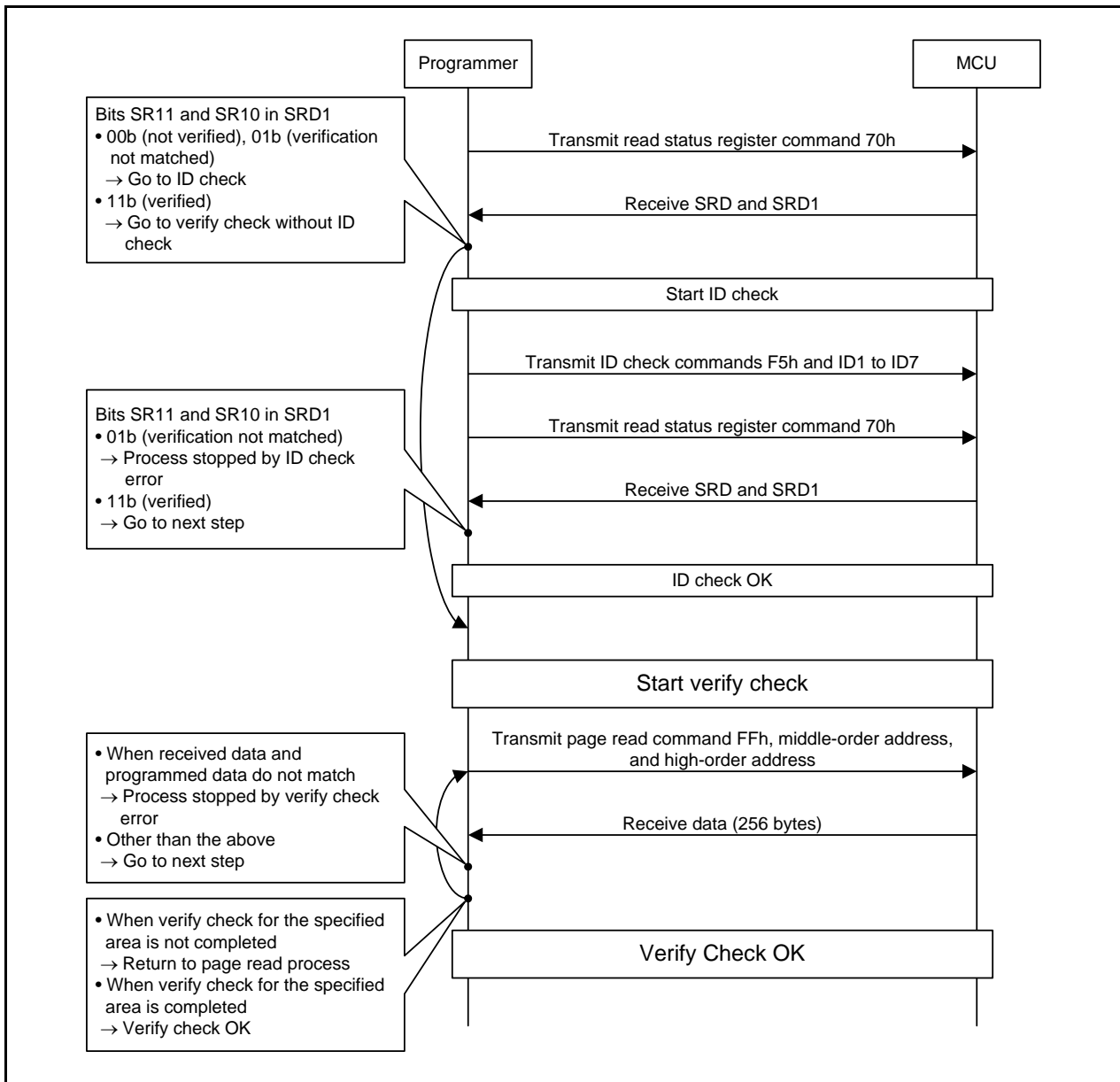
6.5 Program

Data (program) in the MCU's specified on-chip flash memory area automatically or manually is programmed.



6.6 Verify

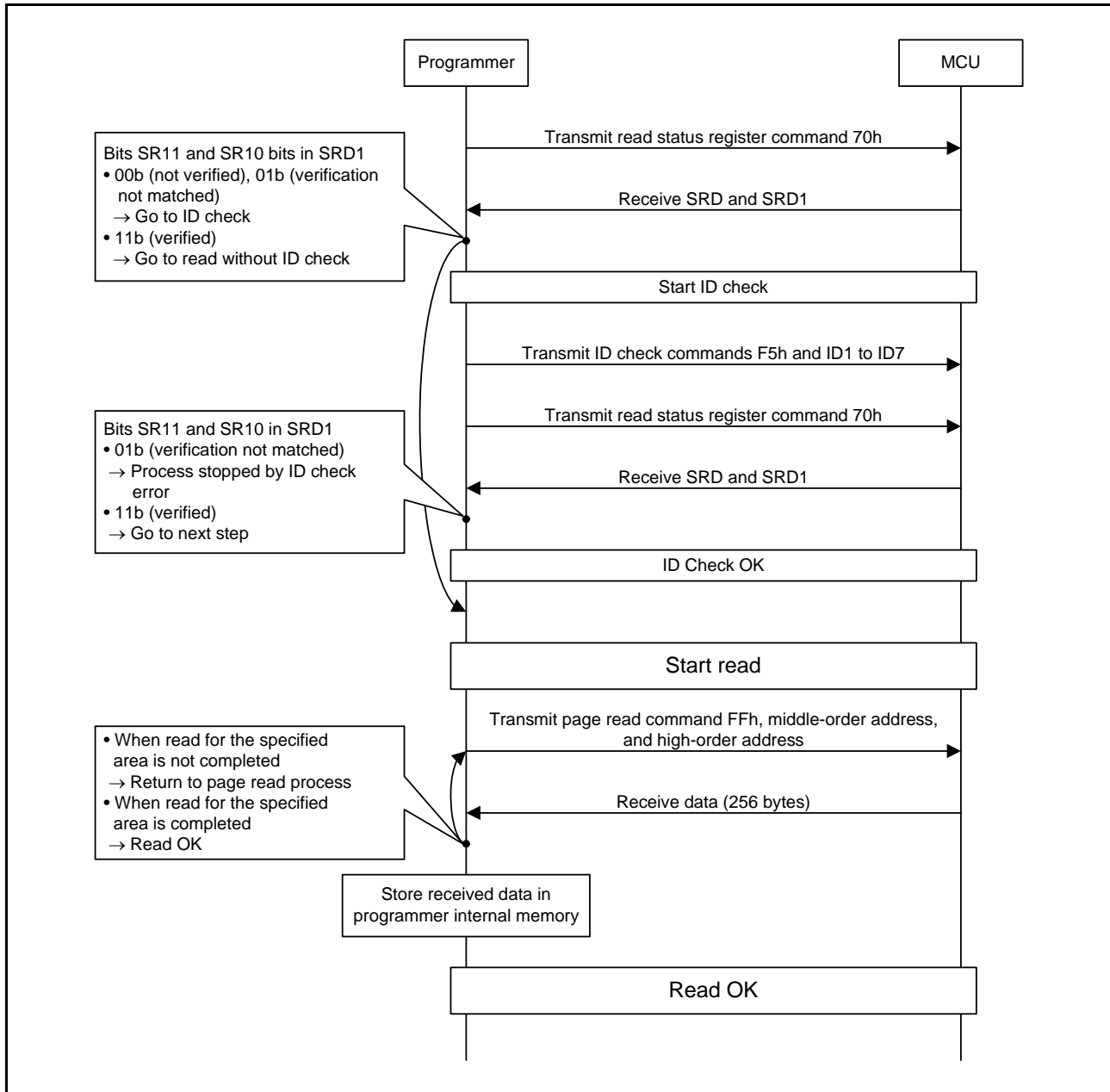
Data (program) in the specified area automatically or manually is read from the MCU's on-chip flash memory. The programmer compares the read data with the memory data (program) in the programmer to confirm that they match.



6.7 Read

This function allows reading the data (program) in the automatically or manually specified area from the MCU with on-chip flash memory.

The programmer stores the read data in its internal memory



7. Sample Programming Code

A sample program can be downloaded from the Renesas Electronics website.

To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

8. Reference Documents

R8C/35C Group User’s Manual: HardwareRev.1.00

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website

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Revision History	R8C/35C Group UART Version Program Downloader
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Rev.	Date	Description	
		Page	Summary
1.00	Apr 30, 2010	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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