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R8C/35C Group

Serial I/O Operation in Clock Synchronous Serial I/O Mode with DTC

1. Abstract

This document describes the setting method and an application example for the serial interface (clock synchronous serial I/O mode) and DTC (normal mode).

2. Introduction

The application example described in this document applies to the following MCU:

- MCU : R8C/35C Group

The sample program in this application note can be used with other R8C/35C Group MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

3.1 Program Outline

3.1.1 Serial Interface

In clock synchronous serial I/O mode, 1-byte data is transmitted/received consecutively for 8 bytes.

Table 3.1 shows the communication method and Figure 3.1 shows the communication format.

Table 3.1 Communication Method

Channel	UART0
Communication mode	Clock synchronous serial I/O mode
Transfer clock frequency	9600 Hz (104 µs period)
Internal/external clock	Internal clock
TXD0 pin data output	CMOS output
CLK polarity	Transmit data is output at the falling edge and receive data input at the rising edge of the transfer clock.
Transfer format	MSB first
UART0 transmit interrupt source	Transmission completed (TXEPT = 1)
UART0 continuous receive mode	Disabled

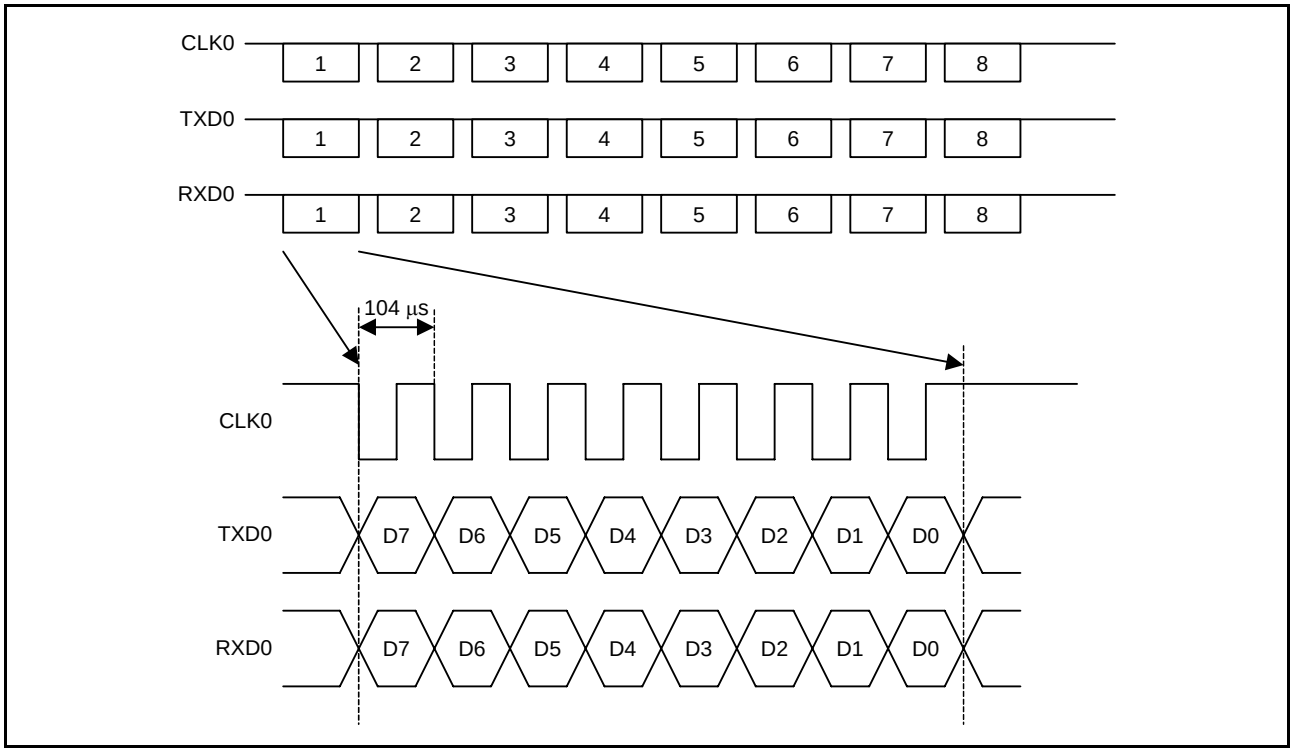


Figure 3.1 Communication Format

3.1.2 DTC Activation by UART0 Transmit Interrupt

Transmission of the first byte of the transmit data is triggered when the data is written to lower byte of the U0TB register. As a UART0 transmit interrupt is generated by this data transmission, DTC is activated and transfers the contents of the transmit data array (address where variables “uart0_tx_data[1]” to “uart0_tx_data[7]” are allocated) to the UART0 transmit register buffer (lower byte of the U0TB register (address 00A2h)).

Table 3.2 shows the settings for DTC triggered by UART0 transmit interrupt and Figure 3.2 shows the DTC activation by UART0 transmit interrupt.

Table 3.2 Settings for DTC (Triggered by UART0 Transmit Interrupt)

DTC activation source	UART0 transmit interrupt
Control data	Control data 0 (addresses 2C40h to 2C47h)
Transfer mode	Normal mode
Source address control	Incremented
Destination address control	Fixed
Chain transfer	Disabled
Size of the data block to be transferred by one activation	1 byte
Number of times of DTC data transfers	7 times
Transfer source address for data transfer	Address where variable “uart0_tx_data[1]” is allocated
Transfer destination address for data transfer	Address 00A2h (address of the lower byte of the U0TB register)

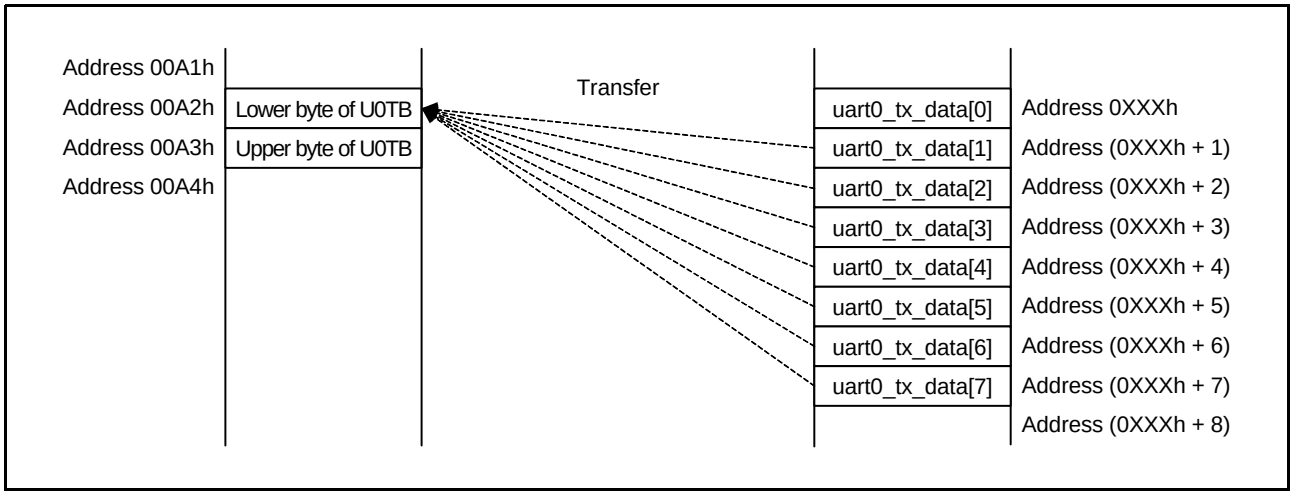


Figure 3.2 DTC Activation by UART0 Transmit Interrupt

3.1.3 DTC Activation by UART0 Receive Interrupt

DTC is activated by a UART0 receive interrupt and transfers the contents of the receive data array (address where variables “uart0_rx_data[0]” to “uart0_rx_data[7]” are allocated) to the UART0 receive register buffer (U0RB register (addresses 00A7h to 00A6h)).

Table 3.3 shows the settings for DTC triggered by the UART0 receive interrupt and Figure 3.3 shows the DTC activation by UART0 receive interrupt.

Table 3.3 Settings for DTC (Triggered by UART0 Receive Interrupt)

DTC activation source	UART0 receive interrupt
Control data	Control data 1 (addresses 2C48h to 2C4Fh)
Transfer mode	Normal mode
Source address control	Fixed
Destination address control	Incremented
Chain transfer	Disabled
Size of the data block to be transferred by one activation	2 bytes
Number of times of DTC data transfers	8 times
Transfer source address for data transfer	Address 00A6h (address of the lower byte of the U0RB register)
Transfer destination address for data transfer	Address where variable “uart0_rx_data[1]” is allocated

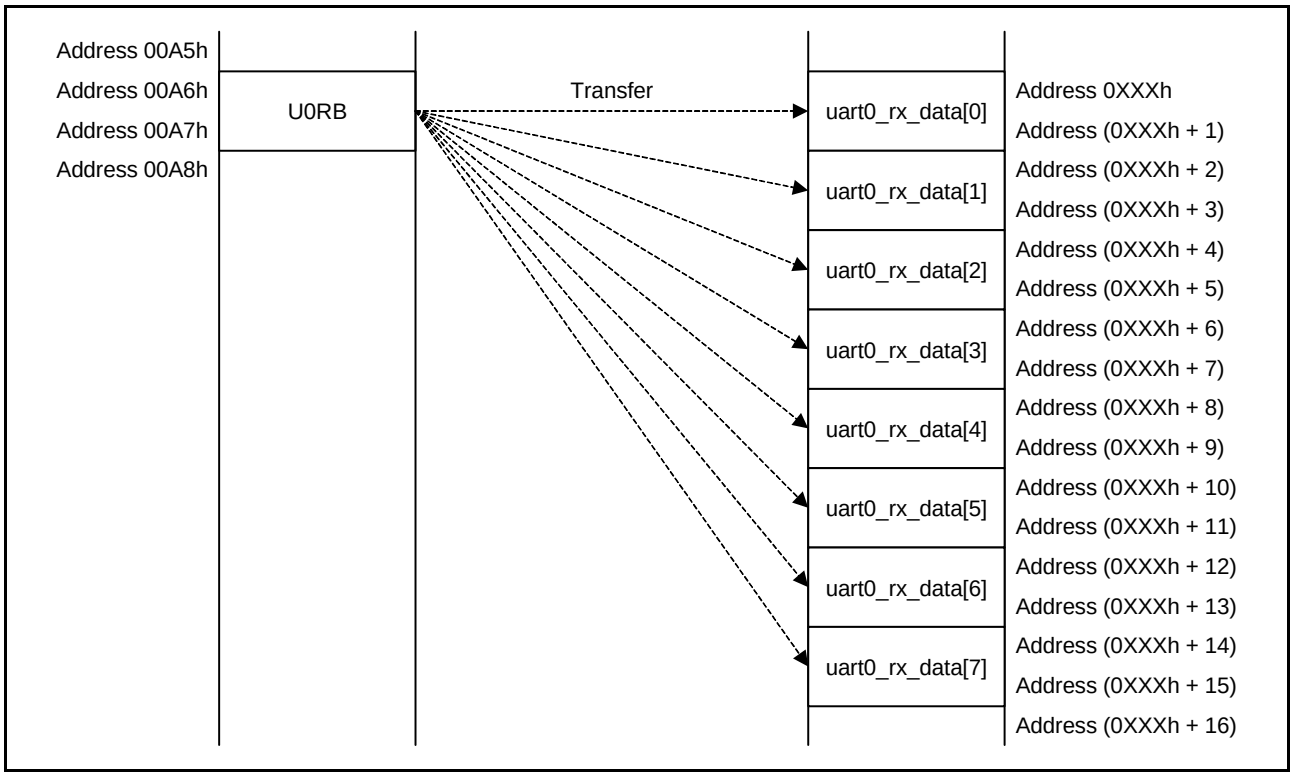


Figure 3.3 DTC Activation by UART0 Receive Interrupt

3.2 Pins and Memory

3.2.1 Pins

Table 3.4 Pins and Their Functions

Pin	I/O	Function
P1_4(/TXD0/TRCCLK)	Output	Serial data output
P1_5(/INT1/RXD0/TRAIO)	Input	Serial data input
P1_6/LVCOUT2/IVREF1(/CLK0)	Output	Transfer clock output

3.2.2 Memory

Table 3.5 Memory

Memory	Size	Remarks
ROM	319 bytes	In the rej05b1336_src.c module
RAM	32 bytes	In the rej05b1336_src.c module
Maximum user stack	9 bytes	
Maximum interrupt stack	19 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies under the following conditions:
C compiler: M16C/60, 30, 20, 10, and Tiny, and R8C/Tiny Series Compiler V.5.45 Release 00
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/35C Group Hardware Manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The system clock (high-speed on-chip oscillator) is set.		

Declaration	void uart_enable(void)		
Outline	Serial interface setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The serial interface (clock synchronous serial I/O mode) is set.		

Declaration	void dtc_enable(void)		
Outline	DTC setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Content
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	DTC (normal mode) is set.		

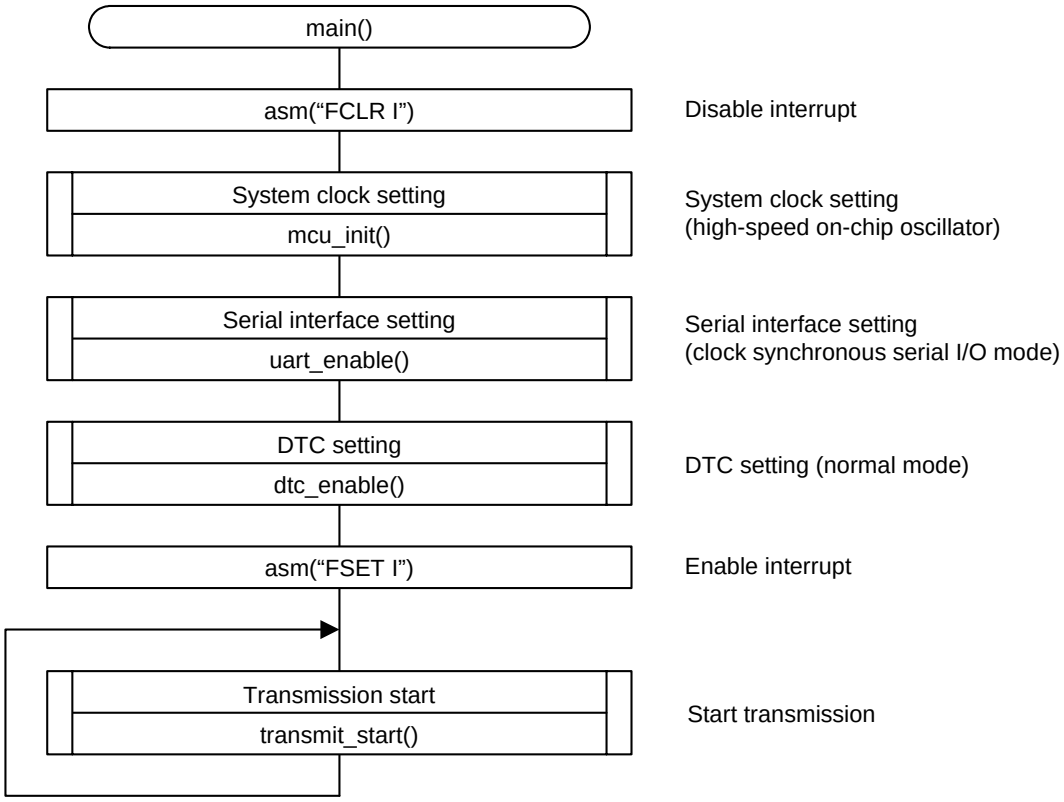
Declaration	void transmit_start(void)		
Outline	Transmission start		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char uart0_tx_data[TX_RX_DATA_SIZE]		Array of transmit data
Returned value	Type	Value	Meaning
	None	—	—
Function	Transmission is started.		

Declaration	void transmit_data_set(void)		
Outline	Transmit data setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Transmit data is created. This application note does not include any processes. Add a process if necessary.		

Declaration	void _uart0_receive(void)		
Outline	UART0 receive interrupt		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned short uart0_rx_data[TX_RX_DATA_SIZE]		Variable which is assigned as DTC data transfer destination address
	unsigned char set_rx_data[TX_RX_DATA_SIZE]		Array of receive data
Returned value	Type	Value	Meaning
	None	—	—
Function	UART0 receive interrupt. (This interrupt is generated after DTC transfer is completed.) The receive data transferred by DTC is set to the receive data array, “set_rx_data[TX_RX_DATA_SIZE]”.		

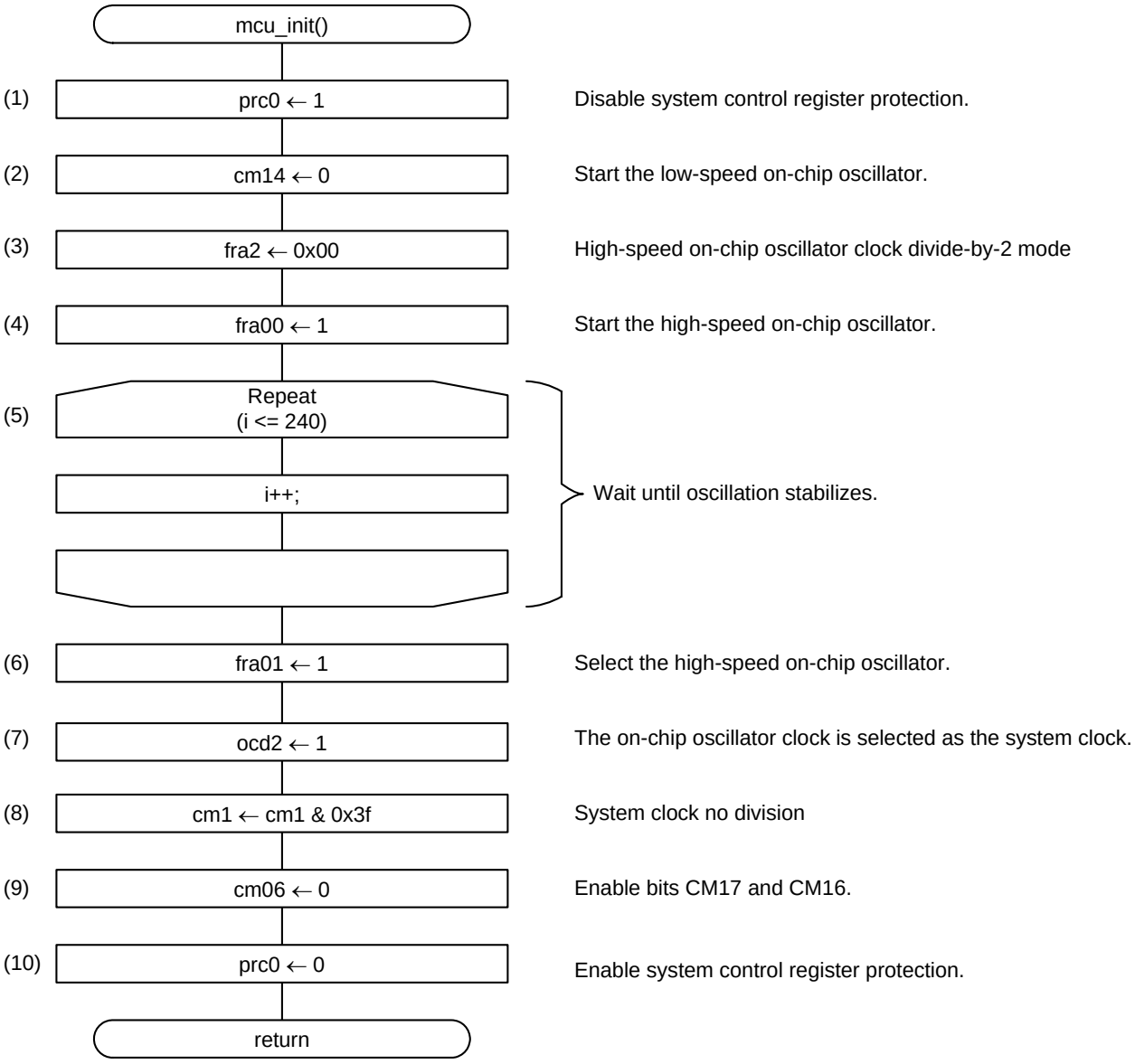
4.2 Main Function

- Flowchart



4.3 System Clock Setting

- Flowchart



• Register Setting

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set system clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	System clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	x	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	System clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

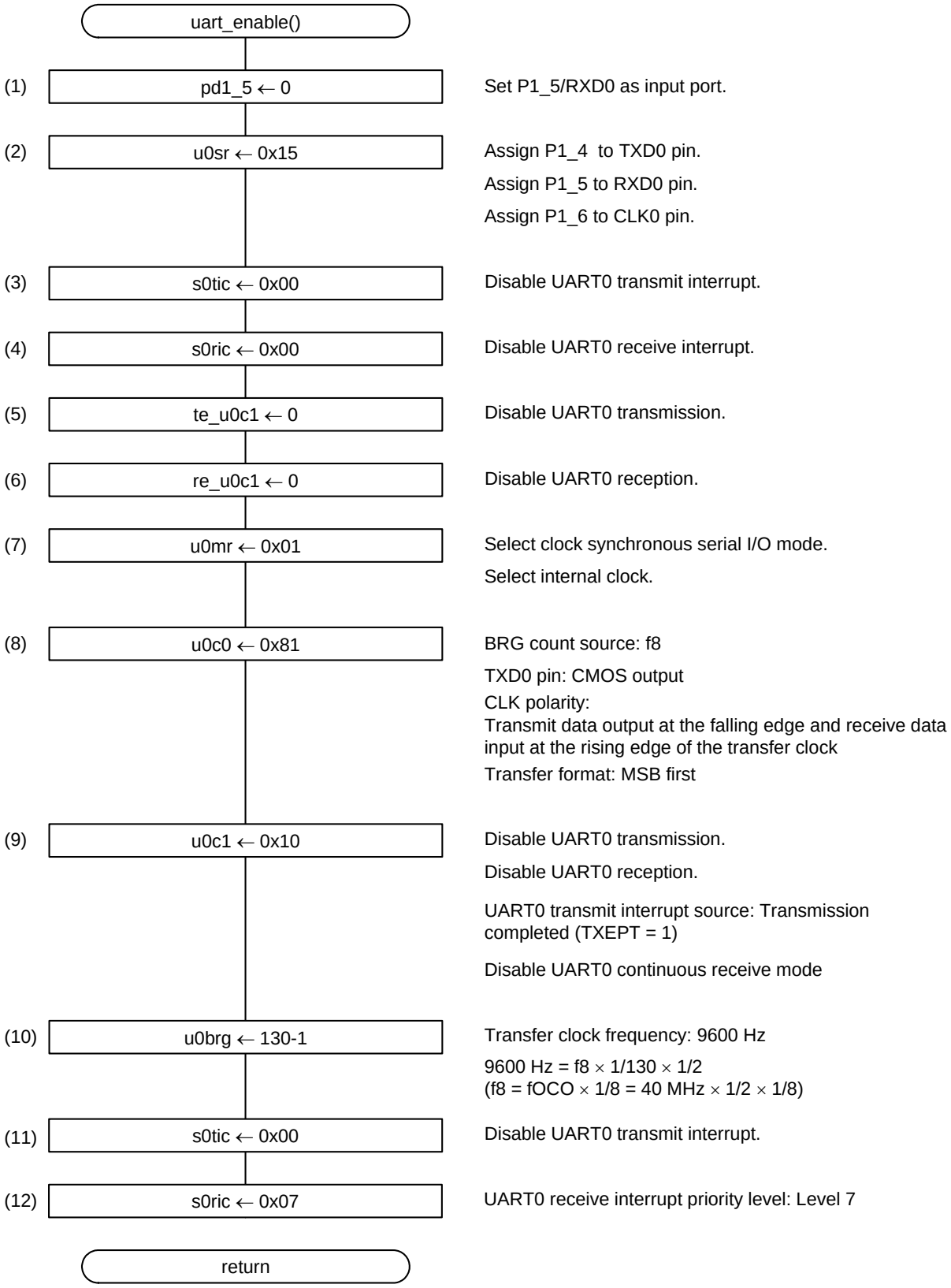
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Serial Interface Setting

- Flowchart



• Register Setting

(1) Set P1_5/RXD0 as an input port.

Port P1 Direction Register (PD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b5	PD1_5	Port PD1_5 direction bit	0: Input mode (functions as an input port)	R/W

(2) Set the UART0 pin select register.

UART0 Pin Select Register (U0SR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	1	—	1	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	1: P1_4 assigned	R/W
b2	RXD0SEL0	RXD0 pin select bit	1: P1_5 assigned	R/W
b4	CLK0SEL0	CLK0 pin select bit	1: P1_6 assigned	R/W

(3) Disable the UART0 transmit interrupt.

Interrupt Control Register (S0TIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(4) Disable the UART0 receive interrupt.

Interrupt Control Register (S0RIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(5) Disable UART0 transmission.

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x		x			0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled	R/W

(6) Disable UART0 reception.

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			x	0	x	

Bit	Symbol	Bit Name	Function	R/W
b2	RE	Receive enable bit	0: Reception disabled	R/W

(7) Set the UART0 transmit/receive mode register (U0MR).

UART0 Transmit/Receive Mode Register (U0MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	x	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 1: Clock synchronous serial I/O mode	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock	R/W

(8) Set UART0 transmit/receive register 0 (U0C0).

UART0 Transmit/Receive Control Register 0 (U0C0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	—	x	—	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	BRG count source select bit	b1 b0 0 1: f8 selected	R/W
b1	CLK1			R/W
b5	NCH	Data output select bit	0: TXD0 pin set to CMOS output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	1: MSB first	R/W

(9) Set UART0 transmit/receive control register 1 (U0C1).

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	1	x	0		0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled	R/W
b2	RE	Receive enable bit	0: Reception disabled	R/W
b4	U0IRS	UART0 transmit interrupt source select bit	1: Transmission completed (TXEPT = 1)	R/W
b5	U0RRM	UART0 continuous receive mode enable bit	0: Continuous receive mode disabled	R/W

(10) Set the UART0 bit rate register (U0BRG). In this program, set the register to 130 - 1 (81h), which is calculated from the formula below to use 9600 Hz.

9600 Hz = f8 × 1/130 × 1/2
(f8 = fOCO × 1/8 = 40 MHz × 1/2 × 1/8)

UART0 Bit Rate Register (U0BRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	0	0	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U0BRG divides the count source by n+1.	00h to FFh	W

(11) Disable the UART0 transmit interrupt.

Interrupt Control Register (S0TIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(12) Set the UART0 receive interrupt priority level.

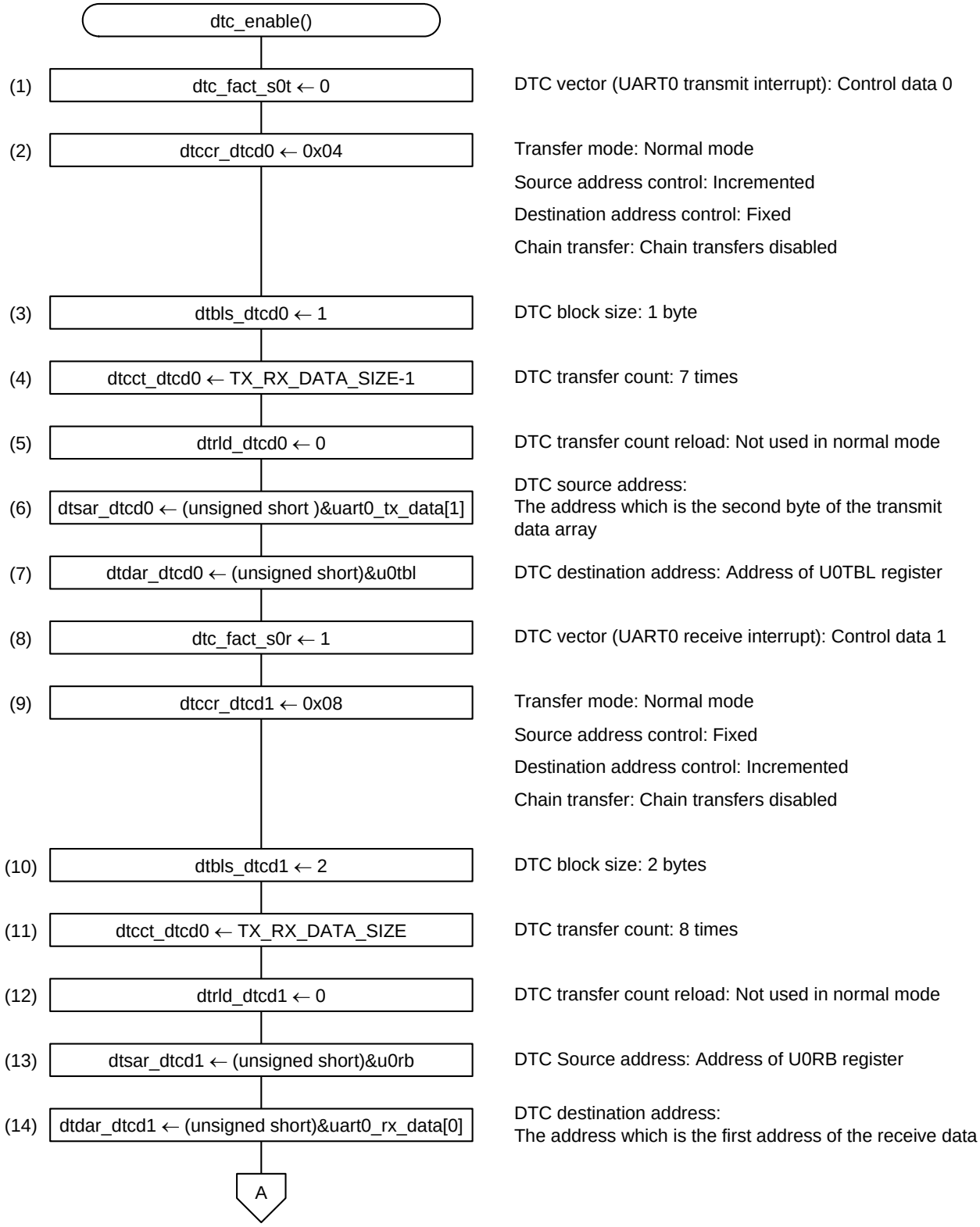
Interrupt Control Register (S0RIC)

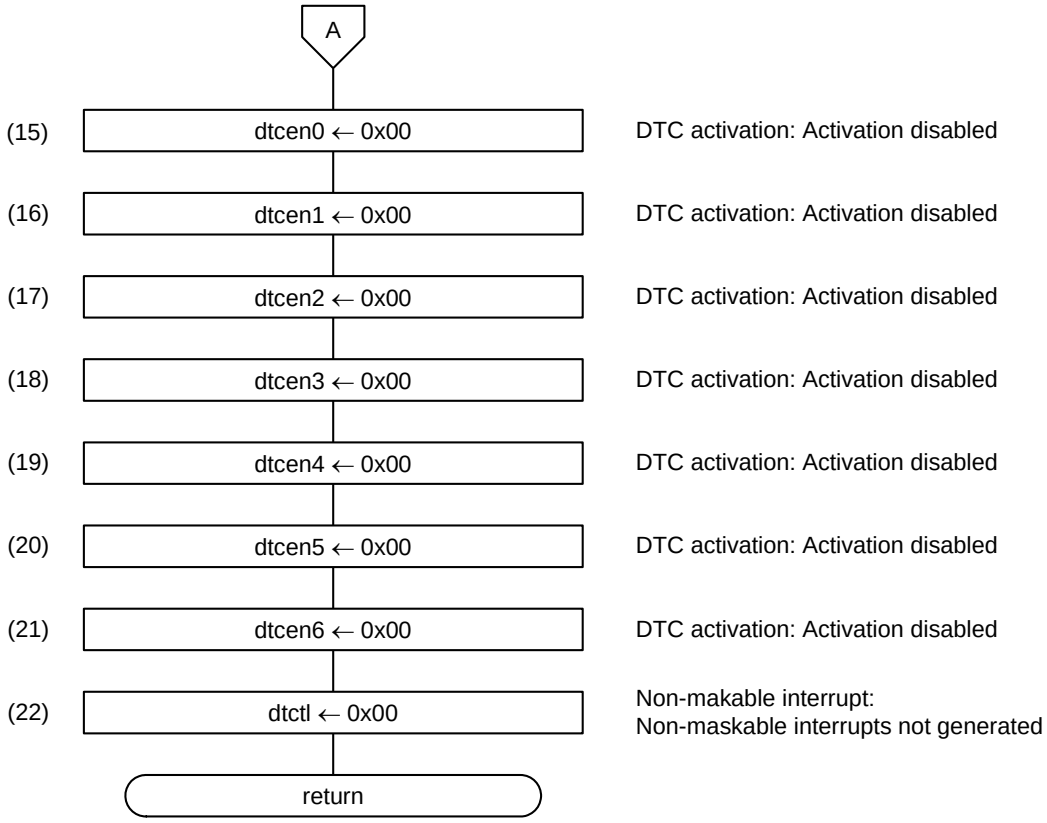
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

4.5 DTC Setting

• Flowchart




A
(15)
dtcen0 ← 0x00
DTC activation: Activation disabled
(16)
dtcen1 ← 0x00
DTC activation: Activation disabled
(17)
dtcen2 ← 0x00
DTC activation: Activation disabled
(18)
dtcen3 ← 0x00
DTC activation: Activation disabled
(19)
dtcen4 ← 0x00
DTC activation: Activation disabled
(20)
dtcen5 ← 0x00
DTC activation: Activation disabled
(21)
dtcen6 ← 0x00
DTC activation: Activation disabled
(22)
dtctl ← 0x00
Non-makable interrupt:
Non-maskable interrupts not generated
return

• Register Setting

(1) Set the DTC control data number to the DTC vector address (address 2C0Bh), which is assigned to the UART0 transmit interrupt. In this program, set address 2C0Bh to 0 to use control data 0.

DTC Vector Address of UART0 Transmit Interrupt

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	These bits store the data from 00000000b to 00010111b. Select one of the 24 groups of control data.	00h to 17h	R/W

(2) Set the DTCCR0 register for control data 0. Set the transfer mode to normal mode, source address to incremented, destination address to fixed, and chain transfer to disabled.

DTC Control Register 0 (DTCCR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	0	0	1	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode	R/W
b2	SAMOD	Source address control bit	1: Incremented	R/W
b3	DAMOD	Destination address control bit	0: Fixed	R/W
b4	CHNE	Chain transfer enable bit	0: Chain transfers disabled	R/W

(3) Set the DTBLS0 register for control data 0. In this program, set it to 1 to transfer 1-byte data seven times.

DTC Block Size Register 0 (DTBLS0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh	R/W

(4) Set the DTCCT0 register for control data 0. In this program, set it to 7 to transfer 1-byte data seven times.

DTC Transfer Count Register 0 (DTCCT0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	1	1	1

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh	R/W

(5) Set the DTRLD0 register for control data 0. As this register is not used in normal mode, set it to 0.

DTC Transfer Count Reload Register 0 (DTRLD0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh	R/W

(6) Set the DTSAR0 register for control data 0. In this program, set the address where the second byte of the transmit data array (uart0_tx_data[1]) is allocated.

DTC Source Address Register 0 (DTSAR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

(7) Set the DTDAR0 register for control data 0. In this program, set address 00A2h where the UART0 transmit buffer register (lower byte of U0TB) is allocated.

DTC Destination Address Register 0 (DTDAR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	1	0	0	0	1	0
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

(8) Set the DTC control data number to the DTC vector address (address 2C0Ah), which is assigned to the UART0 receive interrupt. In this program, set address 2C0Ah to 1 to use control data 1.

DTC Vector Address of UART0 Receive Interrupt

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	These bits store the data from 00000000b to 00010111b. Select one of the 24 groups of control data.	00h to 17h	R/W

(9) Set the DTCCR1 register for control data 1. Set the transfer mode to normal mode, source address to fixed, destination address to incremented, and chain transfer to disabled.

DTC Control Register 1 (DTCCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	0	1	0	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode	R/W
b2	SAMOD	Source address control bit	0: Fixed	R/W
b3	DAMOD	Destination address control bit	1: Incremented	R/W
b4	CHNE	Chain transfer enable bit	0: Chain transfers disabled	R/W

(10) Set the DTBLS1 register for control data 1. In this program, set it to 2 to transfer 2-byte data eight times.

DTC Block Size Register 1 (DTBLS1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	1	0

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh	R/W

(11) Set the DTCCT1 register for control data 1. In this program, set it to 8 to transfer 2-byte data eight times.

DTC Transfer Count Register 1 (DTCCT1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	1	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh	R/W

(12) Set the DTRLD1 register for control data 1. As this register is not used in normal mode, set it to 0.

DTC Transfer Count Reload Register 1 (DTRLD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh	R/W

(13) Set the DTSAR1 register for control data 1. In this program, set address 00A6h where the UART0 receive buffer register (lower byte of U0RB) is allocated.

DTC Source Address Register 1 (DTSAR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	1	0	0	1	1	0
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

(14) Set the DTDAR1 register for control data 1. In this program, set the address where the first byte of the receive data array (“uart0_rx_data[0]”) is allocated.

DTC Destination Address Register 1 (DTDAR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

(15) Set DTC activation enable register 0 (DTCEN0). Disable all DTC activation sources.

DTC Activation Enable Register 0 (DTCEN0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b3	DTCEN03	DTC activation by $\overline{\text{INT4}}$ interrupt enable bit	0: Activation disabled	R/W
b4	DTCEN04	DTC activation by $\overline{\text{INT3}}$ interrupt enable bit	0: Activation disabled	R/W
b5	DTCEN05	DTC activation by $\overline{\text{INT2}}$ interrupt enable bit	0: Activation disabled	R/W
b6	DTCEN06	DTC activation by $\overline{\text{INT1}}$ interrupt enable bit	0: Activation disabled	R/W
b7	DTCEN07	DTC activation by $\overline{\text{INT0}}$ interrupt enable bit	0: Activation disabled	R/W

(16) Set DTC activation enable register 1 (DTCEN1). Disable all DTC activation sources.

DTC Activation Enable Register 1 (DTCEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCEN10	DTC activation by UART2 transmit interrupt enable bit	0: Activation disabled	R/W
b1	DTCEN11	DTC activation by UART2 receive interrupt enable bit	0: Activation disabled	R/W
b2	DTCEN12	DTC activation by UART1 transmit interrupt enable bit	0: Activation disabled	R/W
b3	DTCEN13	DTC activation by UART1 receive interrupt enable bit	0: Activation disabled	R/W
b4	DTCEN14	DTC activation by UART0 transmit interrupt enable bit	0: Activation disabled	R/W
b5	DTCEN15	DTC activation by UART0 receive interrupt enable bit	0: Activation disabled	R/W
b6	DTCEN16	DTC activation by A/D conversion interrupt enable bit	0: Activation disabled	R/W
b7	DTCEN17	DTC activation by key input interrupt enable bit	0: Activation disabled	R/W

(17) Set DTC activation enable register 2 (DTCEN2). Disable all DTC activation sources.

DTC Activation Enable Register 2 (DTCEN2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	—	—	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCEN20	DTC activation by Timer RC input-capture/compare-match B interrupt enable bit	0: Activation disabled	R/W
b1	DTCEN21	DTC activation by timer RC input-capture/compare-match A interrupt enable bit	0: Activation disabled	R/W
b4	DTCEN24	DTC activation by comparator A1 interrupt enable bit	0: Activation disabled	R/W
b5	DTCEN25	DTC activation by comparator A2 interrupt enable bit	0: Activation disabled	R/W
b6	DTCEN26	DTC activation by SSU/I^2C bus transmit data empty interrupt enable bit	0: Activation disabled	R/W
b7	DTCEN27	DTC activation by SSU/I^2C bus receive data full interrupt enable bit	0: Activation disabled	R/W

(18) Set DTC activation enable register 3 (DTCEN3). Disable all DTC activation sources.

DTC Activation Enable Register 3 (DTCEN3)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCEN30	DTC activation by timer RD1 input-capture/compare-match B interrupt enable bit	0: Activation disabled	R/W
b1	DTCEN31	DTC activation by timer RD1 input-capture/compare-match A interrupt enable bit	0: Activation disabled	R/W
b2	DTCEN32	DTC activation by timer RD0 input-capture/compare-match D interrupt enable bit	0: Activation disabled	R/W
b3	DTCEN33	DTC activation by timer RD0 input-capture/compare-match C interrupt enable bit	0: Activation disabled	R/W
b4	DTCEN34	DTC activation by timer RD0 input-capture/compare-match B interrupt enable bit	0: Activation disabled	R/W
b5	DTCEN35	DTC activation by timer RD0 input-capture/compare-match A interrupt enable bit	0: Activation disabled	R/W
b6	DTCEN36	DTC activation by timer RC input-capture/compare-match D interrupt enable bit	0: Activation disabled	R/W
b7	DTCEN37	DTC activation by timer RC input-capture/compare-match C interrupt enable bit	0: Activation disabled	R/W

(19) Set DTC activation enable register 4 (DTCEN4). Disable all DTC activation sources.

DTC Activation Enable Register 4 (DTCEN4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	DTCEN46	DTC activation by timer RD1 input-capture/compare-match D interrupt enable bit	0: Activation disabled	R/W
b7	DTCEN47	DTC activation by timer RD1 input-capture/compare-match C interrupt enable bit	0: Activation disabled	R/W

(20) Set DTC activation enable register 5 (DTCEN5). Disable all DTC activation sources.

DTC Activation Enable Register 5 (DTCEN5)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	DTCEN55	DTC activation by timer RE interrupt enable bit	0: Activation disabled	R/W

(21) Set DTC activation enable register 6 (DTCEN6). Disable all DTC activation sources.

DTC Activation Enable Register 6 (DTCEN6)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	—	0	0	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b3	DTCEN63	DTC activation by flash ready status interrupt enable bit	0: Activation disabled	R/W
b4	DTCEN64	DTC activation by timer RB interrupt enable bit	0: Activation disabled	R/W
b5	DTCEN65	DTC activation by timer RA interrupt enable bit	0: Activation disabled	R/W

(22) Set the DTC activation control register. Disable DTC activation when a non-maskable interrupt (watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

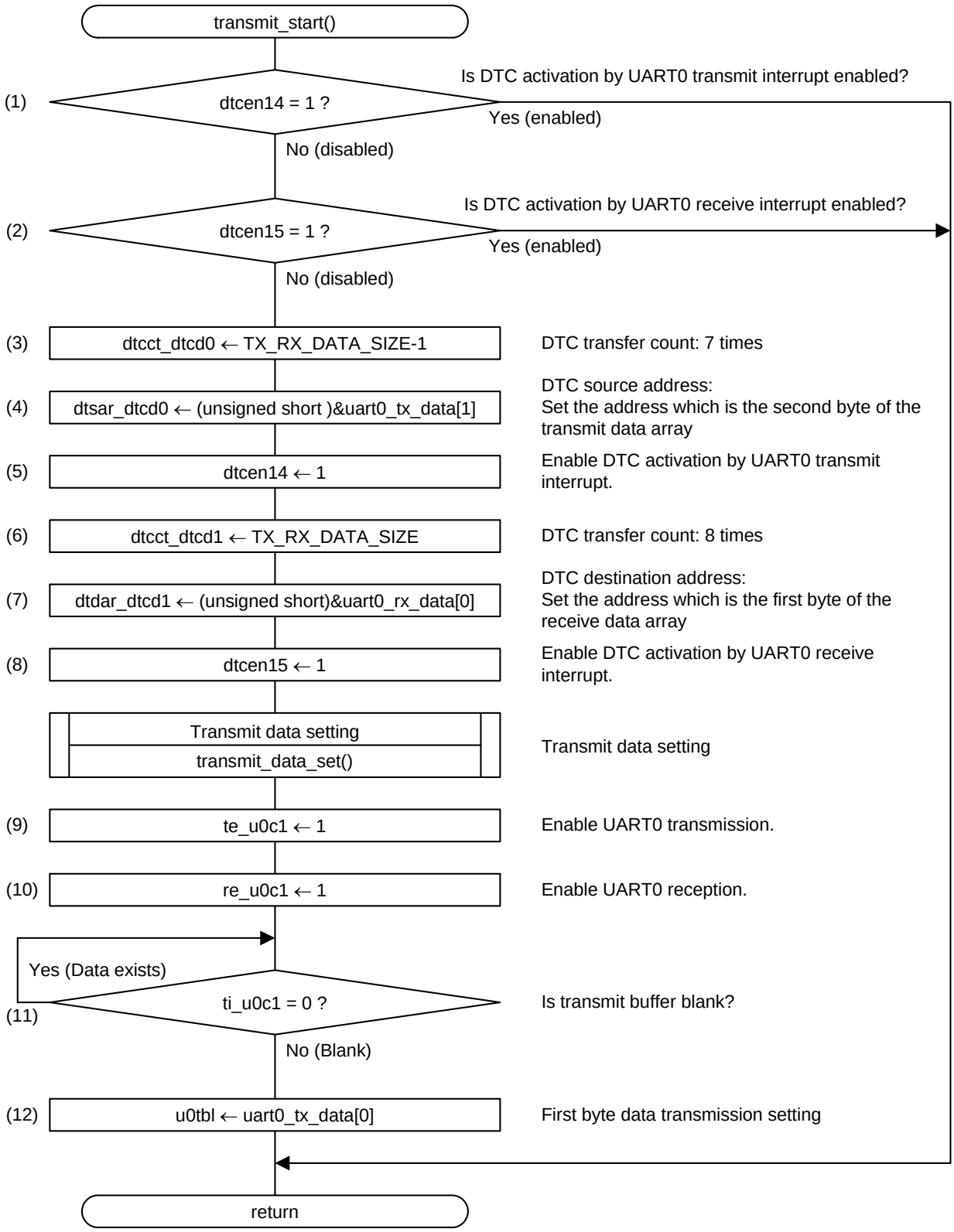
DTC Activation Control Register (DTCTL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	0	—

Bit	Symbol	Bit Name	Function	R/W
b1	NMIF	Non-maskable interrupt generation bit	0: Non-maskable interrupts not generated	R/W

4.6 Transmit Start

• Flowchart



• Register Setting

(1) Check whether DTC activation by the UART0 transmit interrupt enable bit is disabled (DTCEN14 is 0).

(2) Check whether DTC activation by the UART0 receive interrupt enable bit is disabled (DTCEN15 is 0).

(3) Set the DTCCT0 register for control data 0. In this program, set it to 7 to transfer 1-byte data seven times.

DTC Transfer Count Register 0 (DTCCT0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	1	1	1

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh	R/W

(4) Set the DTSAR0 register for control data 0. In this program, set the address where the second byte of the transmit data array (“uart0_tx_data[1]”) is allocated.

DTC Source Address Register 0 (DTSAR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

(5) Enable DTC activation by UART0 transmit interrupt.

DTC Activation Enable Register 1 (DTCEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	1	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	DTCEN14	DTC activation by UART0 transmit interrupt enable bit	1: Activation enabled	R/W

(6) Set the DTCCT1 register for control data 1. In this program, set it to 8 to transfer 2-byte data eight times.

DTC Transfer Count Register 1 (DTCCT1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	1	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh	R/W

(7) Set the DTDAR1 register for control data 1. In this program, set the address where the first byte of the receive data array (“uart0_rx_data[0]”) is allocated.

DTC Destination Address Register 1 (DTDAR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

(8) Enable DTC activation by UART0 receive interrupt.

DTC Activation Enable Register 1 (DTCEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	1	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b5	DTCEN15	DTC activation by UART0 receive interrupt enable bit	1: Activation enabled	R/W

(9) Enable UART0 transmission.

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			x		x	1

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	1: Transmission enabled	R/W

(10) Enable UART0 reception.

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			x	1	x	

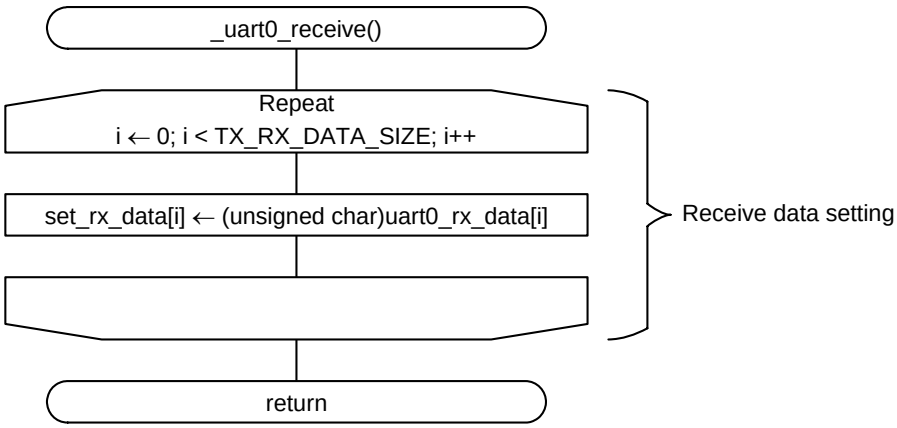
Bit	Symbol	Bit Name	Function	R/W
b2	RE	Receive enable bit	1: Reception enabled	R/W

(11) Check whether the transmit buffer is empty (TI_U0C1 is 1).

(12) Write the transmit data to the UART0 transmit buffer register (lower byte of U0TB).

4.7 UART0 Receive Interrupt

• Flowchart



5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C/Tiny Family page.

6. Reference Documents

Hardware Manual
R8C/35C Group Hardware Manual Rev.0.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	R8C/35C Group Serial I/O Operation in Clock Synchronous Serial I/O Mode with DTC

Rev.	Date	Description	
		Page	Summary
1.00	Oct 23, 2009	–	First Edition issued

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