R8C/35C Group

Rewriting Program ROM Using EW0 Mode

R01AN0073EJ0101
Rev.1.01
Nov. 30, 2010

1. Abstract

This document describes the setting method and an application example for rewriting program ROM using EW0 mode.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/35C Group (ROM 24 KB)
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 EW0 Mode Features

Transfer a CPU rewrite program to RAM and execute the program command and erase command using the CPU rewrite program on RAM in EW0 mode to rewrite the user ROM area. Since the CPU operates during program and erase operations in EW0 mode, peripheral function interrupts can be accepted during program and erase operations by allocating the vector and interrupt program on RAM. In this application note, the CPU rewrite program is transferred to RAM in the main processing. Interrupts cannot be accepted during program and erase operations.

3.2 Program Outline

Rewrite block 1 of the program ROM by the CPU rewrite control program using EW0 mode. The CPU rewrite control program to rewrite block 1 is transferred from ROM to RAM in the procedure below.

(1) In the R1H register, set the number for the ten thousands' place of the start address in the CPU rewrite control program.
(2) In the A0 register, set the number for the thousands' place of the start address in the CPU rewrite control program.
(3) In the A1 register, set the start address of RAM to which the CPU rewrite control program is transferred. In this application note, set address 00A00h as the start address.
(4) Set the program size of the CPU rewrite control program to the R3 register.
(5) Transfer the CPU rewrite control program to RAM area using the SMOVF instruction.
(6) Execute the program transferred to RAM (jump to address 00A00h).

Figure 3.1 shows Program Allocation. Figure 3.2 shows a Program Outline Flowchart.

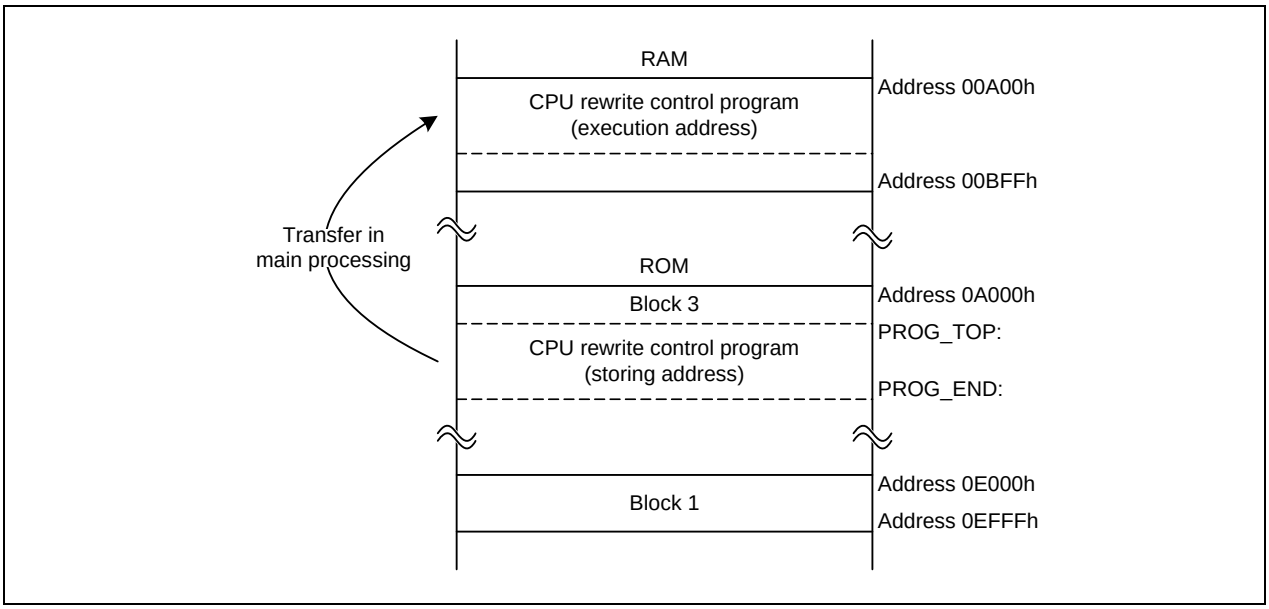


Figure 3.1 Program Allocation

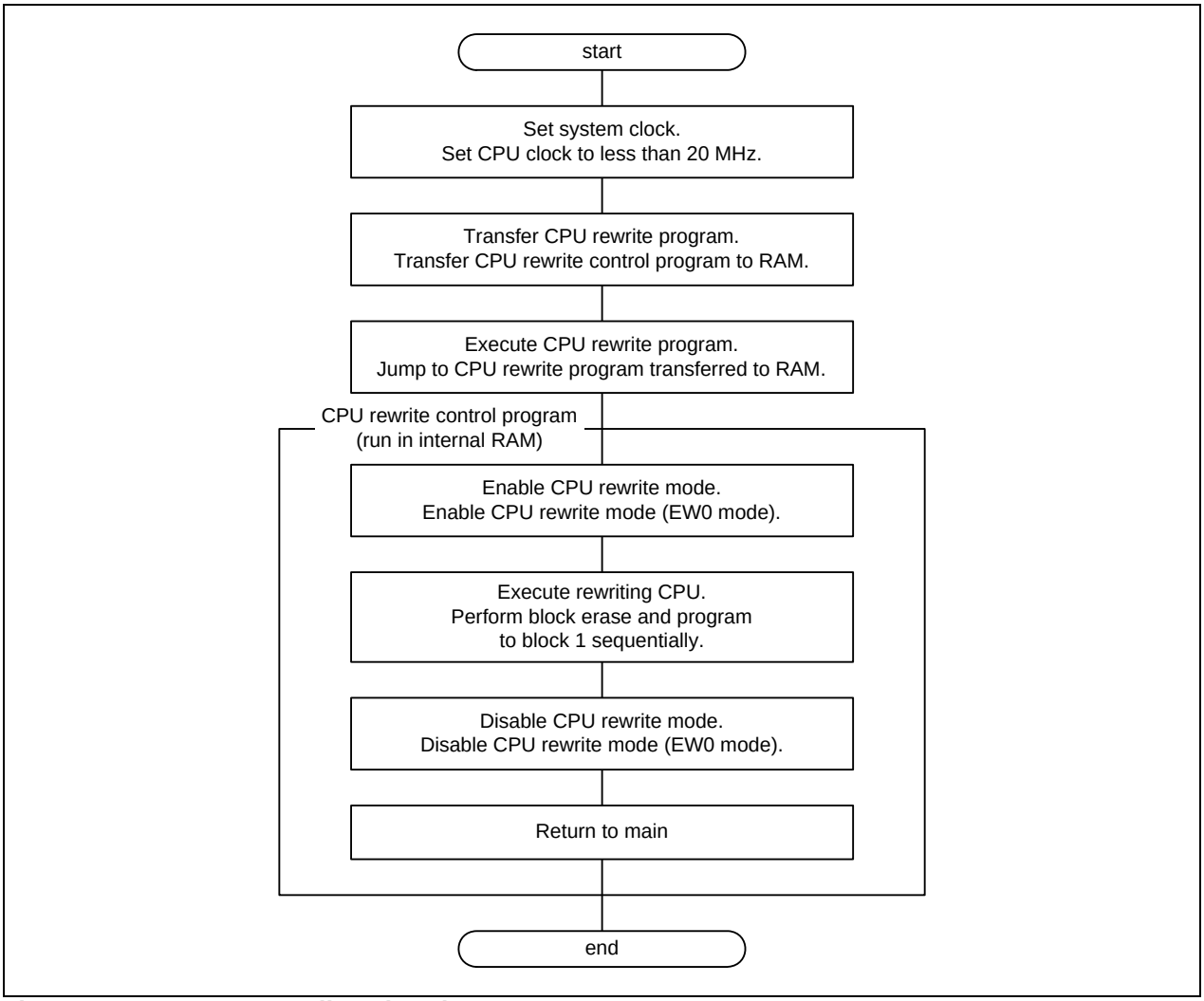


Figure 3.2 Program Outline Flowchart

3.3 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	389 bytes	In the r01an0073_src.c module
RAM	1288 bytes	In the r01an0073_src.c module (including variable (1024 bytes) in which the write data is stored and CPU rewrite control program size (261 bytes))
Maximum user stack	18 bytes	
Maximum interrupt stack	0 bytes	Not used

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile options: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/35C Group hardware user's manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void main (void)		
Outline	Main function		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char ew0_rewrite_program_on_ram[0x200]		CPU rewrite control program area
	unsigned char ew0_status		Status
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform main processing. Set the write data, transfer the CPU rewrite control program, and determine the CPU rewrite result.		

Declaration	void mcu_init (void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (XIN clock).		

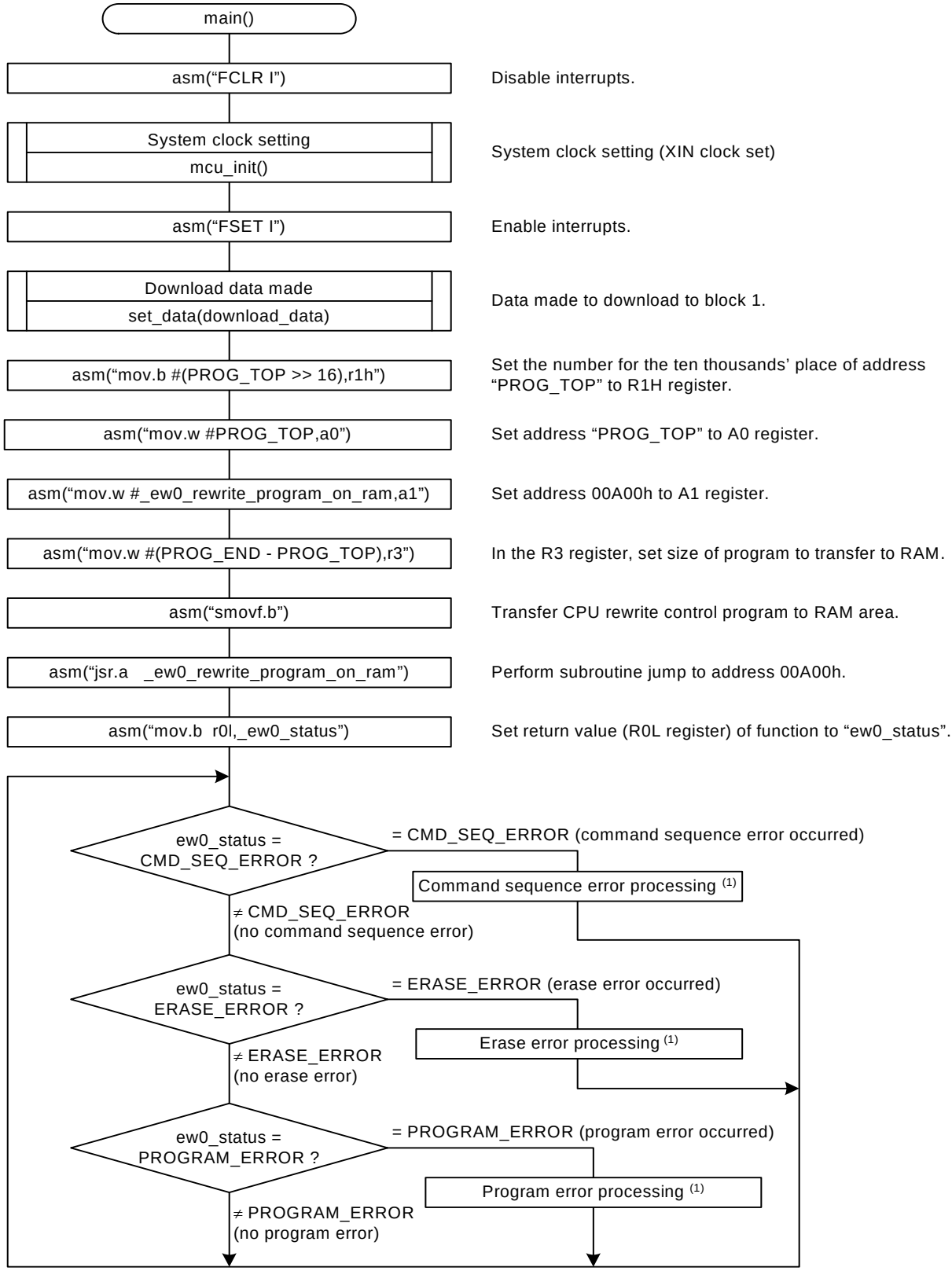
Declaration	void set_data (unsigned char *data)		
Outline	Write data made		
Argument	Argument name		Meaning
	unsigned char *data		Start address of destination write data
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Make the write data in the program ROM (block 1). No processing is performed in this application note. Add processing if necessary.		

Declaration	unsigned char ew0_rewrite_control (void)		
Outline	CPU rewrite control		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char *wp		Write address
	unsigned char download_data[DATA_SIZE]		Write data
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERASE_ERROR	Erase error
		PROGRAM_ERROR	Program error
Function	Execute this processing on RAM and rewrite block 1 in EW0 mode. After executing the block erase, write data set in the write data and return the status of the flash memory.		

Declaration	unsigned char full_sts_chk (unsigned char *chk_adr)		
Outline	Full status check		
Argument	Argument name		Meaning
	unsigned char *chk_adr		Address where erase command or program command data is written
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERASE_ERROR	Erase error
		PROGRAM_ERROR	Program error
Function	Perform full status check.		

4.2 Main Function

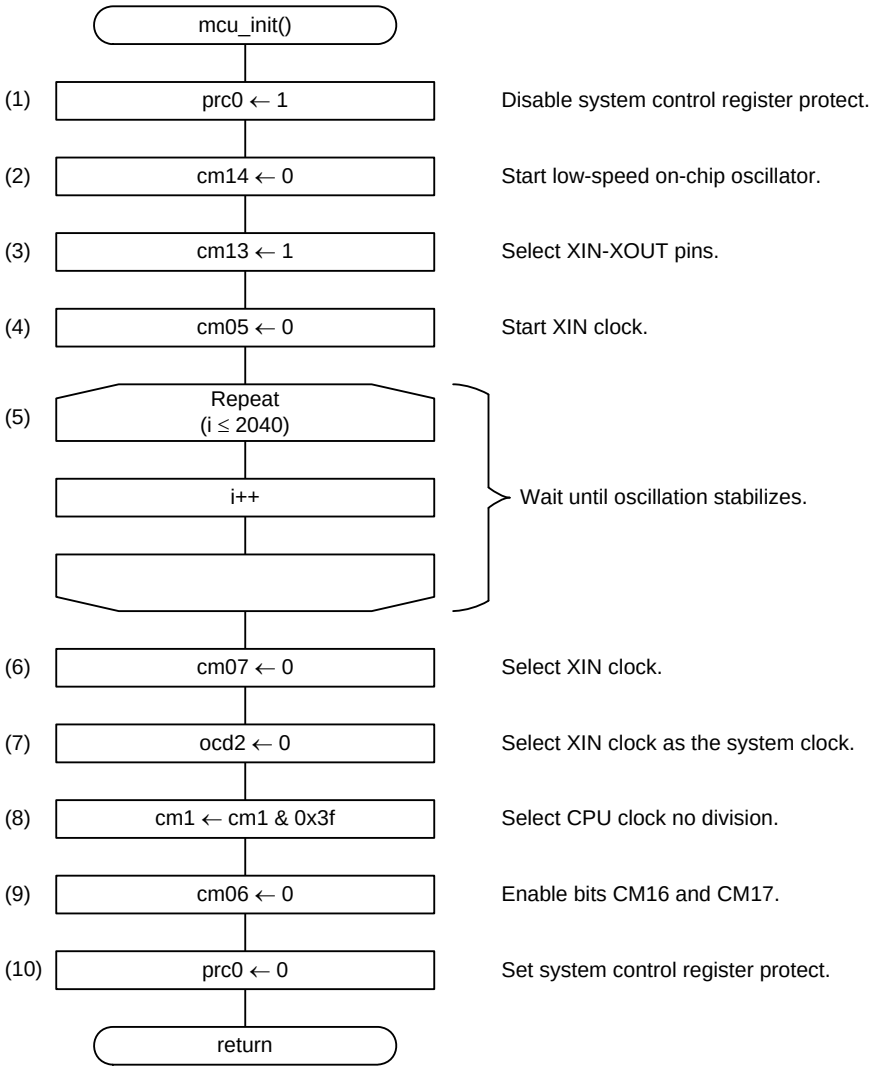
- Flowchart



Note:
1. In this application note, command sequence error processing, erase error processing, and program error processing are not performed. Perform error processing if necessary.

4.3 System Clock Setting

- Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Oscillate the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0		x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Switch ports P4_6 and P4_7 to XIN-XOUT pins.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—		1	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port/XIN-XOUT switch bit	1: XIN-XOUT pins	R/W

(4) Oscillate the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(5) Wait until oscillation stabilizes.

(6) Select the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	0: XIN clock	R/W

(7) Select the system clock as the XIN clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	0: XIN clock selected	R/W

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—			x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

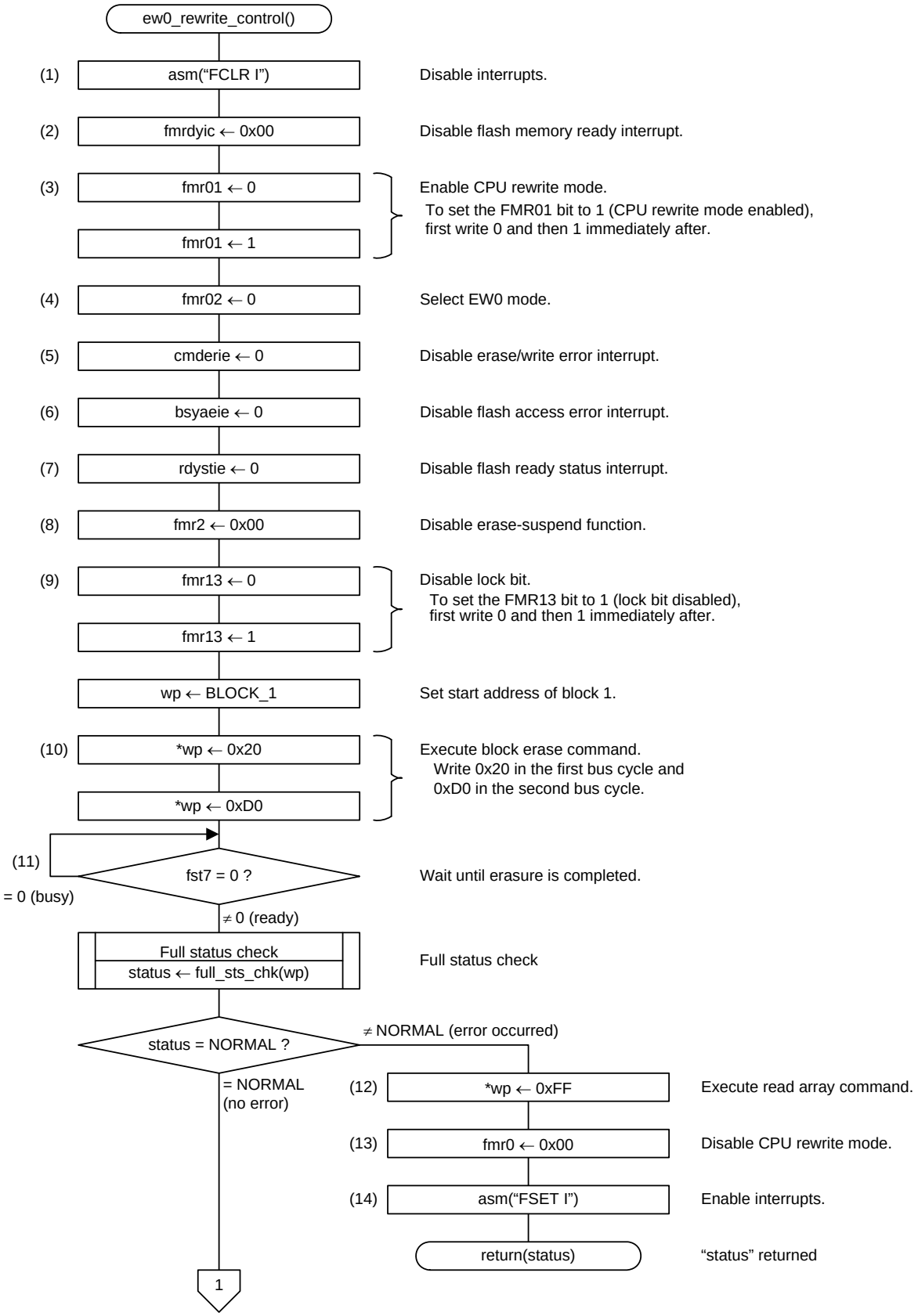
Protect Register (PRCR)

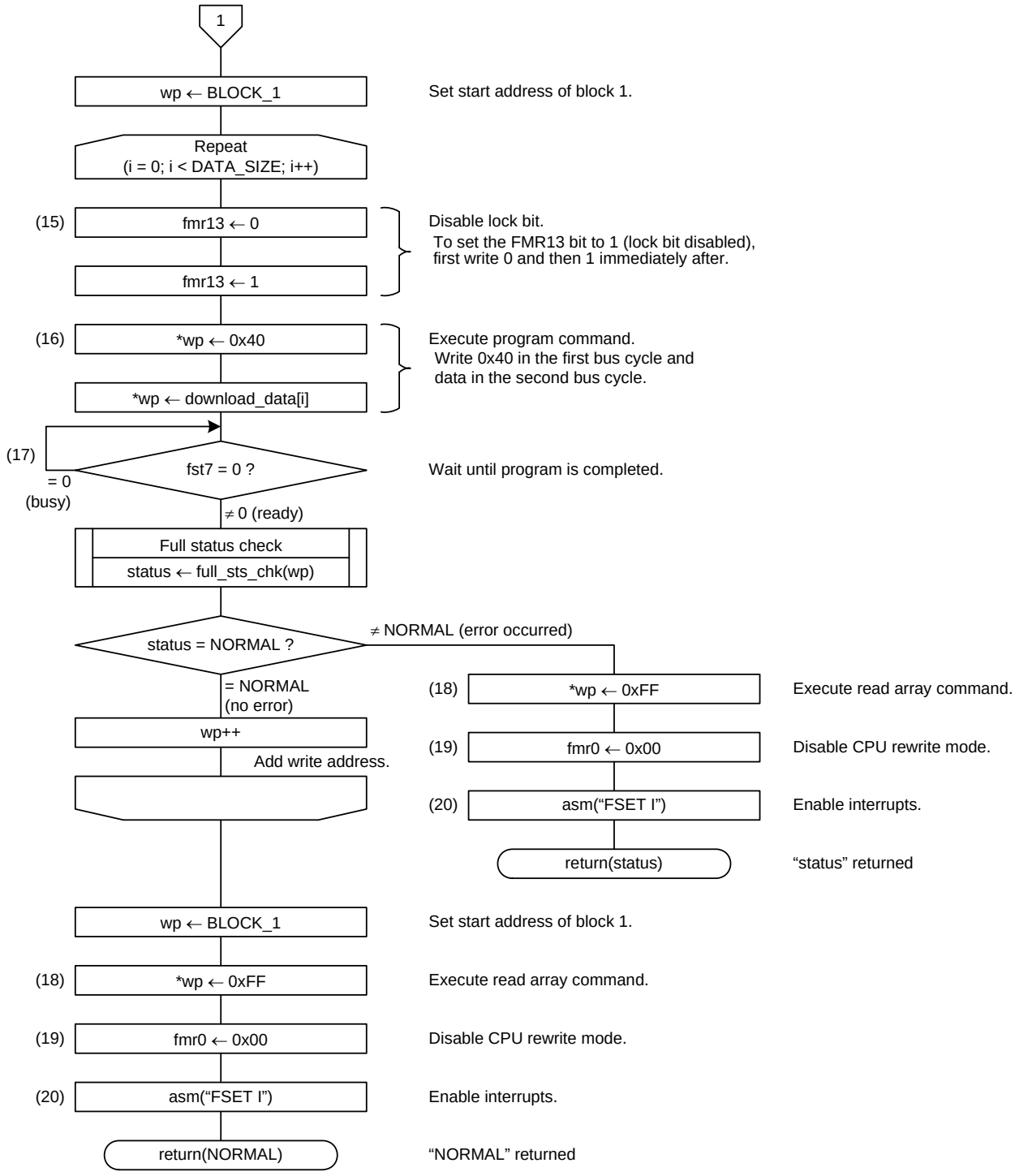
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 CPU Rewrite Control

- Flowchart




1
wp ← BLOCK_1
Set start address of block 1.
Repeat
(i = 0; i < DATA_SIZE; i++)
(15)
fmr13 ← 0
Disable lock bit.
To set the FMR13 bit to 1 (lock bit disabled), first write 0 and then 1 immediately after.
fmr13 ← 1
(16)
*wp ← 0x40
Execute program command.
Write 0x40 in the first bus cycle and data in the second bus cycle.
*wp ← download_data[i]
(17)
fst7 = 0 ?
Wait until program is completed.
= 0 (busy)
≠ 0 (ready)
Full status check
status ← full_sts_chk(wp)
status = NORMAL ?
≠ NORMAL (error occurred)
= NORMAL (no error)
(18)
*wp ← 0xFF
Execute read array command.
wp++
(19)
fmr0 ← 0x00
Disable CPU rewrite mode.
Add write address.
(20)
asm(“FSET I”)
Enable interrupts.
return(status)
“status” returned
wp ← BLOCK_1
Set start address of block 1.
(18)
*wp ← 0xFF
Execute read array command.
(19)
fmr0 ← 0x00
Disable CPU rewrite mode.
(20)
asm(“FSET I”)
Enable interrupts.
return(NORMAL)
“NORMAL” returned

• Register settings

(1) Clear the I flag and disable interrupts.

(2) Disable the flash memory ready interrupt.

Interrupt Control Register (FMRDYIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

(3) Enable CPU rewrite mode. To set the FMR01 bit to 1, first write 0 and then 1 immediately.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x		1	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	1: CPU rewrite mode enabled	R/W

(4) Set to EW0 mode.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x	0		—

Bit	Symbol	Bit Name	Function	R/W
b2	FMR02	EW1 mode select bit	0: EW0 mode	R/W

(5) Disable the erase/write error interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x			—

Bit	Symbol	Bit Name	Function	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled	R/W

(6) Disable the flash access error interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x			—

Bit	Symbol	Bit Name	Function	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled	R/W

(7) Disable the flash ready status interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x			—

Bit	Symbol	Bit Name	Function	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled	R/W

(8) Disable the erase-suspend function.

Flash Memory Control Register 2 (FMR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	—	—	—	—	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit	0: Erase-suspend disabled	R/W

(9) Disable the lock bit. To set the FMR13 bit to 1, first write 0 and then 1 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	1	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b3	FMR13	Lock bit disable select bit	1: Lock bit disabled	R/W

(10) After writing block erase command 20h in the first bus cycle and confirmation command D0h to a given address in the block to be erased in the second bus cycle, erasure (erase and erase verify) starts.

(11) Wait until erasure is completed.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

(12) Write read array command FFh to enter read array mode.

(13) Disable CPU rewrite mode.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x		0	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

(14) Set the I flag to enable interrupts.

(15) Disable the lock bit. To set the FMR13 bit to 1, first write 0 and then 1 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	1	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b3	FMR13	Lock bit disable select bit	1: Lock bit disabled	R/W

(16) After writing program command 40h in the first bus cycle and data in the second bus cycle, writing (data program and verify) starts. In the second bus cycle, set the same address value as the address value specified in the first bus cycle.

(17) Wait until writing is completed.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

(18) Write read array command FFh to enter read array mode.

(19) Disable CPU rewrite mode.

Flash Memory Control Register 0 (FMR0)

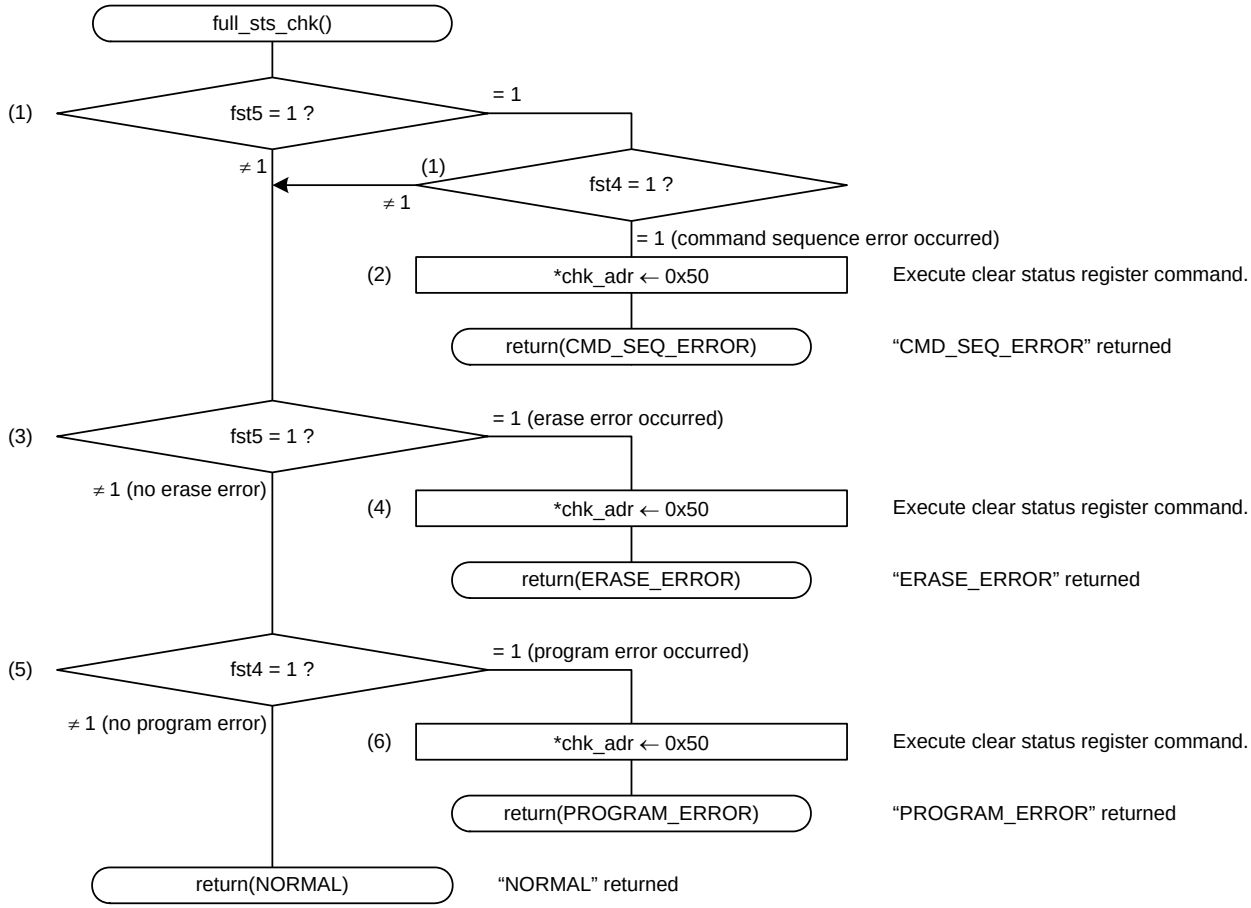
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x		0	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

(20) Set the I flag to enable interrupts.

4.5 Full Status Check

- Flowchart



• Register settings

(1) Confirm that a command sequence error occurs by reading bits FST4 and FST5 in the FST register.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b4	FST4	Program error flag	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error flag	0: No erase error/blank check error 1: Erase error/blank check error	R

(2) Write clear status register command 50h to the address where erase command 20h or program command 40h was written when a program error (FST4 is 1) and an erase error (FST5 is 1) occur.

(3) Confirm that an erase error occurs by reading the FST5 bit in the FST register.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b5	FST5	Erase error/blank check error flag	0: No erase error/blank check error 1: Erase error/blank check error	R

(4) Write clear status register command 50h to the address where erase command 20h was written when an erase error (FST5 is 1) occurs.

(5) Confirm that a program error occurs by reading the FST4 bit in the FST register.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b4	FST4	Program error flag	0: No program error 1: Program error	R

(6) Write clear status register command 50h to the address where program command 40h was written when a program error (FST4 is 1) occurs.

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/35C Group User’s Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

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Revision History	R8C/35C Group Rewriting Program ROM Using EW0 Mode

Rev.	Date	Description	
		Page	Summary
1.01	Nov. 30, 2010	–	First Edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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