R8C/35C Group

Rewriting the Data Flash

R01AN0088EJ0101
Rev.1.01
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1. Abstract

This document describes the setting method and an application example for rewriting the data flash.

2. Introduction

The application example described in this document applies to the following microcomputer MCU:

- MCU: R8C/35C Group

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

When rewriting (writing and/or erasing) the flash memory in EW1 mode in the R8C/35C Group, the following show the differences depending on flash memory areas:

- Program ROM area: CPU is in a hold state (states of the I/O ports are retained prior to command execution).
- Data flash area: CPU is operating due to a background operation (BGO) function.

This application note describes a program for rewriting (writing or erasing) the data flash area in EW1 mode.

3.1 Program Outline

3.1.1 Rewriting Data in the Data Flash Area

This application note assumes that one record is 64 bytes and each block is divided into 16. Divided areas are used as records 0 to 15. Figure 3.1 shows the relationship between the data flash and records.

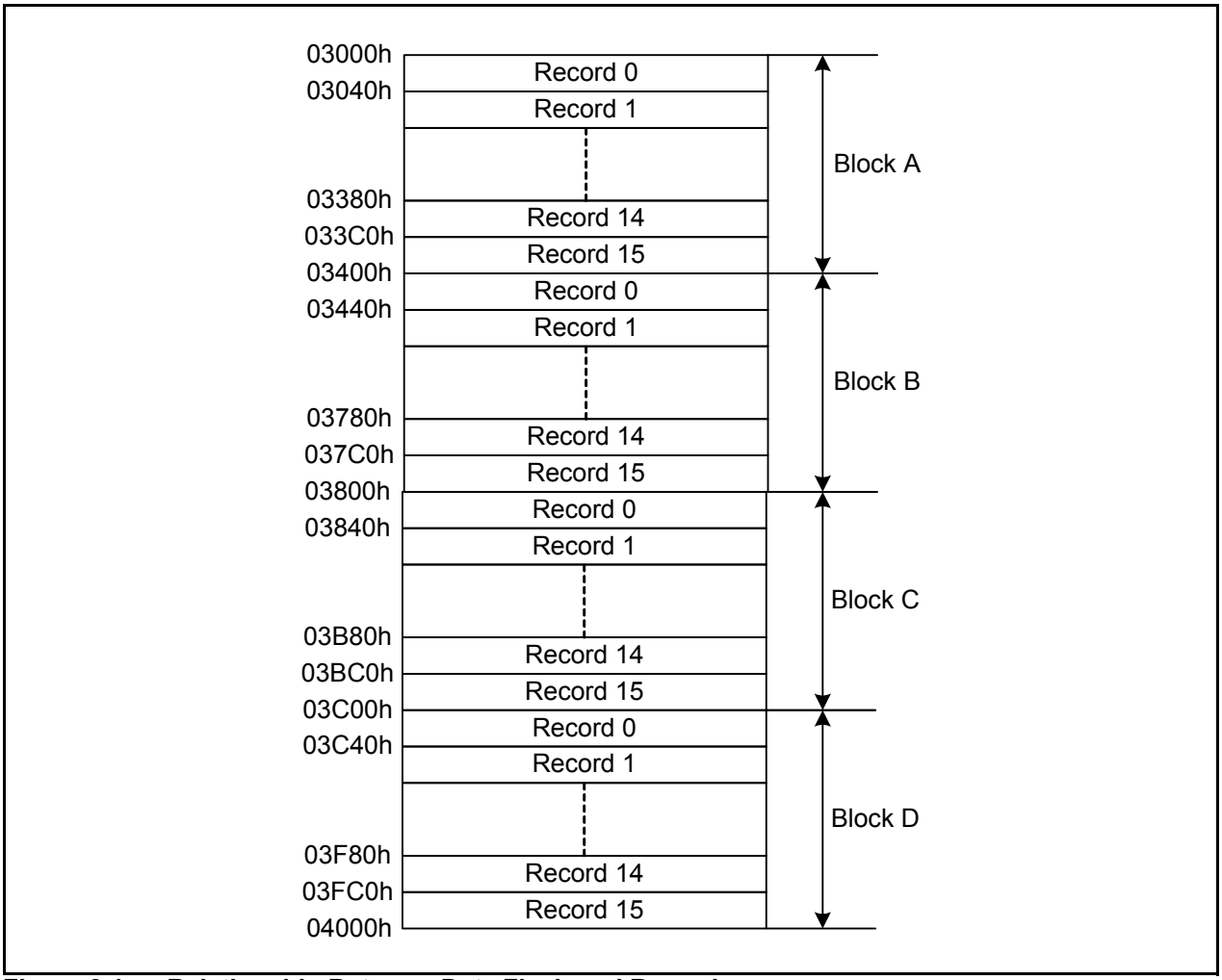


Figure 3.1 Relationship Between Data Flash and Records

When writing data, write in record units starting from record 0 of each block. After writing to record 15, perform a block erase to erase all contents of the next block. When writing the next data, start from record 0 in the block which was just erased. After writing to record 15 of block D, erase all contents of block A, start writing from record 0 of block A, and repeat these steps.

3.2 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	765 bytes	In the r01an0088_src.c module
RAM	42 bytes	In the r01an0088_src.c module
Maximum user stack	30 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile options: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/35C Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void main (void)		
Outline	Main function		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Initialize the system clock and write record. Write to records and determine the results.		

Declaration	void mcu_init (void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (high-speed on-chip oscillator).		

Declaration	void record_init (void)		
Outline	Write record initialization		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char write_record		Write record number
	unsigned char block_select		Block selected
Returned value	Type	Value	Meaning
	None	—	—
Function	Clear data flash area, initialize the selected block (block_select) and write the record number (write_record).		

Declaration	unsigned char write_control (void)		
Outline	Data write control		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char record_data[RECORD_SIZE]		Record data
	unsigned char write_record		Write record number
	unsigned char block_select		Block selected
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERS_BLK_CHK_ERROR	Erase/blank check error
		PROGRAM_ERROR	Program error
Function	After writing the record data, update the write record number (write_record). When writing data to the last record (record 15), erase the next block and change the block selected.		

Declaration	void set_data (unsigned char *data)		
Outline	Write data made		
Argument	Argument name		Meaning
	unsigned char *data		Write data starting address
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Make the record data to write to the data flash. No processing is performed in this application note. Add processing based on the user system.		

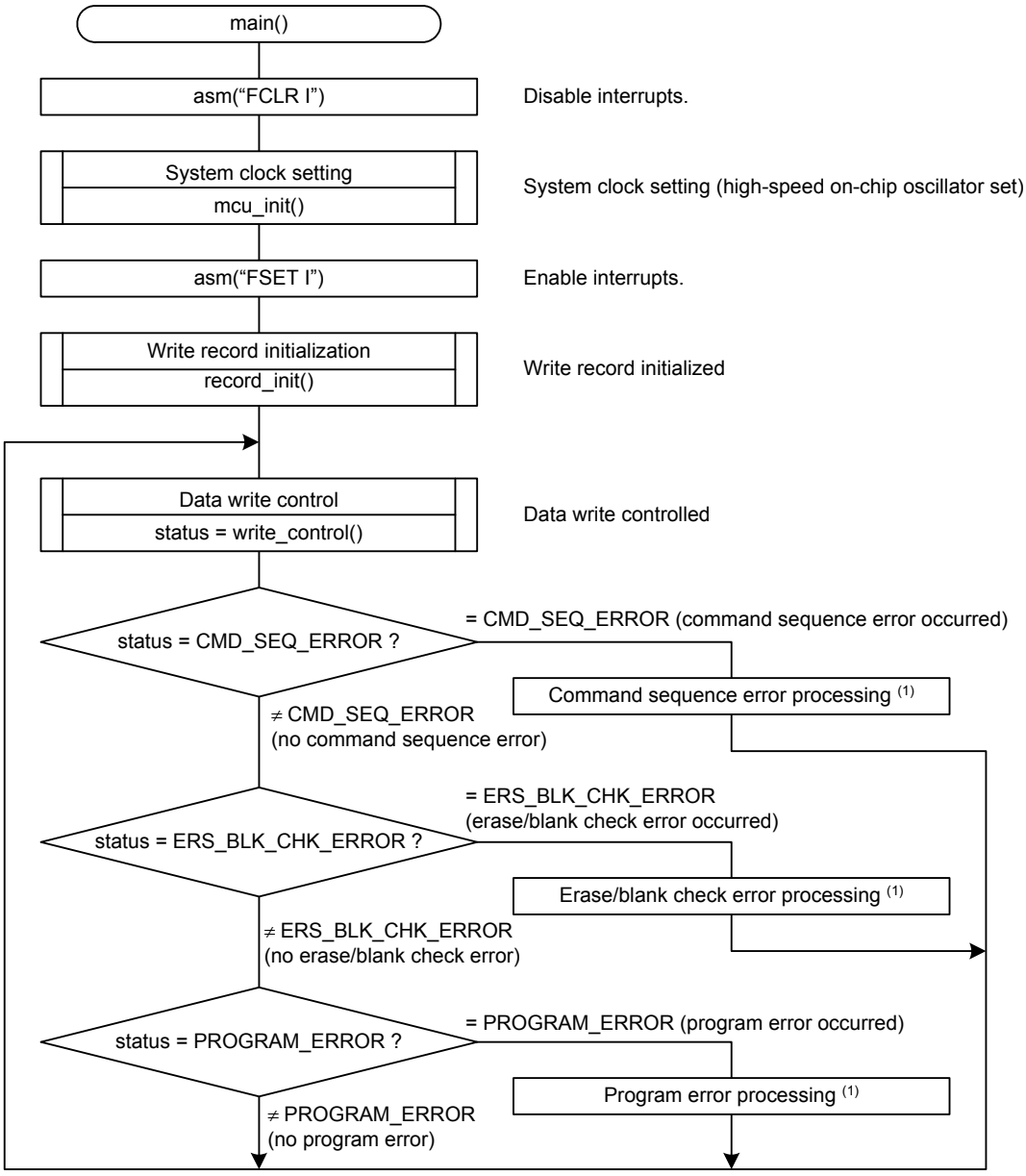
Declaration	unsigned char block_erase (unsigned char block_no)		
Outline	Block erase		
Argument	Argument name		Meaning
	unsigned char block_no		Erase block
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERS_BLK_CHK_ERROR	Erase/blank check error
		PROGRAM_ERROR	Program error
Function	Block erase the specified block in EW1 mode.		

Declaration	unsigned char data_write (unsigned char *data)		
Outline	Programming		
Argument	Argument name		Meaning
	unsigned char *data		Write data starting address
Variable (global)	Variable name		Contents
	unsigned char block_select		Block selected
	unsigned char write_record		Write record number
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERS_BLK_CHK_ERROR	Erase/blank check error
		PROGRAM_ERROR	Program error
Function	Write data to the write record (write_record) of the selected block (block_select) in EW1 mode.		

Declaration	unsigned char full_sts_chk (unsigned char *chk_adr)		
Outline	Full status check		
Argument	Argument name		Meaning
	unsigned char *chk_adr		Address where erase command or program command data is written
Variable (global)	Variable name		Contents
	unsigned char block_select		Block selected
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERS_BLK_CHK_ERROR	Erase/blank check error
		PROGRAM_ERROR	Program error
Function	Perform full status check.		

4.2 Main Function

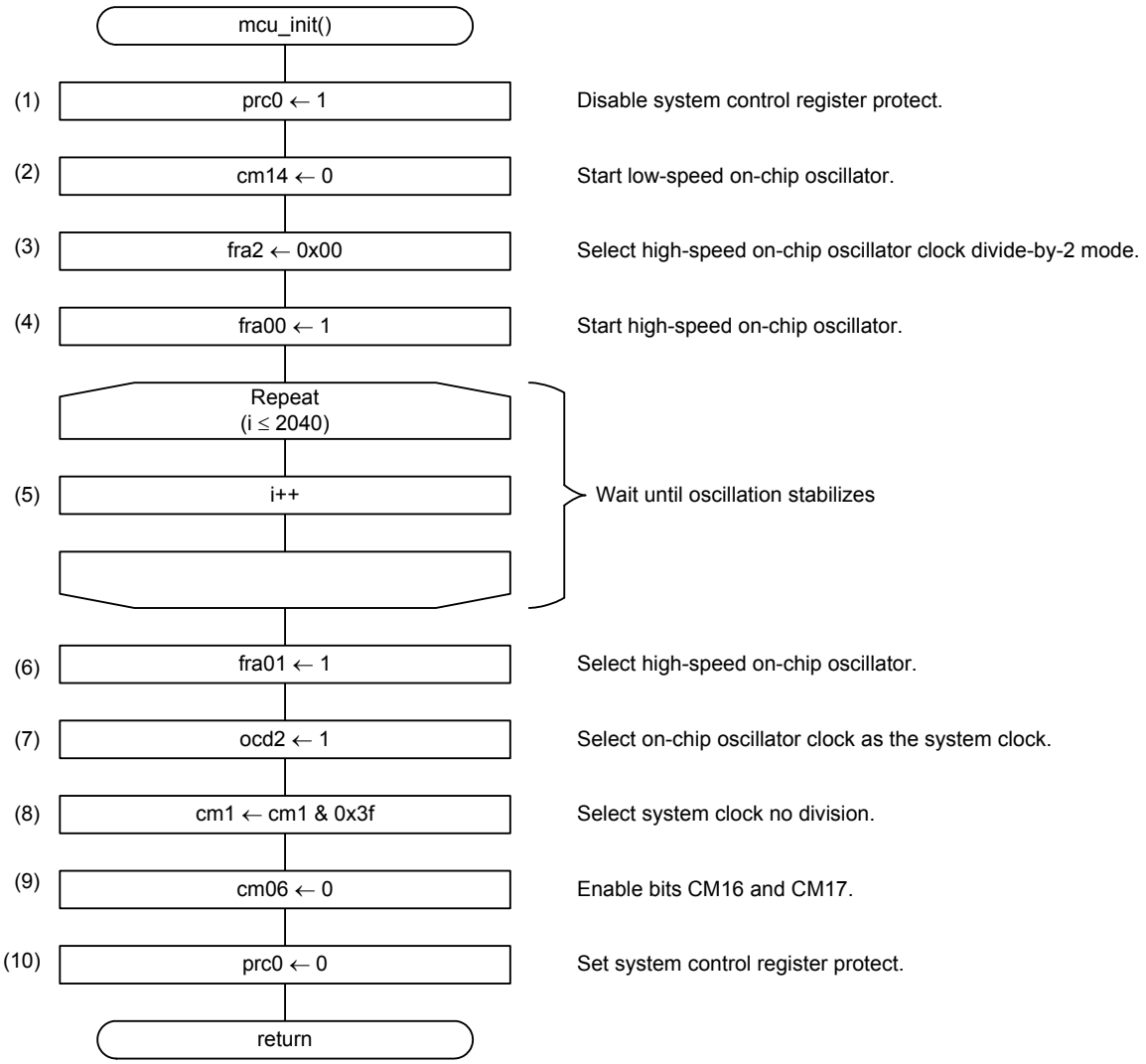
• Flowchart



Note:
1. In this application note, command sequence error processing, erase/blank check error processing, and program error processing are not performed. Perform error processing if necessary.

4.3 System Clock Setting

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Oscillate the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the division ratio for the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Oscillate the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the system clock as the on-chip oscillator clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	x	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10)Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

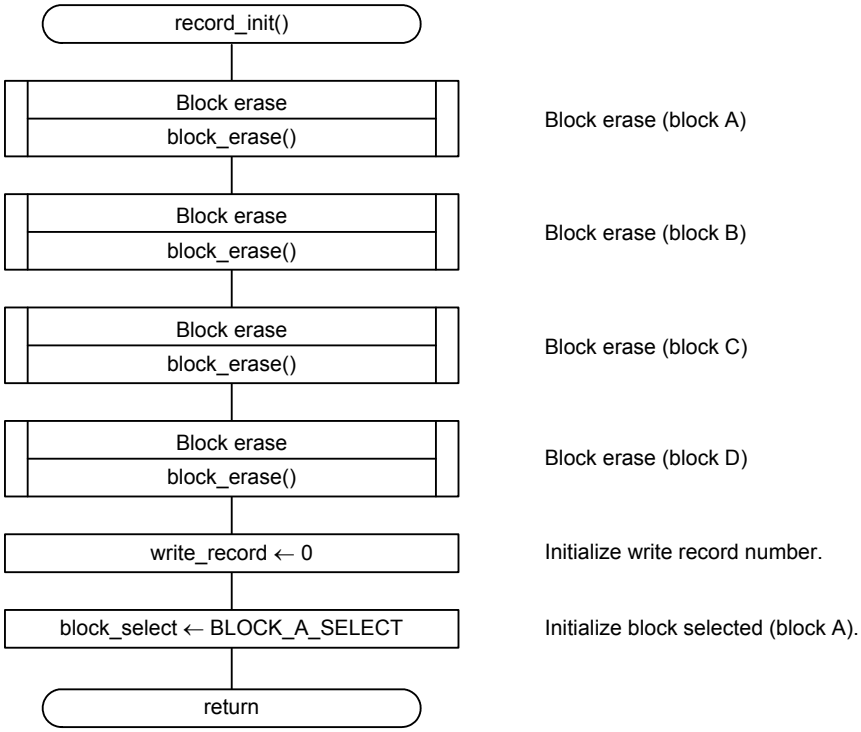
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

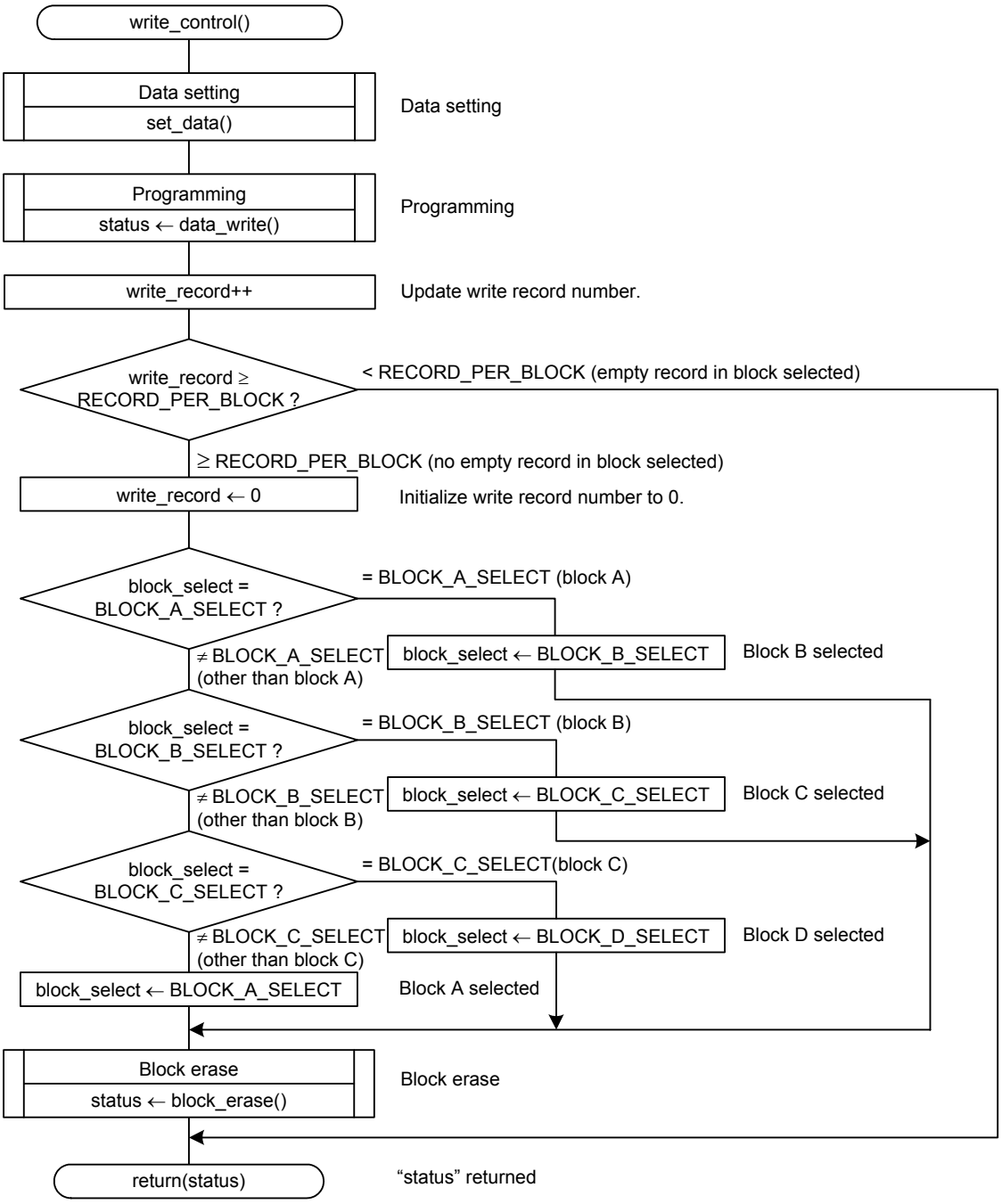
4.4 Write Record Initialization

• Flowchart



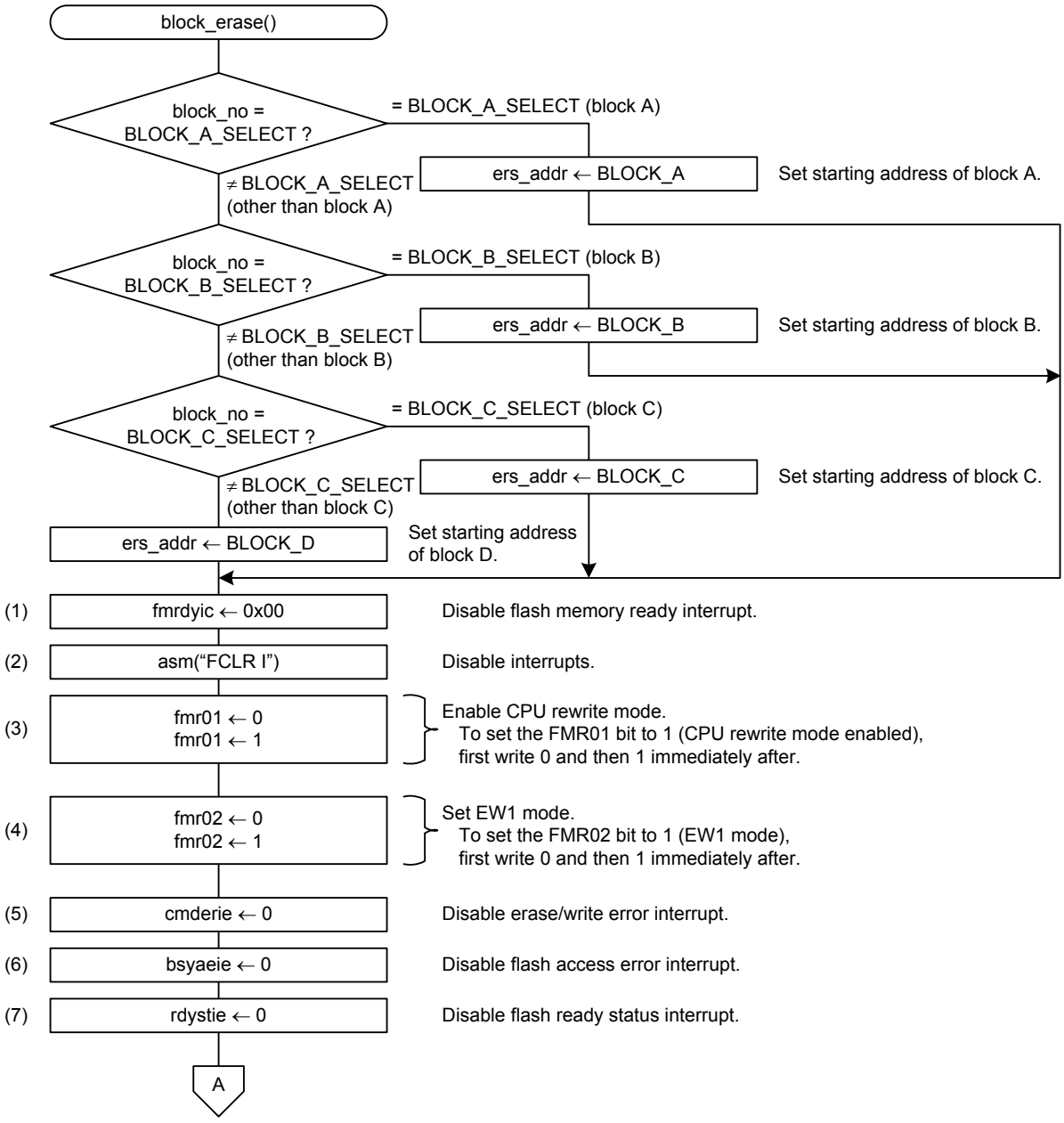
4.5 Data Write Control

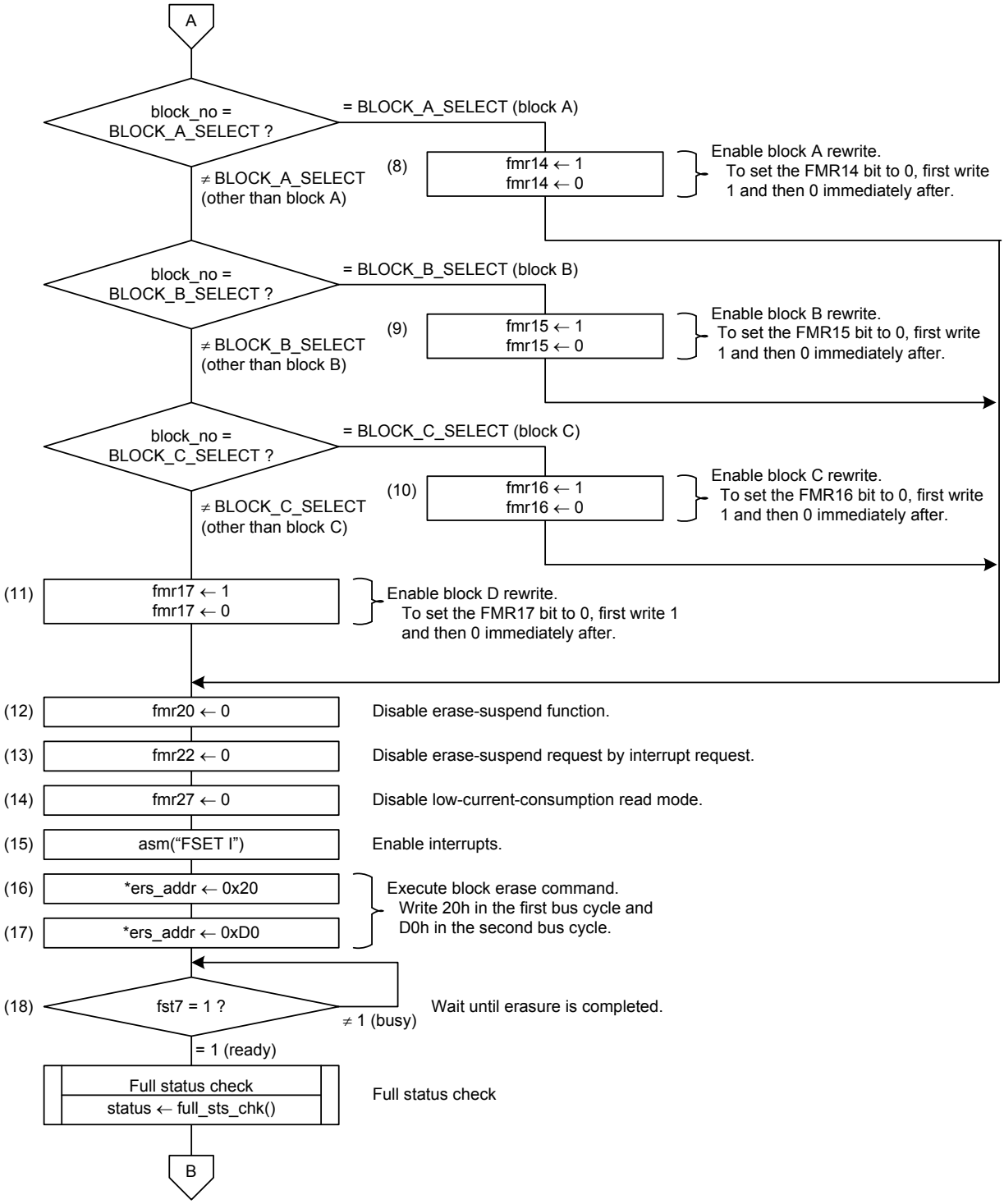
• Flowchart

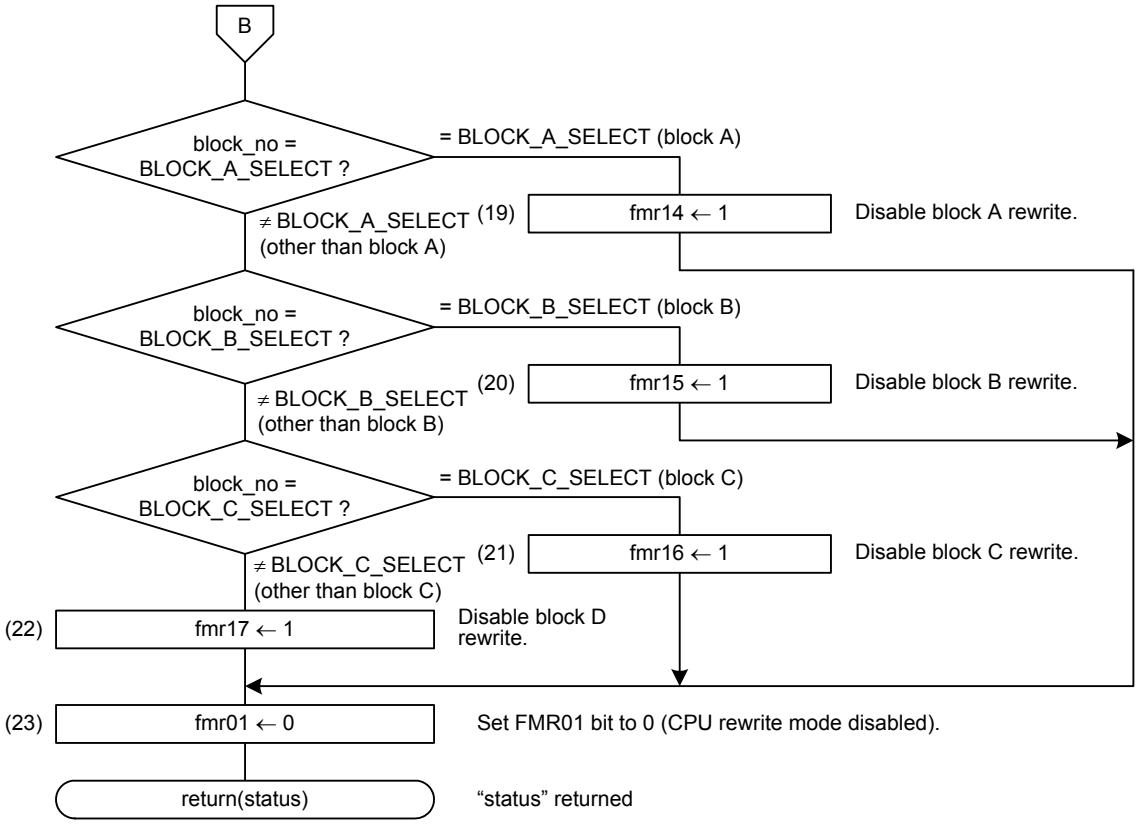


4.6 Block Erase

• Flowchart




A
block_no = BLOCK_A_SELECT ?
= BLOCK_A_SELECT (block A)
≠ BLOCK_A_SELECT (other than block A)
(8)
fmr14 ← 1
fmr14 ← 0
Enable block A rewrite.
To set the FMR14 bit to 0, first write 1 and then 0 immediately after.
block_no = BLOCK_B_SELECT ?
= BLOCK_B_SELECT (block B)
≠ BLOCK_B_SELECT (other than block B)
(9)
fmr15 ← 1
fmr15 ← 0
Enable block B rewrite.
To set the FMR15 bit to 0, first write 1 and then 0 immediately after.
block_no = BLOCK_C_SELECT ?
= BLOCK_C_SELECT (block C)
≠ BLOCK_C_SELECT (other than block C)
(10)
fmr16 ← 1
fmr16 ← 0
Enable block C rewrite.
To set the FMR16 bit to 0, first write 1 and then 0 immediately after.
(11)
fmr17 ← 1
fmr17 ← 0
Enable block D rewrite.
To set the FMR17 bit to 0, first write 1 and then 0 immediately after.
(12)
fmr20 ← 0
Disable erase-suspend function.
(13)
fmr22 ← 0
Disable erase-suspend request by interrupt request.
(14)
fmr27 ← 0
Disable low-current-consumption read mode.
(15)
asm("FSET I")
Enable interrupts.
(16)
*ers_addr ← 0x20
(17)
*ers_addr ← 0xD0
Execute block erase command.
Write 20h in the first bus cycle and D0h in the second bus cycle.
(18)
fst7 = 1 ?
≠ 1 (busy)
Wait until erasure is completed.
= 1 (ready)
Full status check
status ← full_sts_chk()
Full status check
B



• Register settings

(1) Disable the flash memory ready interrupt.

Flash Memory Ready Interrupt Control Register (FMRDYIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W

(2) Clear the I flag and disable interrupts.

(3) Enable CPU rewrite mode. To set this bit to 1, first write 0 and then 1 immediately.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x		1	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	1: CPU rewrite mode enabled	R/W

(4) Set to EW1 mode. To set this bit to 1, first write 0 and then 1 immediately.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x	1		—

Bit	Symbol	Bit Name	Function	R/W
b2	FMR02	EW1 mode select bit	1: EW1 mode	R/W

(5) Disable the erase/write error interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x			—

Bit	Symbol	Bit Name	Function	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled	R/W

(6) Disable the flash access error interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x			—

Bit	Symbol	Bit Name	Function	R/W
b2	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled	R/W

(7) Disable the flash ready status interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x			—

Bit	Symbol	Bit Name	Function	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled	R/W

(8) When erasing block A, enable the data flash block A rewrite disable bit. To set the FMR14 bit to 0, first write 1 and then 0 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				0	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b4	FMR14	Data flash block A rewrite disable bit	0: Rewrite enabled (software command acceptable)	R/W

(9) When erasing block B, enable the data flash block B rewrite disable bit. To set the FMR15 bit to 0, first write 1 and then 0 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0		x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	FMR15	Data flash block B rewrite disable bit	0: Rewrite enabled (software command acceptable)	R/W

(10) When erasing block C, enable the data flash block C rewrite disable bit. To set the FMR16 bit to 0, first write 1 and then 0 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0			x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	FMR16	Data flash block C rewrite disable bit	0: Rewrite enabled (software command acceptable)	R/W

(11) When erasing block D, enable the data flash block D rewrite disable bit. To set the FMR17 bit to 0, first write 1 and then 0 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0				x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	FMR17	Data flash block D rewrite disable bit	0: Rewrite enabled (software command acceptable)	R/W

(12) Disable the erase-suspend function.

Flash Memory Control Register 2 (FMR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		—	—	—	—		x	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit	0: Erase-suspend disabled	R/W

(13) Disable the erase-suspend request by interrupt request.

Flash Memory Control Register 2 (FMR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		—	—	—	—	0	x	

Bit	Symbol	Bit Name	Function	R/W
b2	FMR22	Interrupt request suspend request enable bit	0: Erase-suspend request disabled by interrupt request	R/W

(14) Disable low-current-consumption read mode.

Flash Memory Control Register 2 (FMR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	—	—	—		x	

Bit	Symbol	Bit Name	Function	R/W
b7	FMR27	Low-current-consumption read mode enable bit	0: Low-current-consumption read mode disabled	R/W

(15) Set the I flag and enable interrupts.

(16) Write block erase command 20h to a given address in the block to be erased in the first bus cycle.

(17) When writing confirmation command D0h in the second bus cycle, erasure (erase and erase verify) starts.

(18) Wait until erasure is completed.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

(19) When rewriting of block A is completed, disable the data flash block A rewrite disable bit.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				1	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b4	FMR14	Data flash block A rewrite disable bit	1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

(20) When rewriting of block B is completed, disable the data flash block B rewrite disable bit.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			1		x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	FMR15	Data flash block B rewrite disable bit	1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

(21) When rewriting of block C is completed, disable the data flash block C rewrite disable bit.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		1			x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	FMR16	Data flash block C rewrite disable bit	1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

(22) When rewriting of block D is completed, disable the data flash block D rewrite disable bit.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1				x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	FMR17	Data flash block D rewrite disable bit	1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

(23) Disable CPU rewrite mode.

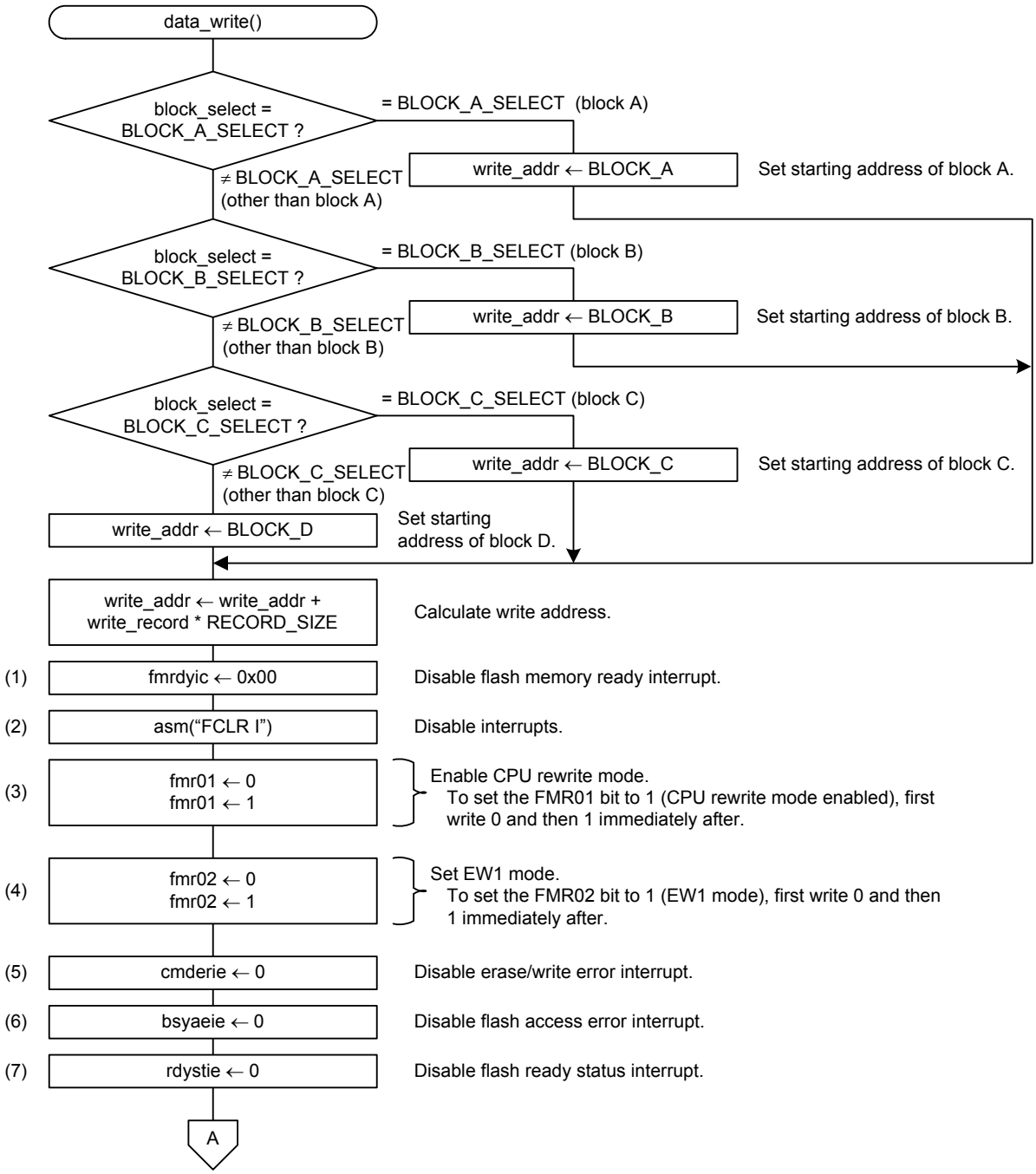
Flash Memory Control Register 0 (FMR0)

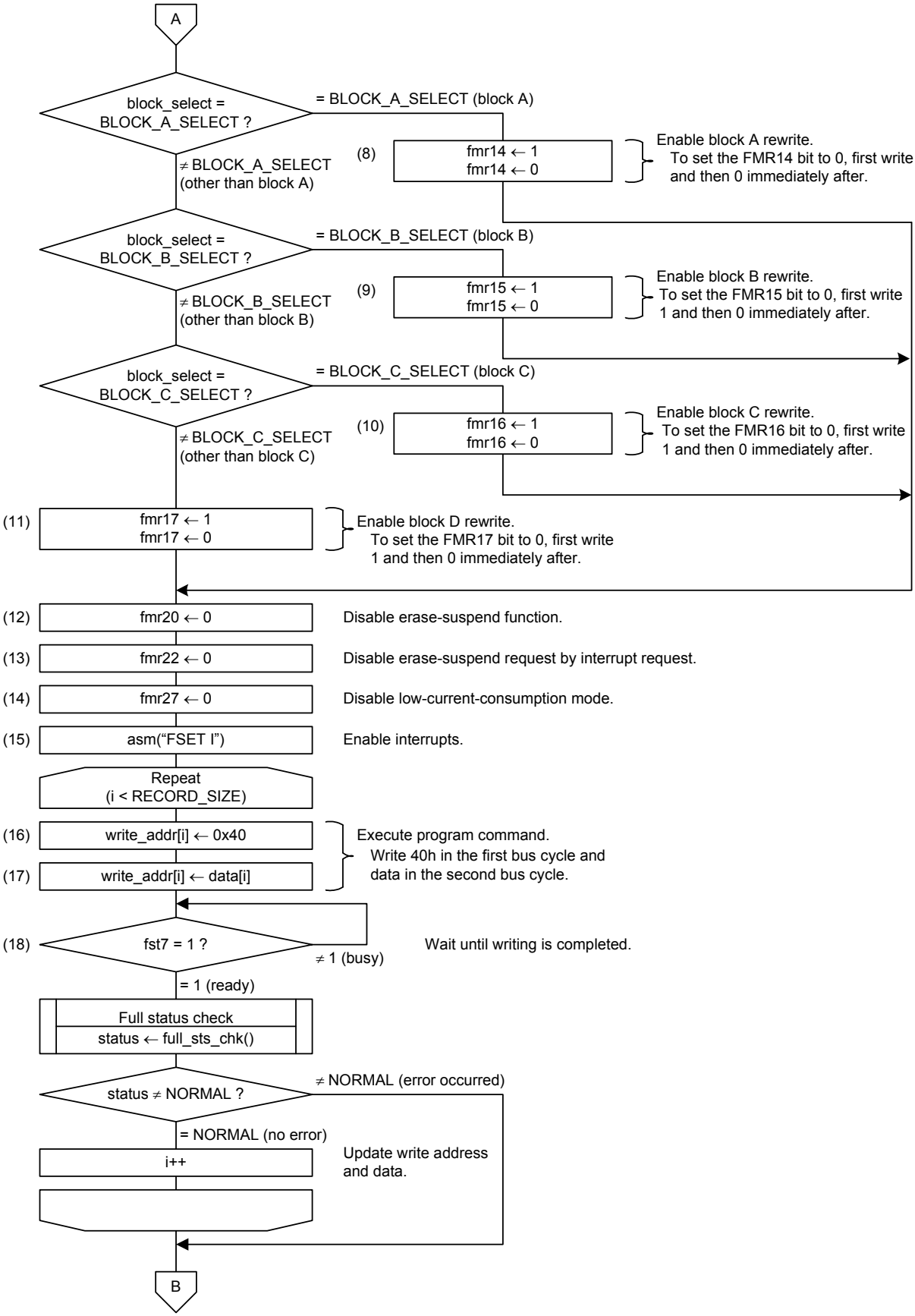
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x		0	—

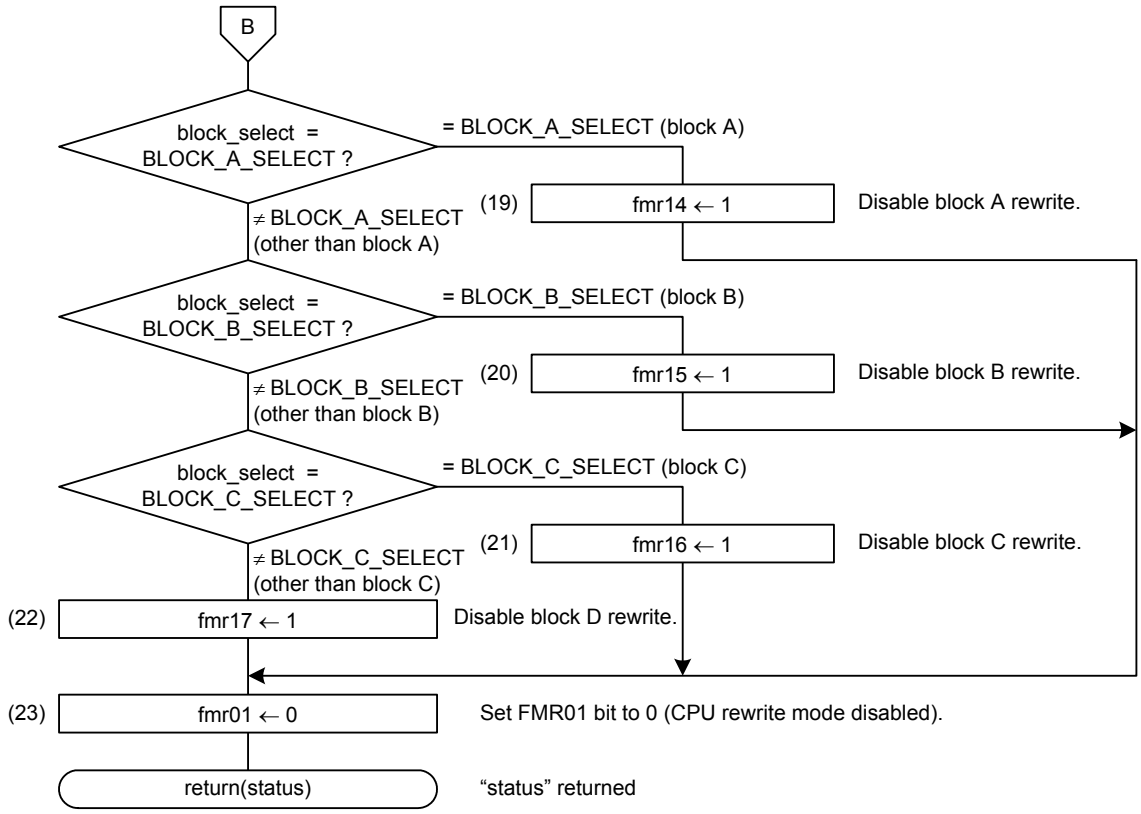
Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

4.7 Programming

• Flowchart




A
block_select = BLOCK_A_SELECT ?
= BLOCK_A_SELECT (block A)
≠ BLOCK_A_SELECT (other than block A)
(8)
fmr14 ← 1
fmr14 ← 0
Enable block A rewrite.
To set the FMR14 bit to 0, first write 1 and then 0 immediately after.
block_select = BLOCK_B_SELECT ?
= BLOCK_B_SELECT (block B)
≠ BLOCK_B_SELECT (other than block B)
(9)
fmr15 ← 1
fmr15 ← 0
Enable block B rewrite.
To set the FMR15 bit to 0, first write 1 and then 0 immediately after.
block_select = BLOCK_C_SELECT ?
= BLOCK_C_SELECT (block C)
≠ BLOCK_C_SELECT (other than block C)
(10)
fmr16 ← 1
fmr16 ← 0
Enable block C rewrite.
To set the FMR16 bit to 0, first write 1 and then 0 immediately after.
(11)
fmr17 ← 1
fmr17 ← 0
Enable block D rewrite.
To set the FMR17 bit to 0, first write 1 and then 0 immediately after.
(12)
fmr20 ← 0
Disable erase-suspend function.
(13)
fmr22 ← 0
Disable erase-suspend request by interrupt request.
(14)
fmr27 ← 0
Disable low-current-consumption mode.
(15)
asm("FSET I")
Enable interrupts.
Repeat
(i < RECORD_SIZE)
(16)
write_addr[i] ← 0x40
(17)
write_addr[i] ← data[i]
Execute program command.
Write 40h in the first bus cycle and data in the second bus cycle.
(18)
fst7 = 1 ?
≠ 1 (busy)
Wait until writing is completed.
= 1 (ready)
Full status check
status ← full_sts_chk()
status ≠ NORMAL ?
≠ NORMAL (error occurred)
= NORMAL (no error)
i++
Update write address and data.
B



• Register settings

(1) Disable the flash memory ready interrupt.

Flash Memory Ready Interrupt Control Register (FMRDYIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W

(2) Clear the I flag and disable interrupts.

(3) Enable CPU rewrite mode. To set the FMR01 bit to 1, first write 0 and then 1 immediately.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x		1	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	1: CPU rewrite mode enabled	R/W

(4) Set to EW1 mode. To set the FMR02 bit to 1, first write 0 and then 1 immediately.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x	1		—

Bit	Symbol	Bit Name	Function	R/W
b2	FMR02	EW1 mode select bit	1: EW1 mode	R/W

(5) Disable the erase/write error interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x			—

Bit	Symbol	Bit Name	Function	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled	R/W

(6) Disable the flash access error interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x			—

Bit	Symbol	Bit Name	Function	R/W
b2	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled	R/W

(7) Disable the flash ready status interrupt.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x			—

Bit	Symbol	Bit Name	Function	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled	R/W

(8) When rewriting block A, enable the data flash block A rewrite disable bit. To set the FMR14 bit to 0, first write 1 and then 0 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				0	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b4	FMR14	Data flash block A rewrite disable bit	0: Rewrite enabled (software command acceptable)	R/W

(9) When rewriting block B, enable the data flash block B rewrite disable bit. To set the FMR15 bit to 0, first write 1 and then 0 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0		x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	FMR15	Data flash block B rewrite disable bit	0: Rewrite enabled (software command acceptable)	R/W

(10) When rewriting block C, enable the data flash block C rewrite disable bit. To set the FMR16 bit to 0, first write 1 and then 0 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0			x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	FMR16	Data flash block C rewrite disable bit	0: Rewrite enabled (software command acceptable)	R/W

(11) When rewriting block D, enable the data flash block D rewrite disable bit. To set the FMR17 bit to 0, first write 1 and then 0 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0				x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	FMR17	Data flash block D rewrite disable bit	0: Rewrite enabled (software command acceptable)	R/W

(12) Disable the erase-suspend function.

Flash Memory Control Register 2 (FMR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		—	—	—	—		x	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit	0: Erase-suspend disabled	R/W

(13) Disable the erase-suspend request by interrupt request.

Flash Memory Control Register 2 (FMR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		—	—	—	—	0	x	

Bit	Symbol	Bit Name	Function	R/W
b2	FMR22	Interrupt request suspend request enable bit	0: Erase-suspend request disabled by interrupt request	R/W

(14) Disable low-current-consumption read mode.

Flash Memory Control Register 2 (FMR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	—	—	—		x	

Bit	Symbol	Bit Name	Function	R/W
b7	FMR27	Low-current-consumption read mode enable bit	0: Low-current-consumption read mode disabled	R/W

(15) Set the I flag and enable interrupts.

(16) Write program command 40h in the first bus cycle to the write address.

(17) When writing data in the second bus cycle, writing (data programmed and verified) starts. Set the same address value in the second bus cycle as the address value specified in the first bus cycle.

(18) Wait until writing is completed.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

(19) When rewriting of block A is completed, disable the data flash block A rewrite disable bit.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				1	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b4	FMR14	Data flash block A rewrite disable bit	1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

(20) When rewriting of block B is completed, disable the data flash block B rewrite disable bit.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			1		x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	FMR15	Data flash block B rewrite disable bit	1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

(21) When rewriting of block C is completed, disable the data flash block C rewrite disable bit.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		1			x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	FMR16	Data flash block C rewrite disable bit	1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

(22) When rewriting of block D is completed, disable the data flash block D rewrite disable bit.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1				x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b7	FMR17	Data flash block D rewrite disable bit	1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

(23) Disable CPU rewrite mode.

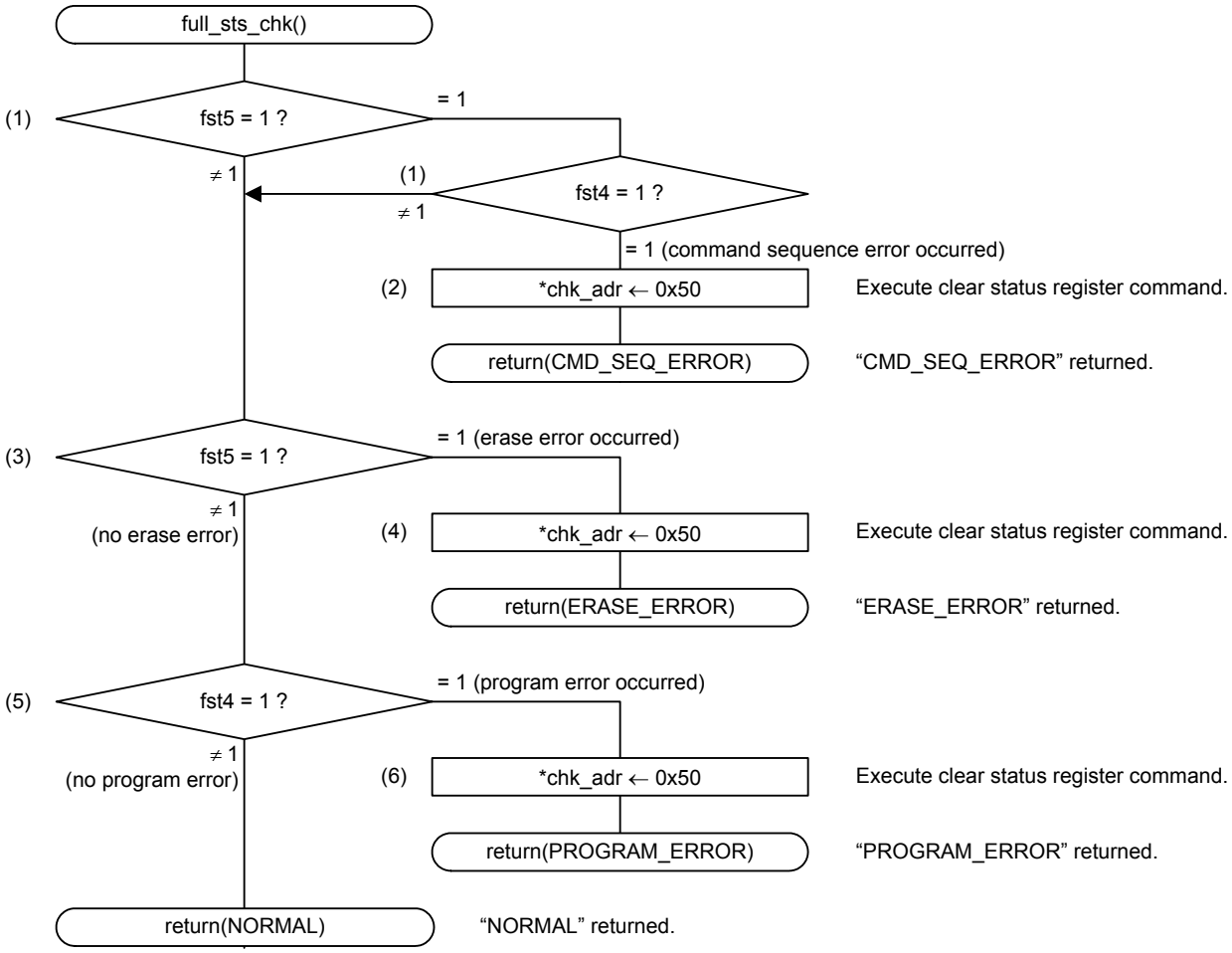
Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value				x	x		0	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

4.8 Full Status Check

• Flowchart



• Register settings

(1) Confirm that a command sequence error occurs by reading bits FST4 and FST5 in the FST register.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b4	FST4	Program error flag	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error flag	0: No erase error/blank check error 1: Erase error/blank check error	R

(2) Write clear status register command 50h to the address where erase command 20h or program command 40h was written when a program error (FST4 is 1) and an erase error (FST5 is 1) occur.

(3) Confirm that an erase error occurs by reading the FST5 bit in the FST register.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b5	FST5	Erase error/blank check error flag	0: No erase error/blank check error 1: Erase error/blank check error	R

(4) Write clear status register command 50h to the address where erase command 20h was written when an erase error (FST5 is 1) occurs.

(5) Confirm that a program error occurs by reading the FST4 bit in the FST register.

Flash Memory Status Register (FST)

Bit	Symbol	Bit Name	Function	R/W
b4	FST4	Program error flag	0: No program error 1: Program error	R

(6) Write clear status register command 50h to the address where program command 40h was written when a program error (FST4 is 1) occurs.

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/35C Group User’s Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	R8C/35C Group Rewriting the Data Flash

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 17, 2010	—	First edition issued
1.01	Dec. 20, 2010	3	Table 3.1 changed
		14, 18	4.6 process (19) deleted, subsequent numbers changed
		23, 27	4.7 process (19) deleted, subsequent numbers changed

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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