1. Abstract

This document describes the slave transmit/receive processes in \( \text{I}^2\text{C} \) bus interface slave communication using the R8C/35C Group serial interface (UART2) special mode 1 (I\(^2\)C mode). For details on UART2 special mode 1, refer to the M16C Family and R8C Family \( \text{I}^2\text{C} \) bus Interface Using UARTi Special Mode 1 application note.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/35C Group
- XIN Clock: 20 MHz

The simplified \( \text{I}^2\text{C} \) bus communication is enabled by controlling additional functions for \( \text{I}^2\text{C} \) bus communication added to the UARTi clock synchronous circuit for \( \text{I}^2\text{C} \) bus interface using UARTi special mode 1. The \( \text{I}^2\text{C} \) bus interface using UARTi special mode 1 has more limitations for software processing time and timing than the \( \text{I}^2\text{C} \) bus interface hardware module. Careful verification and evaluation of your system are recommended, including the interaction between the \( \text{I}^2\text{C} \) bus communication program and programs other than the \( \text{I}^2\text{C} \) bus communication program.
3. Application Example

3.1 Program Outline

I2C bus interface slave communication (slave transmission/reception) using the UART2 special mode 1 is processed in the application example. A maximum of 255 bytes of data can be transmitted/received. This transmission procedure conforms to the I2C bus communication protocol when used under the following conditions:

- Slave address: 7 bits
- Standard-mode and Fast-mode are supported
- Communication data length: 1 to 255 bytes (not including the slave address)
- Restart condition is not supported
- Single master/single slave communication

Figure 3.1 shows the Communication Format, Figure 3.2 shows the Block Diagram, Figure 3.3 shows the Outline Flowchart, and Figure 3.4 to Figure 3.6 show Timing Diagrams.
Figure 3.3 Outline Flowchart

1. Initial setting
2. UART2 receive interrupt
3. UART2 transmit interrupt
4. Stop condition detection interrupt
The numbers in Figure 3.3 correspond to the numbers indicated in the program processing in the operating timing charts in Figure 3.4 to Figure 3.6.

1. Initial setting
   Initialize the system clock, UART2 associated SFRs, and variables used.

2. UART2 receive interrupt
   When a slave address is received, a UART2 receive interrupt is generated at the falling edge of the eighth bit of the SCL clock. The slave address is determined after reading the U2RB register.
   When the slave address is matched:
   • Generate an ACK and set the SCL2 pin to low hold at the ninth bit.
   • Enable the stop condition detection interrupt and UART2 transmit interrupt. Disable the UART2 receive interrupt.
   • Set transmit/receive data to the U2TB register.
   When the slave address is not matched:
   • Generate a NACK.
   After the above processing, release SCL2 pin low hold at the eighth bit.

3. UART2 transmit interrupt
   A UART2 transmit interrupt is generated at the falling edge of the ninth bit of the SCL clock. When the first byte (slave address) is received, ACK output which set in the UART2 receive interrupt handling is released. When transmitting, determine the ACK/NACK and set the next byte transmit data. When receiving, store the receive data and set ACK for the next byte.

4. Stop condition detection interrupt
   When a stop condition is detected, an interrupt is generated. SFR values which changed in mid-communication are returned to the initial settings. Disable the stop condition detection interrupt and UART2 transmit interrupt. Enable the UART2 receive interrupt.

Note:
1. Write data to the U2TB register at slave transmit/receive according to the following procedure.
   • When receiving the first byte data (slave address):
     (1) Write the second byte data to the U2TB register in the receive interrupt handling.
     (2) Write the third byte data to the U2TB register in the transmit interrupt handling.
   • When receiving the second byte data onwards
     Each time a transmit interrupt handling occurs, write 1-byte data sequentially to the U2TB register starting with the fourth byte.
I2C bus Interface Using UART2 Special Mode 1
(Slave Transmit/Receive)

Figure 3.4 Slave Receive Timing

- SCL (master output)
- SDA (master output)
- SCL (slave output)
- SDA (slave output)
- SWC bit in the U2SMR2 register
- SWC9 bit in the U2SMR4 register
- Program processing
- Start condition
- Stop condition
- Slave address
- R/W
- ACK
- UART2 receive interrupt
- UART2 transmit interrupt
- Stop condition detection interrupt

1. Initial setting
2. UART2 receive interrupt
3. UART2 transmit interrupt
4. Stop condition detection interrupt

Automatically becomes 1 when the STAC bit in the U2SMR2 register is 1.
Set to 0 or 1 by a program.
I²C bus Interface Using UART2 Special Mode 1
(Slave Transmit/Receive)

Figure 3.5 Slave Transmit Timing (1)

Figure 3.6 Slave Transmit Timing (2)
3.1.1 Peripheral Functions

Serial interface (UART2) special mode 1 (I²C mode) is used under the following setting conditions:

- I²C mode is used.
- Transfer clock is external clock source.
- f½ used as U2BRG count source.
- SDA2 and SCL2 pins are N-channel open-drain output.
- Transfer format is MSB first.
- Transmission completed (TXEPT is 1) is selected as the UART2 transmit interrupt source.
- With clock delay.
- Seven to eight cycles of U2BRG count source is selected as SDA2 digital delay value.
- UART2 initial setting is used.
- Enable SCL2 wait output.
- Disable SCL2 wait output 2.
- Enable SCL2 wait output 3.
- SDA2 output disable function is used.
- Start condition detection interrupt is not used.
- Stop condition detection interrupt is used.
- UART2 transmit interrupt is used.
- UART2 receive interrupt is used.

<table>
<thead>
<tr>
<th>Table 3.1 Pins Used and Their Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin</td>
</tr>
<tr>
<td>P3_4/SCL2</td>
</tr>
<tr>
<td>P3_7/SDA2</td>
</tr>
</tbody>
</table>

3.1.2 Notes on Using the Attached Sample Program

Note the following when using the program included with this application note:

(1) Do not use multiple interrupts.

(2) The size of the receive buffer and the transmit buffer are set to 255 bytes. The buffer size is defined by the BUFSIZE macro (1 to 255 bytes). When the number of transmit/receive bytes exceeds the size of the buffer, the slave disregards the communication. Disable the UART2 transmit interrupt, and release pins SCL2 and SDA2.

(3) After the master generates a stop condition, when the slave processing time (1) has passed, start the next transmit/receive (start condition is generated).

Note:

1. The slave processing time indicates the time between detecting a stop condition and enabling I²C mode in the main processing, and is dependent on the processing of the user program. The maximum processing time for this sample program is approximately 500 μs.
3.2 Memory

Table 3.2 Memory

<table>
<thead>
<tr>
<th>Memory</th>
<th>Size</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM</td>
<td>694 bytes</td>
<td>In the iic.c module</td>
</tr>
<tr>
<td>RAM</td>
<td>4 bytes</td>
<td>In the iic.c module</td>
</tr>
<tr>
<td>Maximum user stack</td>
<td>21 bytes</td>
<td></td>
</tr>
<tr>
<td>Maximum interrupt stack</td>
<td>27 bytes</td>
<td></td>
</tr>
</tbody>
</table>

Usage memory size varies depending on C compiler version and compile options. The above applies under the following conditions:
C compiler: M16C Series, R8C Family Compiler V.5.45 Release 01
C compile options: -c -info -dir "$(CONFIGDIR)" -R8C
4. Software

This section shows the program example to set the example described in section 3. Application Example. Refer to the latest R8C/35C Group hardware user’s manual for details on individual registers.

4.1 Usage Variables

Definition file name: rej05b1351_src.c

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_tx[BUFSIZE]</td>
<td>255 bytes</td>
<td>Transmit buffer</td>
</tr>
<tr>
<td>unsigned char iic_rx[BUFSIZE]</td>
<td>255 bytes</td>
<td>Receive buffer</td>
</tr>
<tr>
<td>unsigned char rcv_data[BUFSIZE]</td>
<td>255 bytes</td>
<td>Store to receive data read from receive buffer</td>
</tr>
</tbody>
</table>

Definition file name: iic.c

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>Size/Bit-number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>static byte_dt iic_str</td>
<td>-</td>
<td>Structure to store status</td>
</tr>
<tr>
<td></td>
<td>iic_status</td>
<td>1 byte All statuses</td>
</tr>
<tr>
<td></td>
<td>iic_rw</td>
<td>b0 R/W flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Write (W) slave receive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Read (R) slave transmit</td>
</tr>
<tr>
<td></td>
<td>iic_buf_full</td>
<td>b1 Buffer full flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Within buffer size</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Buffer full</td>
</tr>
<tr>
<td></td>
<td>iic_end</td>
<td>b2 Communication completed flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Busy (mid-communication)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Ready (except for mid-communication)</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>b7 to b3 Not used (undefined)</td>
</tr>
<tr>
<td>static unsigned char far* iic_pointer</td>
<td>2 bytes</td>
<td>Transmit/receive buffer pointer</td>
</tr>
<tr>
<td>static unsigned char iic_index</td>
<td>1 byte</td>
<td>Number of transmit/receive bytes</td>
</tr>
</tbody>
</table>
### 4.2 Function Tables

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void main (void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>Main processing</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>unsigned char iic_tx[BUFSIZE]</td>
</tr>
<tr>
<td></td>
<td>unsigned char iic_rx[BUFSIZE]</td>
</tr>
<tr>
<td></td>
<td>unsigned char rcv_data[BUFSIZE]</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Function</td>
<td>After setting the system clock, I²C mode is enabled. Communication status is determined by the returned value of the iic_slave_end function. Each status is processed after communication is completed, and the uart2_init function is called to enable I²C mode.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void mcu_init (void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>System clock setting processing</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Function</td>
<td>Called from main function. Perform system clock (XIN clock) setting.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void uart2_init (unsigned char ini)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>UART2 initial setting</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>unsigned char ini</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>(structure member) iic_status</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Function</td>
<td>Called from main function. Initialize SFR to use UART2 special mode 1 (I²C mode). When I²C mode is enabled, set iic_status to 0x00 (clear all statuses). When executing this function, interrupts are disabled by the I flag.</td>
</tr>
</tbody>
</table>
### I2C Bus Interface Using UART2 Special Mode 1 (Slave Transmit/Receive)

#### Declaration

**void _uart2_bcnic (void)**

**Outline**
Stop condition detection interrupt handling

<table>
<thead>
<tr>
<th>Argument</th>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td></td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable (global)</th>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td></td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Returned value</th>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Function**
An interrupt occurs when a stop condition is detected, and the stp_int function is called.

---

#### Declaration

**static void stp_init (void)**

**Outline**
Stop condition detection processing

<table>
<thead>
<tr>
<th>Argument</th>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td></td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable (global)</th>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>icc_end</td>
<td>Communication completed flag</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Returned value</th>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Function**
Called from stop condition detection interrupt handling. UART2 related SFR values changed mid-communication are returned to their initial values, and the communication completed flag is set to 1.

---

#### Declaration

**void _uart2_receive (void)**

**Outline**
UART2 receive interrupt handling

<table>
<thead>
<tr>
<th>Argument</th>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td></td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable (global)</th>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>icc_pointer</td>
<td>Transmit/receive buffer pointer</td>
<td></td>
</tr>
<tr>
<td>icc_index</td>
<td>Number of transmit/receive bytes</td>
<td></td>
</tr>
<tr>
<td>icc_status</td>
<td>All statuses</td>
<td></td>
</tr>
<tr>
<td>icc_rw</td>
<td>R/W flag</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Returned value</th>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Function**
An interrupt occurs at the falling edge of the eighth bit of the SCL clock. This function calls the iic_id_check function after reading the U2RB register in the function header.

- When the slave address is matched, generate an ACK, and set the SCL2 pin to low hold at the ninth bit. The receive interrupt is disabled, and the transmit interrupt and stop condition detection interrupt are enabled. The number of transmit/receive bytes and all statuses are cleared. When the slave is receiving, set the ACK for the next byte. When the slave is transmitting, set transmit data for the next byte.
- When the slave address is not matched, generate a NACK.

After the above processing, release SCL2 pin low hold.
### I2C bus Interface Using UART2 Special Mode 1

#### Slave Transmit/Receive

**Declaration**

```c
unsigned char* iic_id_check (unsigned char id, unsigned char rw)
```

**Outline**

Slave address determine processing

**Argument**

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char id</td>
<td>Received slave address</td>
</tr>
<tr>
<td>unsigned char rw</td>
<td>R/W flag</td>
</tr>
</tbody>
</table>

**Variable (global)**

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

**Returned value**

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char*</td>
<td>iic_rx</td>
<td>Receive buffer address</td>
</tr>
<tr>
<td></td>
<td>iic_tx</td>
<td>Transmit buffer address</td>
</tr>
<tr>
<td></td>
<td>NULL</td>
<td>Slave address does not match</td>
</tr>
</tbody>
</table>

**Function**

Called from UART2 receive interrupt handling. Received slave address is determined. When the slave address is matched, the returned value is the buffer address. When the slave address is not matched, the returned value is NULL.

---

**Declaration**

```c
void _uart2_trans (void)
```

**Outline**

UART2 transmit interrupt handling

**Argument**

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

**Variable (global)**

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>(structure member) iic_rw</th>
<th>R/W flag</th>
</tr>
</thead>
</table>

**Returned value**

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Function**

An interrupt occurs at the falling edge of the ninth bit of the SCL clock. The U2RB register is read in the function header. When the first byte (slave address) is received, disable ACK output set by the receive interrupt handler. After the first byte is received, the slave_rcv_int function is called when the slave is receiving and the slave_trn_int function is called when the slave is transmitting.
### Declaration

```
static void slave_rcv_int (unsigned char rb_data)
```

### Outline

Slave receive processing

<table>
<thead>
<tr>
<th>Argument</th>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>unsigned char rb_data</td>
<td>Receive data read from the U2RB register</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable (global)</th>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td></td>
<td>unsigned char far* iic_pointer</td>
<td>Transmit/receive buffer pointer</td>
</tr>
<tr>
<td></td>
<td>(structure member) iic_buf_full</td>
<td>Buffer full flag</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Returned value</th>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Function

Called from UART2 transmit interrupt handling.

- The argument value is stored in the receive buffer (except the slave address).
  - When the number of received bytes is less than the buffer size, set an ACK for the next byte. Release SCL2 pin low hold, then set the SCL2 pin to low hold for the next byte.
  - When the number of received bytes is the same as or greater than the buffer size, the buffer full flag is set to 1. Release pins SCL2 and SDA2, and disable the UART2 transmit interrupt.

---

### Declaration

```
static void slave_trn_int (unsigned char rb_data)
```

### Outline

Slave transmit processing

<table>
<thead>
<tr>
<th>Argument</th>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>unsigned char rb_data</td>
<td>ACK/NACK read from the U2RB register</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable (global)</th>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td></td>
<td>unsigned char far* iic_pointer</td>
<td>Transmit/receive buffer pointer</td>
</tr>
<tr>
<td></td>
<td>(structure member) iic_buf_full</td>
<td>Buffer full flag</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Returned value</th>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Function

Called from UART2 transmit interrupt handling.

- When an ACK is detected and the number of transmit bytes is less than the buffer size, set transmit data for the next byte. Release SCL2 pin low hold, then set the SCL2 pin to low hold for the next byte.
- When the number of transmit bytes is the same as or greater than the buffer size, set the buffer full flag to 1. Release pins SCL2 and SDA2, and disable the UART2 transmit interrupt.
- When NACK is detected, release pins SCL2 and SDA2, and disable the UART2 transmit interrupt.
<table>
<thead>
<tr>
<th>Declaration</th>
<th>unsigned short iic_slave_end (void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>Slave control completed processing</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td>(structure member) iic_end</td>
<td>Communication completed flag</td>
</tr>
<tr>
<td>(structure member) iic_rw</td>
<td>R/W flag</td>
</tr>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>unsigned short</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Lower byte</td>
</tr>
<tr>
<td>Function</td>
<td>Called from the main processing. It informs the user of the state of slave control completion. When the communication completed flag is 1 and there is transmit/receive data except for the slave address, disable I2C mode. Otherwise, return IIC_BUSY (mid-communication). After disabling I2C mode, when the communication completed flag is 0, the next communication is determined to be started and the IIC_ERR (overrun error detection) function is returned. When the communication completed flag is 1, return IIC_REND (reception completed) or IIC_TEND (transmission completed).</td>
</tr>
</tbody>
</table>
4.3 Main Processing

```
main()
asm("FCLR I")
System clock initial setting
mcu_init()
asm("FSET I")
loop
    i = 0; i < BUFSIZE; i++
    iic_tx[i] ← i+1
    iic_rx[i] ← 0x00
loop
UART2 initial setting
uart2_init()
UART2 special mode 1 (I2C mode) enabled
Slave control complete processing
iic_slave_end()
temp.all ← returned value
temp.byte.byte0
Read receive buffer (1)
UART2 initial setting
uart2_init()
UART2 special mode 1 (I2C mode) enabled
```

Note:
1. Additional processing can be added as needed.
### 4.4 System Clock Setting

```
cmcu_init()
pro0 ← 1

| cm14 ← 0        | Disable system control register protect. |
| cm13 ← 1        | Start low-speed on-chip oscillator.      |
| cm05 ← 0        | Select XIN-XOUT pin for port/XIN-XOUT switch. |

loop
i <= 2040
i++

| cm07 ← 0        | Oscillate XIN clock.                     |
| cm14 ← 1        | Wait until oscillation stabilizes.       |

| cm06 ← 0        | Select XIN clock.                        |
| cm1 ← cm1 & 0x3F | Select XIN clock as the system clock.    |

| cm14 ← 1        | Select CPU clock no division.            |
| pro0 ← 0        | Enable bits CM16 and CM17.               |
| cm05 ← 0        | Stop low-speed on-chip oscillator.       |
| pro0 ← 0        | Set system control register protect.     |
```

```
| prc0 ← prc0 & 0x01 | Oscillate XIN clock.                     |
| cm06 ← 0          | Select XIN clock.                        |
| cm05 ← 0          | Select XIN-XOUT pin for port/XIN-XOUT switch. |

```

return
```
4.5 UART2 Initial Setting

```c
uart2_init()

asm("FCLR I")

ini = 1 ?

= 1 (I²C mode disabled)

---

ini = 1 (I²C mode enabled)

u2sr0 ← 0x01

Select I²C mode.

u2mr ← 0x08

Select serial interface.

nch_u2c0 ← 1

Set pins SDA2 and SCL2 as N-channel open-drain output.

P_IIC ← P_IIC | P_IIC_INIT

Set initial value: P3_7 (SDA2) = P3_4 (SCL2) = 1 (high)

PD_IIC ← PD_IIC & PD_IIC_INIT

Set port direction: PD3_7 (SDA2) = PD3_4 (SCL2) = 0 (input mode)

u2sr0 ← 0x11

Assign SDA2 to P3_7.

u2sr1 ← 0x00

Assign SCL2 to P3_4.

Initialize U2SR1 register.

u2bcnic ← 0x00

Disable stop condition detection interrupt.

s2tic ← 0x00

Disable UART2 transmit interrupt.

s2ric ← 0x00

Disable UART2 receive interrupt.

u2c1 ← 0x00

Select transmission/reception.

u2mr ← 0x0A

Select I²C mode.

u2smr2 ← 0x11

Select UART2 transmit interrupt/UART2 receive interrupt.

Enable UART2 initialization.

u2smr3 ← 0xE2

Select clock phase with delay.

u2smr4 ← 0x30

Select seven to eight cycles of U2BRG count source as SDA2 digital delay.

Enable NACK output.

u2c0 ← 0xB0

Select f1 as U2BRG count source.

Set N-channel open-drain output for pins SDA2 and SCL2.

Select MSB first as transfer format.

u2c1 ← 0x10

Disable transmission/reception.

Set IR bit to 0.

s2tic ← 0x00

Enable UART2 receive interrupt.

s2ric ← 0x01

Clear all status flags.

iic_status ← 0x00

Enable transmission/reception.

asm("FSET I")

Enable interrupts.

return

---

u2c1 ← 0x00

Disable transmission/reception.

u2sr0 ← 0x00

Set port direction: PD3_7 (SDA2) = PD3_4 (SCL2) = 0 (input mode)

Do not use pins SDA2 and SCL2.

Initialize U2SR1 register.

u2bcnic ← 0x00

Disable stop condition detection interrupt.

s2tic ← 0x00

Disable UART2 transmit interrupt.

s2ric ← 0x00

Disable UART2 receive interrupt.

u2smr2 ← 0x00

Disable UART2 initialization.

u2mr ← 0x00

Disable serial interface.

---

asm("FCLR I")

Disable interrupts.

asm("FSET I")

Enable interrupts.

iic_status ← 0x00

Clear all status flags.

u2c1 ← 0x15

Enable transmission/reception.

asm("FSET I")

Enable interrupts.
```

---

Do not use pins SDA2 and SCL2.

Set IR bit to 0.

Enable UART2 receive interrupt.

Clear all status flags.

Enable transmission/reception.

Enable interrupts.

---

Set initial value: P3_7 (SDA2) = P3_4 (SCL2) = 1 (high)

Set port direction: PD3_7 (SDA2) = PD3_4 (SCL2) = 0 (input mode)

Assign SDA2 to P3_7.

Assign SCL2 to P3_4.

Initialize U2SR1 register.

Disable transmission/reception.

Set port direction: PD3_7 (SDA2) = PD3_4 (SCL2) = 0 (input mode)

Do not use pins SDA2 and SCL2.

Initialize U2SR1 register.

Disable stop condition detection interrupt.

Disable UART2 transmit interrupt.

Disable UART2 receive interrupt.

Disable UART2 initialization.

Disable serial interface.

---

Set initial value: P3_7 (SDA2) = P3_4 (SCL2) = 1 (high)

Set port direction: PD3_7 (SDA2) = PD3_4 (SCL2) = 0 (input mode)

Do not use pins SDA2 and SCL2.

Initialize U2SR1 register.

Disable stop condition detection interrupt.

Disable UART2 transmit interrupt.

Disable UART2 receive interrupt.

Disable UART2 initialization.

Disable serial interface.

---

Select I²C mode.

Select external clock.

Set pins SDA2 and SCL2 as N-channel open-drain output.

Set initial value: P3_7 (SDA2) = P3_4 (SCL2) = 1 (high)

Set port direction: PD3_7 (SDA2) = PD3_4 (SCL2) = 0 (input mode)

Assign SDA2 to P3_7.

Assign SCL2 to P3_4.

Initialize U2SR1 register.

Disable stop condition detection interrupt.

Disable UART2 transmit interrupt.

Disable UART2 receive interrupt.

Select I²C mode.

Select external clock.

Select UART2 transmit interrupt/UART2 receive interrupt.

Enable UART2 initialization.

Select clock phase with delay.

Select seven to eight cycles of U2BRG count source as SDA2 digital delay.

Enable NACK output.

Select f1 as U2BRG count source.

Set N-channel open-drain output for pins SDA2 and SCL2.

Select MSB first as transfer format.

Disable transmission/reception.

Set IR bit to 0.

Enable UART2 receive interrupt.

Clear all status flags.

Enable transmission/reception.

Enable interrupts.
4.6 Stop Condition Detection Interrupt Handling

```
_uart2_bcnic()

bbs = 0 ?

= 0 (start condition detected (busy))

= 0 (stop condition detected)

Stop condition detection processing

stp_int()

return
```

4.7 Stop Condition Detection Processing

```
stp_int()

u2c1 ← 0x10

P_IIC ← P_IIC | P_IIC_INIT

u2mr ← 0x00

Disable transmission/reception.

Set initial value: P3_7 (SDA2) = P3_4 (SCL2) = 1 (high)

Disable serial interface.

u2smr4 ← 0x30

Output NACK (release SDA2 pin).

Select I2C mode.

Select external clock.

u2smr2 ← 0x11

Select UART2 transmit interrupt/UART2 receive interrupt.

u2bcnic ← 0x00

Disable stop condition detection interrupt.

s2tic ← 0x00

Disable UART2 transmit interrupt.

s2ric ← 0x01

Enable UART2 receive interrupt.

iic_end ← 1

Set communication completed flag to 1.

u2c1 ← 0x15

Enable transmission/reception.

return
```
4.8 UART2 Receive Interrupt Handling

```plaintext
_uart2_receive()

temp.all ← u2rb

Slave address determine processing
iic_id_check()
iic_pointer ← returned value

(iicc address not match)
iic_pointer = NULL ?

≠ NULL (slave address match)

u2smr4 ← 0xa0

Wait until SDA2 pin is released
s2ic ← (s2ic | 0x01) & 0x0f

Enable UART2 transmit interrupt.
s2ric ← 0x00

Disabled UART2 receive interrupt.
u2bcnic ← 0x01

Enable stop condition detection interrupt.
iic_index ← 0

Clear number of transmit/receive bytes.
iic_status ← 0x00

Clear all status flags.
iic_rw ← temp.bit.b8

Set R/W (1: Read; 0: Write)
iic_rw = 0 ?

≠ 0 (slave transmit)
temp.byte.byte0 ← *iic_pointer

temp.byte.byte1 ← 0x01

Set transmit data for next byte.
iic_pointer++
u2tb ← temp.all

u2smr2 ← 0x11

Release SCL2 pin low hold.

≠ 0 (slave receive)
temp.byte.byte0 ← *iic_pointer

temp.byte.byte1 ← 0x01

Set transmit data for next byte.

u2tb ← 0x00FF

Set ACK for next byte.

Generate ACK and set SCL2 pin to low hold at ninth bit.

U2BRG count source × wait more than SDA2 digital delay time

Wait until SDA2 pin is released

Enable UART2 transmit interrupt.

Disable UART2 receive interrupt.

Enable stop condition detection interrupt.

Set R/W (1: Read; 0: Write)

Clear all status flags.

Increment transmit buffer pointer.

Set transmit data to U2TB register (transmission starts).
```

Read U2RB register.
4.9 Slave Address Determine Processing

```
(i & 0x7F) = DEVICE_ADDRESS ?

DEVICE_ADDRESS (slave address not match)

= DEVICE_ADDRESS (slave address match)

(rw & 0x01) = 0x00 ?

DEVICE_ADDRESS (slave transmit)

= 0x00 (slave receive)

return(iic_rx)

return(iic_tx)

return(NULL)
```

4.10 UART2 Transmit Interrupt Handling

```
_iic_id_check()

return(NULL)

(id & 0x7F) = DEVICE_ADDRESS ?

DEVICE_ADDRESS (slave address not match)

DEVICE_ADDRESS (slave address match)

(rw & 0x01) = 0x00 ?

DEVICE_ADDRESS (slave address match)

= 0x00 (slave transmit)

= 0x00 (slave receive)

return(iic_rx)

_temp.all ← u2rb

Read UART2 receive buffer register.

= 0 (from the second byte on)

_iic_index = 0 ?

= 0 (first byte (slave address))

ackc ← 0

Disable ACK output.

Wait until SDA2 pin is released \(^{(1)}\)

_iic_rw = 0 ?

= 0 (slave transmit)

= 0 (slave receive)

Slave receive processing

slave_rcv_int()

return

Slave transmit processing

slave_trn_int()

return

Note:

1. U2BRG count source × wait more than SDA2 digital delay time

Wait until SDA2 pin is released \(^{(1)}\)

\(^{(1)}\) \(1\)
4.11 Slave Receive Processing

```
slave_rcv_int()

iic_index < BUFSIZE ?

≥ BUFSIZE (buffer size or greater)

< BUFSIZE (less than buffer size)

iic_index = 0 ?

= 0 (first byte (slave address))

≠ 0 (from the second byte on)

*iic_pointer ← rb_data

Increment receive buffer pointer.

iic_index++

Increment number of transmit/receive bytes.

u2tb ← 0x00FF

Set ACK for next byte.

swc9 ← 0

Release SCL2 pin low hold.

swc9 ← 1

Set SCL2 pin to low hold for next byte.

*iic_pointer ← rb_data

iic_buf_full ← 1

u2smr4 ← 0xb0

Wait until SDA2 pin is released \(^1\)

Release SDA2 pin.

Release SCL2 pin.

Disable UART2 transmit interrupt.
```

Note:
1. U2BRG count source \times wait more than SDA2 digital delay time
### 4.12 Slave Transmit Processing

- **slave_tm_int()**
  - **iic_index** >= BUFSIZE (buffer size or greater)
    - return
  - **iic_index** < BUFSIZE (less than buffer size)
    - **rb_data & 0x01** = 0x00 (NACK detected)
      - **iic_index** >= (BUFSIZE-1)
        - **iic_index** < (BUFSIZE-1)
          - temp.byte.byte0 ← *iic_pointer
            - Set next byte transmit data.
          - temp.byte.byte1 ← 0x01
            - Set data to release SDA2 pin at ninth bit.
          - **iic_pointer++**
            - Increment transmit buffer pointer.
      - **u2tb ← temp.all**
        - Set transmit data to U2TB register (transmission starts).
      - Wait until SDA2 pin is released (1)
        - **iic_index++**
          - Increment number of transmit/receive bytes.
        - **swc9 ← 0**
          - Release SCL2 pin low hold.
        - **swc9 ← 1**
          - Set SCL2 pin to low hold for next byte.
      - **iic_index++**
        - Increment number of transmit/receive bytes.
      - **u2smr4 ← 0xb0**
        - Release SDA2 pin.
      - Wait until SDA2 pin is released (1)
        - **u2smr4 ← 0x30**
          - Release SCL2 pin.
        - **s2tic ← 0x00**
          - Disable UART2 transmit interrupt.
    - = 0x00 (ACK detected)
      - **iic_index++**
        - Increment number of transmit/receive bytes.
      - **u2smr4 ← 0xb0**
        - Release SDA2 pin.
      - Wait until SDA2 pin is released (1)
        - **u2smr4 ← 0x30**
          - Release SCL2 pin.
        - **s2tic ← 0x00**
          - Disable UART2 transmit interrupt.
    - **iic_buf_full ← 1**
      - Set buffer full flag to 1.
      - **u2smr4 ← 0xb0**
        - Release SDA2 pin.
      - Wait until SDA2 pin is released (1)
        - **u2smr4 ← 0x30**
          - Release SCL2 pin.
        - **s2tic ← 0x00**
          - Disable UART2 transmit interrupt.
  - **rb_data & 0x01** = 0x00 (NACK detected)
    - **iic_index** < (BUFSIZE-1)
      - temp.buffer.byte0 ← *iic_pointer
        - Set next byte transmit data.
      - temp.buffer.byte1 ← 0x01
        - Set data to release SDA2 pin at ninth bit.
      - **iic_pointer++**
        - Increment transmit buffer pointer.
      - **u2tb ← temp.all**
        - Set transmit data to U2TB register (transmission starts).
      - Wait until SDA2 pin is released (1)
        - **iic_index++**
          - Increment number of transmit/receive bytes.
      - **swc9 ← 0**
        - Release SCL2 pin low hold.
      - **swc9 ← 1**
        - Set SCL2 pin to low hold for next byte.
      - return

**Note:**
1. U2BRG count source × wait more than SDA2 digital delay time
4.13 Slave Control Completed Processing

```
return(temp.all)
```

```
(iic_end = 1) &
(iic_index > 1) ?

Yes
(mid-communication and with transmit/receive data)

No
(mid-communication or no transmit/receive data )

UART2 initial setting
uart2_init()

UART2 special mode 1
(\(\text{\textasciitilde I^2C\textasciitilde} \text{ mode})\) disabled

```
temp.byte.byte0
\(\text{\textasciitilde IIC\_BUSY}\)
Set status
(mid-communication)
```

```
iic_end = 0 ?
= 0 (mid-communication)

= 0 (other than mid-communication)

iic_buf_full = 1 ?
= 1 (within buffer size)

= 1 (buffer full)
```

```
temp.byte.byte1
\(\text{\textasciitilde iic\_index}\)
Set number of
transmit/receive bytes.
```

```
temp.byte.byte1
\(\text{\textasciitilde iic\_index -1}\)
```

```
iic_rw = 0 ?
= 0 (slave transmit)

= 0 (slave receive)
```

```
temp.byte.byte0
\(\text{\textasciitilde IIC\_REND}\)
Set status
(receive completed)
```

```
temp.byte.byte0
\(\text{\textasciitilde IIC\_TEND}\)
Set status
(transmit completed)
```

```
iic_buf_full = 1 ?
= 1 (buffer full)

\(\text{\textasciitilde iic\_index} \neq 1 \) (within buffer size)
```

```
temp.byte.byte1
= 0 (other than mid-communication)
```

```
iic_end = 0 ?
\(\text{\textasciitilde iic\_index} \neq 1 \) (within buffer size)
```

```
temp.byte.byte0
\(\text{\textasciitilde IIC\_ERR}\)
Set status
(overrun error)
```

REJ05B1351-0102  Rev.1.02
June 1, 2012
5. **Sample Program**

A sample program can be downloaded from the Renesas Electronics website.

6. **Reference Documents**

   Application Note
   M16C Family, R8C Family I²C Bus Interface Using UARTi Special Mode 1 (REJ05B1349)
   The latest version can be downloaded from the Renesas Electronics website.

   R8C/35C Group User’s Manual: Hardware Rev.1.00
   The latest version can be downloaded from the Renesas Electronics website.

   Technical Update/Technical News
   The latest information can be downloaded from the Renesas Electronics website.

   C Compiler Manual
   M16C Series, R8C Family C Compiler Package V.5.45
   C Compiler User’s Manual Rev.1.00
   The latest version can be downloaded from the Renesas Electronics website.

**Website and Support**

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact
## Revision History

### R8C/35C Group

**I²C bus Interface Using UART2 Special Mode 1**

(Slave Transmit/Receive)

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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