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April 1st, 2010
Renesas Electronics Corporation

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R8C/35C Group
A/D Converter in Single Sweep Mode

1. Abstract

This document describes the setting method and an application example for inputting an analog voltage by A/D converter (single sweep mode) on R8C/35C Group.

2. Introduction

The application example described in this document applies to the following MCU and parameters.

- MCU : R8C/35C Group
- VCC/AVCC, VREF : 5 V

The sample program in this application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using this application note.
3. Application Example

3.1 Program Outline

Perform A/D conversion on the analog voltage which is input from the analog input pins (two pins).

**Main settings**
- Select P0_6/AN1 pin and P0_7/AN0 pin for analog input
- Select single sweep mode as the A/D operating mode
- Select f1 as the clock source of fAD
- Select fAD divided-by-2 as the φAD operation clock
- Select 10 bits resolution
- Select a software trigger as the A/D conversion start condition
- Disable the A/D open-circuit detection assist function

Figure 3.1 shows the block diagram, and Figure 3.2 shows the operation in single sweep mode. Table 3.1 lists the pins used and their functions.

![Block Diagram](image1)

**Figure 3.1 Block Diagram**

![Operation Diagram](image2)

**Figure 3.2 Operation in Single Sweep Mode**
### Table 3.1 Pins and Functions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0_6/AN1</td>
<td>Input</td>
<td>A/D input 1</td>
</tr>
<tr>
<td>P0_7/AN0</td>
<td>Input</td>
<td>A/D input 0</td>
</tr>
</tbody>
</table>

### 3.2 Memory

#### Table 3.2 Memory

<table>
<thead>
<tr>
<th>Memory</th>
<th>Size</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM</td>
<td>197 bytes</td>
<td>In the rej05b1332_src.c module</td>
</tr>
<tr>
<td>RAM</td>
<td>4 bytes</td>
<td>In the rej05b1332_src.c module</td>
</tr>
<tr>
<td>Maximum user stack</td>
<td>12 bytes</td>
<td></td>
</tr>
<tr>
<td>Maximum interrupt stack</td>
<td>0 bytes</td>
<td></td>
</tr>
</tbody>
</table>

Memory size varies depending on the C compiler version and compile options. The above applies to the following conditions:

- C compiler: M16C/60, 30, 20, 10, and Tiny and R8C/Tiny Series Compiler V5.45 Release 00
- Compile option: -c -finfo -dir "$(CONFIGDIR)" -R8C
4. Software

This section shows the initial setting procedures and values to set the example described in section 3. Application Example. Refer to the latest R8C/35C Group Hardware Manual for details on individual registers.

The × in the register’s Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void mcu_init(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>System clock setting</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Function</td>
<td>The system clock (high-speed on-chip oscillator) is set.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void ad_init(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>A/D conversion initial setting</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Function</td>
<td>Set the SFR registers to use A/D conversion in single sweep mode.</td>
</tr>
</tbody>
</table>
4.2 Main Function

- Flowchart

```
main()

asm("FCLR I")

System clock setting
mcu_init()

A/D conversion initial setting
ad_init()

(1) adst ← 1

Repeat
i ← 0 ; i < 10 ; i++

(2) Yes
   adst = 1 ?

   No (A/D conversion is completed)

   (3) ad_data[0] ← 0x03ff & ad0

   Read AD0 register.

   (4) ad_data[1] ← 0x03ff & ad1

   Read AD1 register.
```

- Register Setting

(1) Start A/D conversion.

A/D Control Register 0 (ADCON0)

<table>
<thead>
<tr>
<th>Setting Value</th>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>ADST</td>
<td>A/D conversion start flag</td>
<td>1: Start A/D conversion</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(2) Wait until A/D conversion is completed.

(3) Read the A/D conversion result in AN0.

(4) Read the A/D conversion result in AN1.
4.3 System Clock Setting

- Flowchart

```
mcu_init()

(1) prc0 ← 1

(2) cm14 ← 0

(3) fra2 ← 0x00

(4) fra00 ← 1

(5) Repeat
   (i <= 240)

   i++

   Wait until oscillation stabilizes.

(6) fra01 ← 1

(7) ocd2 ← 1

(8) cm1 ← cm1 & 0x3f

(9) cm06 ← 0

(10) prc0 ← 0

return
```

- Disable system control register protection.
- Start the low-speed on-chip oscillator.
- High-speed on-chip oscillator clock divide-by-2 mode
- Start the high-speed on-chip oscillator.
- Select the high-speed on-chip oscillator.
- The on-chip oscillator clock is selected as the system clock.
- System clock no division
- Enable bits CM17 and CM16.
- Enable system control register protection.
Register Setting

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>PRC0</td>
<td>Protect bit 0</td>
<td>Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled</td>
</tr>
</tbody>
</table>

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>b4</td>
<td>CM14</td>
<td>Low-speed on-chip oscillator stop bit</td>
<td>0: Low-speed on-chip oscillator on</td>
</tr>
</tbody>
</table>

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>FRA00</td>
<td>High-speed on-chip oscillator enable bit</td>
<td>1: High-speed on-chip oscillator on</td>
</tr>
</tbody>
</table>

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

(5) Wait until oscillation stabilizes.
(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

<table>
<thead>
<tr>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b1</td>
<td>FRA01</td>
<td>High-speed on-chip oscillator select bit</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(7) Select the on-chip oscillator clock as a system clock.

Oscillation Stop Detection Register (OCD)

<table>
<thead>
<tr>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b2</td>
<td>OCD2</td>
<td>System clock select bit</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

<table>
<thead>
<tr>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b6</td>
<td>CM16</td>
<td>CPU clock division select bit 1</td>
<td>R/W</td>
</tr>
<tr>
<td>b7</td>
<td>CM17</td>
<td>CPU clock division select bit 1</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

<table>
<thead>
<tr>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b6</td>
<td>CM06</td>
<td>CPU clock division select bit 0</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

<table>
<thead>
<tr>
<th>Bit Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>PRC0</td>
<td>Protect bit 0</td>
<td>R/W</td>
</tr>
</tbody>
</table>
4.4 A/D Conversion Initial Setting

- Flowchart

```
ad_init()

(1) work ← pd0 & 0x3f
    Read PD0 register.

(2) prc2 ← 1
    Disable PD0 register protect.

(3) pd0 ← work
    P0_6/AN1, P0_7/AN0: Set as input port

(4) adic ← 0x00
    Disable A/D conversion interrupt.

(5) adcon0 ← 0x00
    Stop A/D conversion.

(6) prc3 ← 1
    Disable the protects to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

(7) ocvrefan ← 0
    On-chip reference voltage to analog input connect: cut off

(8) prc3 ← 0
    Enable the protects to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

(9) admod ← 0x22
    Division: fAD divided by 2
    Clock source: f1
    Select single sweep mode
    A/D conversion trigger: software trigger

    Repeat
    i ← 0 ; i < 10 ; i++

    When the CKS2 bit is changed, wait for 3 φAD cycles or more before starting A/D conversion.

(10) adinsel ← 0x00
    A/D sweep pin count: 2 pins
    Select port 0 group

(11) adcon1 ← 0x30
    Extended analog input pin not selected
    8/10-bit mode: 10-bit mode
    A/D standby: A/D operation enabled
    Disable A/D open-circuit detection assist function

    Repeat
    i ← 0 ; i < 10 ; i++

    When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for 1 φAD cycle or more before starting A/D conversion.

return
```
Register Setting

1. Read the PD0 register.

2. Enable writing to the PD0 register.

Protect Register (PRCR)

3. Set P0_6 and P0_7 direction bits as input ports.

Port P0 Direction Register (PD0)


Interrupt Control Register (ADIC)

5. Stop A/D conversion.

A/D Control Register 0 (ADCON0)
(6) Enable writing to the registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b3</td>
<td>PRC3</td>
<td>Protect bit 3</td>
<td>Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(7) Cut off on-chip reference voltage from the analog input.

On-Chip Reference Voltage Control Register (OCVREFCR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>OCVREFAN</td>
<td>On-chip reference voltage to analog input connect bit</td>
<td>0: On-chip reference voltage and analog input are cut off</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(8) Disable writing to the registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b3</td>
<td>PRC3</td>
<td>Protect bit 3</td>
<td>Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(9) Set the A/D mode register.

A/D Mode Register (ADMOD)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>CKS0</td>
<td>Division select bit</td>
<td>b1 b0: fAD divided by 2</td>
<td>R/W</td>
</tr>
<tr>
<td>b1</td>
<td>CKS1</td>
<td></td>
<td>1 0: Select f1</td>
<td>R/W</td>
</tr>
<tr>
<td>b2</td>
<td>CKS2</td>
<td>Clock source select bit</td>
<td>0: Select f1</td>
<td>R/W</td>
</tr>
<tr>
<td>b3</td>
<td>MD0</td>
<td>A/D operating mode select bit</td>
<td>b5 b4 b3 1 0 0: Single sweep mode</td>
<td>R/W</td>
</tr>
<tr>
<td>b4</td>
<td>MD1</td>
<td></td>
<td>1 0 0: Single sweep mode</td>
<td>R/W</td>
</tr>
<tr>
<td>b5</td>
<td>MD2</td>
<td></td>
<td>0 0 0: A/D conversion start by software trigger (ADST bit in the ADCON0 register)</td>
<td>R/W</td>
</tr>
<tr>
<td>b6</td>
<td>ADCAP0</td>
<td>A/D conversion trigger select bit</td>
<td>b7 b6</td>
<td>R/W</td>
</tr>
<tr>
<td>b7</td>
<td>ADCAP1</td>
<td></td>
<td>0 0</td>
<td>R/W</td>
</tr>
</tbody>
</table>
(10) Select the A/D sweep pin count as 2 pins and A/D input group as port P0.

A/D Input Select Register (ADINSEL)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name/Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b4</td>
<td>SCAN0</td>
<td>A/D sweep pin count select bits b4 b5 0 0: 2 pins</td>
<td>R/W</td>
</tr>
<tr>
<td>b5</td>
<td>SCAN1</td>
<td>A/D input group select bits b7 b6 0 0: Port P0 group selected</td>
<td>R/W</td>
</tr>
</tbody>
</table>

(11) Set the A/D control register 1.

A/D Control Register 1 (ADCON1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit Name/Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>ADEX0</td>
<td>Extended analog input pin select bit 0: Extended analog input pin not selected</td>
<td>R/W</td>
</tr>
<tr>
<td>b4</td>
<td>BITS</td>
<td>8/10-bit mode select bit 1: 10-bit mode</td>
<td>R/W</td>
</tr>
<tr>
<td>b5</td>
<td>ADSTBY</td>
<td>A/D standby bit 1: A/D operation enabled</td>
<td>R/W</td>
</tr>
<tr>
<td>b6</td>
<td>ADDDAEN</td>
<td>A/D open-circuit detection assist function enable bit 0: Disabled</td>
<td>R/W</td>
</tr>
</tbody>
</table>
5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

Hardware Manual
R8C/35C Group Hardware Manual Rev.0.10
The latest version can be downloaded from the Renesas Technology website.

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