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R8C/35C Group

A/D Converter (Single Sweep Mode Using DTC)

1. Abstract

This document describes the setting method and an application example of the A/D converter in single sweep mode and data transfer controller (DTC) in normal mode.

2. Introduction

The application example described in this document applies to the following MCU and parameters.

- MCU : R8C/35C Group
- VCC/AVCC, VREF : 5 V
- ϕ AD : 20 MHz (f1)

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the R8C/35C Group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

In this sample program, DTC is activated by an A/D conversion interrupt and transfers the A/D conversion result stored in the registers (AD0 register (addresses 00C0h - 00C1h) to AD3 register (addresses 00C6h - 00C7h)) to the on-chip memory (addresses 0600h - 0607h).

Table 3.1 lists the settings for the A/D converter, and Table 3.2 lists the settings for the DTC. Figure 3.1 shows the contents of the data transfer.

Table 3.1 A/D Converter Settings

Function	Setting
Operating clock ϕ AD	fAD (= f1) divided by 1 (no division)
Operating mode	Single sweep mode
A/D conversion start condition	Software trigger
Resolution	10 bits
A/D sweep pin count	4
Analog input pin	AN8 to AN11 (AD0 register to AD3 register)
On-chip reference voltage to analog input	On-chip reference voltage and analog input are cut off
A/D open-circuit detection assist function	Disabled
Extended analog input pin	Not selected

Table 3.2 DTC Settings

Function	Setting
DTC activation source	A/D conversion interrupt
Control data	Control data 0 (address 2C40h to 2C47h)
Transfer mode	Normal mode
Source address control	Fixed
Destination address control	Fixed
Chain transfer	Disabled
Size of the data block to be transferred by one activation	8 bytes
Number of times of DTC data transfers	1
Transfer source address for data transfer	00C0h (address in the AD0 register)
Transfer destination address for data transfer	0600h (address in on-chip memory)

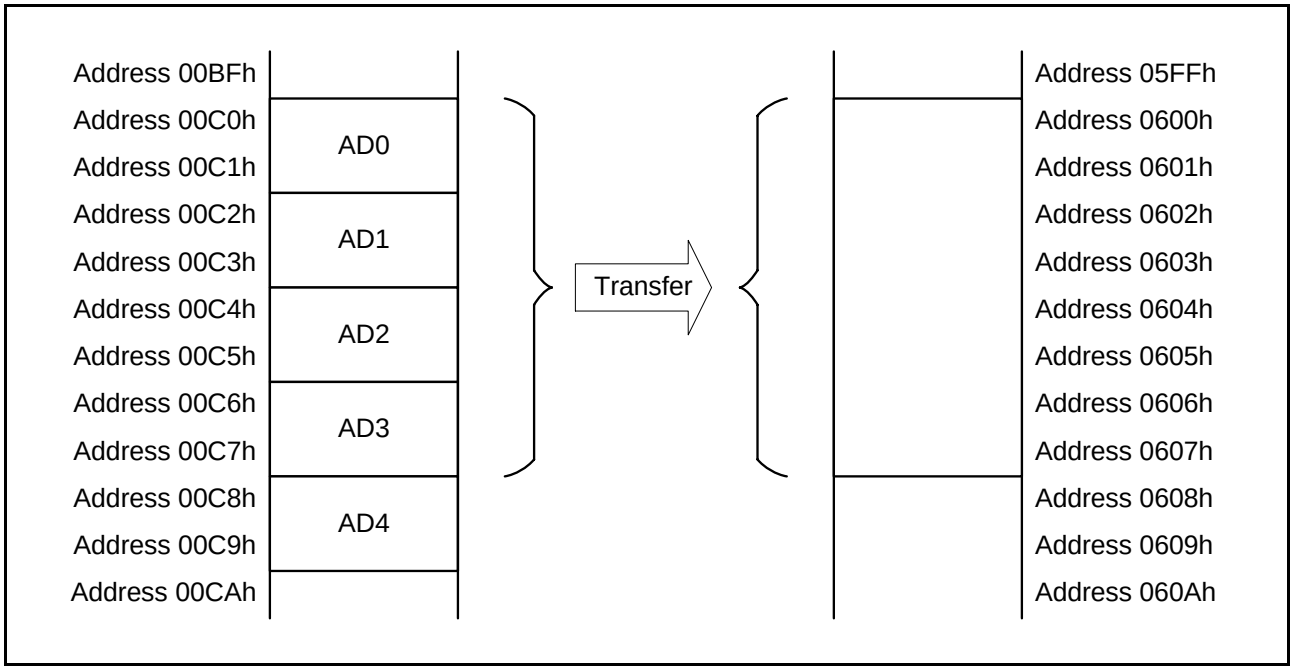


Figure 3.1 Data Transfer Contents

3.2 Advantage of Using DTC

Figure 3.2 compares the numbers of execution cycles required for DTC with those required for data transfer by an interrupt process.
In this application example, while data transfer by an interrupt requires 121 cycles, DTC requires only 28 cycles– about 76.9 percent shorter than an interrupt.
.

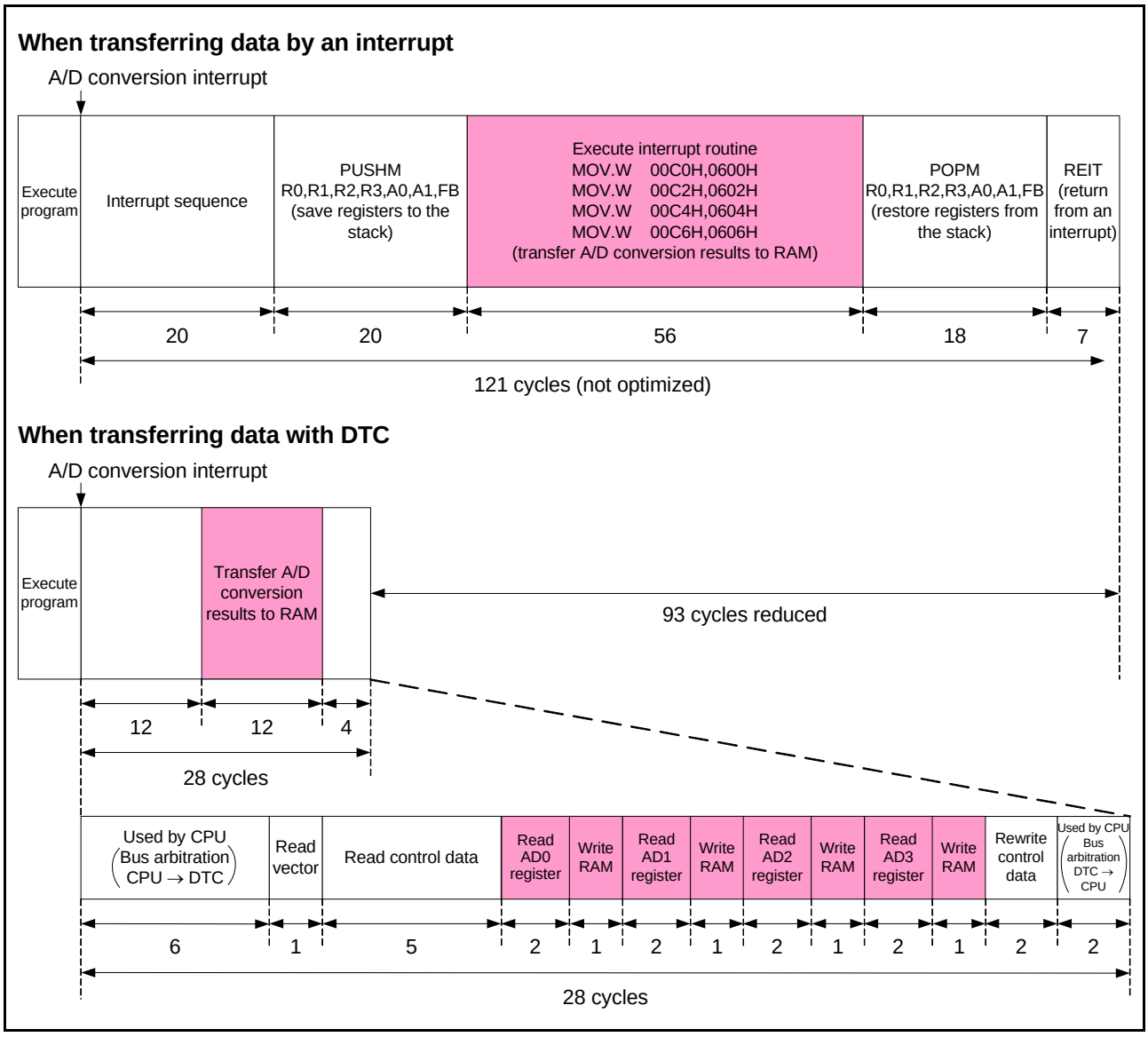


Figure 3.2 Numbers of Data Transfer Cycles

3.3 Pins and Memory

3.3.1 Pins

Table 3.3 Pins and Their Functions

Pin Name	I/O	Function
P1_0/AN8	Input	AN8 analog input pin
P1_1/AN9	Input	AN9 analog input pin
P1_2/AN10	Input	AN10 analog input pin
P1_3/AN11	Input	AN11 analog input pin

3.3.2 Memory

Table 3.4 Memory

Memory	Size	Remarks
ROM	271 bytes	In the rej05b1337_src.c module
RAM	16 bytes	In the rej05b1337_src.c module
Maximum user stack	9 bytes	main function: 3 bytes mcu_init function: 6 bytes ad_converter_enable function: 6 bytes dtc_enable function: 3 bytes
Maximum interrupt stack	18 bytes	ad_converter_int function: 18 bytes

Memory size varies depending on the C compiler version and compile options. The above applies to the following conditions:

C compiler: M16C/60, 30, 20, 10, and Tiny and R8C/Tiny Series Compiler V.5.45 Release 00
Compile option: -c -finfo (see Note) -dir “$(CONFIGDIR)” -R8C
Note: -c -finfo cannot be used for the R8C/Tiny-only Free-version.

4. Setup

This section shows the initial setting procedures and values to set the example described in 3. Application Example. Refer to the R8C/35C Group Hardware Manual for details on individual registers.

4.1 Setting System Clock

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value	—	—	—	—	—	—	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator (OCO).

System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
Setting Value	—	—	—	0	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit (1, 2)	0: Low-speed on-chip oscillator on	R/W

Notes:
1. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
2. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

(3) Set the divide ratio of the high-speed OCO.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 0025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	FRA22	FRA21	FRA20
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA2 register.

(4) Start the high-speed OCO.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
Setting Value	—	—	—	—	—	—	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

(5) Wait until oscillation stabilizes.

(6) Select the high-speed OCO.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
Setting Value	—	—	—	—	—	—	1	—

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	1: High-speed on-chip oscillator selected	R/W

Note:
1. Change the FRA01 bit in the following conditions.
   - FRA00 = 1 (high-speed on-chip oscillator on)
   - The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division mode can be set when VCC = 3.0 V to 5.5 V 000b to 111b
     Divide ratio of 4 or more when VCC = 2.7 V to 5.5 V 010b to 111b (divide-by-4 or more)
     Divide ratio of 8 or more when VCC = 2.2 V to 5.5 V 110b to 111b (divide-by-8 or more)

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

(7) Set the system clock division select bit 1.

System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
Setting Value	0	0	—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	System clock division select bit 1 (1)	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

Note:
1. When the CM06 bit is set to 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

(8) Set the system clock division select bit 0.

System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	CM01	—
Setting Value	—	0	—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0 (1)	0: Bits CM16 and CM17 in CM1 register enabled	R/W

Note:
1. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

(9) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value	—	—	—	—	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write Disabled	R/W

4.2 Setting A/D Converter (Single Sweep Mode)

(1) Set P1_0 (AN8), P1_1 (AN9), P1_2 (AN10), and P1_3 (AN11) as input ports.

Port P1 Direction Register (PD1)

Address 00E3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD1_7	PD1_6	PD1_5	PD1_4	PD1_3	PD1_2	PD1_1	PD1_0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD1_0	Port P1_0 direction bit	0: Input mode (functions as an input port)	R/W
b1	PD1_1	Port P1_1 direction bit		R/W
b2	PD1_2	Port P1_2 direction bit		R/W
b3	PD1_3	Port P1_3 direction bit		R/W

The PD1 register selects whether I/O ports are used for input or output. Each bit in the PD1 register corresponds to one port.

(2) Disable A/D conversion interrupt.

Interrupt Control Register (ADIC)

Address 004Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated.

(3) Stop A/D conversion.

A/D Control Register 0 (ADCON0)

Address 00D6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	0: Stop A/D conversion	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

ADST Bit (A/D conversion start flag)
Conditions for setting this bit to 1:
When A/D conversion starts or during A/D conversion.
Condition for setting this bit to 0:
When A/D conversion stops.

(4) Enable writing to the OCVREFCR register.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value	—	—	—	—	1	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled	R/W

(5) Cut off on-chip reference voltage from the analog input.

On-Chip Reference Voltage Control Register (OCVREFCR)

Address 0026h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	OCVREFAN
Setting Value	—	—	—	—	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCVREFAN	On-chip reference voltage to analog input connect bit (1)	0: On-chip reference voltage and analog input are cut off	R/W

Note:
1. When on-chip reference voltage is used as analog input, first set the ADEX0 bit in the ADCON1 register to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the OCVREFCR register.
If the contents of the OCVREFCR register are rewritten during A/D conversion, the conversion result is undefined.

(6) Disable writing to OCVREFCR register.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value	—	—	—	—	0	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled	R/W

(7) Set the A/D mode register.

A/D Mode Register (ADMOD)

Address 00D4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	MD2	MD1	MD0	CKS2	CKS1	CKS0
Setting Value	0	0	1	0	0	0	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0 1 1: fAD divided by 1 (no division)	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit (1)	0: Select f1	R/W
b3	MD0	A/D operating mode select bit	b5 b4 b3 1 0 0: Single sweep mode	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6 0 0: A/D conversion start by software trigger (ADST bit in the ADCON0 register)	R/W
b7	ADCAP1			R/W

Note:
1. When the CKS2 bit is changed, wait for 3 ϕAD cycles or more before starting A/D conversion.

If the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

(8) Wait for three or more ϕAD cycles.

(9) Set the A/D input select register.

A/D Input Select Register (ADINSEL)

Address 00D5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADGSEL1	ADGSEL0	SCAN1	SCAN0	—	CH2	CH1	CH0
Setting Value	0	1	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Analog input pin select bits	Refer to **Table 4.1 Analog Input Pin Selection**	R/W
b1	CH1			R/W
b2	CH2			R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	SCAN0	A/D sweep pin count select bits	b5 b4 0 1: 4 pins	R/W
b5	SCAN1			R/W
b6	ADGSEL0	A/D input group select bits	b7 b6 0 1: Port P1 group selected	R/W
b7	ADGSEL1			R/W

If the ADINSEL register is rewritten during A/D conversion, the conversion result is undefined.

Table 4.1 Analog Input Pin Selection

Bits CH2 to CH0	Bits ADGSEL1, ADGSEL0 = 00b	Bits ADGSEL1, ADGSEL0 = 01b
000b	AN0	AN8
001b	AN1	AN9
010b	AN2	AN10
011b	AN3	AN11
100b	AN4	Do not set.
101b	AN5	
110b	AN6	
111b	AN7	

(10) Set A/D control register 1.

A/D Control Register 1 (ADCON1)

Address 00D7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADDDAEL	ADDDAEN	ADSTBY	BITS	—	—	—	ADEX0
Setting Value	0	0	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	Extended analog input pin select bit (1)	0: Extended analog input pin not selected	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	BITS	8/10-bit mode select bit	1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit (2)	1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit (3)	0: Disabled	R/W
b7	ADDDAEL	A/D open-circuit detection assist method select bit (3)	0: Discharge before conversion	R/W

Notes:
1. When on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit in the OCVREFCR register to 1 (on-chip reference voltage and analog input are connected).
   When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).
2. When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for 1 ϕAD cycle or more before starting A/D conversion.
3. To enable the A/D open-circuit detection assist function, select the conversion start state with the ADDDAEL bit after setting the ADDDAEN bit to 1 (enabled).
   The conversion result with an open circuit varies with external circuits. Careful evaluation should be performed according to the system before using this function.

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

(11) Wait one or more ϕAD cycles.

(12) Set the A/D conversion interrupt priority level.

Interrupt Control Register (ADIC)

Address 004Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
Setting Value	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated.

4.3 Setting DTC (Normal Mode)

(1) Set the DTC control data number in the DTC vector address (address 2C09h) which is assigned to the A/D conversion interrupt. In this program, set 0 to address 2C09h to use control data 0.

DTC Vector Address for A/D Conversion Interrupt

Address 2C09h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7 - b0	Stores the data from 00000000b to 00010111b, and selects one control data out of 24 groups.	00h - 17h	R/W

(2) Set the DTC control register allocated for control data 0. Set “Normal mode” for the transfer mode, “Fixed” for the source address, “Fixed” for the destination address, and “Disabled” for the chain transfer.

DTC Control Register (DTCCR)

Address 2C40h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
Setting Value	0	0	—	0	0	0	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode	R/W
b1	RPTSEL	Repeat area select bit (1)		R/W
b2	SAMOD	Source address control bit (2)	0: Fixed	R/W
b3	DAMOD	Destination address control bit (2)	0: Fixed	R/W
b4	CHNE	Chain transfer enable bit	0: Chain transfers disabled	R/W
b5	RPTINT	Repeat mode interrupt enable bit (1)		R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. This bit is valid when the MODE bit is 1 (repeat mode).
2. Settings of bits SAMOD and DAMOD are invalid for the repeat area.

(3) Set the DTC block size register allocated for control data 0. In this program, set 8 in this register to transfer 8-byte data once.

DTC Block Size Register (DTBLS)

Address 2C41h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	1	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh (1)	R/W

Note:
1. When the DTBLS register is set to 00h, the block size is 256 bytes.

(4) Set the DTC transfer count register allocated for control data 0. In this program, set 1 in this register to transfer 8-byte data once.

DTC Transfer Count Register (DTCCT)

Address 2C42h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh (1)	R/W

Note:
1. When the DTCCT register is set to 00h, the number of transfer times is 256. Each time the DTC is activated, the DTCCT register is decremented by 1.

(5) Set the DTC transfer count reload register allocated for control data 0. As normal mode does not use this register, set 0.

DTC Transfer Count Reload Register (DTRLD)

Address 2C43h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh (1)	R/W

Note:
1. Set the initial value for the DTCCT register.

(6) Set the DTC source address register allocated for control data 0. In this program, set the source address 00C0h.

DTC Source Address Register (DTSAR)

Address 2C44h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
Setting Value	1	1	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

(7) Set the DTC destination register allocated for control data 0. In this program, set the destination address 0600h.

DTC Destination Register (DTDAR)

Address 2C46h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	1	1	0

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

(8) Set the DTC activation enable registers. Set all DTC activation source to “Activation disabled”.

DTC Activation Enable Registers (DTCENi) (i = 0 to 6**)**

Address 0088h (DTCEN0), 0089h (DTCEN1), 008Ah (DTCEN2), 008Bh (DTCEN3), 008Ch (DTCEN4), 008Dh (DTCEN5), 008Eh (DTCEN6)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCENi0	DTC activation enable bits	0: Activation disabled 1: Activation enabled	R/W
b1	DTCENi1			R/W
b2	DTCENi2			R/W
b3	DTCENi3			R/W
b4	DTCENi4			R/W
b5	DTCENi5			R/W
b6	DTCENi6			R/W
b7	DTCENi7			R/W

i = 0 to 6

The DTCENi register enables/disables DTC activation using by interrupt sources. Table 4.2 shows the correspondences between bits DTCENi0 to DTCENi7 (i = 0 to 6) and interrupt sources.

Table 4.2 Correspondences Between Bits DTCENi0 to DTCENi7 (i = 0 to 6) and Interrupt Sources

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	$\overline{\text{INT3}}$	$\overline{\text{INT4}}$	—	—	—
DTCEN1	Key input	A/D conversion	UART0 reception	UART0 transmission	UART1 reception	UART1 transmission	UART2 reception	UART2 transmission
DTCEN2	SSU/I^{2}C bus receive data full	SSU/I^{2}C bus transmit data empty	Voltage Monitor 2/ Comparator A2	Voltage Monitor 1/ Comparator A1	—	—	Timer RC input-capture/ compare-match A	Timer RC input-capture/ compare-match B
DTCEN3	Timer RC input-capture/ compare-match C	Timer RC input-capture/ compare-match D	Timer RD0 input-capture/ compare-match A	Timer RD0 input-capture/ compare-match B	Timer RD0 input-capture/ compare-match C	Timer RD0 input-capture/ compare-match D	Timer RD1 input-capture/ compare-match A	Timer RD1 input-capture/ compare-match B
DTCEN4	Timer RD1 input-capture/ compare-match C	Timer RD1 input-capture/ compare-match D	—	—	—	—	—	—
DTCEN5	—	—	Timer RE	—	—	—	—	—
DTCEN6	—	Timer RA	—	Timer RB	Flash memory ready status	—	—	—

(9) Set the DTC activation control register. Disable DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

DTC Activation Control Register (DTCTL)

Address 0080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. This bit is set to 0 when the read result is 1 and 0 is written to the same bit. This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. This bit remains unchanged if 1 is written to it.

The DTCTL register controls DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

Non-Maskable Interrupt Generation Bit (NMIF Bit)

The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, a voltage monitor 1 interrupt, or a voltage monitor 2 interrupt is generated.
When the NMIF bit is 1, the DTC is not activated even if the interrupt which enables DTC activation is generated. If the NMIF bit becomes 1 during DTC transfer, the transfer continues until it is completed.

4.4 Starting A/D Conversion

(1) Confirm that DTC activation with A/D conversion enable bit has been disabled (dtcen16 = 0).

(2) Set the DTC transfer count register allocated for control data 0. In this program, set 1 to transfer 8-byte data once.

DTC Transfer Count Register (DTCCT)

Address 2C42h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh (1)	R/W

Note:
1. When the DTCCT register is set to 00h, the number of transfer times is 256. Each time the DTC is activated, the DTCCT register is decremented by 1.

(3) Use A/D conversion interrupt source to enable DTC activation.

DTC Activation Enable Registers (DTCEN1)

Address 0089h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTCEN17	DTCEN16	DTCEN15	DTCEN14	DTCEN13	DTCEN12	DTCEN11	DTCEN10
Setting Value	—	1	—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	DTCEN16	DTC activation with A/D conversion interrupt enable bit	1: Activation enabled	R/W

(4) Start A/D conversion.

A/D Control Register 0 (ADCON0)

Address 00D6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
Setting Value	—	—	—	—	—	—	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	1: Start A/D conversion	R/W

ADST Bit (A/D conversion start flag)
Conditions for setting to 1:
When A/D conversion starts and during A/D conversion.
Condition for setting to 0:
When A/D conversion stops.

5. Function Table and Flowchart

5.1 Function Table

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		–
Variable (global)	Variable name		Contents
	None		–
Returned value	Type	Value	Meaning
	None	–	–
Function	Set system clock (high-speed on-chip oscillator)		

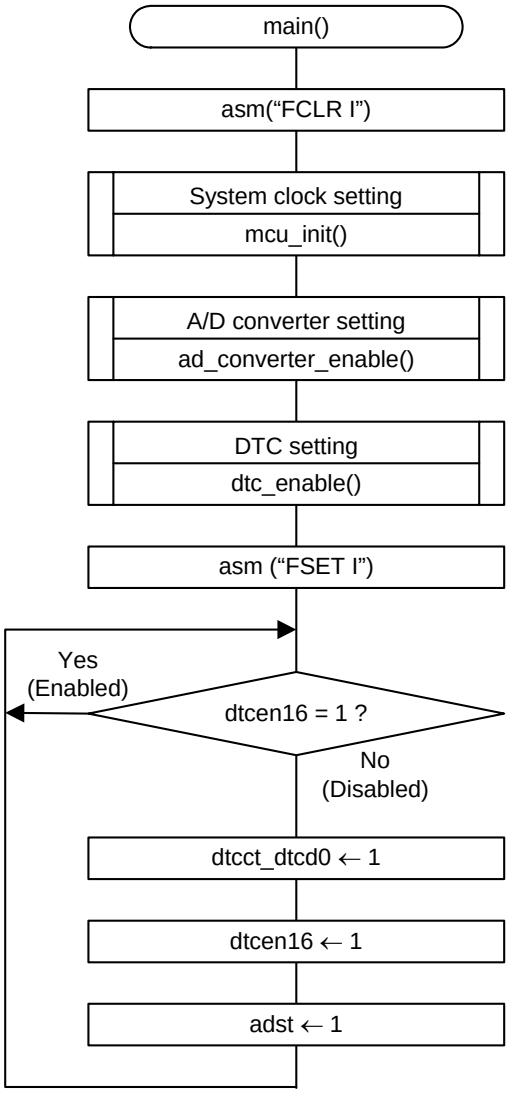
Declaration	void ad_converter_enable(void)		
Outline	A/D convertor setting		
Argument	Argument name		Meaning
	None		–
Variable (global)	Variable name		Contents
	None		–
Returned value	Type	Value	Meaning
	None	–	–
Function	Set A/D converter (single sweep mode)		

Declaration	void dtc_enable(void)		
Outline	DTC setting		
Argument	Argument name		Meaning
	None		–
Variable (global)	Variable name		Contents
	None		–
Returned value	Type	Value	Meaning
	None	–	–
Function	Set DTC (normal mode)		

Declaration	void ad_converter_int(void)		
Outline	A/D conversion interrupt		
Argument	Argument name		Meaning
	None		–
Variable (global)	Variable name		Contents
	unsigned short ad_value[4]		Reference
	unsigned short an8_value		Setting
	unsigned short an9_value		Setting
	unsigned short an10_value		Setting
	unsigned short an11_value		Setting
Returned value	Type	Value	Meaning
	None	–	–
Function	This interrupt process takes place after A/D conversion is completed. (This interrupt starts when DTC transfer is completed.) A/D conversion values in AN8 to AN11, which are transferred from DTC, are set to each parameter.		

5.2 Flow Chart

5.2.1 Main Function



Interrupt disabled

System clock setting (set high-speed OCO)

A/D converter setting (single sweep mode)

DTC setting (normal mode)

Interrupt enabled

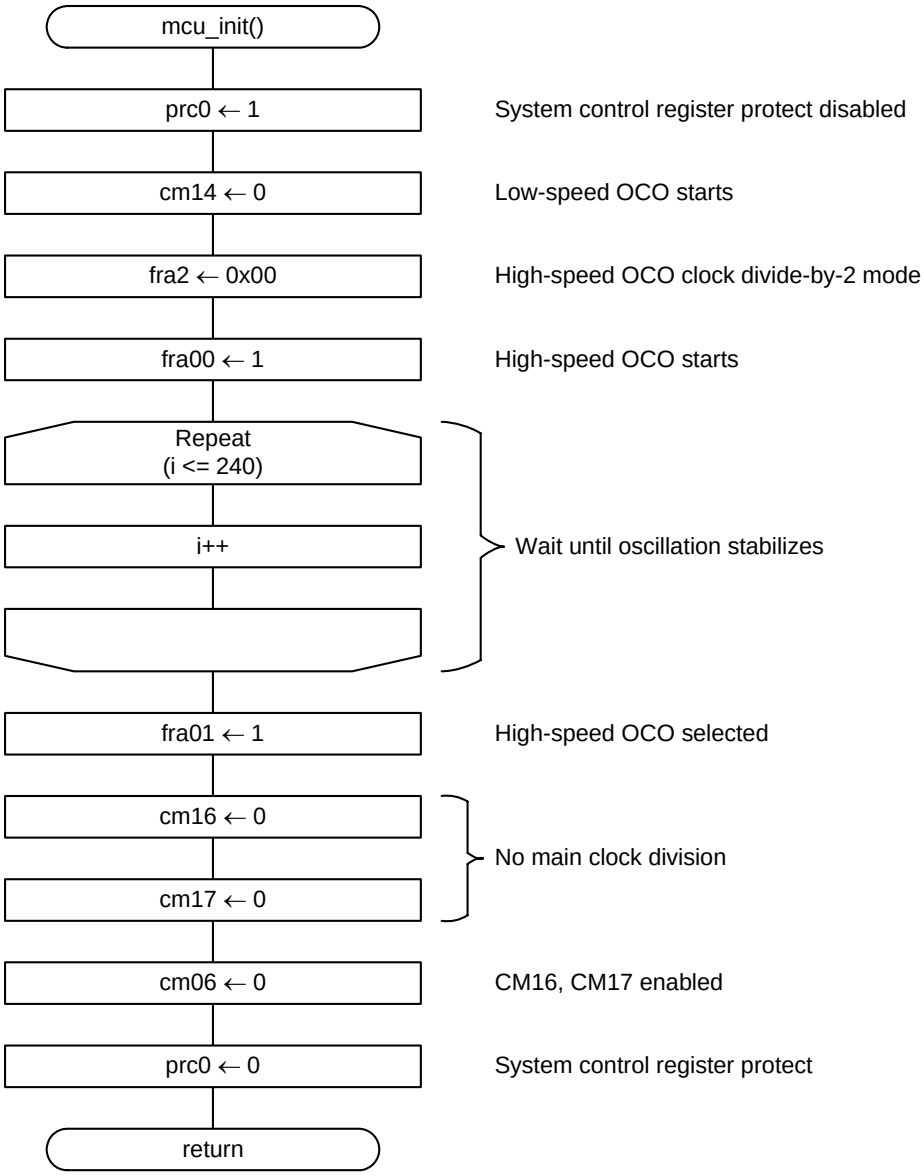
Is DTC activation with A/D conversion interrupt enabled?

Number of DTC data transfers: 1

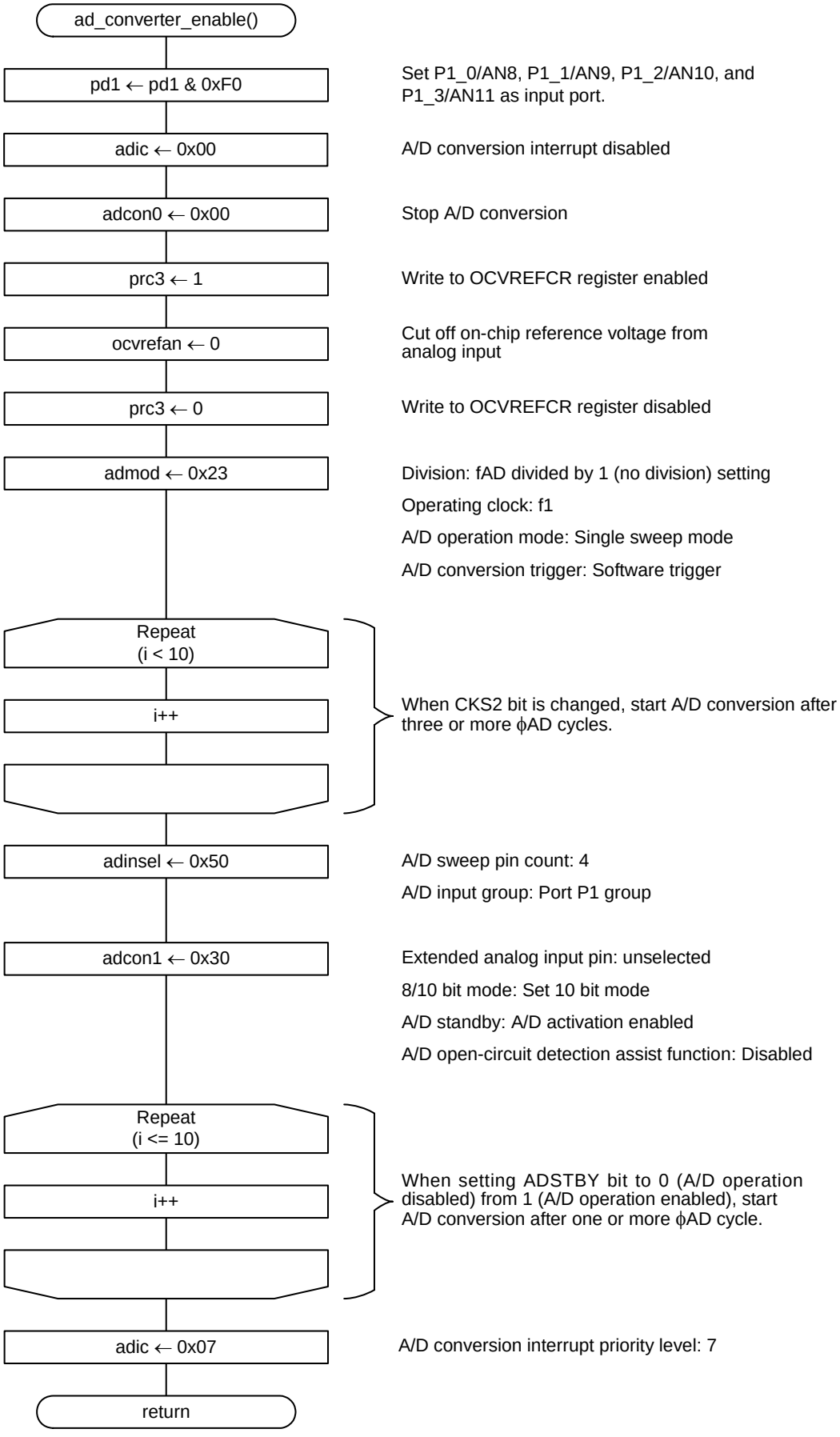
DTC activation with A/D conversion interrupt enabled

Start A/D conversion

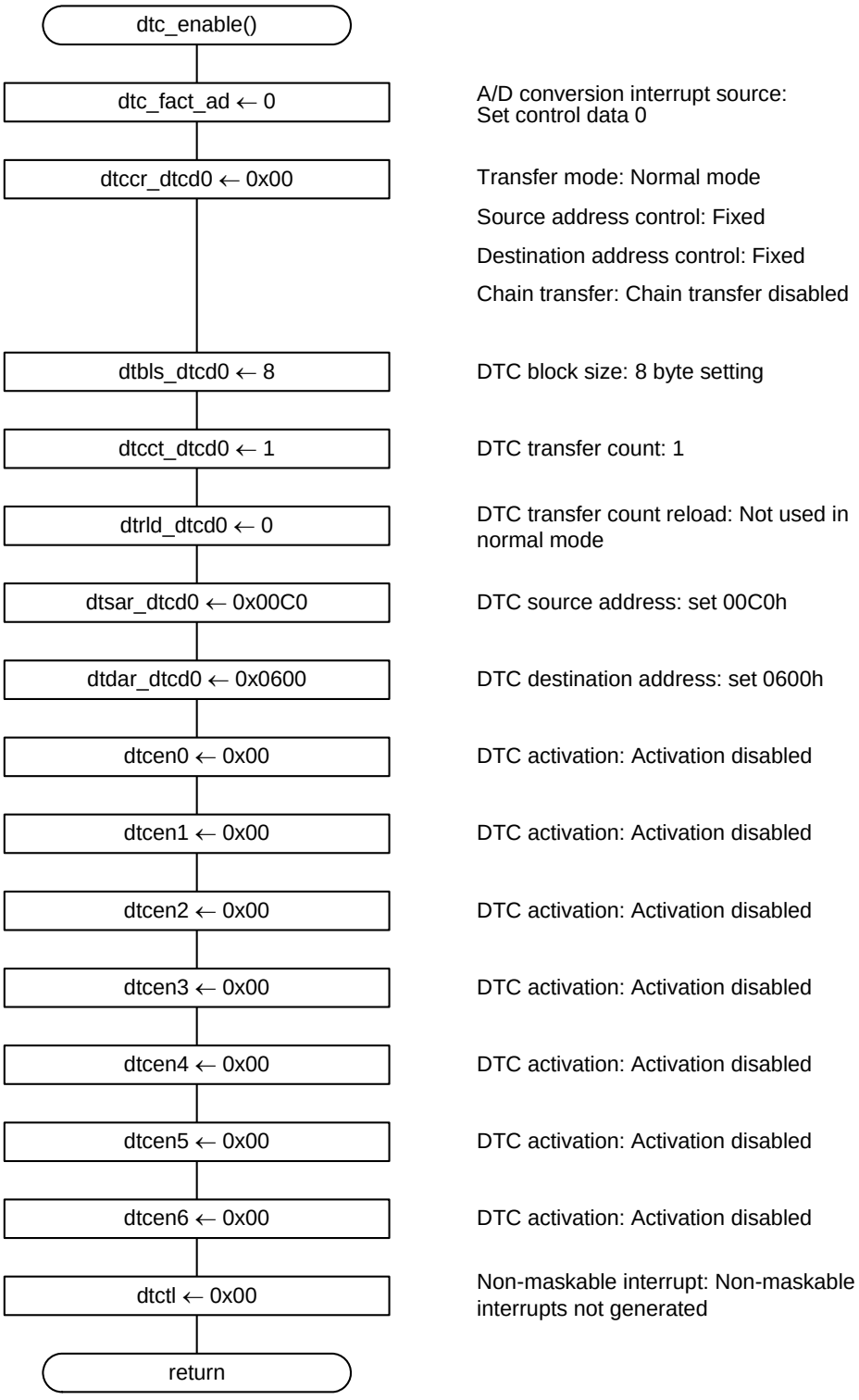
5.2.2 System Clock Setting Process



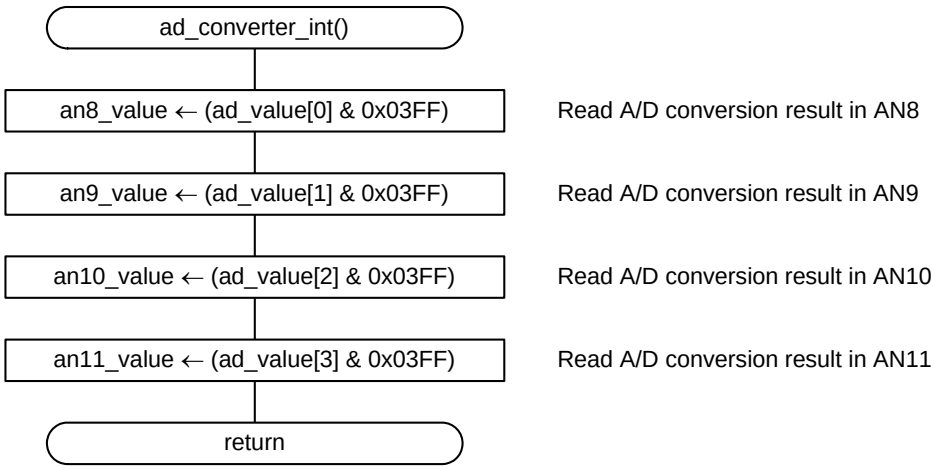
5.2.3 A/D Converter Setting



5.2.4 DTC Setting



5.2.5 A/D Conversion Interrupt



6. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C/Tiny Series page.

7. Reference Documents

Hardware Manual
R8C/35C Group Hardware Manual Rev.0.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	R8C/35C Group A/D Converter (Single Sweep Mode Using DTC)

Rev.	Date	Description	
		Page	Summary
1.00	Oct 26, 2009	–	First Edition issued

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