R8C/35A Group

Timer RA (Pulse Output Mode)

REJ05B1285-0100
Rev.1.00
July 23, 2010

1. Abstract

This document describes a method and an application example for timer RA pulse output mode in the R8C/35A Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameters:

- MCU: R8C/35A Group
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

Use the prescaler register (TRAPRE) and timer RA register (TRA) to count count source f8. Use the TRA register underflow signal to generate an inverted waveform from pins TRAIO and TRAO every millisecond.

Settings

- TRAPRE = 249, TRA = 9
- Select the 20 MHz XIN clock as the system clock.

Calculation formula for setting time

$1\ \text{ms} = (1 \div f8) \times (\text{TRAPRE} + 1) \times (\text{TRA} + 1)$

$= \{1 \div (20\ \text{MHz} \div 8)\} \times 250 \times 10$

$= (4 \times 10^{-7})\text{s} \times 2500$

Figure 3.1 shows a Block Diagram and Figure 3.2 shows a Timing Diagram.

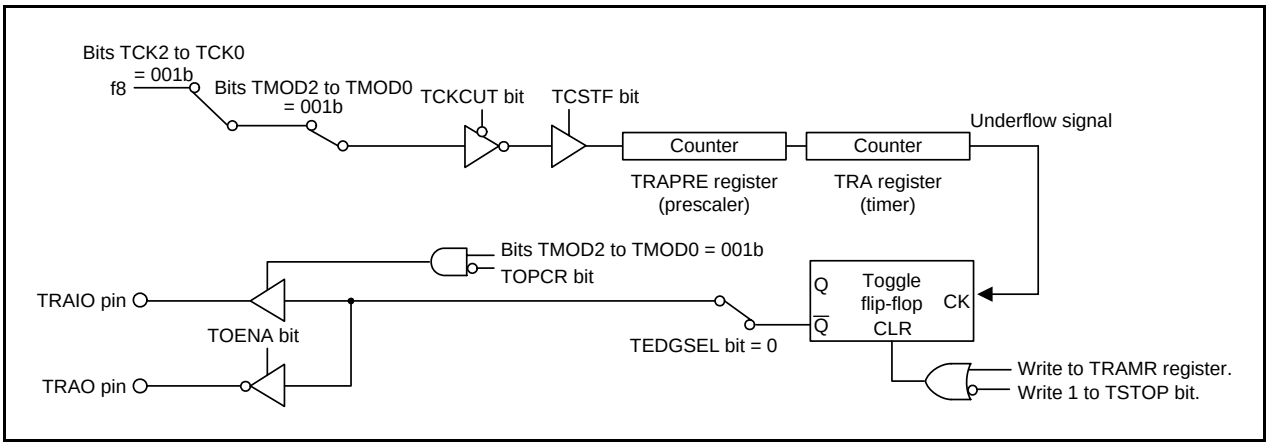


Figure 3.1 Block Diagram

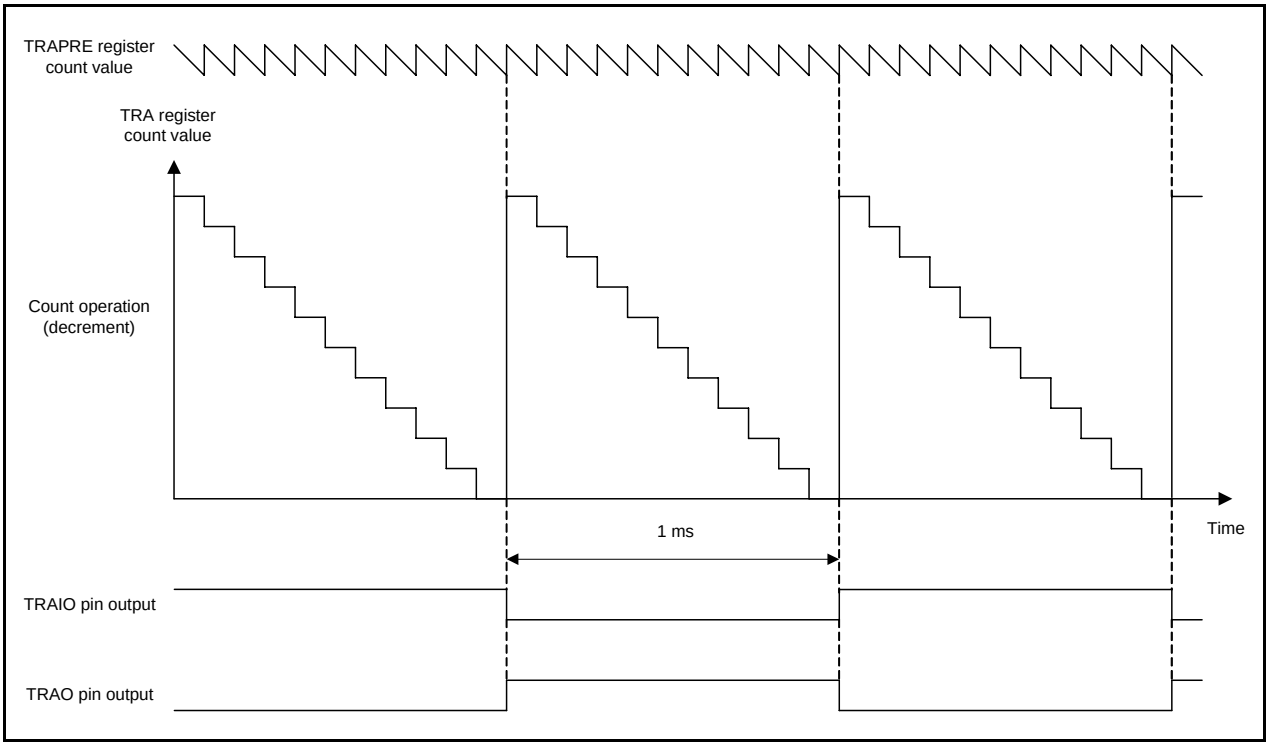


Figure 3.2 Timing Diagram

3.2 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	98 bytes	In the rej05b1285_src.c module
RAM	0 bytes	
Maximum user stack	10 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C/60,30,20,10,Tiny,R8C/Tiny Series Compiler V.5.44 Release 00
Compile option: -D__UART0__ -c -finfo -dir "$(CONFIGDIR)" -R8CE

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/35A Group hardware user's manual** for details on individual registers.

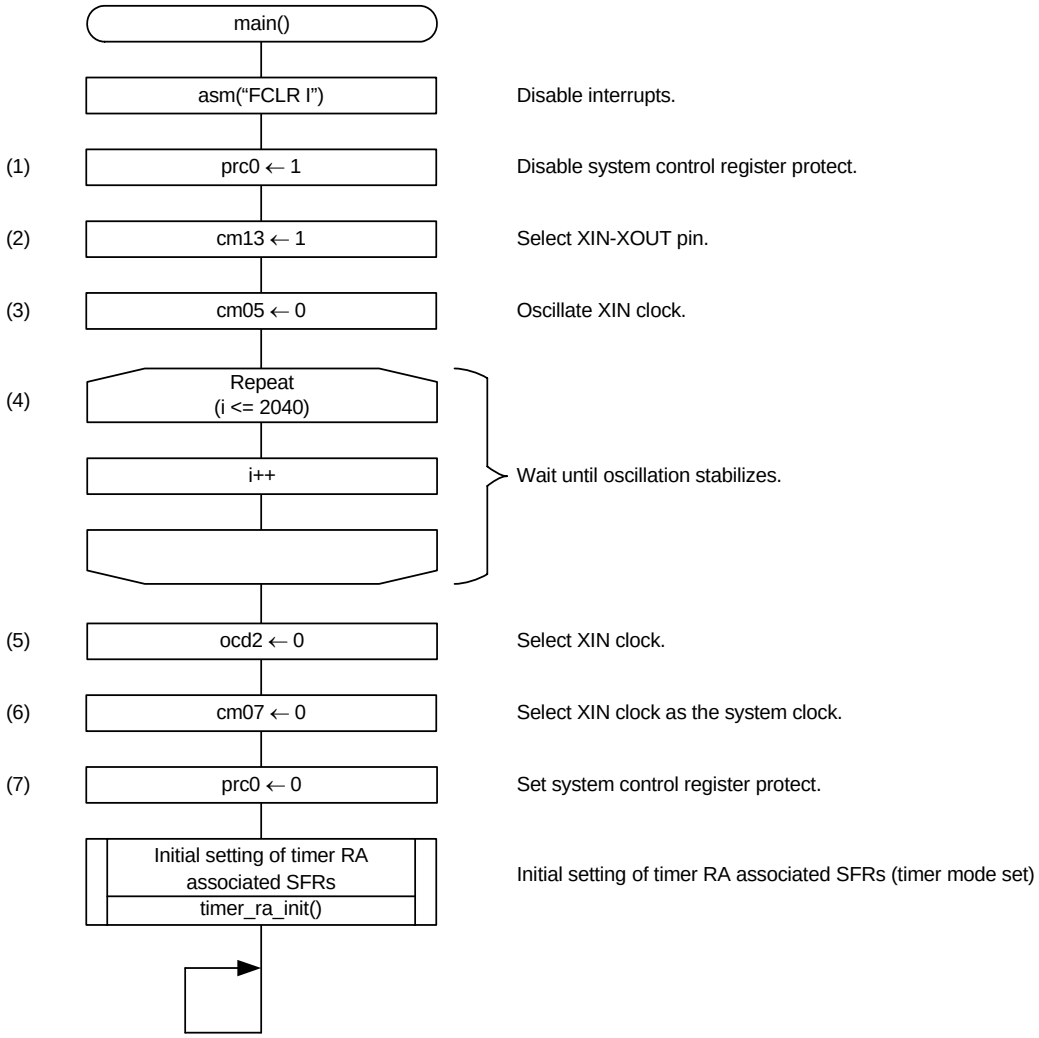
The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void timer_ra_init(void)		
Outline	Initial setting of timer RA associated SFRs		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform initial setting of timer RA associated SFRs.		

4.2 Main Function

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Select the XIN-XOUT pin.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	—	x	1	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port/XIN-XOUT switch bit	1: XIN-XOUT pin	R/W

(3) Oscillate the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		x	0	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(4) Wait until oscillation stabilizes.

(5) Select the XIN clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	0: XIN clock selected	R/W

(6) Select the XIN clock as the system clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	x		x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	0: XIN clock	R/W

(7) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

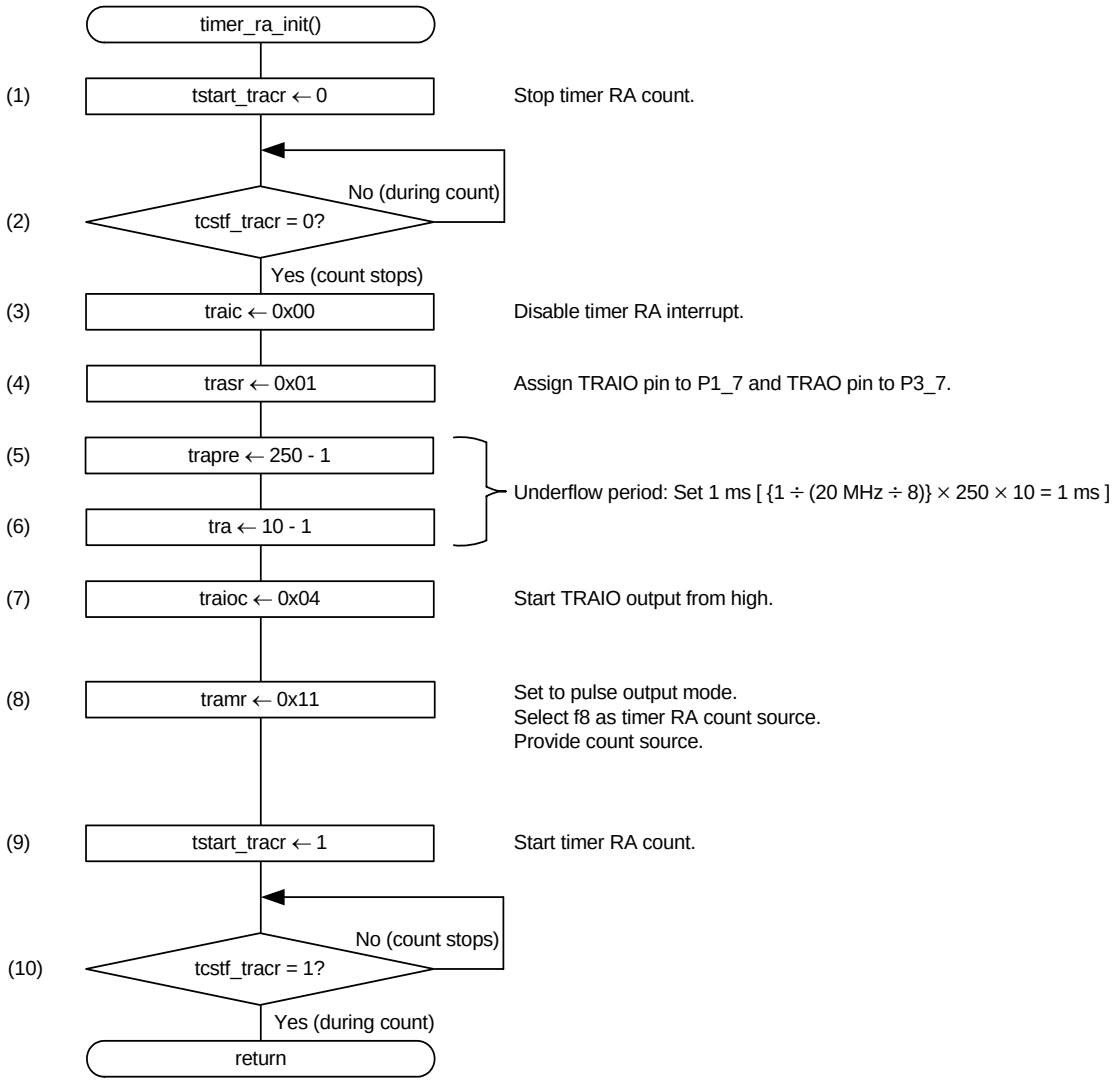
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.3 Initial Setting of Timer RA Associated SFRs

• Flowchart



• Register settings

(1) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	x	—	x		0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(2) Wait until the timer RA count stops.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

(3) Disable the timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(4) Set the timer pin select register.

Timer RA Pin Select Register (TRASR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	0	0	—	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 0 1: P1_7 assigned	R/W
b1	TRAIOSEL1			R/W
b3	TRAOSEL0	TRAO pin select bit	b4 b3 0 0: P3_7 assigned	R/W
b4	TRAOSEL1			R/W

(5) Set the timer RA prescaler register to F9h.

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	0	0	1

Bit	Function	Setting Range	R/W
b7-b0	Counts an internal count source	00h to FFh	R/W

(6) Set timer RA register to 09h.

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	1	0	0	1

Bit	Function	Setting Range	R/W
b7-b0	Counts on underflow of TRAPRE register	00h to FFh	R/W

(7) Set the timer RA I/O control register.

Timer RA I/O Control Register (TRAIOC) [in Pulse Output Mode]

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: TRAIO output starts at “H”	R/W
b1	TOPCR	TRAIO output control bit	0: TRAIO output	R/W
b2	TOENA	TRAO output enable bit	1: TRAO output (inverted TRAIO output from P3_7)	R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in pulse output mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

(8) Set the timer RA mode register.

Timer RA Mode Register (TRAMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	1	—	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 1: Pulse output mode	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 1: f8	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source	R/W

(9) Start the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	x	—	x		1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

(10) Wait until the timer RA count starts.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/35A Group User’s Manual: Hardware Rev.0.40
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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Revision History	R8C/35A Group Timer RA (Pulse Output Mode)

Rev.	Date	Description	
		Page	Summary
1.00	July 23, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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