R8C/2D Group

Rewriting the Data Flash Using the Suspend Function in EW1 Mode

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1. Abstract

This document describes the setting method and an application example for rewriting the data flash using the suspend function in EW1 mode with the R8C/2D Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/2D Group
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

This application note describes a method of rewriting for the flash memory after enabling the suspend function in EW1 mode.

3.1 Program Outline

Rewrite block A and block B of the data flash in EW1 mode. The erase operation is halted temporarily when the suspend function is used during erasure. Use timer RA timer mode for interrupts to suspend erase and write operations.

3.1.1 Writing Data in the Data Flash Area

This application note assumes that one record is 64 bytes and each block is divided into 16. Divided areas are used as records 0 to 15. Blocks A and B each have 16 records for a total of 32 records. Figure 3.1 shows the relationship between the data flash and records.

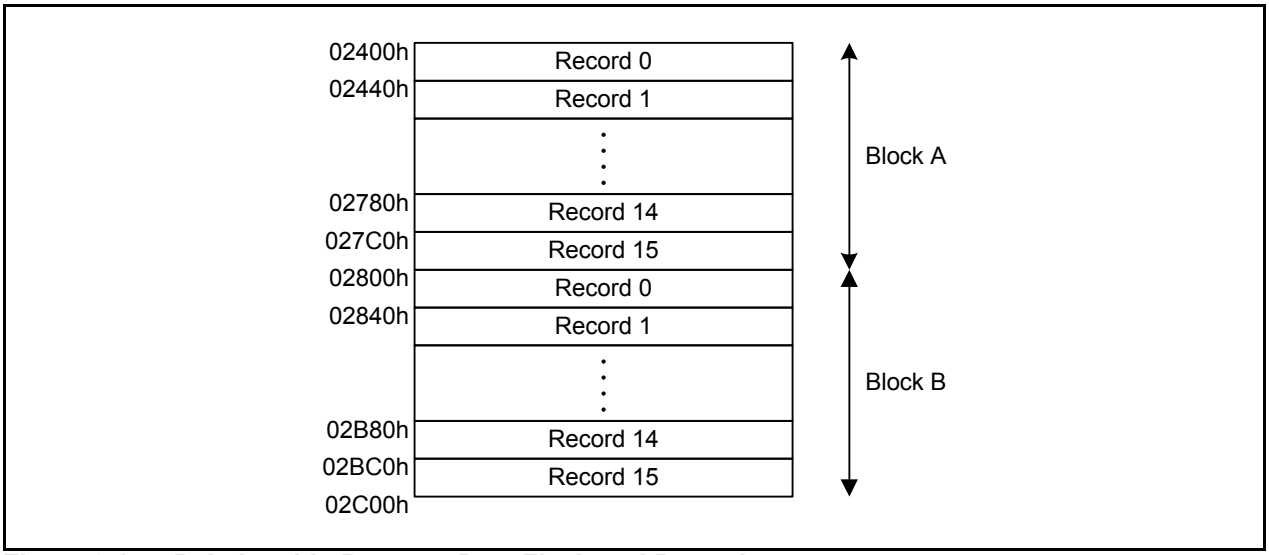


Figure 3.1 Relationship Between Data Flash and Records

When writing data, write in record units starting from record 0 of each block. After writing to record 15, perform a block erase to erase all content from the next block. When writing the next data, start from record 0 in the block which was just erased. After writing to record 15 of block B, erase all content from block A, start writing from record 0 of block A, and repeat these steps.

3.2 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	577 bytes	In the r01an0109_src.c module
RAM	35 bytes	In the r01an0109_src.c module
Maximum user stack	28 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile options: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/2D Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void main (void)		
Outline	Main function		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform main processing. Determine the write and erase results.		

Declaration	void mcu_init (void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (XIN clock).		

Declaration	void timer_ra_init (void)		
Outline	Initial setting of timer RA		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform initial setting of SFRs to use timer RA.		

Declaration	void set_data (unsigned char *data)		
Outline	Write data made		
Argument	Argument name		Meaning
	unsigned char *data		Write data destination starting address
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Make the write data for the data flash. No processing is performed in this application note. Add processing based on the user system.		

Declaration	void write_address_init (void)		
Outline	Initial setting of write record		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char block_select		Block used
	unsigned char *write_addr		Write address
Returned value	Type	Value	Meaning
	None	—	—
Function	Erase block A and block B. Set the starting address of block A (write_addr) and block to be used (block_select).		

Declaration	unsigned char write_control (void)		
Outline	Data write control		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char record_data[RECORD_SIZE]		Record data
	unsigned char *write_addr		Write address
	unsigned char block_select		Block used
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERASE_ERROR	Erase error
		PROGRAM_ERROR	Program error
Function	After writing the record data, update the write address (write_addr). When writing data to the last record (record 15), erase the next block and set the write address.		

Declaration	unsigned char block_erase (unsigned char block_no)		
Outline	Block erase		
Argument	Argument name		Meaning
	unsigned char block_no		Erase block number
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERASE_ERROR	Erase error
		PROGRAM_ERROR	Program error
Function	Erase the specified block in CPU rewrite mode (EW1 mode).		

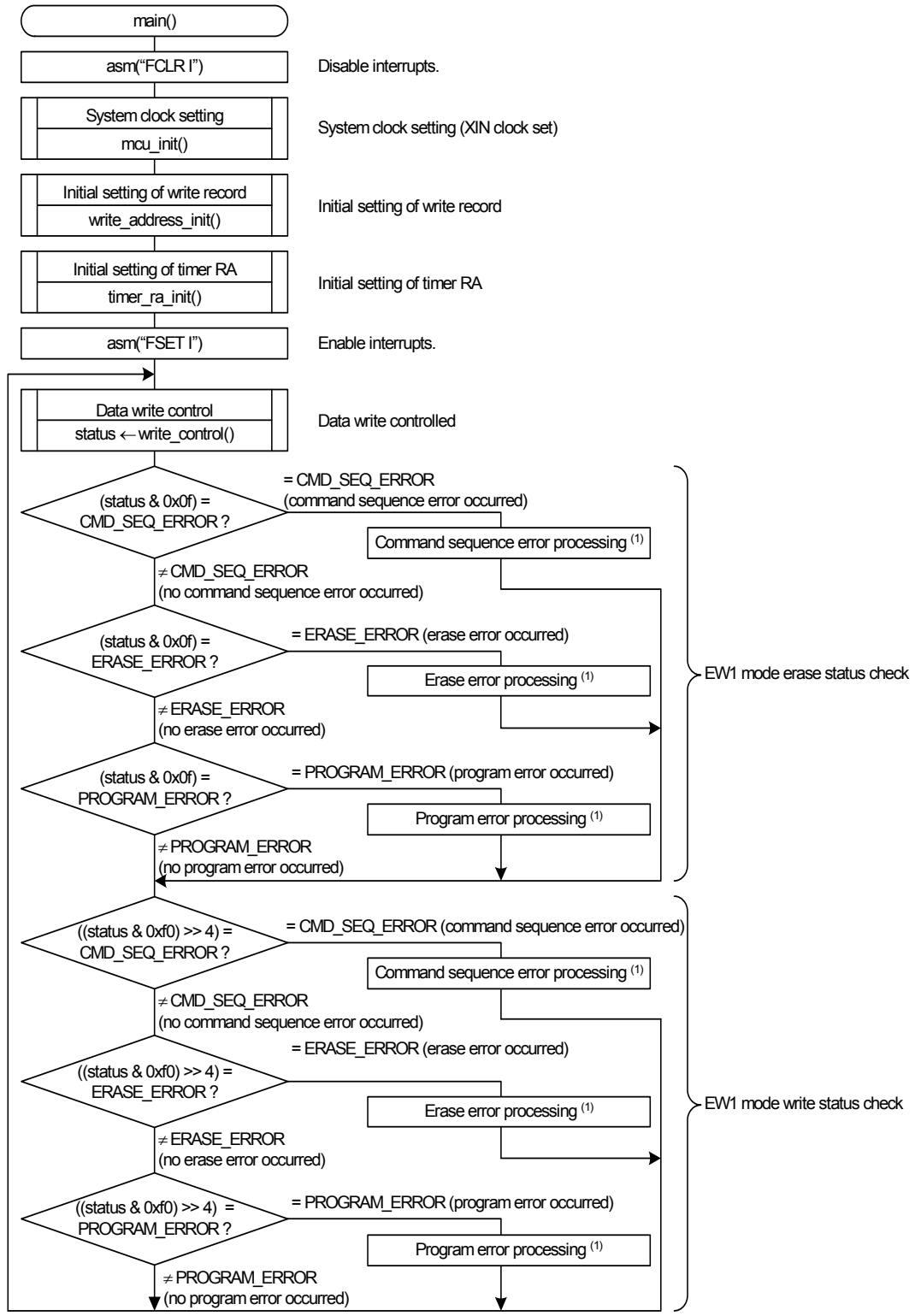
Declaration	unsigned char data_write (unsigned char *data)		
Outline	Data writing		
Argument	Argument name		Meaning
	unsigned char *data		Write data destination starting address
Variable (global)	Variable name		Contents
	unsigned char *write_addr		Write address
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERASE_ERROR	Erase error
		PROGRAM_ERROR	Program error
Function	Write one record of data from the write address (write_addr) in CPU rewrite mode (EW1 mode).		

Declaration	unsigned char full_sts_chk (unsigned char *chk_adr)		
Outline	Full status check		
Argument	Argument name		Meaning
	unsigned char *chk_adr		Address where erase command or program command data is written
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	unsigned char	NORMAL	Completed normally
		CMD_SEQ_ERROR	Command sequence error
		ERASE_ERROR	Erase error
		PROGRAM_ERROR	Program error
Function	Perform full status check.		

Declaration	void_timer_ra (void)		
Outline	Timer RA interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform timer RA interrupt handling. No processing for memory access is performed in this application note. Add processing for memory access based on the user system.		

4.2 Main Function

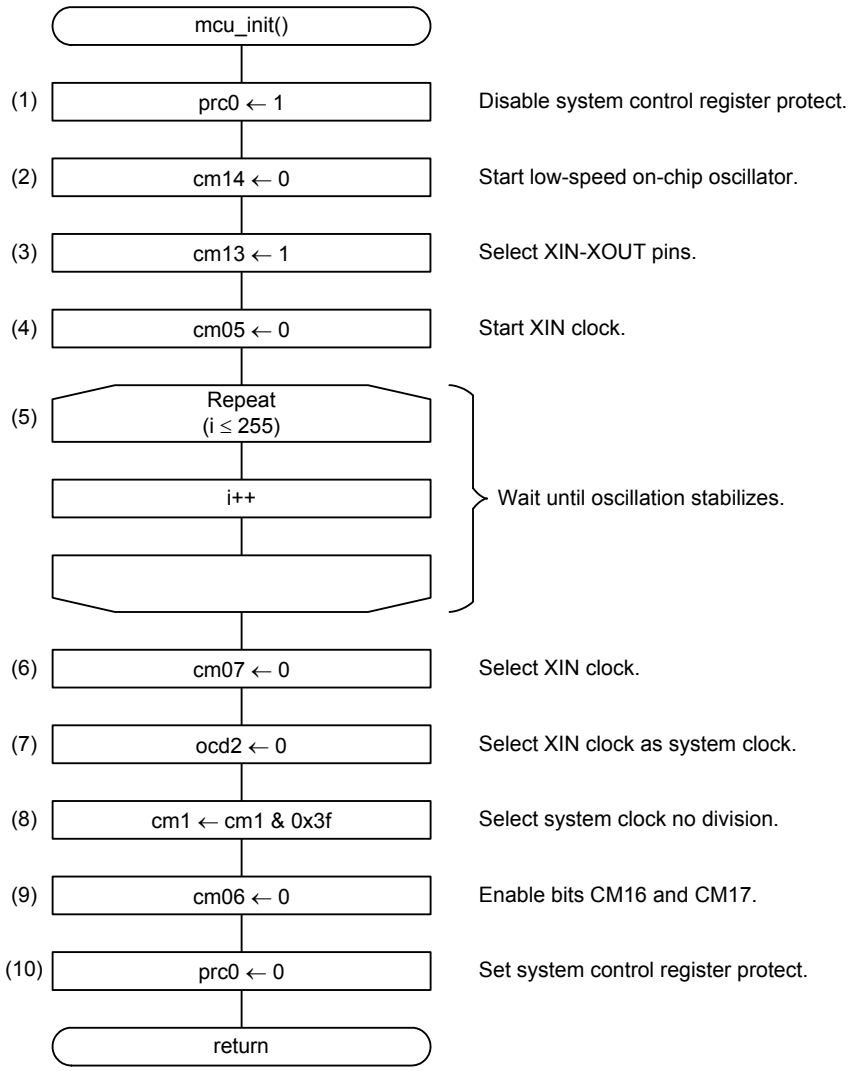
• Flowchart



Note:
1. In this application note, command sequence error processing, erase error processing, and program error processing are not performed. Perform error processing if necessary.

4.3 System Clock Setting

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 1: Write enabled	R/W

(2) Oscillate the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			x	0		x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Switch ports P4_6 and P4_7 to XIN-XOUT pins.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			x		1	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port XIN-XOUT switch bit	1: XIN-XOUT pins	R/W

(4) Oscillate the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(5) Wait until oscillation stabilizes.

(6) Select the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	CPU clock select bit	0: System clock	R/W

(7) Select the XIN clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	0: Selects XIN clock	R/W

(8) Set system clock division select bits 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	x			x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	System clock division select bits 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	System clock division select bit 0	0: CM16, CM17 enabled	R/W

(10) Disable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

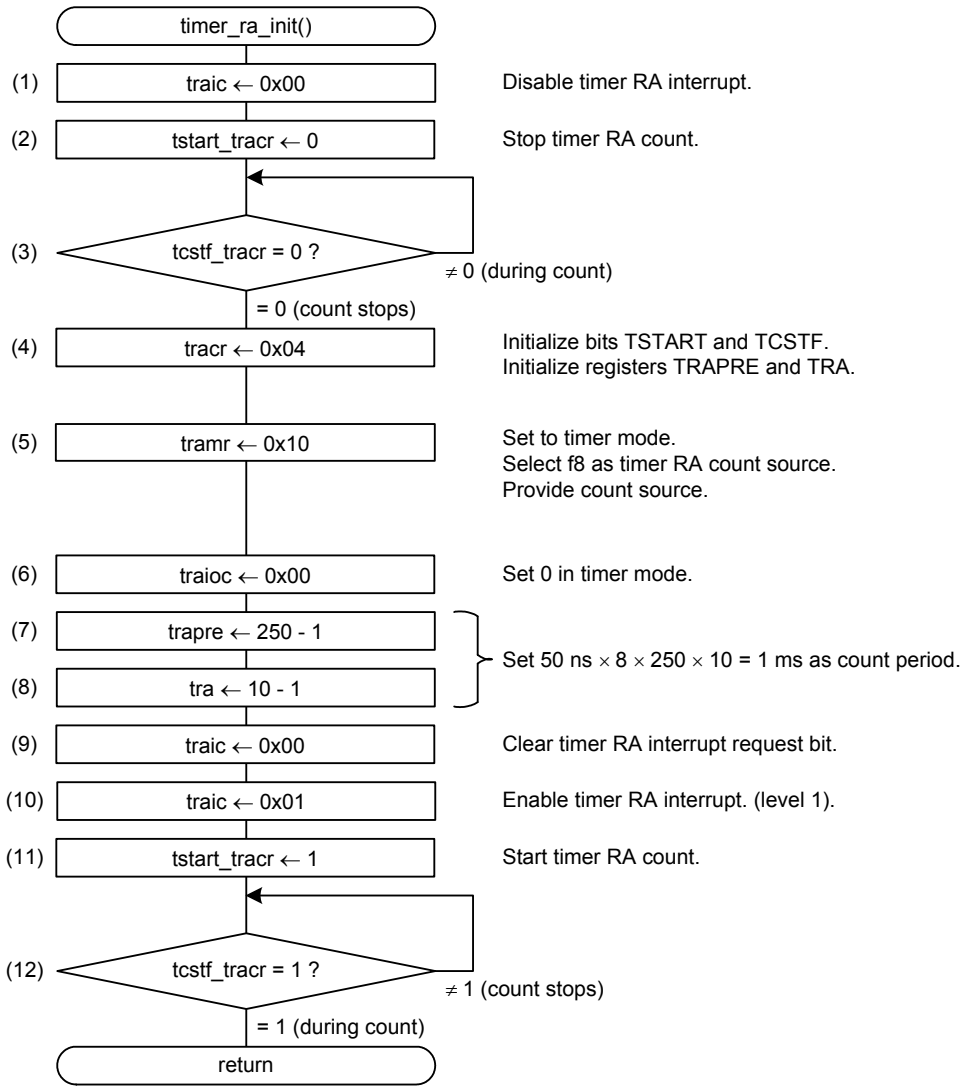
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2. 0: Write disabled	R/W

4.4 Initial Setting of Timer RA

• Flowchart



• Register settings

(1) Disable the timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0: Level 0 (interrupt disable)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: Requests no interrupt	R/W

(2) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	x	—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(3) Wait until the timer RA count stops.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

(4) Initialize bits TSTART and TCSTF, and registers TRAPRE and TRA.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	x	—	1		0

Bit	Symbol	Bit Name	Function	R/W
b2	TSTOP	Timer RA count forcible stop bit	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	R/W

(5) Set the timer RA mode register.

Timer RA Mode Register (TRAMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	1	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bits	b2 b1 b0 0 0 0: Timer mode	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b4	TCK0	Timer RA count source select bits	b6 b5 b4 0 0 1: f8	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source	R/W

(6) Set the timer RA I/O control register.

Timer RA I/O Control Register (TRAIOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0: $\overline{\text{INT1}}$/TRAIO pin (P1_7)	R/W
b4	TIPF0	TRAIO input filter select bits	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W

(7) Set the timer RA prescaler register to 250-1 (F9h).

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	0	0	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W

(8) Set the timer RA register to 10-1 (09h).

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	1	0	0	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts on underflow of timer RA prescaler register	00h to FFh	R/W

(9) Clear the timer RA interrupt request bit.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0			

Bit	Symbol	Bit Name	Function	R/W
b3	IR	Interrupt request bit	0: Requests no interrupt	R/W

(10) Enable the timer RA interrupt (level 1).

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W

(11) Start the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	x	—			1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

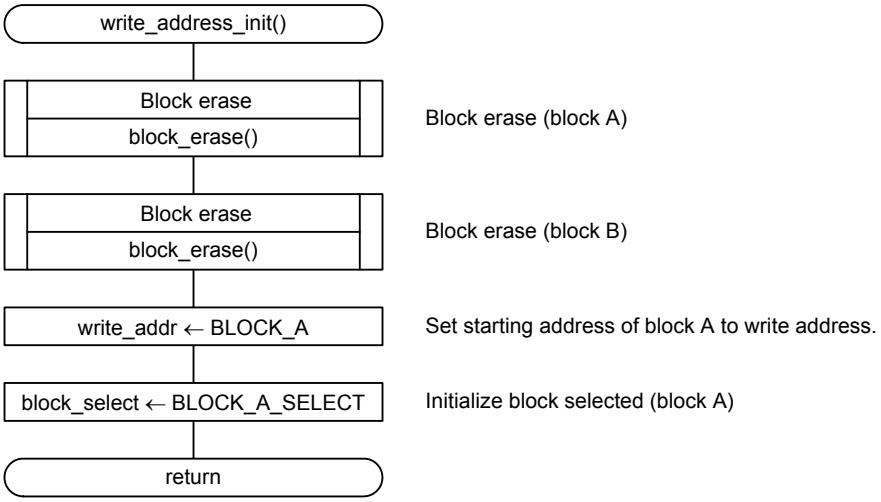
(12) Wait until the timer RA count starts.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R

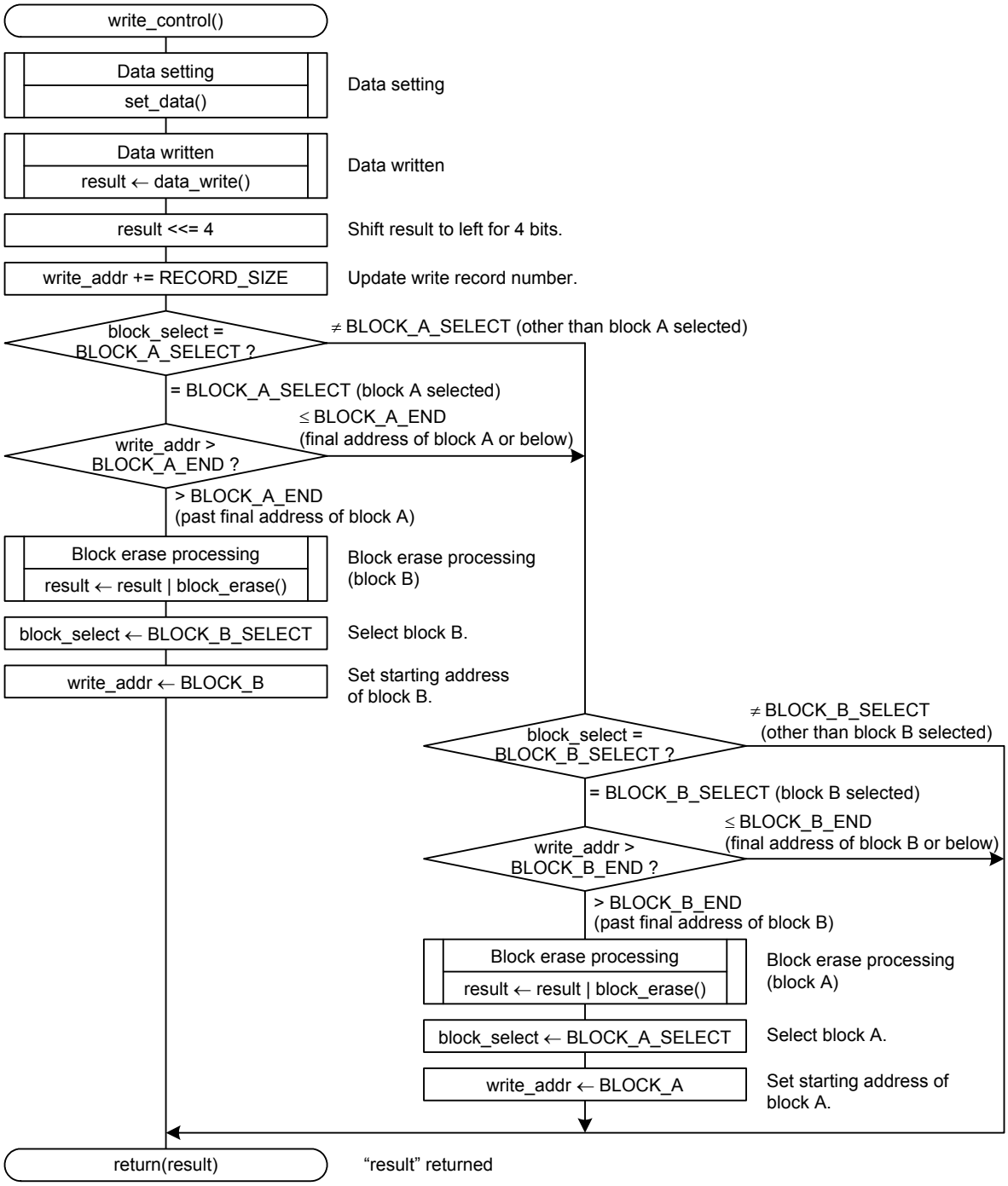
4.5 Initial Setting of Write Record

• Flowchart

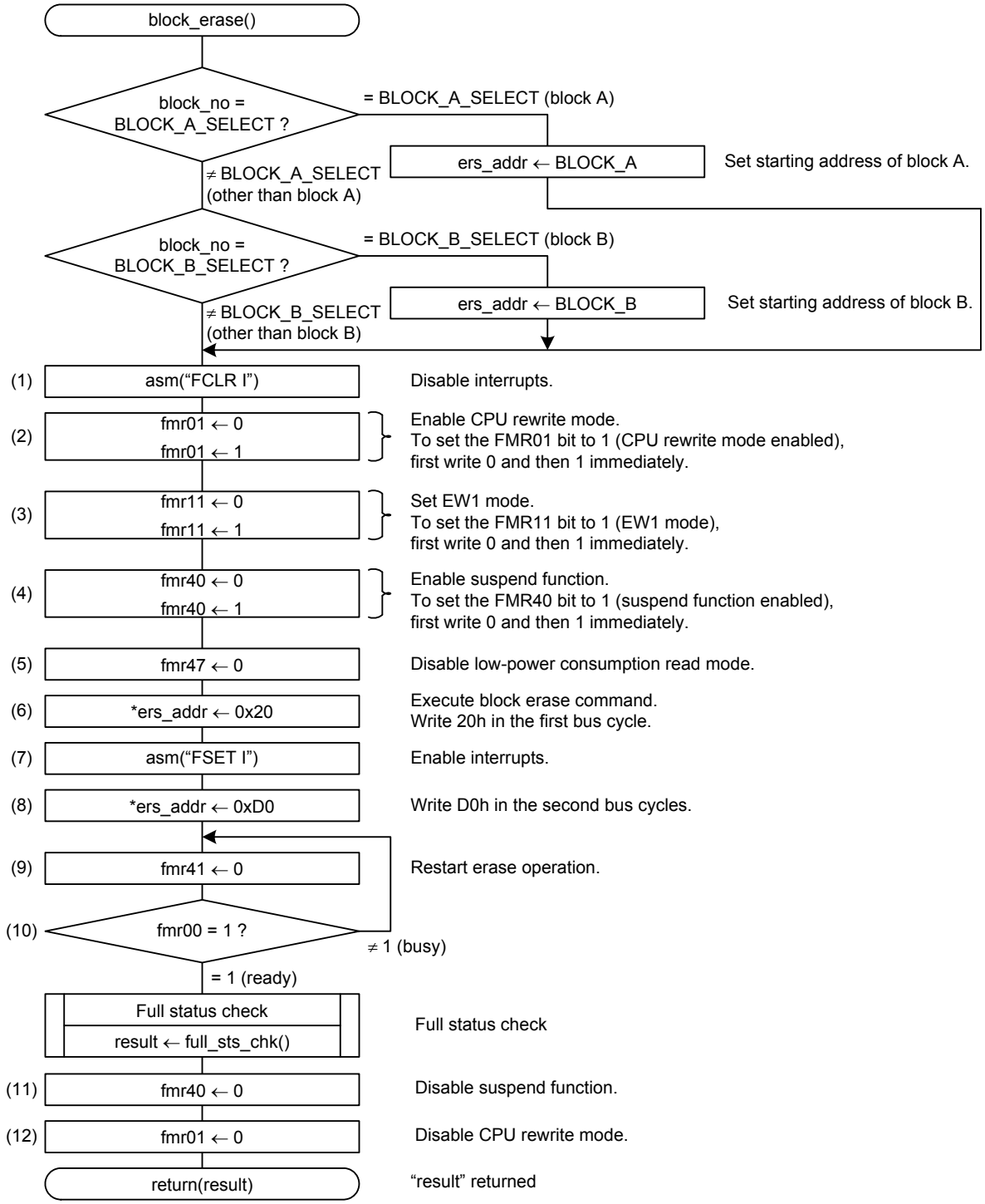


4.6 Data Write Control

• Flowchart



4.7 Block Erase Processing



• Register settings

(1) Clear the I flag to disable interrupts.

(2) Enable CPU rewrite mode. When setting the FMR01 bit to 1, first write 0 and then write 1 immediately.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	—	x	x	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	1: CPU rewrite mode enabled	R/W

(3) Select EW1 mode. When setting the FMR11 bit to 1, first write 0 and then write 1 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	—	—	—	1	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR11	EW1 mode select bit	1: EW1 mode	R/W

(4) Enable suspend function. When setting the FMR40 bit to 1, first write 0 and then write 1 immediately.

Flash Memory Control Register 4 (FMR4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		x	—		x			1

Bit	Symbol	Bit Name	Function	R/W
b0	FMR40	Erase-suspend function enable bit	1: Enable	R/W

(5) Disable low-power consumption read mode.

Flash Memory Control Register 4 (FMR4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	x	—		x			

Bit	Symbol	Bit Name	Function	R/W
b7	FMR47	Low-power consumption read mode enable bit	0: Disable	R/W

(6) Write block erase command 20h to a given address in the block to be erased in the first bus cycle.

(7) Set the I flag to enable interrupts.

(8) Erasure (erase and erase verify) starts by writing confirmation command D0h in the second bus cycle.

(9) Restart erase operation.

Flash Memory Control Register 4 (FMR4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		x	—		x		0	

Bit	Symbol	Bit Name	Function	R/W
b1	FMR41	Erase-suspend request bit	0: Erase restart	R/W

(10) Wait until erase operation (suspend period included) is completed.

Flash Memory Control Register 0 (FMR0)

Bit	Symbol	Bit Name	Function	R/W
b0	FMR00	RY/$\overline{\text{BY}}$ status flag	0: Busy 1: Ready	R

(11) Disable the suspend function.

Flash Memory Control Register 4 (FMR4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		x	—		x			0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR40	Erase-suspend function enable bit	0: Disable	R/W

(12) Disable CPU rewrite mode.

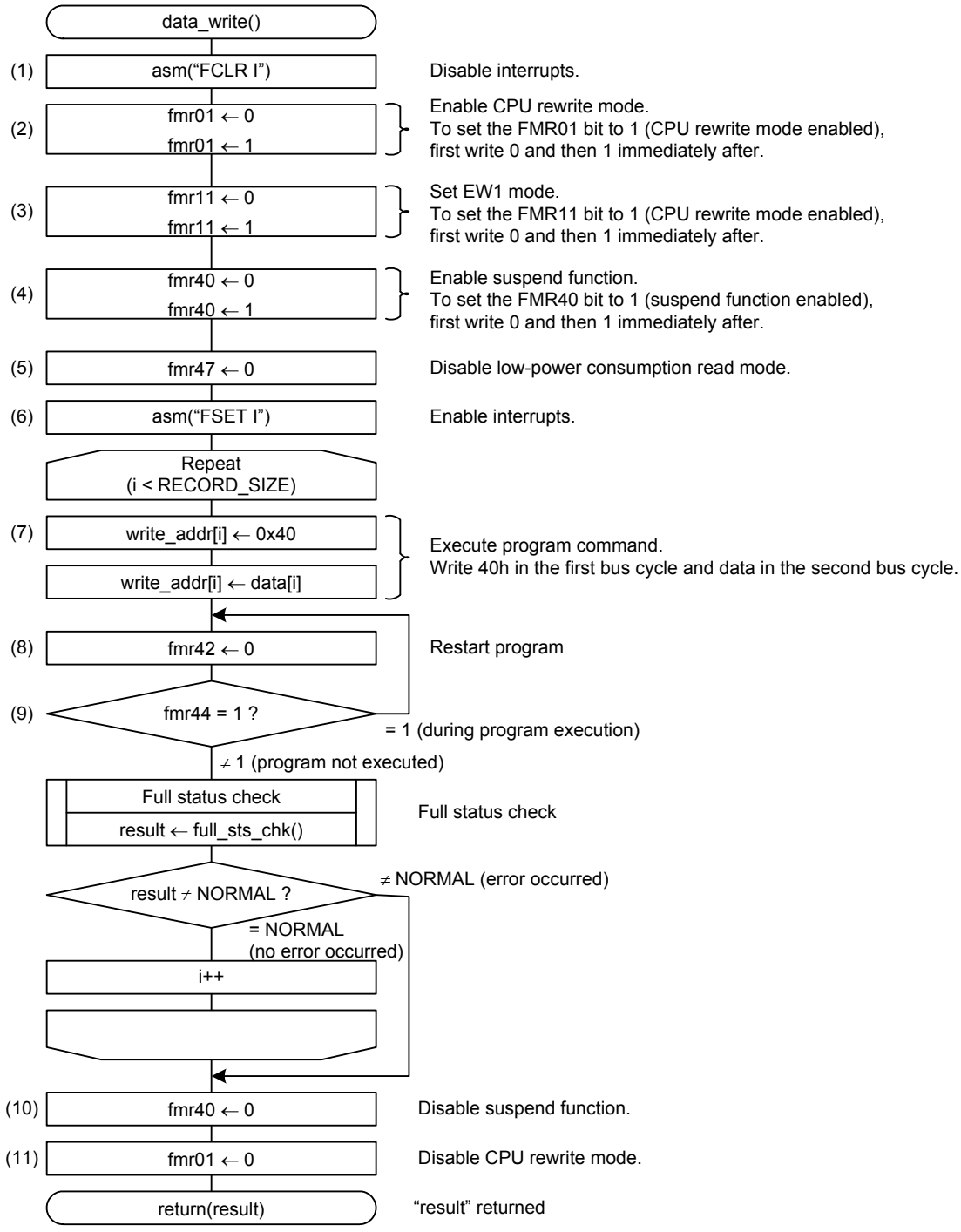
Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	—	x	x	0	

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

4.8 Data Writing

• Flowchart



• Register settings

(1) Clear the I flag to disable interrupts.

(2) Enable CPU rewrite mode. When setting the FMR01 bit to 1, first write 0 and then write 1 immediately.

Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	—	x	x	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	1: CPU rewrite mode enabled	R/W

(3) Select EW1 mode. When setting the FMR11 bit to 1, first write 0 and then 1 immediately.

Flash Memory Control Register 1 (FMR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	—	—	—	1	—

Bit	Symbol	Bit Name	Function	R/W
b1	FMR11	EW1 mode select bit	1: EW1 mode	R/W

(4) Enable suspend function. When setting the FMR40 bit to 1, first write 0 and then write 1 immediately.

Flash Memory Control Register 4 (FMR4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		x	—		x			1

Bit	Symbol	Bit Name	Function	R/W
b0	FMR40	Erase-suspend function enable bit	1: Enable	R/W

(5) Disable low-power consumption read mode.

Flash Memory Control Register 4 (FMR4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	x	—		x			

Bit	Symbol	Bit Name	Function	R/W
b7	FMR47	Low-power consumption read mode enable bit	0: Disable	R/W

(6) Set the I flag to enable interrupts.

(7) Writing (data programmed and verified) starts by writing program command 40h in the first bus cycle to the write address and data in the second bus cycle. Set the same address value in the second bus cycle as the address value specified in the first bus cycle.

(8) Restart the program.

Flash Memory Control Register 4 (FMR4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		x	—		x	0		

Bit	Symbol	Bit Name	Function	R/W
b2	FMR42	Program-suspend request bit	0: Program restart	R/W

(9) Wait until writing is completed.

Flash Memory Control Register 4 (FMR4)

Bit	Symbol	Bit Name	Function	R/W
b4	FMR44	Program command flag	0: Program not executed 1: Program execution in progress	R

(10) Disable the suspend function.

Flash Memory Control Register 4 (FMR4)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		x	—		x			0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR40	Erase-suspend function enable bit	0: Disable	R/W

(11) Disable CPU rewrite mode.

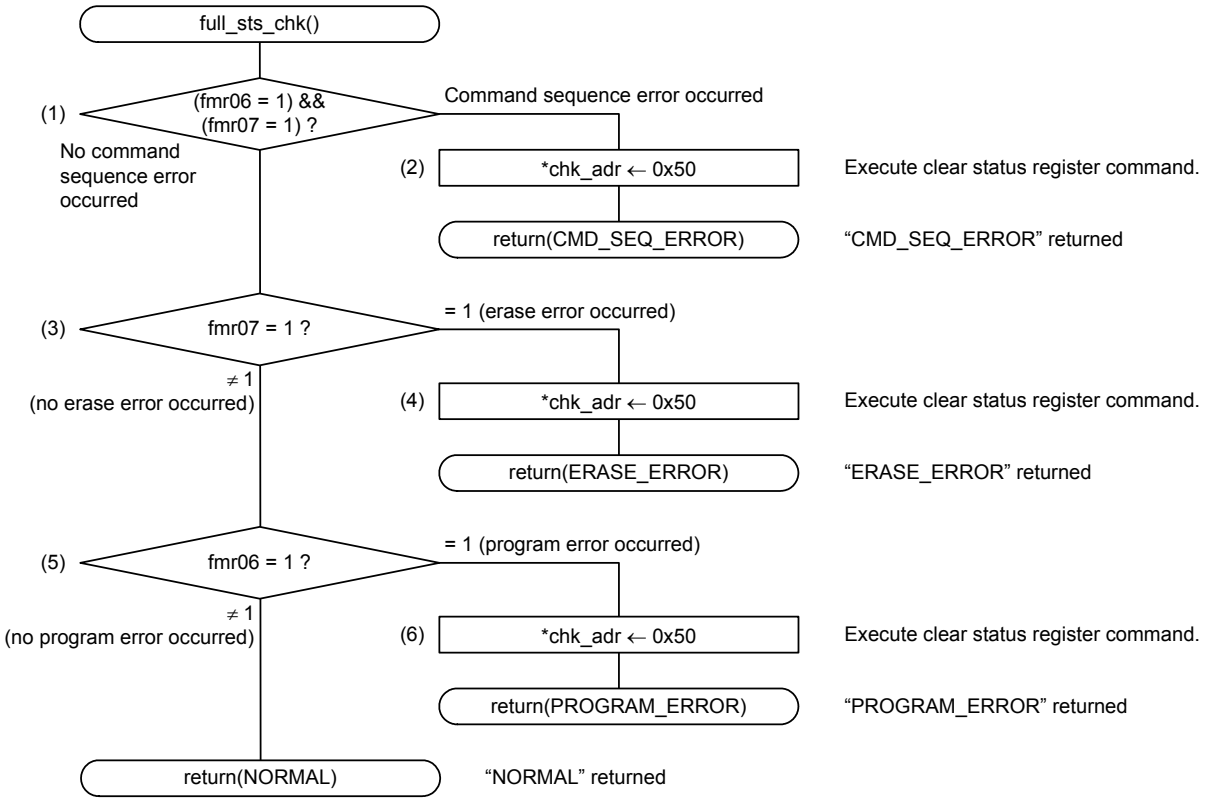
Flash Memory Control Register 0 (FMR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	—	x		0	

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

4.9 Full Status Check

• Flowchart



• Register settings

(1) Confirm that a command sequence error occurs by reading bits FMR06 and FMR07 in the FMR0 register.

Flash Memory Control Register 0 (FMR0)

Bit	Symbol	Bit Name	Function	R/W
b6	FMR06	Program status flag	0: Completed successfully 1: Terminated by error	R
b7	FMR07	Erase status flag	0: Completed successfully 1: Terminated by error	R

(2) Write clear status register command 50h to the address where erase command 20h or program command 40h was written when a command sequence error (FMR06 bit is 1 and FMR07 is 1) occurs.

(3) Confirm that an erase error occurs by reading the FMR07 bit.

Flash Memory Control Register 0 (FMR0)

Bit	Symbol	Bit Name	Function	R/W
b7	FMR07	Erase status flag	0: Completed successfully 1: Terminated by error	R

(4) Write clear status register command 50h to the address where erase command 20h was written when an erase error (the FMR07 bit is 1) occurs.

(5) Confirm that a program error occurs by reading the FMR06 bit.

Flash Memory Control Register 0 (FMR0)

Bit	Symbol	Bit Name	Function	R/W
b6	FMR06	Program status flag	0: Completed successfully 1: Terminated by error	R

(6) Write clear status register command 50h to the address where program command 40h was written when a program error (FMR06 bit is 1) occurs.

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/2D Group User’s Manual: Hardware Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
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Revision History	R8C/2D Group Rewriting the Data Flash Using the Suspend Function in EW1 Mode

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 18, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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