R8C/29 Group and R8C/32C Group

Differences between R8C/29 Group and R8C/32C Group

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1. Abstract

This document is reference material for identifying differences between the R8C/29 Group and R8C/32C Group.

2. Introduction

This document applies to the following microcomputers (MCUs):

- MCUs: R8C/29 Group and R8C/32C Group

3. Upward Compatibility of Functions

Since the R8C/32C Group is an upward compatible product of the R8C/29 Group, replacing the R8C/29 Group with the R8C/32C Group is easy. For more details, refer to 4. Group Differences and the hardware user's manual.

3.1 Upward Compatibility of Functions

Additional functions for the R8C/32C Group are as follows:

(1) Add detection level selections to voltage detection 0 and voltage detection 1.
(2) Add a data transfer controller (DTC).
(3) Add a low-speed on-chip oscillator for the watchdog timer.
(4) Add event input control to timer RA.
(5) Add A/D trigger generation to timer RC.
(6) Add one channel of the serial interface (UART2) with clock synchronous serial I/O mode, clock asynchronous serial I/O mode (UART mode), special mode (I^2C mode), and multiprocessor communication function.
(7) Add bus collision detection to the hardware LIN during Synch Break transmission.
(8) Add repeat mode 1, single sweep mode, and repeat sweep mode to A/D converter operating mode. Add timer RC and an external trigger for the A/D conversion start conditions of repeat mode 0. Add AD1 to AD7 to the storage registers for the A/D conversion results.
(9) Add comparator B.
(10) Add a data protect function and background operation (BGO) function to the flash memory. Add two blocks of data flash.

4. Group Differences

4.1 Function and Specification Differences

Table 4.1 to Table 4.6 list differences in the functions and specifications. For more details regarding pin function differences, refer to 4.2 Pin Function Differences.

Table 4.1 Function and Specification Differences (1) (1)

Item		R8C/29 Group	R8C/32C Group
Memory	ROM/RAM	• 8 KB/512 B •16 KB/1 KB • 32 KB/1.5 KB	• 4 KB/512 B • 8 KB/1 KB • 16 KB/1.5 KB
Reset		• Reset source determination function: Not included • CPU clock after reset: low-speed on-chip oscillator divided by 8 • Flash memory start time of reset sequence: 14 cycles of CPU clock	• Reset source determination function: Included • CPU clock after reset: low-speed on-chip oscillator no division • Flash memory start time of reset sequence: 148 cycles of CPU clock
Voltage detection circuits	Voltage detection 0	• Voltage monitor 0: Included (2) • Detection voltage cannot be selected. • Digital filter function: Included (digital filter can be selected as included or not included)	• Voltage monitor 0: Included • Detection voltage can be selected (four levels). • Digital filter function: Not included
	Voltage detection 1	• Detection voltage cannot be selected. • Detection edge cannot be selected. • Digital filter sampling time: (fOCO-S divided by n) x 4 n: 1, 2, 4, 8 • Voltage monitor 1 reset: Included • Voltage monitor 1 interrupt: Included (2) (non-maskable interrupt fixed) • Monitor: Included (2)	• Detection voltage can be selected (16 levels). • Detection edge can be selected (one edge or both edges). • Digital filter sampling time: (fOCO-S divided by n) x 2 n: 1, 2, 4, 8 • Voltage monitor 1 reset: Not included • Voltage monitor 1 interrupt: Included (non-maskable interrupt or maskable interrupt can be selected) • Monitor: Included
	Voltage detection 2	• Detection edge cannot be selected. • Digital filter sampling time: (fOCO-S divided by n) x 4 n: 1, 2, 4, 8 • Voltage monitor 2 reset: Included • Voltage monitor 2 interrupt: Included (non-maskable interrupt fixed)	• Detection edge can be selected (one edge or both edges). • Digital filter sampling time: (fOCO-S divided by n) x 2 n: 1, 2, 4, 8 • Voltage monitor 2 reset: Not included • Voltage monitor 2 interrupt: Included (non-maskable interrupt or maskable interrupt can be selected.)

Notes:
1. Refer to the hardware user's manual for details and electrical characteristics.
2. This only applies to the N and D versions in the R8C/29 Group.

Table 4.2 Function and Specification Differences (2) (1)

Item	R8C/29 Group	R8C/32C Group
I/O ports	• I/O ports: 13 • Input ports: 3 • Input threshold value cannot be selected. • Drive capacity cannot be controlled. • Ports for LED drive: 8 (2) • Port input function cannot be selected.	• I/O ports: 15 • Input port: 1 • Input threshold value can be selected. • Drive capacity can be controlled. • High current drive ports: 15 • Port input function can be selected (selectable dependent/not dependent on the direction register).
Clock generation circuits	• XCIN clock oscillation circuit can be used. (2) • Wait control bit (CM30): Not included • CPU clock cannot be selected when exiting wait mode or stop mode. • Clock source for fOCO128 depends on the FRA01 bit. • fC cannot be selected as the peripheral function clock. • Low-speed on-chip oscillator for watchdog timer: Not included • XIN-XOUT drive capacity can be selected. • XCIN-XCOUT drive capacity can be selected.	• XCIN clock oscillation circuit can be used. • Wait control bit (CM30): Included • CPU clock can be selected when exiting wait mode or stop mode. • Clock source for fOCO128 depends on the FRA03 bit. • fC can be selected as the peripheral function clock. • Low-speed on-chip oscillator for watchdog timer: Included • XIN-XOUT drive capacity cannot be selected. • XCIN-XCOUT drive capacity cannot be selected.
High-speed on-chip oscillator	• Divide-by-2 or divide-by-3 for high-speed on-chip oscillator clock division ratio cannot be selected. (3) • No correction value for 32 MHz • Frequency correction data for all supply voltage ranges: Necessary	• Divide-by-2 or divide-by-3 for high-speed on-chip oscillator clock division ratio can be selected. • Correction value for 32 MHz • Frequency correction data for all supply voltage ranges: Not necessary
Interrupts	• Interrupt sources: 24 (2) • External interrupt inputs: 7 ($\overline{\text{INT}}$ x 3, key input x 4)	• Interrupt sources: 30 • External interrupt inputs: 7 ($\overline{\text{INT}}$ x 3, key input x 4)
Watchdog timer	• Underflow period cannot be selected when the count source protection mode is enabled. • Refresh acknowledgement period cannot be selected. • 15 bits x 1 channel	• Underflow period can be selected when the count source protection mode is enabled (four steps). • Refresh acknowledgement period can be selected (four steps). • 14 bits x 1 channel
DTC	Not included	Included

Notes:
1. Refer to the hardware user's manual for details and electrical characteristics.
2. These only apply to the N and D versions in the R8C/29 Group.
3. This only applies to the K version in the R8C/29 Group.

Table 4.3 Function and Specification Differences (3) (1)

Item		R8C/29 Group	R8C/32C Group
Timer RA	Count source	• fC32 can be selected. (2) • fC cannot be selected.	• fC32 can be selected. • fC can be selected.
	–	Event input control function: Not included	Event input control function: Included
Timer RC	Count source	• fOCO-F cannot be selected.	• fOCO-F can be selected.
	–	Module operation enable bit (MSTTRC bit): Not included	Module operation enable bit (MSTTRC bit): Included
	Output compare function	• TRCGRC register cannot be used to control TRCIOA pin output. • TRCGRD register cannot be used to control TRCIOB pin output. • A/D trigger is not generated.	• TRCGRC register can be used to control TRCIOA pin output. • TRCGRD register can be used to control TRCIOB pin output. • A/D trigger generation can be selected.
	PWM mode	• Use shared bit to set active level/initial output. • A/D trigger is not generated.	• Use each bit to set active level/initial output. • A/D trigger generation can be selected.
	PWM2 mode	A/D trigger is not generated.	A/D trigger generation can be selected.
Timer RE (real-time clock mode)		Included (2)	Included
Timer RE (output compare mode)	Count source	fC4 can be selected. (2)	fC4 can be selected.
Serial interface (UART0)	Count source	fC cannot be selected.	fC can be selected.
Serial interface (UART1)		Included	Not included
Serial interface (UART2)		Not included	Included
Clock synchronous serial interface (synchronous serial communication unit)		• Module operation enable bit (MSTIIC bit): Not included • Transfer data length: 8 bits fixed • Transmit/receive data register length: 8 bits	• Module operation enable bit (MSTIIC bit): Included • Transfer data length: 8 bits to 16 bits can be selected. • Transmit/receive data register length: 16 bits
Clock synchronous serial interface (I^2C-bus interface)		• Module operation enable bit (MSTIIC bit): Not included • Double or half transfer cannot be selected. • SDA digital delay: Not included	• Module operation enable bit (MSTIIC bit): Included • Double or half transfer can be selected. • SDA digital delay: Included (three steps)
Hardware LIN		Bus collision during Sync Break transmission cannot be detected.	Bus collision during Sync Break transmission can be detected (enable/disable can be switched).

Notes:
1. Refer to the hardware user's manual for details and electrical characteristics.
2. These only apply to the N and D versions in the R8C/29 Group.

Table 4.4 Function and Specification Differences (4) (1)

Item		R8C/29 Group	R8C/32C Group
A/D converter	Operating modes	• One-shot mode • Repeat mode	• One-shot mode • Repeat mode 0 • Repeat mode 1 • Single sweep mode • Repeat sweep mode
	A/D conversion start conditions	• Software trigger	• Software trigger • Timer RC • External trigger
	Registers for storing A/D conversion results	One	Eight
	Operating clocks (ϕAD)	• f1, f2, f4, and fOCO-F	• fAD, fAD divided by 2, fAD divided by 4, fAD divided by 8 (fAD = f1 or fOCO-F)
	Conversion rate (2)	33 ϕAD cycles	Minimum 44 ϕAD cycles
	Sample and hold function	Included or not included: Can be selected	Included or not included: Cannot be selected (fixed as included)
	On-chip reference voltage	Not included	Included
Comparator B		Not included	Included

Notes:
1. Refer to the hardware user's manual for details and electrical characteristics.
2. The conversion rate is based on the conditions of one-shot mode, 10-bit resolution, and the sample and hold function.

Table 4.5 Function and Specification Differences (5) (1)

Item	R8C/29 Group	R8C/32C Group
Flash memory	• Program ROM size is 8 KB or 16 KB per block. • Data flash area: 1 KB × 2 blocks • Data protect function: Not included • BGO function: Not included • Erase/write error interrupt: Not included • Flash access error interrupt : Not included • Flash ready status interrupt: Not included • Rewrite control program in EW0 mode is executed in areas other than flash memory. •Mode after program or erase in EW0 mode: Read status register mode • Rewrite control for program ROM area: Each block can be controlled by the rewrite disable bits (FMR15 and FMR16) in blocks 0 and 1. • Rewrite control for data flash area: Individual blocks cannot be controlled. • CPU clock limit in EW0 mode: 5 MHz or below • Program suspend function: Included • Read status register command: Included • Lock bit program command: Not included • Read lock bit status command: Not included • Block blank check command: Not included	• Program ROM size is 2 KB, 4 KB, or 8 KB per block. • Data flash area: 1 KB × 4 blocks • Data protect function: Included • BGO function: Included • Erase/write error interrupt: Included • Flash access error interrupt: Included • Flash ready status interrupt: Included • Rewrite control program in EW0 mode can be executed in program ROM area when data flash area is rewritten. • Mode after program or erase in EW0 mode: Read array mode • Rewrite control for program ROM area: Each block can be controlled by the lock bit disable select bit (FMR13) and software command. • Rewrite control for data flash area: Each block can be controlled by block A, block B, block C, and block D rewrite disable bits (FMR14, FMR15, FMR16, and FMR17). • CPU clock limit in EW0 mode: 20 MHz or below • Program suspend function: Not included • Read status register command: Not included • Lock bit program command: Included • Read lock bit status command: Included • Block blank check command: Included

Note:
1. Refer to the hardware user's manual for details and electrical characteristics.

Table 4.6 Function and Specification Differences (6) (1)

Item	R8C/29 Group	R8C/32C Group
Supply voltage	• VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (2) • VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz)(3) • VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) • VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (4)	• VCC = 2.7 to 5.5 V (f(XIN) = 20 MHz) • VCC = 1.8 to 5.5 V (f(XIN) = 5 MHz)
Low current consumption	• Typical 10 mA (4) (VCC = 5 V, f(XIN) = 20 MHz) • Typical 6 mA (4) (VCC = 3 V, f(XIN) = 10 MHz) • Typical 2.0 μA (4) (VCC = 3 V, wait mode) (f(XCIN) = 32 kHz) • Typical 0.7 μA (4) (VCC = 3 V, stop mode)	• Typical 6.5 mA (VCC = 5 V, f(XIN) = 20 MHz) • Typical 3.5 mA (VCC = 3 V, f(XIN) = 10 MHz) • Typical 3.5 μA (VCC = 3 V, wait mode) (f(XCIN) = 32 kHz) • Typical 2.0 μA (VCC = 3 V, stop mode)

Notes:
1. Refer to the hardware user's manual for details and electrical characteristics.
2. This applies to all versions except for the K version in the R8C/29 Group.
3. This only applies to the K version in the R8C/29 Group.
4. These only apply to the N and D versions in the R8C/29 Group.

4.2 Pin Function Differences

Table 4.7 lists pin function differences.

Table 4.7 Pin Function Differences

Pin Name	R8C/29 Group	R8C/32C Group
XCIN	P4_6 (1)	P4_6
XCOUT	P4_7 (1)	P4_7
TRCCLK	P3_3	P3_3, P1_4
TRCIOC	P3_4	P3_4, P1_3
TRCIOD	P3_5	P3_5, P1_0
RXD1	P4_5, P3_7	—
TXD1	P3_7	—
CLK2	—	P3_5
RXD2	—	P4_5, P3_7, P3_4
TXD2	—	P3_7, P3_4
$\overline{\text{CTS2}}$	—	P3_3
$\overline{\text{RTS2}}$	—	P3_3
SCL2	—	P4_5, P3_7, P3_4
SDA2	—	P3_7, P3_4
SDA	P3_4	P3_7
SSI	P3_3, P1_6	P3_4
$\overline{\text{SCS}}$	P3_4	P3_3
$\overline{\text{ADTRG}}$	—	P4_5
IVCMP1	—	P1_7
IVCMP3	—	P3_3
IVREF1	—	P1_6
IVREF3	—	P3_4

Note:
1. These only apply to the N and D versions in the R8C/29 Group.

4.3 SFR Differences

Table 4.8 to Table 4.12 list differences in the SFRs.

Table 4.8 SFR Differences (1)

R8C/29 Group	R8C/32C Group	Remarks
—	RSTFR	
—	CMPA	
—	VCAC	
VCA1	VCA1	Allocation addresses are different.
VCA2	VCA2	• Bit 5 added (1) • Allocation addresses are different.
—	VD1LS	
VW0C	VW0C	• Reset values are different. • Bits 1 and 4 to 7 deleted
VW1C	VW1C	• Reset values are different. • Bits 2 and 3 added (1) • Bit 6 deleted • Allocation addresses are different.
VW2C	VW2C	• Reset values are different. • Bit 6 deleted • Allocation addresses are different.
P1	P1	Reset values are different.
P3	P3	Reset values are different.
P4	P4	Reset values are different.
PD4	PD4	Bits 6 and 7 added
PINSR1	—	
PINSR2	—	
PINSR3	—	• Bit 3 moved to bits 0 and 1 in TRCPSR1 register and functions added • Bit 4 moved to bits 4 and 5 in TRCPSR1 register and functions added
PMR	—	• Functions in bits 3 to 6 deleted • Bit 7 moved to bit 0 in SSUIICSR register.
—	TRASR	
—	TRBRCSR	
—	TRCPSR0	
—	TRCPSR1	
—	U0SR	
—	U2SR0	
—	U2SR1	
—	SSUIICSR	
—	INTSR	
—	PINSR	
PUR0	PUR0	Allocation addresses are different.
PUR1	PUR1	Functions added to bit 1 and allocation addresses are different.

Note:
1. These only apply to the J and K versions in the R8C/29 Group.

Table 4.9 SFR Differences (2)

R8C/29 Group	R8C/32C Group	Remarks
P1DRR (1)	P1DRR	Allocation addresses are different.
—	DRR0	
—	DRR1	
—	VLT0	
—	VLT1	
CM0	CM0	• Reset values are different. • Functions in bits 3 and 4 changed and bit 7 added
CM1	CM1	Bit 5 deleted
—	CM3	
CPSRF (1)	CPSRF	
FRA0	FRA0	Bit 3 added
—	FRA3	
FRA4 (1)	FRA4	Functions are different.
—	FRA5	
FRA6 (1)	FRA6	Functions are different.
FRA7 (1)	FRA7	Functions and allocation addresses are different.
PRCR	PRCR	Functions in bits 0 and 3 changed
—	FMRDYIC	
—	S2TIC	
—	S2RIC	
S1TIC	—	
S1RIC	—	
—	U2BCNIC	
—	VCMP1IC	
—	VCMP2IC	
INTEN	INTEN	Allocation addresses are different.
INTF	INTF	Allocation addresses are different.
KIEN	KIEN	Allocation addresses are different.
AIER	AIER0	• Register name changed and allocation addresses are different. • Functions in bit 1 moved to bit 0 in AIER1 register.
—	AIER1	
RMAD0	RMAD0	Allocation addresses and reset values are different.
RMAD1	RMAD1	Allocation addresses and reset values are different.
WDC	WDTC	• Reset values are different. • Register name changed and bit 5 added

Note:
1. These only apply to the N and D versions in the R8C/29 Group.

Table 4.10 SFR Differences (3)

R8C/29 Group	R8C/32C Group	Remarks
—	DTCTL	
—	DTCEN0	
—	DTCEN1	
—	DTCEN2	
—	DTCEN3	
—	DTCEN5	
—	DTCEN6	
—	DTCVCT0 to DTCVCT63 (1)	
—	DTCD0 to DTCD23	
TRAIOC	TRAIOC	• Functions in bit 3 changed • Functions in bit 3 moved to bits 0 and 1 in TRASR register, and bit 1 in INTSR register • Bits 6 and 7 added
TRAMR	TRAMR	Functions added to bits 4 to 6
—	MSTCR	
TRCCR1	TRCCR1	Functions added to bits 4 to 6
TRCIOR1	TRCIOR1	Bits 3 and 7 added
TRCCR2	TRCCR2	Bits 0 to 2 added
—	TRCADCR	
TREHR (2)	TREHR	
TREWK (2)	TREWK	
TRECSR (2)	TRECSR	Functions added to bits 0 and 1.

Notes:
1. DTC transfer vector area (2C00h to 2C3Fh)
2. These only apply to the N and D versions in the R8C/29 Group.

Table 4.11 SFR Differences (4)

R8C/29 Group	R8C/32C Group	Remarks
U0C0	U0C0	Functions added to bits 0 and 1
U1MR	—	
U1BRG	—	
U1TB	—	
U1C0	—	
U1C1	—	
U1RB	—	
—	U2MR	
—	U2BRG	
—	U2TB	
—	U2C0	
—	U2C1	
—	U2RB	
—	URXDF	
—	U2SMR	
—	U2SMR2	
—	U2SMR3	
—	U2SMR4	
—	U2SMR5	
—	SSBR	
SSTDR/ICDRT	SSTDR/ICDRT	SSTDR register sizes and allocation addresses are different.
—	SSTDRH	
SSRDR/ICDRR	SSRDR/ICDRR	SSRDR register sizes and allocation addresses are different.
—	SSRDRH	
SSCRH/ICCR1	SSCRH/ICCR1	Allocation addresses are different.
SSCRL/ICCR2	SSCRL/ICCR2	Allocation addresses are different.
SSMR/ICMR	SSMR/ICMR	• Reset values are different. • Allocation addresses are different and bit 3 added (only for SSMR register).
SSMR2/SAR	SSMR2/SAR	Allocation addresses are different.
SSER/ICIER	SSER/ICIER	Allocation addresses are different.
SSSR/ICSR	SSSR/ICSR	Allocation addresses are different.
—	LINCR2	

Table 4.12 SFR Differences (5)

R8C/29 Group	R8C/32C Group	Remarks
—	OCVREFCR	
AD	AD0	Register name changed
—	AD1	
—	AD2	
—	AD3	
—	AD4	
—	AD5	
—	AD6	
—	AD7	
—	ADMOD	
—	ADINSEL	
ADCON0	ADCON0	• Functions in bits 0 to 2 moved to bits 0 to 2 in ADINSEL register • Functions in bit 3 moved to bits 3 to 5 in ADMOD register and functions added • Functions in bit 4 moved to bits 6 and 7 in ADINSEL register and functions added • Functions in bit 6 moved to bit 0 • Functions in bit 7 moved to bits 0 to 2 in ADMOD register and functions added
ADCON1	ADCON1	• Bit 0 added • Functions in bit 3 moved to bit 4 • Functions in bit 4 moved to bits 0 to 2 in ADMOD register and functions added • Bit 5 symbol names changed • Bits 6 and 7 added
ADCON2	—	
—	INTCMP	
—	FST	
FMR0	FMR0	• Reset values are different. • Functions in bit 0 moved to bit 7 in FST register • Functions in bit 2 changed • Bits 4 and 5 added • Functions in bit 6 moved to bit 4 in FST register • Functions in bit 6 changed • Functions in bit 7 moved to bit 5 in FST register • Functions in bit 7 changed • Allocation addresses are different.
FMR1	FMR1	• Reset values are different. • Functions in bit 1 moved to bit 2 in FMR0 register • Bits 3, 4, and 7 added • Functions in bits 5 and 6 added
FMR4	—	
—	FMR2	

Table 4.13 Option Function Select Area Differences (1)

R8C/29 Group	R8C/32C Group	Remarks
OFS	OFS	• Bit 4 added and functions in bit 5 changed • Functions in bit 5 moved to bit 6
—	OFS2	

Note:
1. The option function select area is allocated in the flash memory, not in the SFRs.

4.4 Interrupt Vector Differences

Table 4.14 lists differences in the fixed vector table and Table 4.15 lists differences in the relocatable vector table.

Table 4.14 Differences in Fixed Vector Table

Vector addresses Addresses (L) to (H)	Interrupt Source of R8C/29 Group	Interrupt Source of R8C/32C Group
0FFF0h to 0FFF3h	Watchdog timer Oscillation stop detection Voltage monitor 1 (1) Voltage monitor 2	Watchdog timer Oscillation stop detection Voltage monitor 1 Voltage monitor 2

Table 4.15 Relocatable Vector Table Differences

Software Interrupt Number	Interrupt Source of R8C/29 Group	Interrupt Source of R8C/32C Group
1	—	Flash memory ready
11	—	UART2 transmit/NACK2
12	—	UART2 receive/ACK2
19	UART1 transmit	—
20	UART1 receive	—
30	—	UART2 bus collision detection
50	—	Voltage monitor 1
51	—	Voltage monitor 2

5. Reference Documents

R8C/29 Group User's Manual: Hardware Rev.2.10
R8C/32C Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

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Revision History	R8C/29 Group and R8C/32C Group Differences between R8C/29 Group and R8C/32C Group

Rev.	Date	Description	
		Page	Summary
1.00	June 30, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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