R8C/25 Group

Timer RD in Input Capture Function

R01AN1284EJ0110
Rev. 1.10
June 1, 2012

1. Abstract

This document describes how to set up and use timer RD in the input capture function in the R8C/25 Group.

2. Introduction

The application example described in this document is applied to the following MCU and parameter(s):

- MCU: R8C/25 Group

This program can be used with other R8C/Tiny Series which have the same special function registers (SFRs) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

Note on oscillation stabilization wait time
In chapter 4.2.1 , select the high-speed on-chip oscillator after starting the high-speed on-chip oscillator and waiting until oscillation stabilizes.

3. Application Description

3.1 Timer RD

Timer RD has two 16-bit timers (channels 0 and 1). Each channel has four I/O pins.
The operation clock of timer RD is f1 or fOCO40M. Table 3.1 lists the Timer RD Operation Clocks.

Table 3.1 Timer RD Operation Clocks

Conditions	Operation Clock of Timer RD
The count source is f1, f2, f4, f8, f32, or TRDCLK input (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to a value from 000b to 101b).	f1
The count source is fOCO40M (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 110b).	fOCO40M

Figure 3.1 shows a Block Diagram of Timer RD. Timer RD has five modes:

- Timer mode
  - Input capture function — Transfer the counter value to a register with an external signal as the trigger
  - Output compare function — Detect register value matches with a counter (Pin output can be changed at detection)

The following four modes use the output compare function:

- PWM mode — Output pulse of any width continuously
- Reset synchronous PWM mode — Output three-phase waveforms (six) without sawtooth wave modulation and dead time
- Complementary PWM mode — Output three-phase waveforms (six) with triangular wave modulation and dead time
- PWM3 mode — Output PWM waveform (two) with a fixed period

In the input capture function, output compare function, and PWM mode, channels 0 and 1 have the equivalent functions, and functions or modes can be selected individually for each pin. Also, a combination of these functions and modes can be used in one channel.
In reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, a waveform is output with a combination of counters and registers in channels 0 and 1.

Tables 3.2 to 3.10 list the Pin Functions of timer RD.

Table 3.2 Pin Functions TRDIOA0/TRDCLK(P2_0)

Register	TRDOER1	TRDFCR			TRDIORA0		Function
Bit	EA0	PWM3	STCLK	CMD1, CMD0	IOA3	IOA2_IOA0	
Setting value	0	0	0	00b	X	XXXb	PWM3 mode waveform output
	0	1	0	00b	1	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	0	00b	X	1XXb	Timer mode trigger input (input capture function)(1)
		1	1	XXb	X	000b	External clock input (TRDCLK)(1)
	Other than above						I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_0 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function) and external clock input (TRDCLK).

Table 3.3 Pin Functions TRDIOB0(P2_1)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORA0	Function
Bit	EB0	PWM3	CMD1, CMD0	PWMB0	IOB2_IOB0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	0	00b	X	XXXb	PWM3 mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_1 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.4 Pin Functions TRDIOC0(P2_2)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC0	Function
Bit	EC0	PWM3	CMD1, CMD0	PWMC0	IOC2_IOC0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_2 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.5 Pin Functions TRDIOD0(P2_3)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC0	Function
Bit	ED0	PWM3	CMD1, CMD0	PWMD0	IOD2_IOD0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_3 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.6 Pin Functions TRDIOA1(P2_4)

Register	TRDOER1	TRDFCR		TRDIORA1	Function
Bit	EA1	PWM3	CMD1, CMD0	IOA2_IOA0	
Setting value	0	X	1Xb	XXXb	Complementary PWM mode waveform output
	0	X	01b	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above				I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_4 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.7 Pin Functions TRDIOB1(P2_5)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORA1	Function
Bit	EB1	PWM3	CMD1, CMD0	PWMB1	IOB2_IOB0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_5 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.8 Pin Functions TRDIOC1(P2_6)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC1	Function
Bit	EC1	PWM3	CMD1, CMD0	PWMC1	IOC2_IOC0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_6 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.9 Pin Functions TRDIOD1(P2_7)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC1	Function
Bit	ED1	PWM3	CMD1, CMD0	PWMD1	IOD2_IOD0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_7 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 3.10 Pin Functions $\overline{\text{INT0}}$(P4_5)

Register	TRDOER2	INTEN		PD4	Function
Bit	PTO	INT0PL	INT0EN	PD4_5	
Setting value	1	0	1	0	Pulse output forced cutoff signal input
	Other than above				I/O port or $\overline{\text{INT0}}$ interrupt input

X: can be 0 or 1, no change in outcome

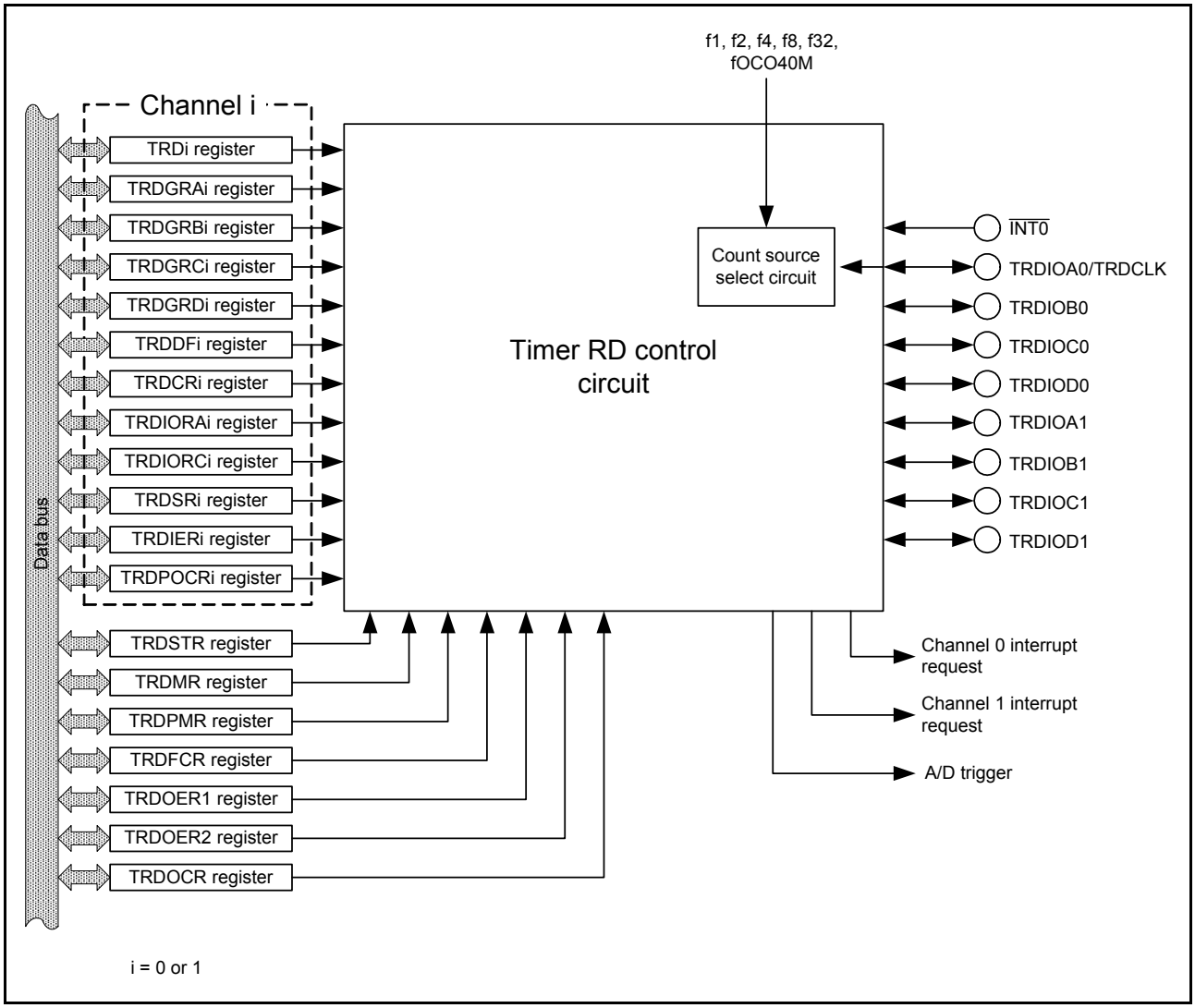


Figure 3.1 Block Diagram of Timer RD

3.2 Count Sources

The count source selection method is the same in all modes. However, in PWM3 mode, the external clock cannot be selected.

Table 3.11 Count Source Selection

Count Source	Selection
f1, f2, f4, f8, f32	The count source is selected by bits TCK2 to TCK0 in the TRDCRi register.
fOCO40M(1)	The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator frequency). Bits TCK2 to TCK0 in the TRDCRi register are set to 110b (fOCO40M)
External signal input to TRDCLK pin	The STCLK bit in the TRDFCR register is set to 1 (external clock input enabled). Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (count source: external clock). The valid edge is selected by bits CKEG1 to CKEG0 in the TRDCRi register. The PD2_0 bit in the PD2 register is set to 0 (input mode).

i = 0 or 1

NOTE:

1. The count source fOCO40M can be used with VCC = 3.0 to 5.5 V.

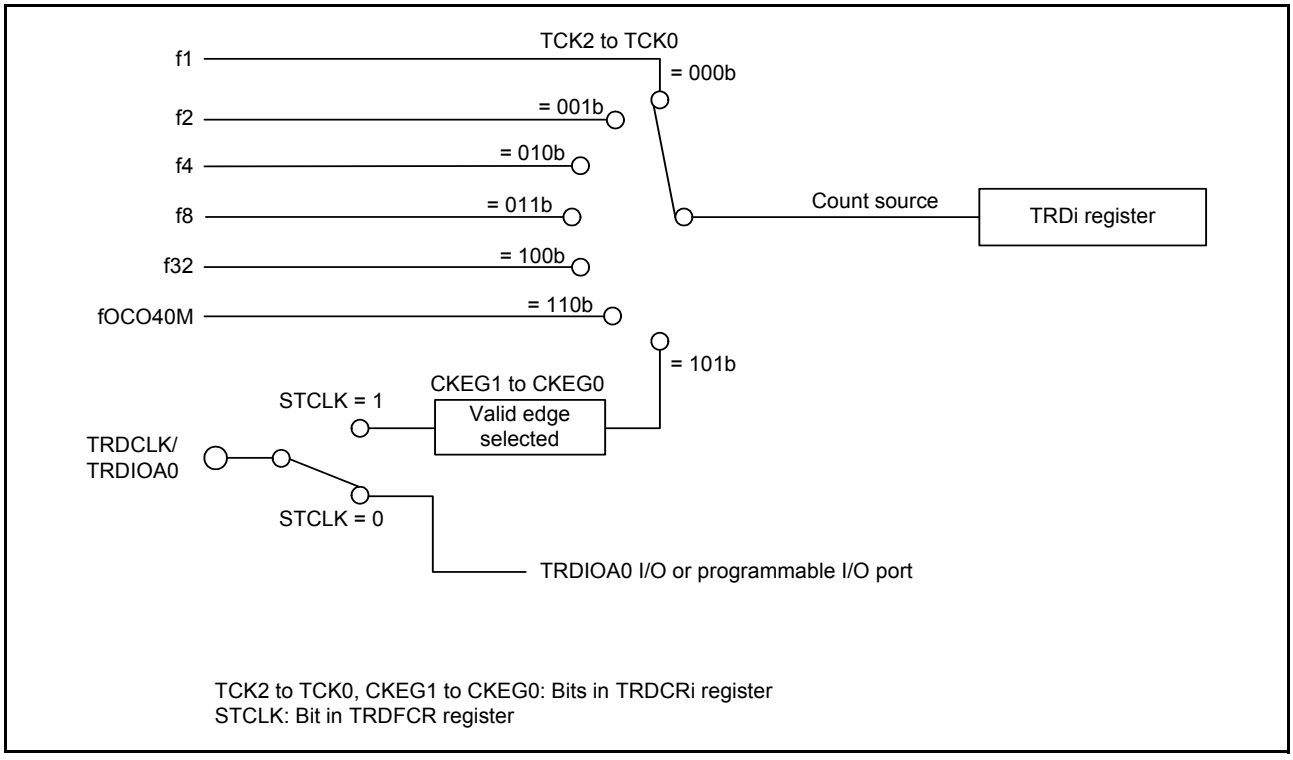


Figure 3.2 Block Diagram of Count Source

Set the pulse width of the external clock which inputs to the TRDCLK pin to three or more cycles of the operation clock of timer RD (refer to **Table 3.1 Timer RD Operation Clocks**).

When selecting fOCO40M for the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on) before setting bits TCK2 to TCK0 in the TRDCRi register (i = 0 or 1) to 110b (fOCO40M).

3.3 Buffer Operation

The TRDGRCi (i = 0 to1) register can be used as the buffer register of the TRDGRAi register, and the TRDGRDi register can be used as the buffer register of the TRDGRBi register by means of bits BFCi (i = 0 to1) and BFDi in the TRDMR register.

- TRDGRAi buffer register: TRDGRCi register
- TRDGRBi buffer register: TRDGRDi register

Buffer operation depends on the mode. Table 3.12 lists the Buffer Operation in Each Mode.

Table 3.12 Buffer Operation in Each Mode

Function and Mode	Transfer Timing	Transfer Register
Input capture function	Input capture signal input	Transfer content in TRDGRAi (TRDGRBi) register to buffer register
Output compare function PWM mode	Compare match with TRDi register and TRDGRAi (TRDGRBi) register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Reset synchronous PWM mode	Compare match withTRD0 register and TRDGRA0 register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Complementary PWM mode	• Compare match with TRD0 register and TRDGRA0 register • TRD1 register underflow	Transfer content in buffer register to registers TRDGRB0, TRDGRA1, and TRDGRB1
PWM3 mode	Compare match with TRD0 register and TRDGRA0 register	Transfer content in buffer register to registers TRDGRA0, TRDGRB0, TRDGRA1, and TRDGRB1

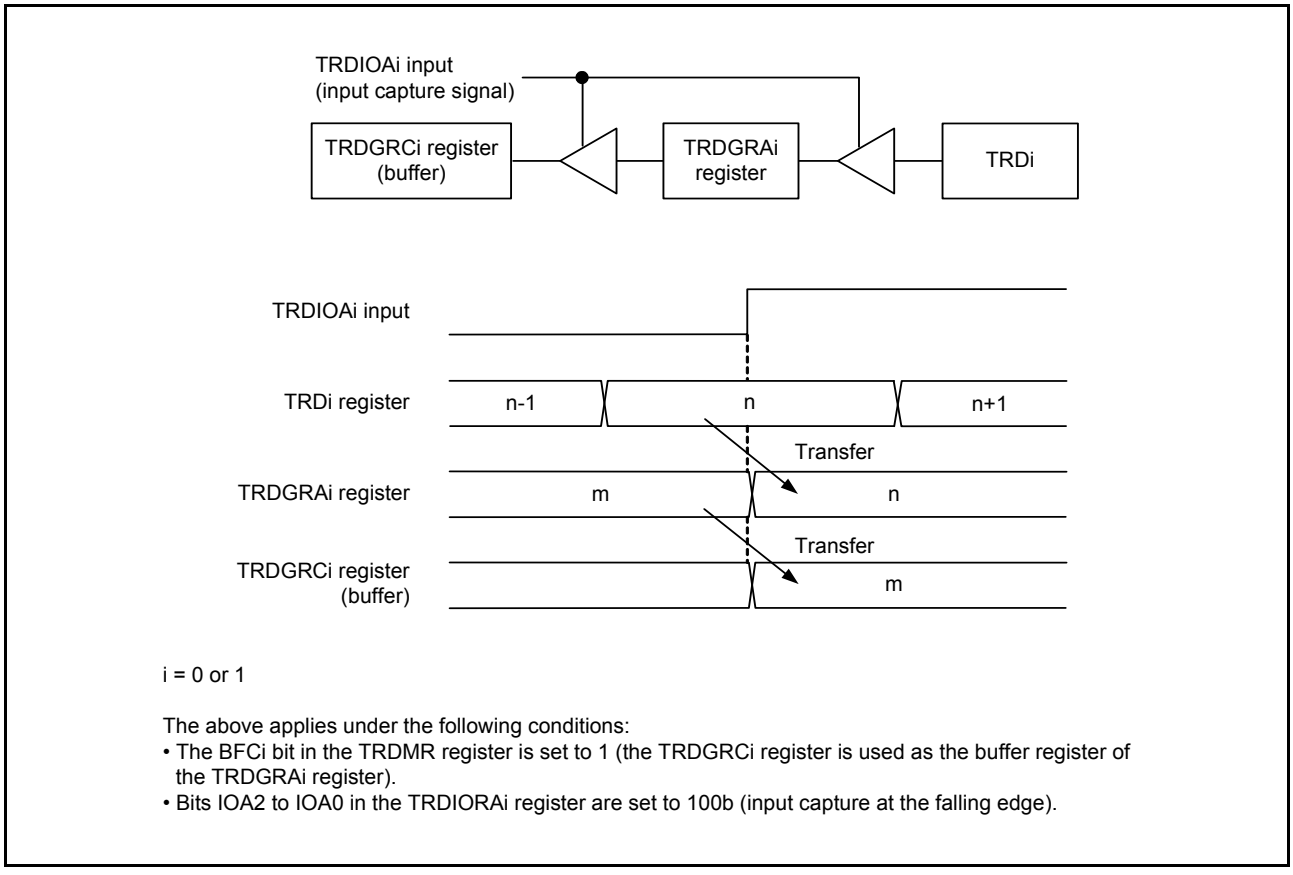


Figure 3.3 Buffer Operation in Input Capture Function

Perform the following for the timer mode (input capture and output compare functions).
When using the TRDGRCi (i = 0 or 1) register as the buffer register of the TRDGRAi register:

- Set the IOC3 bit in the TRDIORCi register to 1 (general register or buffer register).
- Set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.

When using the TRDGRDi register as the buffer register of the TRDGRBi register:

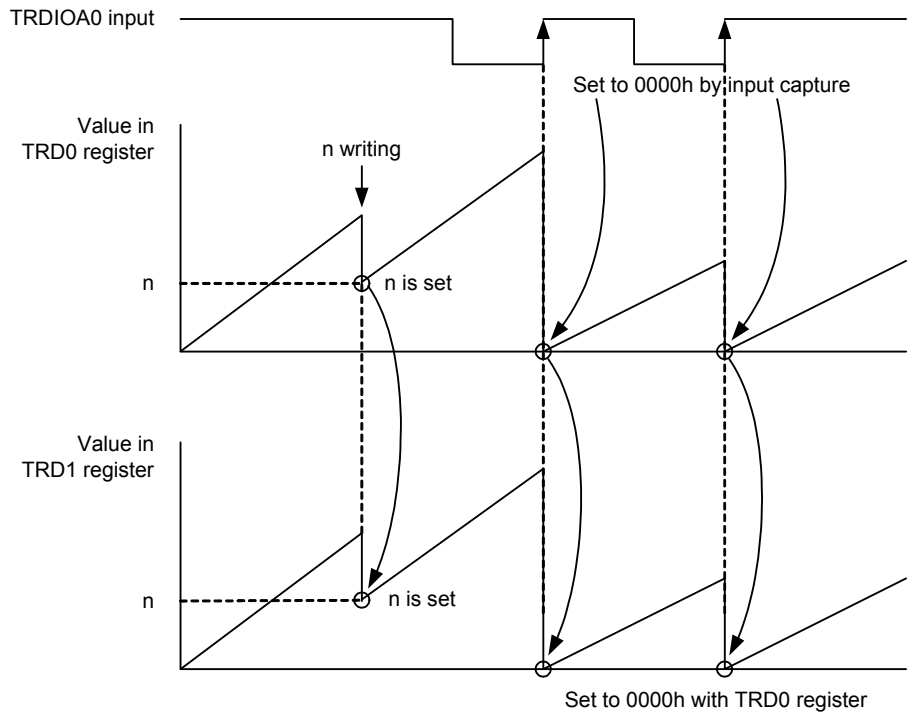
- Set the IOD3 bit in the TRDIORDi register to 1 (general register or buffer register).
- Set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

Bits IMFC and IMFD in the TRDSRi register are set to 1 at the input edge of the TRDIOCi pin when also using registers TRDGRCi and TRDGRDi as the buffer register in the input capture function.

3.4 Synchronous Operation

The TRD1 register is synchronized with the TRD0 register.

- Synchronous preset
  When the SYNC bit in the TRDMR register is set to 1 (synchronous operation), the data is written to both the TRD0 and TRD1 registers after writing to the TRDi register.
- Synchronous clear
  When the SYNC bit in the TRDMR register is set to 1 and bits CCLR2 to CCLR0 in the TRDCRi register are set to 011b (synchronous clear), the TRD0 register is set to 0000h at the same time the TRD1 register is set to 0000h.
  Also, when the SYNC bit in the TRDMR register is set to 1 and bits CCLR2 to CCLR0 in the TRDCRi register are set to 011b (synchronous clear), the TRD1 register is set to 0000h at the same time the TRD0 register is set to 0000h.



The above applies under the following conditions:

- The SYNC bit in the TRDMR register is set to 1 (synchronous operation).
- Bits CCLR2 to CCLR0 in the TRDCR0 register are set to 001b (set the TRD0 register to 0000h in input capture).
  Bits CCLR2 to CCLR0 in the TRDCR1 register are set to 011b (set the TRD1 register to 0000h synchronizing with the TRD0 register).
- Bits IOA2 to IOA0 in the TRDIORA0 register are set to 100b.
- Bits CMD1 to CMD0 in the TRDFCR register are set to 00b.
  The PWM 3 bit in the TRDFCR register is set to 1.

} (Input capture at the rising edge of the TRDIOA0 input)

Figure 3.4 Synchronous Operation

3.5 Input Capture Function

The input capture function measures the external signal width and period. The content of the TRDi register (counter) is transferred to the TRDGRji register as a trigger of the TRDIOji (i = 0 or 1, j = either A, B, C, or D) pin external signal (input capture). Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the input capture function, or any other mode or function, can be selected for each individual pin.

The TRDGRA0 register can also select fOCO128 signal as input-capture trigger input.

Figure 3.5 shows a Block Diagram of Input Capture Function, Table 3.13 lists the Input Capture Function Specification, Figures 3.6 to 3.16 show the Registers Associated with Input Capture Function, and Figure 3.17 shows an Operating Example of Input Capture Function.

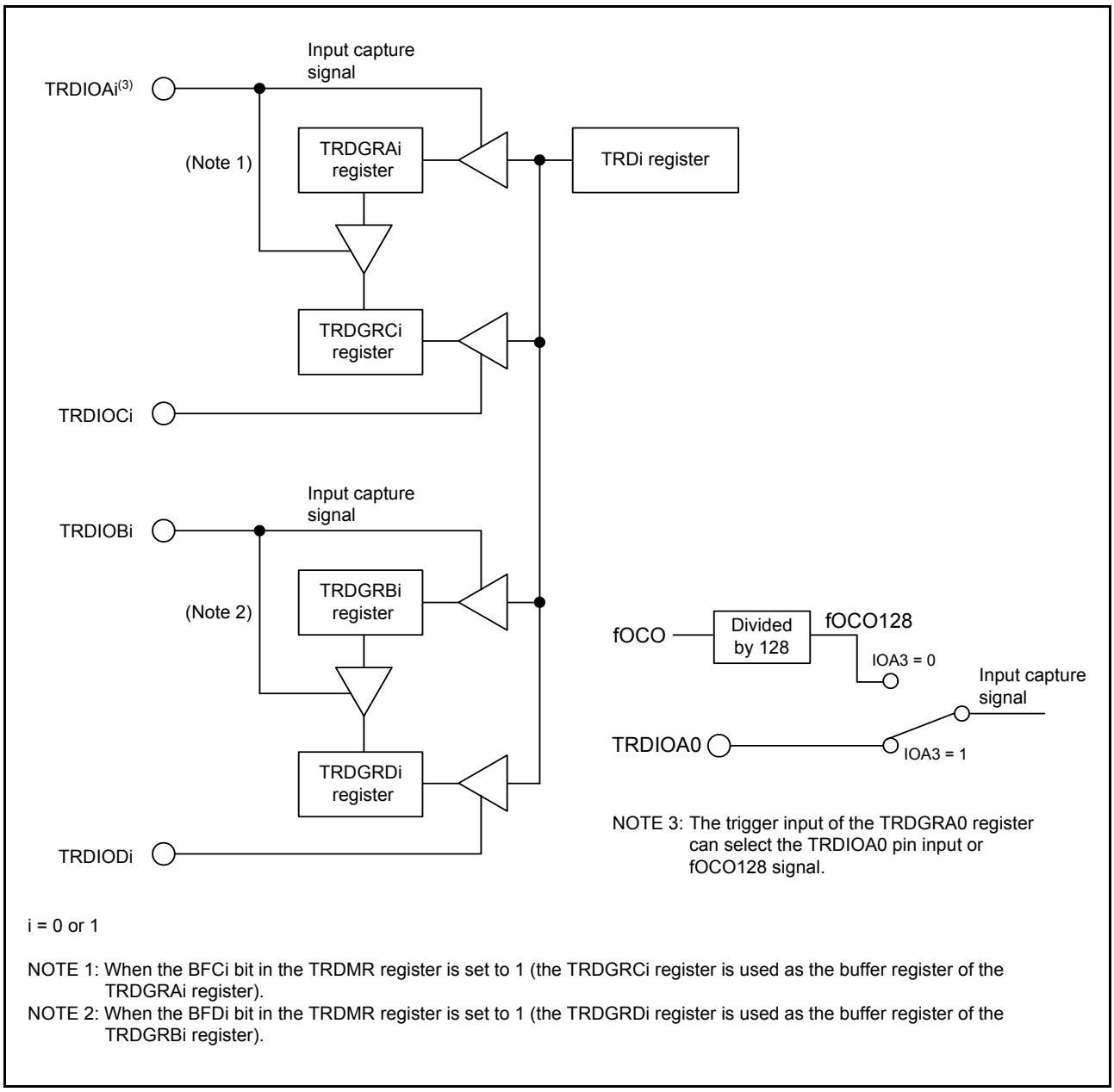


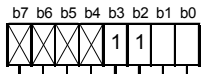
Figure 3.5 Block Diagram of Input Capture Function

Table 3.13 Input Capture Function Specification

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	Increment
Count period	When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation). 1/fk × 65536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop condition	0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1.
Interrupt request generation timing	• Input capture (valid edge of TRDIOji input or fOCO128 signal edge) • TRDi register overflows
TRDIOA0 pin function	Programmable I/O port, input-capture input, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port, or input-capture input (selectable by pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (channels 0 and 1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (channels 0 and 1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Select functions	• Input-capture input pin selected Either 1 pin or multiple pins among TRDIOAi, TRDIOBi, TRDIOCi, or TRDIODi. • Input-capture input valid edge selected Rising edge, falling edge, or both edges • Timing when the TRDi register is set to 0000h At overflow or input capture • Buffer operation (refer to **3.3 Buffer Operation**) • Synchronous operation (refer to **3.4 Synchronous Operation**) • Digital filter The TRDIOji input is sampled and when the sampled input level matches three times, the level is determined. • Input-capture trigger selected fOCO128 can be selected for input-capture trigger input of the TRDGRA0 register.

i = 0 or 1, j = either A, B, C, or D

Timer RD Start Register(1)

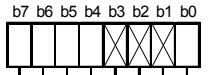


Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag	0: Count stops 1: Count starts	RW
TSTART1	TRD1 count start flag	0: Count stops 1: Count starts	RW
CSEL0	TRD0 count operation select bit	Set to 1 in the input capture function	RW
CSEL1	TRD1 count operation select bit	Set to 1 in the input capture function	RW
— (b7 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTE:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to 3.9.1 **TRDSTR Register** of **Notes on Timer RD**.

Timer RD Mode Register

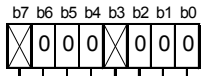


Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	0: Registers TRD0 and TRD1 operate independently 1: Registers TRD0 and TRD1 operate synchronously	RW
— (b3 - b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	RW

Figure 3.6 Registers TRDSTR and TRDMR in Input Capture Function

Timer RD PWM Mode Register



Symbol	Address	After Reset
TRDPMR	0139h	10001000b

Bit Symbol	Bit Name	Function	RW
PWMB0	PWM mode of TRDIOB0 select bit	Set to 0 (timer mode) in the input capture function.	RW
PWMC0	PWM mode of TRDIOC0 select bit	Set to 0 (timer mode) in the input capture function.	RW
PWMD0	PWM mode of TRDIOD0 select bit	Set to 0 (timer mode) in the input capture function.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PWMB1	PWM mode of TRDIOB1 select bit	Set to 0 (timer mode) in the input capture function.	RW
PWMC1	PWM mode of TRDIOC1 select bit	Set to 0 (timer mode) in the input capture function.	RW
PWMD1	PWM mode of TRDIOD1 select bit	Set to 0 (timer mode) in the input capture function.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 3.7 TRDPMR Register in Input Capture Function

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1						0	0

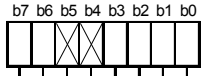
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode select bits(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in the input capture function.	RW
CMD1			RW
OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the input capture function.	RW
OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the input capture function.	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in the input capture function.	RW
ADEG	A/D trigger edge select bit (in complementary PWM mode)	This bit is disabled in the input capture function.	RW
STCLK	External clock input select bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode select bit(2)	Set this bit to 1 (other than PWM3 mode) in the input capture function.	RW

NOTES:
1. Set bits CMD1 to CMD0 w hen both the TSTART0 and TSTART1 bits are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the PWM3 bit setting is enabled.

Figure 3.8 TRDFCR Register in Input Capture Function

Timer RD Digital Filter Function Select Register i (i = 0 or 1)



Symbol	Address	After Reset
TRDDF0	013Eh	00h
TRDDF1	013Fh	00h

Bit Symbol	Bit Name	Function	RW
DFA	TRDIOA pin digital filter function select bit	0: Function is not used 1: Function is used	RW
DFB	TRDIOB pin digital filter function select bit	0: Function is not used 1: Function is used	RW
DFC	TRDIOC pin digital filter function select bit	0: Function is not used 1: Function is used	RW
DFD	TRDIOD pin digital filter function select bit	0: Function is not used 1: Function is used	RW
— (b5 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
DFCK0	Clock select bits for digital filter function	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRDCRi register)	RW
DFCK1			RW

Figure 3.9 Registers TRDDF0 to TRDDF1 in Input Capture Function

Timer RD Control Register i (i = 0 or 1)

b7 b6 b5 b4 b3 b2 b1 b0

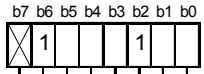
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source select bits	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input(1) 1 1 0: fOCO40M 1 1 1: Do not set.	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge select bits(2)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	RW
CKEG1			RW
CCLR0	TRDi counter clear select bits	b7 b6 b5 0 0 0: Disable clear (free-running opearation) 0 0 1: Clear by input capture in the TRDGRAi register 0 1 0: Clear by input capture in the TRDGRBi register 0 1 1: Synchronous clear (clear simultaneously w ith other channel counter)(3) 1 0 0: Do not set. 1 0 1: Clear by input capture in the TRDGRCi register 1 1 0: Clear by input capture in the TRDGRDi register 1 1 1: Do not set.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This setting is enabled w hen the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. Bits CKEG1 to CKEG0 are enabled w hen bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. This setting is enabled w hen the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).

Figure 3.10 Registers TRDCR0 to TRDCR1 in Input Capture Function

Timer RD I/O Control Register Ai (i = 0 or 1)



Symbol	Address	After Reset
TRDIORA0	0141h	10001000b
TRDIORA1	0151h	10001000b

Bit Symbol	Bit Name	Function	RW
IOA0	TRDGRA control bits	b1 b0 0 0: Input capture to the TRDGRAi register at the rising edge 0 1: Input capture to the TRDGRAi register at the falling edge 1 0: Input capture to the TRDGRAi register at both edges 1 1: Do not set.	RW
IOA1			RW
IOA2	TRDGRA mode select bit(1)	Set to 1 (input capture) in the input capture function.	RW
IOA3	Input capture input switch bit(3, 4)	0: fOCO128 Signal 1: TRDIOA0 pin input	RW
IOB0	TRDGRB control bits	b5 b4 0 0: Input capture to the TRDGRBi register at the rising edge 0 1: Input capture to the TRDGRBi register at the falling edge 1 0: Input capture to the TRDGRBi register at both edges 1 1: Do not set.	RW
IOB1			RW
IOB2	TRDGRB mode select bit(2)	Set to 1 (input capture) in the input capture function.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.
3. The IOA3 bit is enabled in the TRDIORA0 register only. Set to the IOA3 bit in TRDIORA1 to 1.
4. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

Figure 3.11 Registers TRDIORA0 to TRDIORA1 in Input Capture Function

Timer RD I/O Control Register Ci (i = 0 or 1)

b7	b6	b5	b4	b3	b2	b1	b0
1	1			1	1		

Symbol	Address	After Reset
TRDIORC0	0142h	10001000b
TRDIORC1	0152h	10001000b

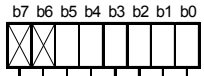
Bit Symbol	Bit Name	Function	RW
IOC0	TRDGRC control bits	b1 b0 0 0: Input capture to the TRDGRCi register at the rising edge 0 1: Input capture to the TRDGRCi register at the falling edge 1 0: Input capture to the TRDGRCi register at both edges 1 1: Do not set.	RW
IOC1			RW
IOC2	TRDGRC mode select bit(1)	Set to 1 (input capture) in the input capture function.	RW
IOC3	TRDGRC register function select bit	Set to 1 (general register or buffer register) in the input capture function.	RW
IOD0	TRDGRD control bits	b5 b4 0 0: Input capture to the TRDGRDi register at the rising edge 0 1: Input capture to the TRDGRDi register at the falling edge 1 0: Input capture to the TRDGRDi register at both edges 1 1: Do not set.	RW
IOD1			RW
IOD2	TRDGRD mode select bit(2)	Set to 1 (input capture) in the input capture function.	RW
IOD3	TRDGRD register function select bit	Set to 1 (general register or buffer register) in the input capture function.	RW

NOTES:

1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

Figure 3.12 Registers TRDIORC0 to TRDIORC1 in Input Capture Function

Timer RD Status Register i (i = 0 or 1)



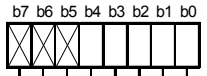
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] TRDSR0 register: fOCO128 signal edge when the IOA3 bit in the TRDIORA0 register is set to 0 (fOCO128 signal) TRDIOA0 pin input edge when the IOA3 bit in the TRDIORA0 register is set to 1 (TRDIOA0 input)(3) TRDSR1 register: Input edge of TRDIOA1 pin(3)	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] Input edge of TRDIOBi pin(3)	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] Input edge of TRDIOCi pin(4)	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] Input edge of TRDIODi pin(4)	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] When the TRDi register overflows	RW
UDF	Underflow flag(1)	This bit is disabled in the input capture function.	RW
— (b7 - b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Edge selected by bits IOj1 to IOj0 (j = A or B) in the TRDIORAi register.
4. Edge selected by bits IOk1 to IOk0 (k = C or D) in the TRDIORCi register.
   Including when the BFki bit in the TRDMR register is set to 1 (TRDGRki is used as the buffer register).

Figure 3.13 Registers TRDSR0 to TRDSR1 in Input Capture Function

Timer RD Interrupt Enable Register i (i = 0 or 1)

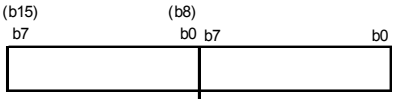


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	RW
— (b7 - b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 3.14 Registers TRDIER0 to TRDIER1 in Input Capture Function

Timer RD Counter i (i = 0 or 1)(1)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Count the count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

Figure 3.15 Registers TRD0 to TRD1 in Input Capture Function

Timer RD General Registers Ai, Bi, Ci, and Di (i = 0 or 1)(1)

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 3.14 TRDGRji Register Functions in Input Capture Function**.	RW

NOTE:
1. Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

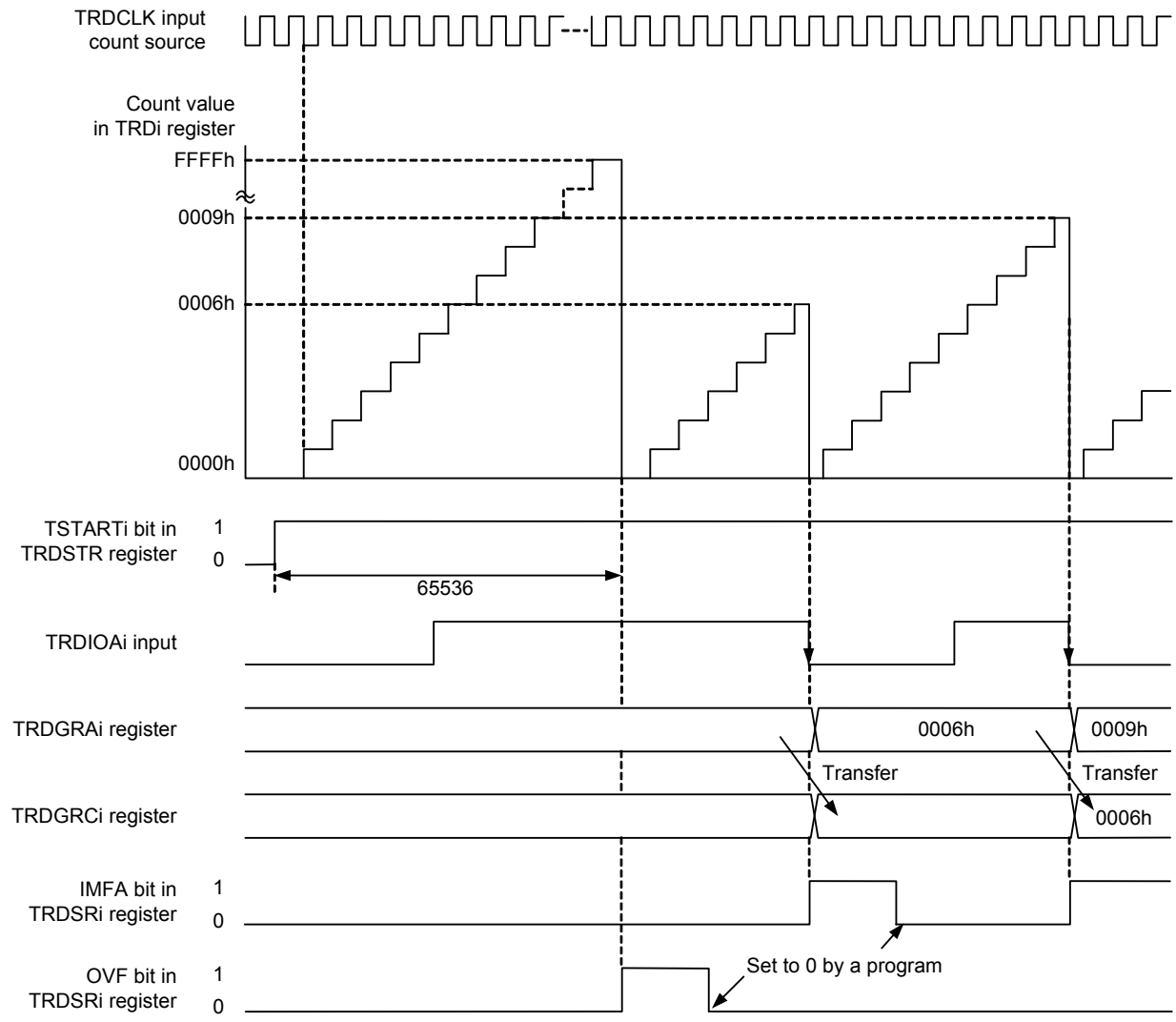
Figure 3.16 Registers TRDGRAi, TRDGRBi, TRDGRCi and TRDGRDi in Input Capture Function

The following registers are disabled in input capture function: TRDOER1, TRDOER2, TRDOCR, TRDPOCR0, and TRDPOCR1.

Table 3.14 TRDGRji Register Functions in Input Capture Function

Register	Setting	Register Function	Input-Capture Input Pin
TRDGRAi	–	General register The value in the TRDi register can be read at input capture.	TRDIOAi
TRDGRBi			TRDIOBi
TRDGRCi	BFCi = 0	General register The value in the TRDi register can be read at input capture.	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register The value in the TRDi register can be read at input capture (refer to **3.3 Buffer Operation**).	TRDIOAi
TRDGRDi	BFDi = 1		TRDIOBi

Set the pulse width of the input capture signal applied to the TRDIOji pin to three or more cycles of the timer RD operation clock (refer to **Table 3.1 Timer RD Operation Clocks**) for no digital filter (the DFj bit in the TRDDFi register set to 0).



i = 0 or 1

The above applies under the following conditions:
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (the TRDi register set to 0000h by TRDGRAi register input capture).
Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (TRDCLK input for the count source).
Bits CKEG1 to CKEG0 in the TRDCRi register are set to 01b (count at the falling edge for the count source).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 101b (input capture at the falling edge of the TRDIOAi input).
The BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).

Figure 3.17 Operating Example of Input Capture Function

3.6 Digital Filter

The TRDIOji input is sampled, and when the sampled input level matches three times, its level is determined. Select the digital filter function and sampling clock by the TRDDFi register.

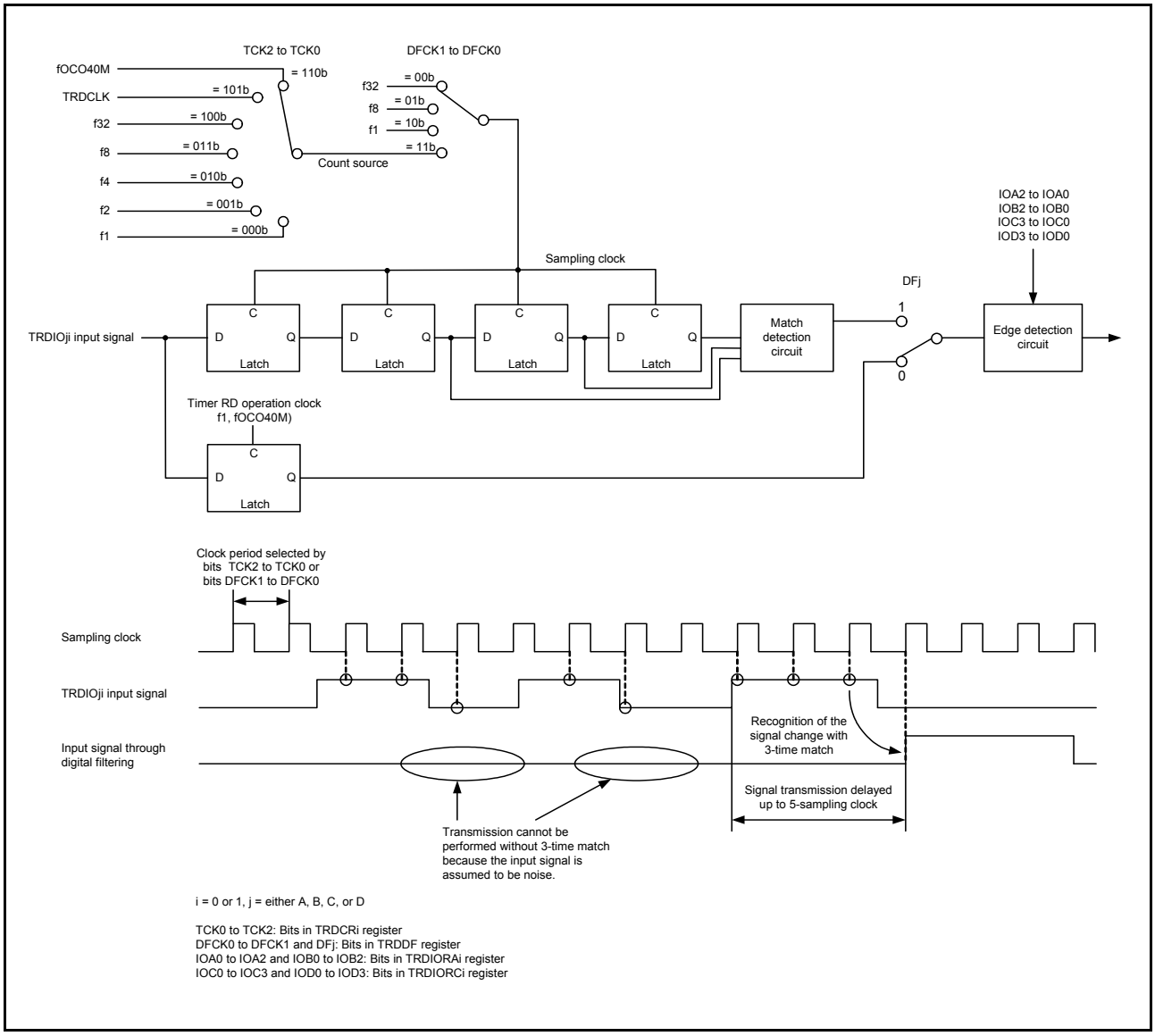


Figure 3.18 Block Diagram of Digital Filter

3.7 Timer RD Interrupt

Timer RD generates the timer RD interrupt request based on six sources for each channel. The timer RD interrupt has one TRDiIC register (bits IR, and ILVL0 to ILVL2), and one vector for each channel. Table 3.15 lists the Registers Associated with Timer RD Interrupt, and Figure 3.19 shows a Block Diagram of Timer RD Interrupt.

Table 3.15 Registers Associated with Timer RD Interrupt

	Timer RD Status Register	Timer RD Interrupt Enable Register	Timer RD Interrupt Control Register
Channel 0	TRDSR0	TRDIER0	TRD0IC
Channel 1	TRDSR1	TRDIER1	TRD1IC

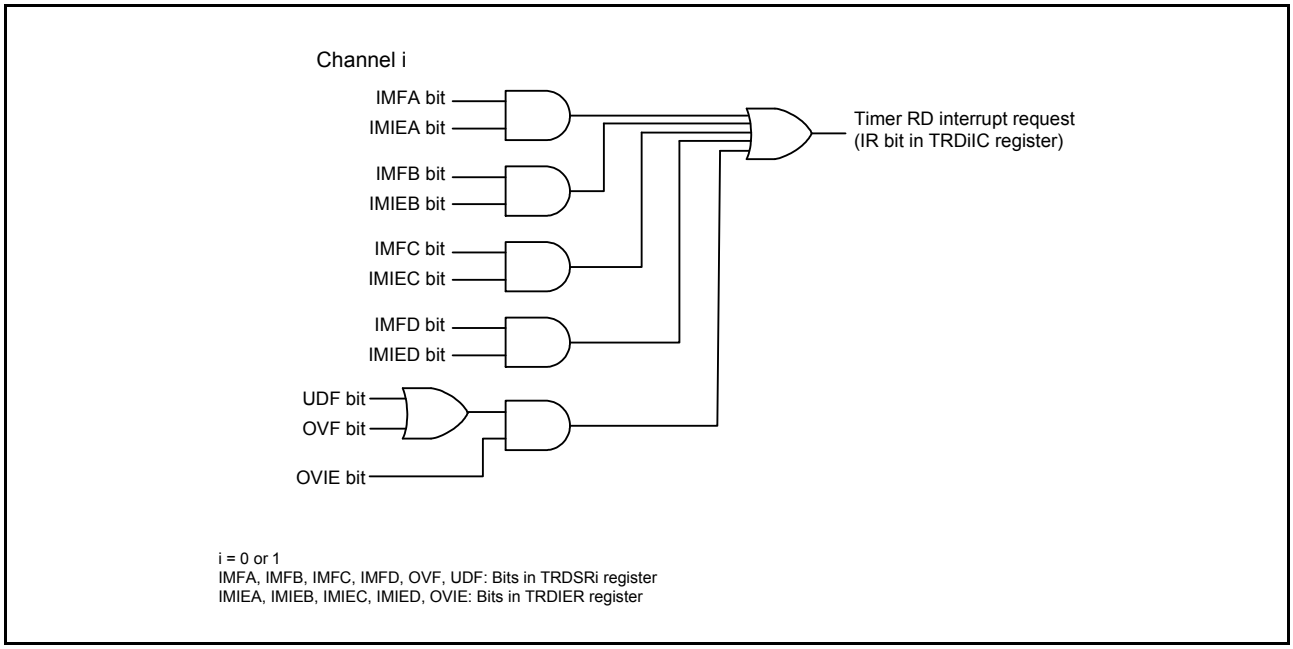


Figure 3.19 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the timer RD interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since the interrupt source (timer RD interrupt) is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the TRDSRi register corresponding to bits set to 1 in the TRDIERi register are set to 1 (enable interrupt), the IR bit in the TRDiIC register is set to 1 (interrupt requested).
- When either bits in the TRDSRi register or bits in the TRDIERi register corresponding to bits in the TRDSRi register, or both, are set to 0, the IR bit is set to 0 (interrupt not requested). Therefore, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be maintained.
- When the conditions of other request sources are met, the IR bit remains 1.
- When multiple bits in the TRDIERi register are set to 1, which request source causes an interrupt is determined by the TRDSRi register.
- Since each bit in the TRDSRi register is not automatically set to 0 even if the interrupt is acknowledged, set each bit to 0 in the interrupt routine. For information on how to set these bits to 0, refer to the descriptions of the registers used in the different modes (**Figure 3.13**).

Refer to **Registers TRDSR0 to TRDSR1 in each mode (Figure 3.13)** for the TRDSRi register. Refer to **Registers TRDIER0 to TRDIER1 in each mode (Figure 3.14)** for the TRDIERi register.
Refer to the **R8C/25 Group Hardware Manual** for information on the TRDiIC register and the interrupt vectors.

3.8 Notes on Timer RD

3.8.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.

- When the CSELi (i = 0 to 1) is set to 0 (the count stops after the count is cleared at compare match of registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
- Therefore, set the TSTARTi bit to 0 to change other bits without changing the TSTARTi bit when the CSELi bit is set to 0.
- To stop counting by a program, set the TSTARTi bit after setting the CSELi bit to 1. Although the CSELi bit is set to 1 and the TSTARTi bit is set to 0 at the same time (with one instruction), the count cannot be stopped.
- Table 3.16 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops to use the TRDIOji (j = A, B, C, or D) pin with the timer RD output.

Table 3.16 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Count Stop	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, set the TSTARTi bit to 0 and the count stops.	Hold the output level immediately before the count stops.
When the CSELi bit is set to 0, the count stops after the count is cleared at compare match of registers TRDi and TRDGRAi.	Hold the output level after output changes by compare match.

3.8.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid overlapping with the timing for setting the TRDi register to 0000h, and then write. If the timing for setting the TRDi register to 0000h overlaps with the timing for writing the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These precautions are applicable when selecting the following by bits CCLR2 to CCLR0 in the TRDCRi register.
  - 001b (Clear by the TRDi register at compare match with the TRDGRAi register.)
  - 010b (Clear by the TRDi register at compare match with the TRDGRBi register.)
  - 011b (Synchronous clear)
  - 101b (Clear by the TRDi register at compare match with the TRDGRCi register.)
  - 110b (Clear by the TRDi register at compare match with the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.W   TRD0,DATA        ;Reading
```

3.8.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0      ;Writing
                    JMP.B   L1                ;JMP.B
                L1: MOV.B   TRDSR0,DATA       ;Reading
```

3.8.4 Count Source Switch

- Switch the count source after the count stops.

Change procedure:

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.

- When changing the count source from fOCO40M to another source and stopping fOCO40M, wait two or more cycles of f1 after setting the clock switch, and then stop fOCO40M.

Change procedure:

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait two or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator stops).

3.8.5 Input Capture Function

- Set the pulse width of the input capture signal to three or more cycles of the timer RD operation clock (refer to **Table 3.1 Timer RD Operation Clocks**).
- The value in the TRDi register is transferred to the TRDGRji register two to three cycles of the timer RD operation clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C, or D) (no digital filter).

3.8.6 Count Source fOCO40M

- The count source fOCO40M can be a supply voltage VCC = 3.0 to 5.5 V. For the supply voltage other than that, do not set bits TCK to TCK0 in registers TRDCR0 and TRDCR to 110b (select fOCO40M as the count source).

4. Program Overview

When a valid edge is detected (IMFA bit = 1) from the external signal input to the TRDIOA0 pin, each content of the general register (TRDGRA0) and buffer register (TRDGRC0) is read in the main processing. Setting conditions of this program are as follows:

- The high-speed on-chip oscillator (fOCO40M) is used as the count source.
- The input capture to the TRDGRA0 is deteced at both edges.
- The timer RD counter 0 (TRD0) is cleared when a valid edge is detected. Figure 4.1 shows the Assigned Pin.

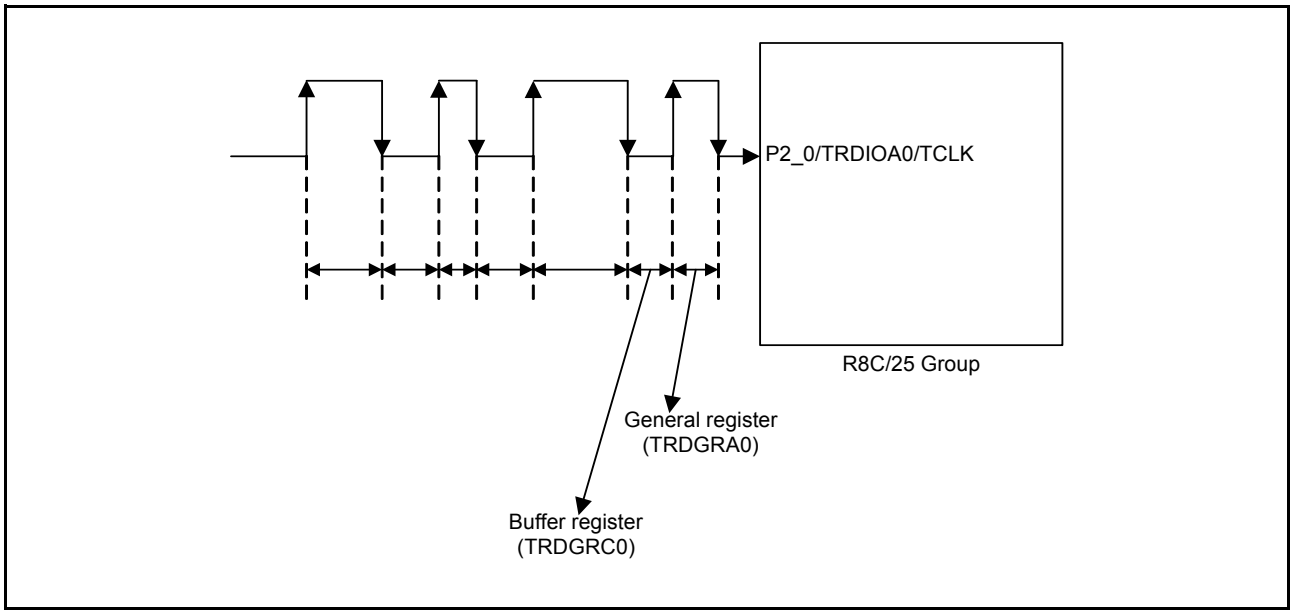


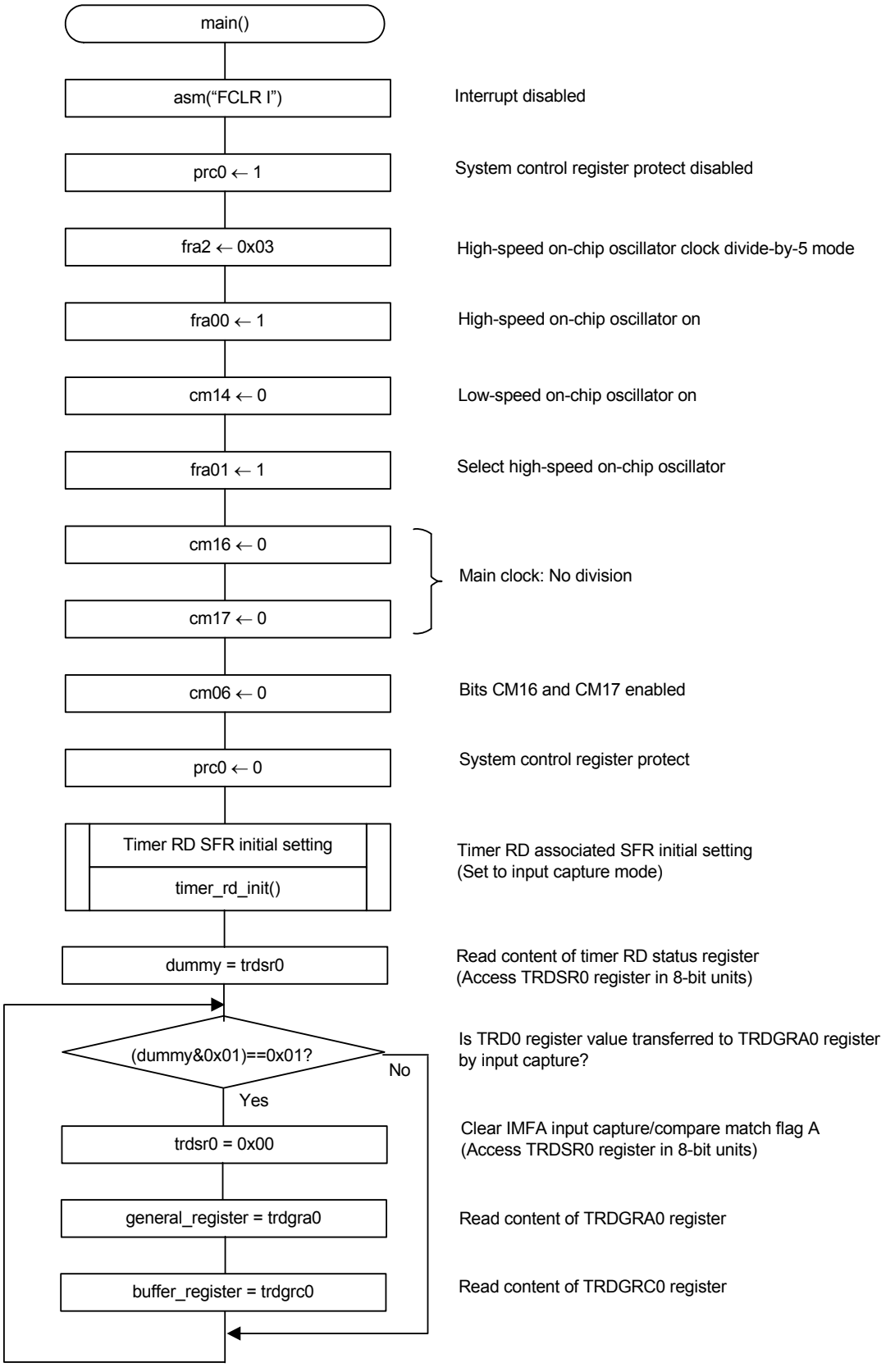
Figure 4.1 Assigned Pin

4.1 Function Table

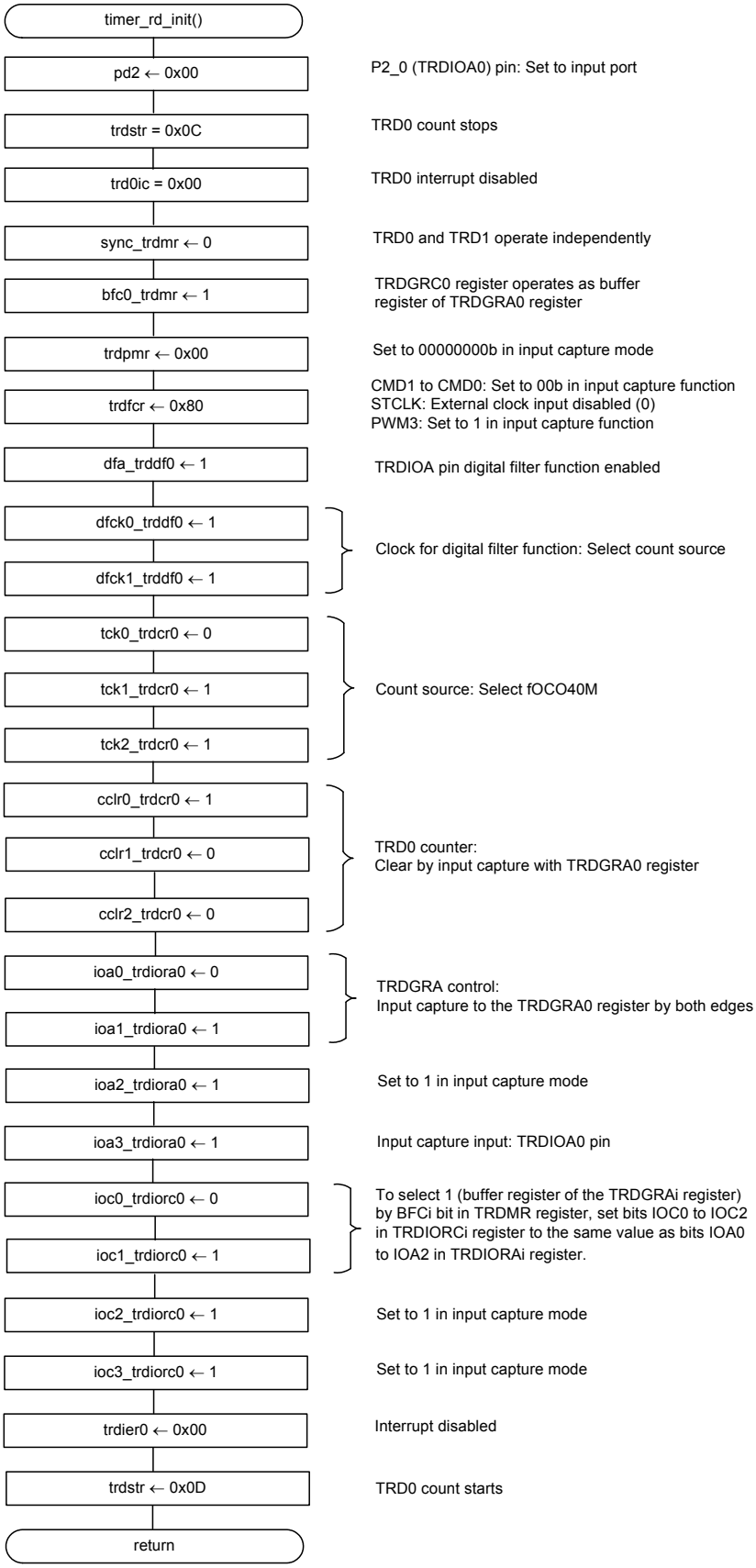
Declaration	void timer_rd_init (void)		
Overview	SFR initial setting associated Timer RD		
Argument	Argument name		Meaning
	None		
Variable used (global)	Variable name		Usage
	None		
Returned value	Type	Value	Meaning
	None		
Functions	Initialize the SFR registers associated with timer RD		

4.2 Flow Chart

4.2.1 Main Function



4.2.2 Timer RD SFR Initial Setting



5. Sample Programming Code

A sample program can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
R8C/25 Group Hardware Manual
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com

Inquiries
http://www.renesas.com/contact/

REVISION HISTORY	R8C/25 Group Timer RD in Input Capture Function

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 01, 2006	–	First Edition issued
1.10	June 1, 2012	1	Note on oscillation stabilization wait time added
		–	Previous document number: REJ05B0806

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 2.0