Abstract
This document describes a method for using the DMA controller (DMAC) in single transfer mode with the R32C/100 Series.

Products
MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.
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1. Specifications

Direct Memory Access (DMA) is a system that can control data transfer without using the CPU. The R32C/100 Series’ four channel DMAC transmits 8-bit (byte), 16-bit (word), or 32-bit (long word) data in cycle-steal mode from a source address to a destination address every time a transfer request is generated.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 and Figure 1.2 show the Block Diagram and Bus Timing, respectively.

### Table 1.1 Peripheral Function and Its Application

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAC (DMA0)</td>
<td>Data transfer</td>
</tr>
</tbody>
</table>

![Figure 1.1 Block Diagram](image)

During DMA transfer, the CPU gives up the bus.

![Figure 1.2 Bus Timing](image)

Transfer data without a CPU instruction.

The CPU cannot execute instructions during DMA transfer.
2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

<table>
<thead>
<tr>
<th>Table 2.1 Operation Confirmation Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Item</td>
</tr>
<tr>
<td>MCU used</td>
</tr>
<tr>
<td>Operating frequencies</td>
</tr>
<tr>
<td>Operating voltage</td>
</tr>
<tr>
<td>Integrated development environment</td>
</tr>
<tr>
<td>C compiler</td>
</tr>
<tr>
<td>Compile options</td>
</tr>
<tr>
<td>Operating mode</td>
</tr>
<tr>
<td>Sample code version</td>
</tr>
<tr>
<td>Board used</td>
</tr>
</tbody>
</table>

3. Reference Application Notes

The application notes associated with this application note are listed below. Refer to the following application notes for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)
- R32C/100 Series Configuring DMAC (REJ05B1220-0100)

4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

<table>
<thead>
<tr>
<th>Table 4.1 Pin Used and Its Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin Name</td>
</tr>
<tr>
<td>P8_2/INT0</td>
</tr>
</tbody>
</table>
5. **Software**

5.1 **Operation Overview**

DMA0 is activated to perform memory-to-memory transfer. In this application note, set the falling edge of \( \text{INT0} \) as a trigger for DMA.

(1) **DMAC initial settings**

Set DMAC operation and a trigger for DMA. Also set the \( \text{INT0} \) pin to use the \( \text{INT0} \) interrupt as a trigger for DMA.

Settings for DMA0 are as follows:
- Transfer mode: Single transfer
- Transfer size: 8 bits
- Source addressing: Increment
- Destination addressing: Fixed
- Transfer counter (DCT0 register): Five times
- Source address (DSA0 register): Start address of source data (400h)
- Destination address (DDA0 register): Destination address (1000h)
- Select a trigger for DMA: \( \text{INT0} \) falling edge

(2) **When a DMA trigger (\( \text{INT0} \) falling edge) is generated**

When the falling edge of a signal is applied to the \( \text{INT0} \) pin, data is DMA transferred from the address specified by the DSA0 register to the address specified by the DDA0 register. After the DMA transfer, 1 is subtracted from the DCT register and 1 is added to the DSA0 register. \(^{(1)}\)

When the DCT0 register becomes 000000h, DMA transfer is not performed even if a DMA trigger is generated.

**Note:**

1. When the transfer size is 8 bits. When the transfer size is 16 bits, 2 is added.
Figure 5.1 shows a DMA Transfer Operation Example.

<table>
<thead>
<tr>
<th>Invariable Name</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEST_ADDRESS</td>
<td>1000h</td>
<td>DMA destination address</td>
</tr>
<tr>
<td>TRANS_COUNT</td>
<td>5</td>
<td>Number of DMA transfers</td>
</tr>
</tbody>
</table>

5.2 Invariable Table

Table 5.1 lists the Invariables Used in the Sample Code.
5.3 Variable Table

Table 5.2 lists the Global Variable.

Table 5.2 Global Variable

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>data[]</td>
<td>DMA transfer source data (11h, 22h, 33h, 44h, and 55h)</td>
<td>DMAC_init</td>
</tr>
</tbody>
</table>

5.4 Flowcharts

5.4.1 Main Processing

Figure 5.2 shows the Main Processing.

![Figure 5.2 Main Processing](image-url)
### 5.4.2 DMAC Initial Setting

Figure 5.3 shows the DMAC Initial Setting.

```
DMAC_init

(1) Disable DMA0 transfer
   Bits MD01 and MD00 ← 00b : Disable DMA transfer.

(2) Set DMA0 register
   DMD0 register ← 00000010h
      Bits BW01 and BW00 = 00b : Set transfer size to 8 bits.
      USA0 bit = 1 : Set source addressing mode to incrementing addressing.
      UDA0 bit = 0 : Set destination addressing mode to non-incrementing addressing.

   DM0SL register ← 01h
      Bits DSEL4 to DSEL0 = 0001b : Set the falling edge of INT0 as a trigger for DMA0.
      DM0SL2 register ← 00h
      Bits DSEL24 to DSEL20 = 0000b
      DSR bit = 0
      DCT0 register ← TRANS_COUNT : Set the number of transfers.
      DDA0 register ← DEST_ADDRESS : Set the destination address.
      DSA0 register ← Starting address of the source address area
      DM0IC register ← 00h : Disable the DMA0 interrupts.

   USA0 bit = 1 : Set source addressing mode to incrementing addressing.
   UDA0 bit = 0 : Set destination addressing mode to non-incrementing addressing.

(3) Wait six or more peripheral clocks

(4) Set DMA0 mode register
   DMD0 register ← 00000011h
      Bits MD01 and MD00 = 01b : Single transfer

(5) Set DMA0 transfer mode

   return
```

---

**Figure 5.3** DMAC Initial Setting
6. **Sample Code**
   Sample code can be downloaded from the Renesas Electronics website.

7. **Reference Documents**
   - R32C/118 Group User's Manual: Hardware Rev.1.10
   The latest versions can be downloaded from the Renesas Electronics website.

   Technical Update/Technical News
   The latest information can be downloaded from the Renesas Electronics website.

   - C Compiler Manual
   - R32C/100 Series C Compiler Package V.1.02
   - C Compiler User’s Manual Rev.2.00
   The latest version can be downloaded from the Renesas Electronics website.

8. **Website and Support**
   - Renesas Electronics website
     http://www.renesas.com/

   Inquiries
   http://www.renesas.com/inquiry
### Revision History

**R32C/100 Series**  
**Using DMAC in Single Transfer Mode**

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Jan. 31, 2011</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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