Abstract

This document describes a method of transmitting/receiving data with a master while in slave mode using serial interface special mode 2 in the R32C/100 Series.

Products

MCUs: R32C/116 Group
    R32C/117 Group
    R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.
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1. **Specifications**

Transmit/receive data from a master while in slave mode using serial interface special mode 2. Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows Communication Control in Serial Interface Special Mode 2.

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial interface (UART0)</td>
<td>Slave transmission/reception using special mode 2</td>
</tr>
</tbody>
</table>

Figure 1.1 Communication Control in Serial Interface Special Mode 2
2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU used</td>
<td>R5F64189DFD (R32C/118 Group)</td>
</tr>
</tbody>
</table>
| Operating frequencies         | - Main clock: 16 MHz  
- PLL clock: 100 MHz  
- Base clock: 50 MHz  
- CPU clock: 50 MHz  
- Peripheral bus clock: 25 MHz  
- Peripheral function clock source: 25 MHz |
| Operating voltage             | 5 V                                                                      |
| Integrated development       | Renesas Electronics Corporation                                          |
| environment                  | High-performance Embedded Workshop Version 4.07                         |
| C compiler                   | Renesas Electronics Corporation                                          |
|                              | R32C/100 Series Compiler V.1.02 Release 01                               |
|                              | Compile options  
-D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300  
-DVECTOR_ADR=0xFFFFFBDC -c -finfo -dir "$(CONFIGDIR)" |
|                              | (Default setting is used in the integrated development environment.)     |
| Operating mode               | Single-chip mode                                                         |
| Sample code version          | Version 1.00                                                             |
| Board used                   | Renesas Starter Kit for R32C/118 (product name: R0K564189S000BE)        |

3. Reference Application Note

The application note associated with this application note is listed below. Refer to this application note for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)

4. Hardware

4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P6_0/SS0</td>
<td>Input</td>
<td>This pin functions as the SS0 pin.</td>
</tr>
<tr>
<td>P6_1/CLK0</td>
<td>Input</td>
<td>This pin functions as the transmit/receive clock.</td>
</tr>
<tr>
<td>P6_2/STXD0</td>
<td>Output</td>
<td>This pin transmits data.</td>
</tr>
</tbody>
</table>
5. **Software**

The sample program uses UART0 to transmit/receive data to/from a master. The settings are listed below.

**Settings**
- Use UART0 in special mode 2.
- Use an external clock for the transfer clock.
- For the CLK polarity, select output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge.
- Use LSB first as the transfer format.
- Select STXD0 and SRXD0 (slave mode) as the serial input pins.
- Select no clock delay for the clock phase setting.
- Enable the SS function.
- Do not use the UART0 transmit interrupt.
- Use the UART0 receive interrupt.
- Set ports P6_2 and P6_3 as N-channel open-drain output.

5.1 **Operation Overview**

Operation of the sample program is as follows:

1. **Initial setting**
   - Initialize UART0 and the ports.

2. **Enable transmission/reception**
   - Set the RE bit in the U0C1 register to 1 (reception enabled) and set the TE bit to 1 (transmission enabled).

3. **Wait for transmission**
   - Set dummy data to the U0TB register in order to fulfill the conditions for starting transmission/reception. (In the specifications of the sample program, data that was received in the previous receive operation is set as the transmit data. As there is no receive data in the first reception, set dummy data as transmit data.)

4. **Slave disabled period**
   - When the SS0 pin is high, the clock input is ignored, and transmit/receive operations are not performed.

5. **Slave enabled**
   - When the SS0 pin is low, the clock input is valid.

6. **Start transmission/reception**
   - Transmission/reception starts when a clock is input to the CLK0 pin.

7. **Transmission/reception completed**
   - A UART0 receive interrupt is generated when transmission/reception is completed.

8. **Reading received data**
   - Read the U0RB register value in the UART0 receive interrupt handling.

9. **Slave disabled**
   - When the SS0 pin is high, the slave is ignored.

Figure 5.1 shows the Timing Diagram.
Figure 5.1 Timing Diagram

Note:
1. If input to the CLK0 pin is high before receiving data, satisfy the following:
   - The TE bit in the U0C1 register must be 1 (transmission enabled).
   - The RE bit in the U0C1 register must be 1 (reception enabled).
   - Write dummy data to the U0TB register.
5.2 Constants

Table 5.1 lists the Constants Used in the Sample Code.

Table 5.1 Constants Used in the Sample Code

<table>
<thead>
<tr>
<th>Constant Name</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>OVR_ERROR_MASK</td>
<td>1000h</td>
<td>Mask value of the overrun error</td>
</tr>
<tr>
<td>OVR_ERROR</td>
<td>1000h</td>
<td>Comparative value of the overrun error</td>
</tr>
<tr>
<td>DUMMY_DATA</td>
<td>55h</td>
<td>Write dummy data</td>
</tr>
<tr>
<td>SUCCESS</td>
<td>00h</td>
<td>Transmission completed successfully</td>
</tr>
<tr>
<td>ERROR</td>
<td>FFh</td>
<td>Overrun error</td>
</tr>
</tbody>
</table>

5.3 Variable

Table 5.2 lists the Global Variable.

Table 5.2 Global Variable

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char</td>
<td>error_flag</td>
<td>Error flag</td>
<td>main(), _uart0_receive()</td>
</tr>
</tbody>
</table>

5.4 Functions

Table 5.3 lists the Functions.

Table 5.3 Functions

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>uart0_init</td>
<td>UART0 initial setting</td>
</tr>
<tr>
<td>_uart0_receive</td>
<td>UART0 receive interrupt handling</td>
</tr>
</tbody>
</table>
### 5.5 Function Specifications

The following tables list the sample code function specifications.

<table>
<thead>
<tr>
<th>Function</th>
<th>Outline</th>
<th>Header</th>
<th>Declaration</th>
<th>Explanation</th>
<th>Argument</th>
<th>Returned value</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>uart0_init</td>
<td>UART0 initial setting</td>
<td>None</td>
<td>void uart0_init(void)</td>
<td>Perform initial setting on UART0.</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>_uart0_receive</td>
<td>UART0 receive interrupt handling</td>
<td>None</td>
<td>void _uart0_receive(void)</td>
<td>Read receive data from the U0RB register. When there is an overrun error, change the status to overrun. In all other cases, set the error flags to completed successfully, and set receive data to the U0TB register.</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>
5.6 Flowcharts

5.6.1 Main Processing

Figure 5.2 shows the Main Processing.

![Main Processing Flowchart]

- **main**

1. **Disable maskable interrupts**
   - I flag ← 0

2. **PLL clock setting**
   - Set PLLClock()
   - Set clock frequencies in PLL mode.

3. **UART0 initial setting**
   -_uart0_init()

4. **Enable maskable interrupts**
   - I flag ← 1

5. **Enable UART0 transmit/receive**
   - U0C1 register ← 05h
     - TE bit = 1: Transmission enabled
     - RE bit = 1: Reception enabled
     - U0RS bit = 0: U0TB register is empty
     - U0RRM bit = 0: Continuous receive mode disabled
     - U0LCH bit = 0: Data non logic-inverted

6. **Transmit dummy data**
   - U0TB register ← DUMMY_DATA

7. **Overrun error occurred?**
   - Yes: Error handling (1)
   - No:

Note:
1. Error handling is not performed in this application note.

Figure 5.2 Main Processing
5.6.2 UART0 Initial Setting

Figure 5.3 shows the initial setting for UART0.

```
uart0_init

(1) Set UART0 transmit/receive mode
    register
    U0MR register ← 09h
    Bits SMD2 to SMD0 = 001b : Synchronous serial interface mode
    CKDIR bit = 1 : External clock

(2) Set UART0 transmit/receive control
    register 0
    U0C0 register ← 10h
    Bits CLK1 to CLK0 = 00b : f1 selected as U0BRG count source
    CRD bit = 1 : CTS disabled
    CKPOL bit = 0 : Output transmit data on the falling edge of the
    transmit/receive clock and input receive data on the
    falling edge
    UFORM bit = 0 : LSB first

(3) Set UART0 transmit/receive control
    register 1
    U0C1 register ← 00h
    TE bit = 0 : Transmission disabled
    RE bit = 0 : Reception disabled
    U0IR bit = 0 : U0TB register is empty
    U0RRM bit = 0 : Continuous receive mode disabled
    U0LCH bit = 0 : Data non logic-inverted

(4) Set UART0 special mode registers
    U0SMR register ← 00h : UART0 special mode register
    U0SMR2 register ← 00h : UART0 special mode register 2
    U0SMR3 register ← 05h : UART0 special mode register 3
    SSE bit = 1 : SS enabled
    CKPH bit = 0 : Non clock delayed
    DINC bit = 1 : Select the STXD0/SRXD0 pin (slave mode)
    ERR bit = 0 : No error detected
    U0SMR4 register ← 00h : UART0 special mode register 4

(5) Set interrupt control registers
    SOITC register ← 00h : Disable interrupts
    S0RIC register ← 01h : Set interrupt request level to 1

(6) Set I/O ports
    P6_0S register ← 00h : Port P6_0 functions as an I/O port
    P6_1S register ← 00h : Port P6_1 functions as an I/O port
    P6_2S register ← 44h
    Bits PSEL2 to PSEL0 = 100b : UART0/UART1 special function output
    NOD bit = 1 : N-channel open drain output
    P6_3S register ← 40h
    Bits PSEL2 to PSEL0 = 000b : I/O port P6_3
    NOD bit = 1 : N-channel open drain output
    P6 register ← 04h
    P6_0 bit = 0 : Port P6_0 functions as an input port
    P6_1 bit = 0 : Port P6_1 functions as an input port
    P6_2 bit = 0 : Port P6_2 functions as an output port
    P6_3 bit = 0 : Port P6_3 functions as an input port
```

Figure 5.3 UART0 Initial Setting
5.6.3 UART0 Receive Interrupt Handling

Figure 5.4 shows the handling for the UART0 receive interrupt.

```
(1) Read received data
   Overrun error occurred?
     No
     Yes

(4) Set overrun to error flag

(2) Write transmitted data
   U0TB register ← read_buf

(3) Set completed successfully to error flag
   error_flag ← SUCCESS
```

Figure 5.4 UART0 Receive Interrupt Handling
6. **Sample Code**
   Sample code can be downloaded from the Renesas Electronics website.

7. **Reference Documents**
   - R32C/118 Group User's Manual: Hardware Rev.1.10
   The latest versions can be downloaded from the Renesas Electronics website.

   Technical Update/Technical News
   The latest information can be downloaded from the Renesas Electronics website.

   - C Compiler Manual
   - R32C/100 Series C Compiler Package V.1.02
   - C Compiler User’s Manual Rev.2.00
   The latest version can be downloaded from the Renesas Electronics website.

**Website and Support**

- Renesas Electronics website
  http://www.renesas.com/

- Inquiries
  http://www.renesas.com/inquiry
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>July 22, 2011</td>
<td>First edition issued</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

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1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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