R32C/100 Series

Application Example of A/D Converter Operation in One-shot Mode Using DMAC

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Abstract

This document describes the DMA transfer of A/D conversion results (using the A/D converter in one-shot mode) to internal RAM for the R32C/100 Series microcomputer (MCU).

Products

MCU: R32C/100 Series

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

Perform A/D conversion at a given period, and transfer the conversion result to a conversion result storage buffer using DMAC. As the conversion result storage buffer is used repeatedly, the DMA uses repeat transfer mode.
Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the Block Diagram.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
A/D converter	Performs A/D conversion on the input voltage from the AN_0 pin
DMAC	Transfers A/D converted result to internal RAM area
Timer A0	Trigger to start A/D conversion (software trigger)

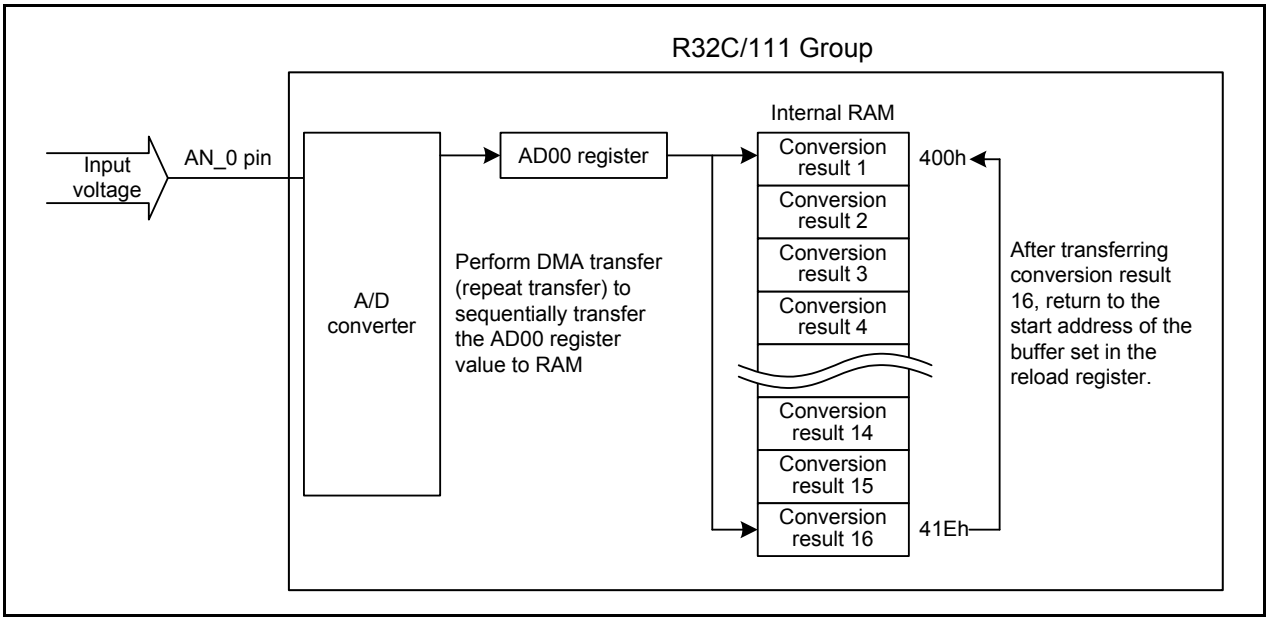

Figure 1.1 Block Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64112DFD (R32C/111 Group)
Operating frequencies	•Main clock: 16 MHz •PLL clock: 100 MHz •Base clock: 50 MHz •CPU clock: 50 MHz •Peripheral bus clock: 25 MHz •Peripheral function clock source: 25 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir “$(CONFIGDIR)”
Operating mode	Single-chip mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit for R32C/111 (product name: R0K564112S000BE)

3. Reference Application Notes

Application notes associated with this application note are listed below. Refer to these application notes for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)
- R32C/100 Series Configuring DMAC (REJ05B1220-0100)
- R32C/100 Series Using DMAC in Repeat Transfer Mode (R01AN0448EJ0100)
- R32C/100 Series A/D Converter Operation in One-Shot Mode Using DMAC (R01AN0491EJ0100)

4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

Table 4.1 Pin Used and Its Function

Pin Name	I/O	Function
P10_0/AN_0	Input	A/D converter input voltage

5. Software

Using a periodic timer (timer A0), start A/D conversion every 100 µs. When conversion is completed, use DMA transfer (repeat transfer) to transfer the result to the RAM storage buffer.

5.1 Operation Overview

Operations for this program are as follows.

(1) Initial setting
Initialize the DMAC, A/D converter, and timer A0.

(2) Start the timer A0 count
Set the TA0S bit in the TABSR register to 1 (start counter).

(3) Timer A0 interrupt handling
A timer A0 interrupt is generated every 100 µs. In the timer A0 interrupt handler, set the ADST bit in the AD0CON0 register to 1 (A/D conversion started).

(4) A/D conversion completed, DMA transfer started
When A/D conversion is completed, the conversion result is transferred to the AD00 register, the ADST bit becomes 0 (A/D conversion stopped), the IR bit in the AD0IC register becomes 1 (interrupt requested), and the conversion result in the AD00 register is transferred to an internal RAM area using DMA transfer.

Figure 5.1 shows the Timing Diagram.

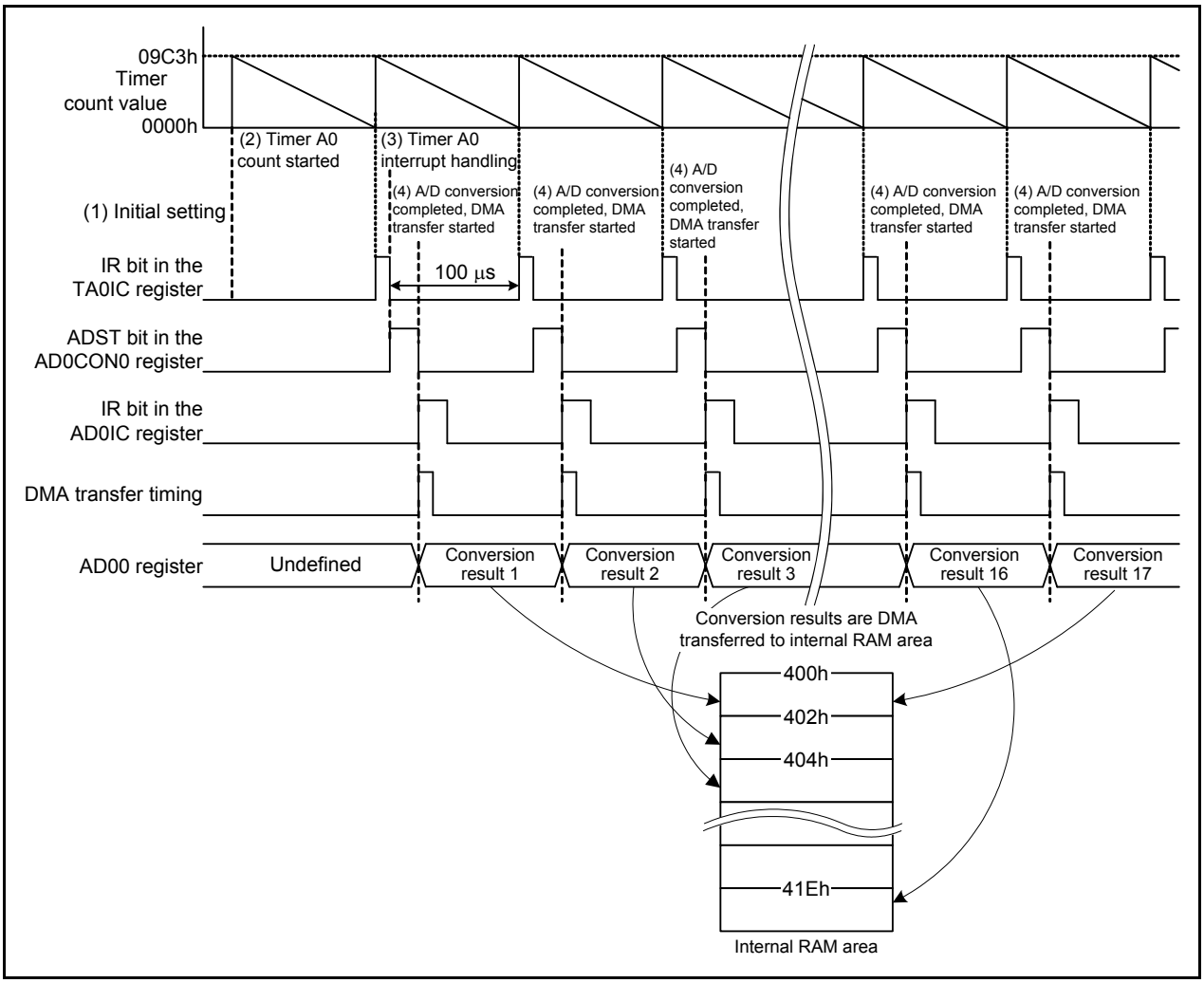

Figure 5.1 Timing Diagram

5.2 Constant

Table 5.1 lists the Constant Used in the Sample Code.

Table 5.1 Constant Used in the Sample Code

Constant Name	Setting Value	Contents
BUF_SIZE	16	Buffer size in which A/D conversion result is stored

5.3 Variable

Table 5.2 lists the Global Variable.

Table 5.2 Global Variable

Type	Variable Name	Contents	Function Used
unsigned short	ad_result[]	Array in which A/D conversion result is stored	Not used with functions

5.4 Flowcharts

5.4.1 Main Processing

Figures 5.2 and 5.3 show the main processing.

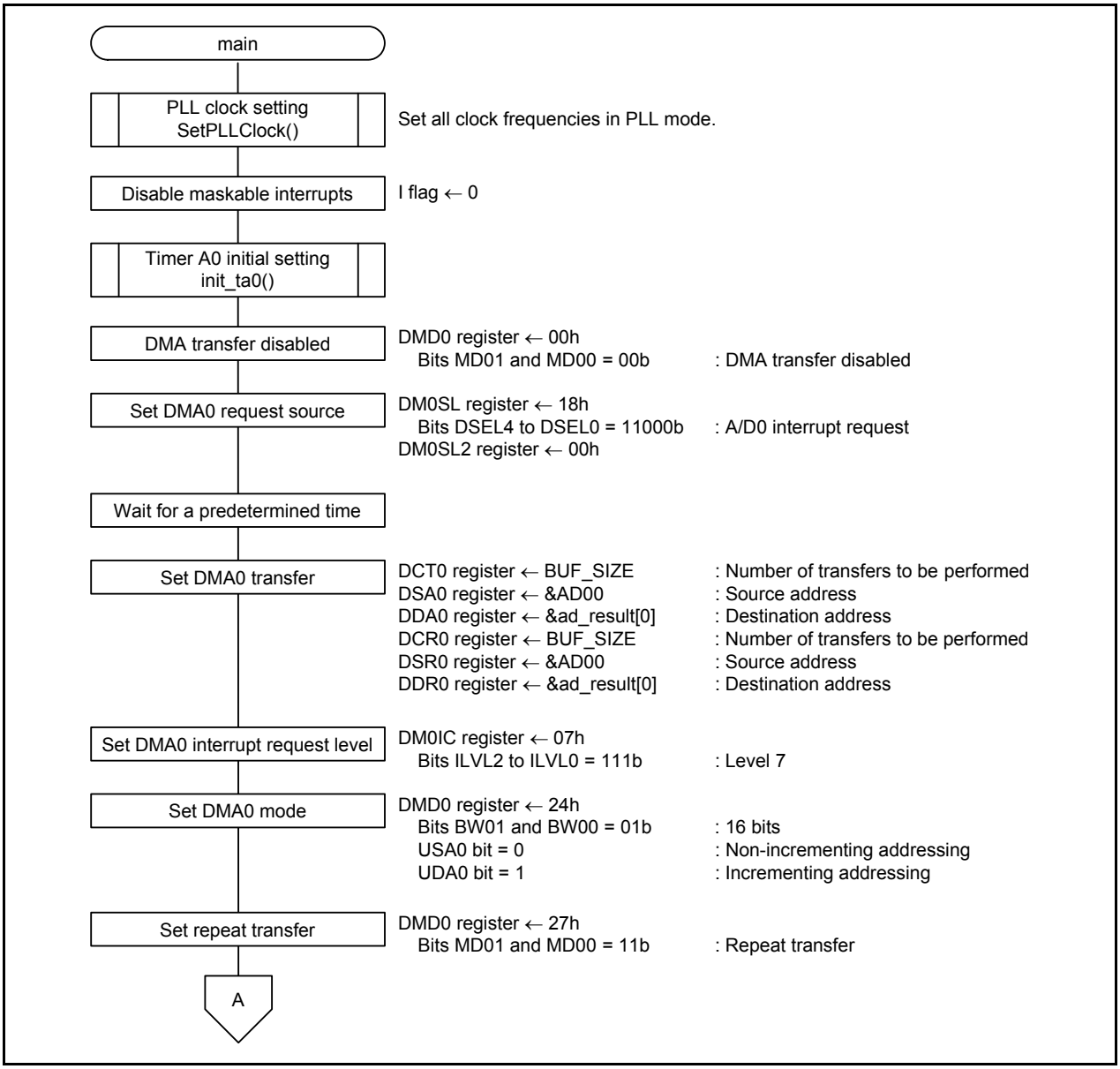

Figure 5.2 Main Processing (1/2)

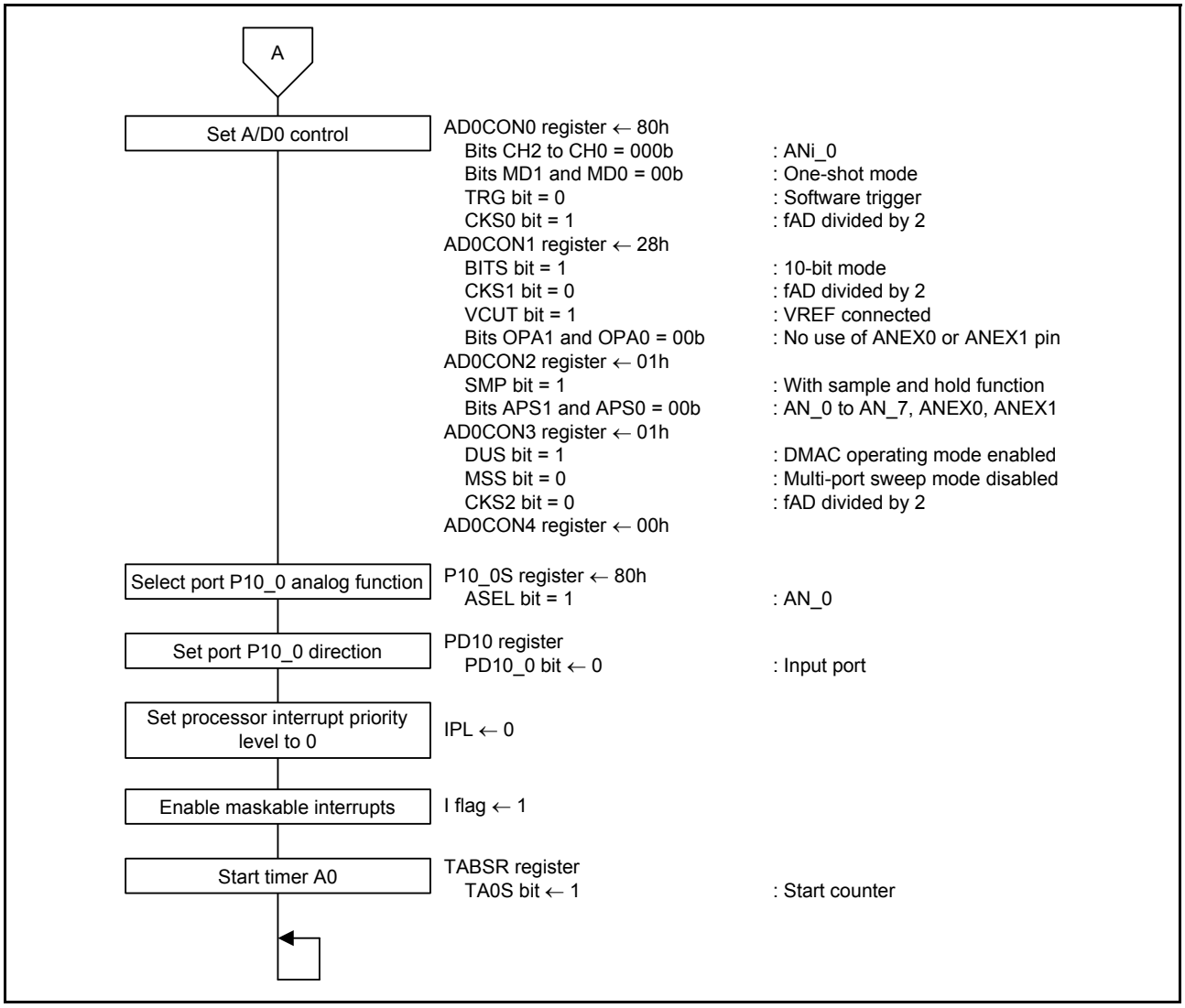

Figure 5.3 Main Processing (2/2)

5.4.2 Timer A0 Initial Setting

Figure 5.4 shows the Timer A0 Initial Setting.

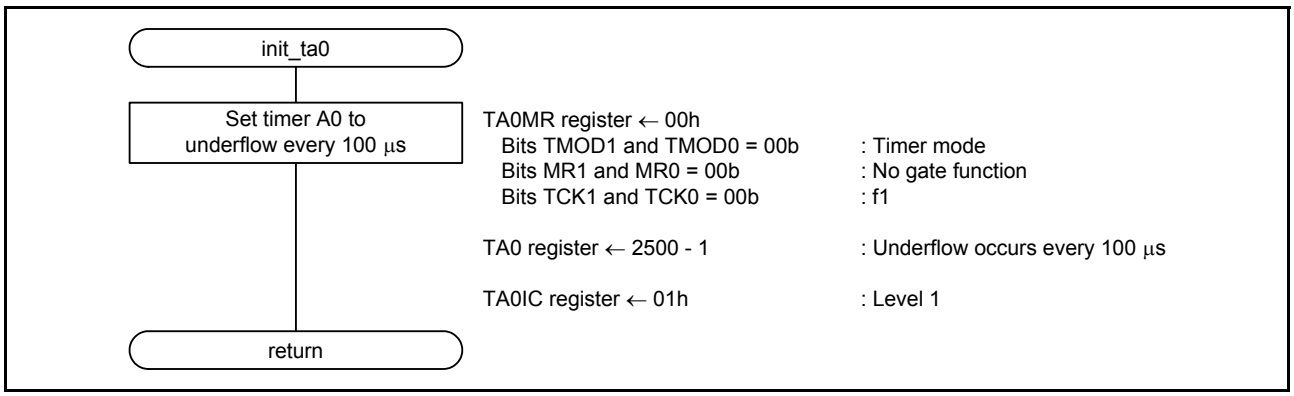

Figure 5.4 Timer A0 Initial Setting

5.4.3 Timer A0 Interrupt Handling

Figure 5.5 shows the Timer A0 Interrupt Handling.

Figure 5.5 Timer A0 Interrupt Handling

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

R32C/111 Group User's Manual: Hardware Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

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http://www.renesas.com/

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http://www.renesas.com/inquiry

Revision History	R32C/100 Series Application Example of A/D Converter Operation in One-shot Mode Using DMAC

Rev.	Date	Description	
		Page	Summary
1.00	May 31, 2011	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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