1. Abstract

This document describes a method for transferring an A/D converted result in one-shot mode to an internal RAM area using DMA.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):

MCUs: R32C/111 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above group. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Application Example

In one-shot mode, the analog voltage applied to the AN_0 pin is converted into a digital code only once. The converted result is transferred to an internal RAM area using DMA. Table 3.1 and Table 3.2 list the A/D Converter Operating Conditions and DMAC Operating Conditions, respectively.

### Table 3.1 A/D Converter Operating Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating clock</td>
<td>fAD divided by 2</td>
</tr>
<tr>
<td>Resolution</td>
<td>10-bit mode</td>
</tr>
<tr>
<td>A/D conversion start condition</td>
<td>Software trigger</td>
</tr>
<tr>
<td>A/D conversion method</td>
<td>With sample and hold function</td>
</tr>
<tr>
<td>Analog input pin</td>
<td>AN_0 (P10_0)</td>
</tr>
<tr>
<td>External op-amp</td>
<td>Not used</td>
</tr>
<tr>
<td>DMAC operating mode</td>
<td>Enabled (2, 3)</td>
</tr>
</tbody>
</table>

Notes:
1. The fAD frequency should be as follows:
   - When VCC = 4.2 to 5.5 V, 16 MHz or below.
   - When VCC = 3.0 to 4.2 V, 10 MHz or below.
   - Without the sample and hold function, 250 kHz or above.
   - With the sample and hold function, 1 MHz or above.
2. When DMAC operating mode is enabled, all A/D converted results are stored in the AD00 register.
3. If this register is read by a program while the DMAC operating mode is enabled, the value is undefined.

### Table 3.2 DMAC Operating Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMA trigger</td>
<td>A/D0 interrupt request</td>
</tr>
<tr>
<td>Transfer mode</td>
<td>Single transfer</td>
</tr>
<tr>
<td>Transfer size</td>
<td>16 bits</td>
</tr>
<tr>
<td>Addressing</td>
<td>Fixed address (AD00 register) to fixed address (internal RAM area)</td>
</tr>
</tbody>
</table>
3.1 Explanation

The following steps are for operation by the sample program:

1. Initial setting
   Initialize the DMAC and A/D converter.

2. A/D conversion started
   When setting the ADST bit in the AD0CON0 register to 1 (A/D conversion started), A/D conversion starts.

3. A/D conversion completed
   After A/D conversion is completed, the converted result is transferred to the AD00 register. Then, the ADST bit becomes 0 (A/D conversion stopped) and the IR bit in the AD0IC register becomes 1. At the same time, the result transferred to the AD00 register is transferred to an internal RAM area using DMA.

Figure 3.1 shows an Operation Example in One-shot Mode Using DMAC.

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**Figure 3.1 Operation Example in One-shot Mode Using DMAC**

1. Number of cycles with sample and hold function at 10-bit resolution.
   In other cases, the number of cycles are as follows:
   - Without sample and hold function at 10-bit resolution: 59 cycles
   - With sample and hold function at 8-bit resolution: 28 cycles
   - Without sample and hold function at 8-bit resolution: 49 cycles
3.2 Settings

The section shows the setting procedure and setting values to execute 3.1 “Explanation”. Refer to hardware user’s manuals for details of each register.

![Diagram of setting procedure]

Start of setting

- Set PLL Clock
- Disable maskable interrupts
- Set DMAC

ADCON0 ← 80h
- Set A/D control register 0.
  - Analog input pin selected: AN_0
  - A/D operating mode: One-shot mode
  - Frequency selected: fAD divided by 2 (1)

ADCON1 ← 28h
- Set A/D control register 1, (1, 2)
  - 10-bit mode selected
  - VREF connected

ADCON2 ← 01h
- Set A/D control register 2.
  - A/D conversion method: With sample and hold function
  - Analog input port selected: AN_0 to AN_7

ADCON3 ← 01h
- Set A/D control register 3. (1)
  - DMAC operating mode enabled
  - Multi-port sweep mode disabled

ADCON4 ← 00h
- Use P10_0 as A/D converter input (AN_0)
- Set the processor interrupt priority level to 0
- Enable maskable interrupts
- End of setting

Set DMAC

ADST_ADM0CON0 ← 1
- A/D conversion started

Notes:
1. The operating clock φAD is selected from a combination of the CKS0 bit in the AD0CON0 register, the CKS1 bit in the AD0CON1 register, and the CKS2 bit in the AD0CON3 register.
2. When the VCUT bit is switched from 0 to 1, A/D conversion should be started after at least 1 µs.

Figure 3.2 Setting Procedure of A/D Converter Operation in One-shot Mode Using DMAC (1/2)
A/D Converter Operation in One-shot Mode Using DMAC

Figure 3.3 Setting Procedure of A/D Converter Operation in One-shot Mode Using DMAC (2/2)

- **Start of DMAC setting**
- **DMD0 ← 00h**
- **DM0SL ← 18h**
  - **DM0SL2 ← 00h**
- **DCT0 ← 00000001h**
- **DSA0 ← &AD00**
- **DDA0 ← &ad_result**
- **DM0IC ← 07h**
- **DMD0 ← 04h**
- **DMD0 ← 05h**
  - **End of setting**

- Set DMA transfer mode. DMA transfer disabled.
- Select DMA trigger. A/D0 interrupt request.
- Set the number of DMA transfers.
- Set DMA source address. AD00 register.
- Set DMA destination address. Store internal variable to internal RAM area.
- Set DMA transfer complete interrupt request level.
- Set DMA transfer mode. Transfer size: 16 bits Source addressing: Non-incrementing addressing Destination addressing: Non-incrementing addressing
- Set DMA transfer mode. Transfer mode: Single transfer.
4. Sample Program
A sample program can be downloaded from the Renesas Electronics website.

5. Reference Documents
User’s Manuals
R32C/111 Group User’s Manual: Hardware Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02 C Compiler User’s Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support
Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
### REVISION HISTORY

<table>
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<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Jan. 31, 2011</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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