Linear Voltage Regulators

Fundamental Theory of PMOS Low-Dropout Voltage Regulators

Abstract

Most linear modern linear regulators use a PMOS architecture. This application note explains the key characteristics of a PMOS Low-Dropout Voltage Regulator (LDO) and the theory behind it.

1. Fundamentals

A voltage regulator is a constant voltage source that adjusts its internal resistance to any occurring changes of load resistance to provide a constant voltage at the regulator output. The internal resistance of a constant voltage source (Figure 1) must be significantly smaller than the external load resistor ($R_{IN} << R_L$) to ensure a constant output voltage over a certain range of load.

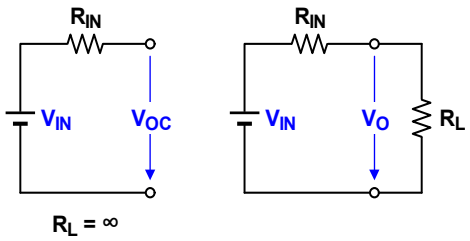

Figure 1. Constant-Voltage Source

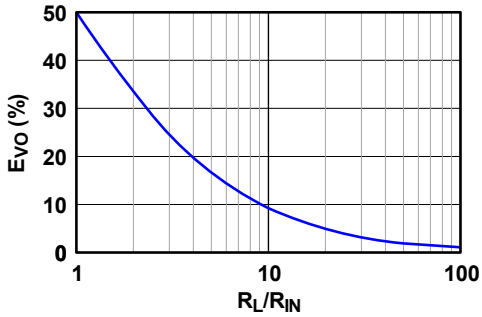

Figure 2. Output-Voltage Error vs Load Resistance

The output voltage of a voltage source under load condition is calculated with:

(EQ. 1) $$V_O = V_{IN} \cdot \frac{R_L}{R_{IN} + R_L}$$

Under the no-load condition ($R_L = \infty$), the open-circuit output voltage (V_{OC}) is the maximum possible output voltage, which is equal to the input voltage: $V_{OC} = V_{IN}$. As the load increases, the output voltage drops from its maximum value and introduces an output-voltage error, E_{VO}. This error is defined as the percentage difference between V_{OC}, the output voltage under no-load condition, and V_O, the output voltage under load condition:

(EQ. 2) $$E_{VO} = \frac{V_{OC} - V_O}{V_{OC}}$$

When replacing V_{OC} with V_{IN} and substituting V_O with Equation 1, the output voltage error is expressed through the resistor ratio of R_{IN} to R_L:

(EQ. 3) $$E_{VO} = \frac{R_{IN}}{R_{IN} + R_L}$$

A plot of the voltage error over a series of R_L/R_{IN} ratios confirms that the output voltage error, E_{VO}, increases with decreasing load resistance R_L, as shown in Figure 2.

To minimize the error, we need a circuit that senses any occurring load changes and, using some kind of feedback, adjusts a variable internal resistor to keep a constant ratio of internal-resistance to load resistance, as described by Equation 4.

(EQ. 4) $R_{IN} = k \cdot R_L$

When the relationship described in Equation 4 is true, R_{IN} must follow R_L in a linear relation, as expressed by Equation 4. The corresponding equivalent circuit is shown in Figure 3.

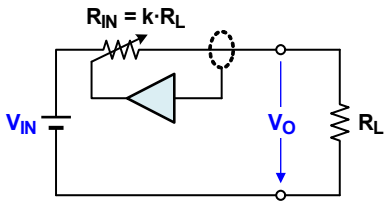

Figure 3. Linear Relation Between R_{IN} and R_L

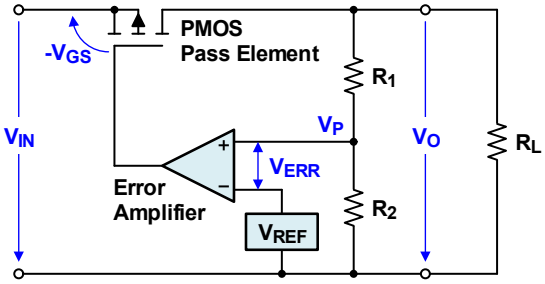

Figure 4. Basic Linear-Voltage Regulator

An electronic circuit that achieves this relationship by adjusting the variable input resistance is basically a linear-voltage regulator (Figure 4). Its functional building blocks are discussed in the following sections.

1.1 Voltage Reference, V_{REF}

The voltage reference is the foundation of all regulators. This reference is of the band-gap-type, which has the ability to operate at low supply voltages while providing sufficient accuracy and thermal stability to meet the less-stringent performance requirements of regulators. Bandgap references typically have an initial error of 0.5% to 1.0% and a temperature coefficient of 25ppm/°C to 50ppm/°C.

1.2 Error Amplifier

The error amplifier senses a scaled-down version of the output, $V_P = V_O \cdot R_2/(R_1 + R_2)$, compares it against the reference voltage ($V_P = V_{REF}$), and adjusts V_O using the series-pass element to the value required to drive the error signal ($V_{ERR} = V_P - V_{REF}$) as close as possible to zero. Setting $V_{REF} = V_P$ and solving for V_O yields Equation 5:

(EQ. 5) $$V_O = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

This calculation holds true only if V_{IN} is sufficiently high to keep the error amplifier and the pass element from saturating.

1.3 Feedback Network

The feedback network scales V_O to a value suitable for comparison against V_{REF} by the error amplifier. Because V_{REF} is fixed, the only way to program the value of V_O is by adjusting the ratio R_1 / R_2.

1.4 Pass Element

The series-pass element boosts the output-current capability of the error amplifier to the higher levels required by the load. This process involves transferring large currents from the source, V_{IN}, to the load under the low-power supervision of the error amplifier. A suitable pass element to carry out this task is a PMOS enhancement FET.

A PMOS FET has the two p-islands for the source and the drain terminals embedded in an n-substrate (Figure 5). The substrate is connected to the source, which usually has the most positive potential. The drain receives the most negative potential.

As the PMOS name indicates, the device uses p-type conductivity, which is established by applying a voltage to the gate that is negative relative to the source. The holes, which are the minority carriers in the n-substrate, are attracted by the negative gate electrode. Moving towards the upper region between the two p-islands, the holes

now become free-charge carriers, establishing a p-conductive bridge between source and drain. This way, the conductivity of the bridge and the drain current I_D, are controlled by the gate-source voltage, V_{GS}.

Because this type of FET enhances its conductivity with increasing V_{GS}, it is called an enhancement or normally-off type (Figure 6).

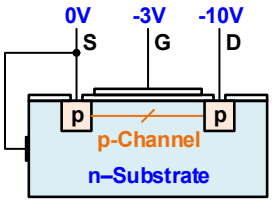

Figure 5. PMOS FET Basic Structure

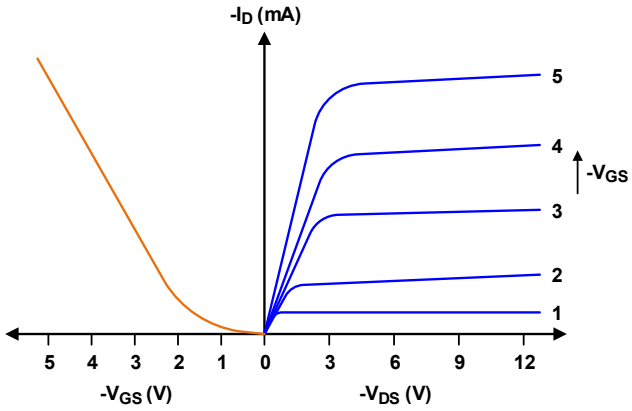

Figure 6. PMOS FET Input and Output Characteristics

2. Regulator Sequence

This section describes the regulation sequence when R_L drops as shown in Figure 9. Figure 7 depicts how the regulation sequence described relates to the internal LDO blocks.

When the load resistance drops, the output voltage falls from V_{O1} to V_{O2}, and the voltage across the pass element rises from $–V_{DS1}$ to $–V_{DS2}$. V_P (the scaled-down version of V_O) falls significantly below VREF causing the gate-source voltage to jump from $–V_{GS1}$ to $–V_{GS2}$.

The PMOS FET now conducts harder, increasing the output current from I_{O1} to I_{O2}. The output voltage and, by virtue of V_P, the error voltage starts to recover. The gate voltage increases gradually to $–V_{GS3}$, therefore causing the increased output current I_{O3} to generate an output voltage V_O. When this output voltage is scaled down using R_1 and R_2, the result is a zero-error voltage $V_{ERR} = 0$.

The output characteristic shown in Figure 8 confirms the regulation sequence. When R_L drops, the PMOS FET operating point jumps from P_1 to P_2 and then regulates to P_3.

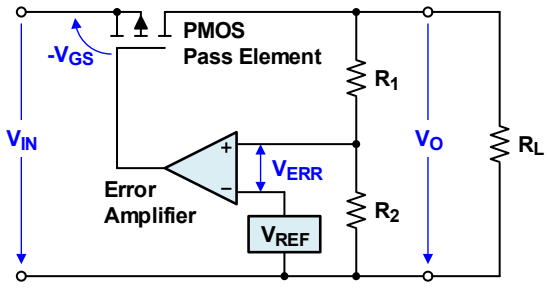

Figure 7. Regulator Block Diagram

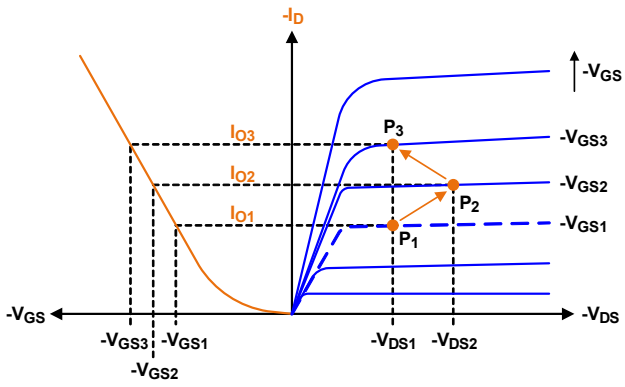

Figure 8. PMOS Input/Output Characteristic

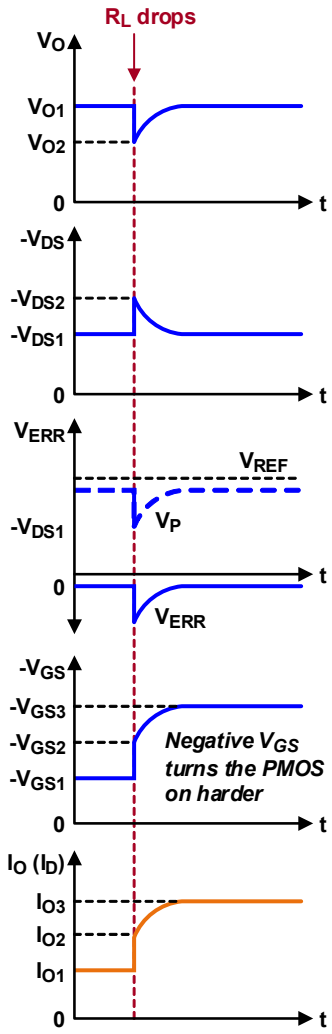

Figure 9. Regulation Sequence when R_L Drops

For a given quiescent point, P_3, where the output voltage is stabilized (that is, V_{OUT} and V_{DS} are constant), the corresponding output current, I_{OUT3}, is defined through Equation 6:

(EQ. 6) $$I_{OUT3} = \frac{V_{DS}}{R_{IN}} = \frac{V_O}{R_L}$$

Then, solving for R_{IN} yields:

(EQ. 7) $$R_{IN} = R_L \cdot \frac{V_{DS}}{V_O}$$

With $k = V_{DS}/V_O$, Equation 7 provides the linear resistance relation required by a linear voltage regulator.

3. Revision History

Rev.	Date	Description
1.00	May.21.20	Initial release

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