**Abstract**

Analog-to-Digital Converters (ADCs) that convert the sampled input signal through Successive Approximation (SAR), are known as SAR-ADCs. While there are various methods of performing successive approximation, Renesas SAR-ADCs use a method known as capacitive charge redistribution.

This application note explains the functional principle of a SAR-ADC based on charge redistribution.

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**Related Literature**

For a full list of related documents, visit our website:

- [SAR A/D Converter page](#)
1. Introduction

Figure 1 shows the simplified, switched-capacitor structure of a 5-bit SAR-ADC. The capacitor values are binary weighted from C, C/2 …C/16 or C/2^n-1. The last two capacitors have the same value of C/2^n-1. Only the first capacitor (connected to S0) is switched during the charge redistribution (the actual conversion). The other capacitor remains connected to ground.

MOS-transistors implement the required n+3 switches, and the voltage comparator provides the appropriate steering of these switches using auxiliary logic circuitry.

The conversion process is performed in three steps:

- Sample mode
- Hold mode
- Redistribution mode (the actual conversion)

2. Sample Mode

In the sampling mode (Figure 2), bus switch SB is switched to the input voltage, VIN, and SA is closed to ground. The capacitor switches, S4….S0’, are turned to the common bus B and all capacitors are charged to VIN. The total charge of QIN = VIN • 2C is stored on the left plates of the capacitors.
3. Hold Mode

During the hold mode (Figure 3), switch $S_A$ is open while the switches $S_4$,...,$S_0'$ are connected to ground, thereby making the voltage at the inverting comparator input $V_C = -V_{IN}$. This means that the switched-cap circuit already has a built-in sample-and-hold function.

![Figure 3. Hold Mode](image)

4. Redistribution Mode

The actual conversion is performed by charge redistribution. The first conversion step, shown in Figure 4, connects $C$ (the largest capacitor) using $S_4$ to the reference voltage $V_{REF}$, which corresponds to the Full-Scale Range (FSR) of the ADC.

![Figure 4. Conversion Step 1 Determines the MSB (Bit 4)](image)

Capacitor $C$ forms a 1:1 capacitance divider with the remaining capacitors connected to ground. The comparator input voltage becomes $V_C = -V_{IN} + V_{REF}/2$. This voltage is compared with the voltage potential of 0V at the non-inverting input. Therefore, if $|V_{IN}| > V_{REF}/2$, $V_C < 0$, and the comparator output $V_O$ goes high, setting the Most Significant Bit (MSB) ($Bit 4$) = 1. However, if $|V_{IN}| < V_{REF}/2$, $V_C > 0$, $V_O$ remains low, and $Bit 4 = 0$. If $V_O = high$, $S_4$ remains connected to $V_{REF}$ for the rest of the conversion. If $V_O = low$, $S_4$ is switched back to GND.

This procedure is repeated for switches, $S_3$ to $S_0$, except $S_0'$, which remains connected to GND for the entire conversion.

Summarizing, the conversion or charge redistribution procedure can be expressed by two equations:

(EQ. 1) \[ \text{If } -V_{IN} + V_{REF} \cdot X > 0 \Rightarrow V_O = \text{High} \quad \Rightarrow \quad \text{maintain switch position} \]

(EQ. 2) \[ \text{If } -V_{IN} + V_{REF} \cdot X < 0 \Rightarrow V_O = \text{Low} \quad \Rightarrow \quad \text{connect switch back to GND} \]

with $X$ as the ratio of the capacitive voltage divider because of a given switch position.
Therefore, the comparator input voltage of the final conversion step is:

\[
V_C = -V_{IN} + \text{bit 4} \cdot \frac{V_{REF}}{2} + \text{bit 3} \cdot \frac{V_{REF}}{4} + \text{bit 2} \cdot \frac{V_{REF}}{8} + \text{bit 1} \cdot \frac{V_{REF}}{16} + \text{bit 0} \cdot \frac{V_{REF}}{32}
\]

5. Conversion Example

The following example shows the conversion process of a 5-bit SAR-ADC for \( V_{IN} = 3V \) and \( V_{REF} = 5V \). According to Equation 3, the comparator input voltage of the final conversion step must be:

\[
V_C = -3V + [1] \cdot 2.5V + [0] \cdot 1.25V + [0] \cdot 0.625V + [1] \cdot 0.3125V + [1] \cdot 0.15625V = -0.03125V
\]

**Sample Mode:** All capacitors are connected to voltage bus B using \( S_4 \) to \( S_0' \) and to ground using \( S_A \). Bus B is connected to \( V_{IN} \). All capacitors are charged up to \( V_{IN} = 3V \) (Figure 5).

**Hold Mode:** The left side of the capacitors is connected to ground using \( S_4 \) to \( S_0' \). The common (right) side of the capacitors is disconnected from ground using \( S_A \), therefore, creating a comparator input voltage of \(-V_{IN} = -3V\) (Figure 6).

**Redistribution Mode:** The actual conversion starts by connecting \( S_B \) to \( V_{REF} = 5V \).

**Bit 4 (MSB):** The first conversion step determines the most significant bit (MSB = Bit 4) connecting C to \( V_{REF} \) using \( S_4 \). The ratio of the capacitive voltage divider becomes \( X = \frac{1}{2} \) and creates a comparator input voltage of \( V_C = -0.5V \). This turns the comparator output high and sets Bit 4 to 1. It also means that \( S_4 \) must remain in the present position for the rest of the conversion process (Figure 7).
Bit 3: The second conversion step determines Bit 3 by connecting C/2 to VREF using S3. The divider ratio changes to X = 3/4, causing a comparator input of VC = +0.75V. This turns the comparator output low and sets Bit 3 to 0. It also means that S3 must be switched back to ground (Figure 8).

Bit 2: The third conversion step determines Bit 2 by connecting C/4 to VREF using S2. The divider ratio changes to X = 5/8, causing a comparator input of VC = +0.125V. This turns the comparator output low and sets Bit 2 to 0. It also means that S2 must be switched back to ground (Figure 9).

Bit 1: The fourth conversion step determines Bit 1 by connecting C/8 to VREF using S1. The divider ratio changes to X = 9/16, causing a comparator input of VC = -0.1875V. This turns the comparator output high and sets Bit 1 to 1. It also means that S1 must remain in the present position for the rest of the conversion process (Figure 10).
Bit 0: The fifth conversion step determines Bit 0 by connecting C/16 to VREF using S0. The divider ratio changes to \( X = \frac{19}{32} \), causing a comparator input of \( V_C = -0.03125V \). This turns the comparator output high and sets Bit 0 to 1. It also means that S0 must remain in the present position (Figure 11).

Figure 10. Bit 1: Because \( V_O = H \), Bit 1 = 1. Therefore, S1 Must Remain in its Current Position

Figure 11. Bit 0: Because \( V_O = H \), Bit 0 = 1. Therefore, S0 Must Remain in its Current Position

6. Timing Diagram

Figure 12 shows the timing diagrams for the bus voltage (\( V_B \)) the comparator input voltage (\( V_C \)) the On/Off status of all switches (1 = On), and the individual capacitor voltages, \( V_{C1} \) to \( V_{C16} \).
7. Revision History

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<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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<tbody>
<tr>
<td>1.00</td>
<td>Sep.17.20</td>
<td>Initial release</td>
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