Instrumentation Amplifiers

Working with the ISL2853x and ISL2863x High-Precision Instrumentation Amplifiers

Abstract

The ISL2853x and the ISL2863x are zero-drift instrumentation amplifiers (INAs) with nine programmable gain settings and rail-to-rail inputs and outputs. Their low offset, low noise, low gain error, and high CMRR makes these amplifiers ideal for high precision applications over the full industrial temperature range.

Both amplifiers possess the same programmable input stage, whose output terminals, VA+ and VA-, allow for the sensing of the input common-mode voltage. Their outputs, however, differ. The ISL2853x provides a single-ended output and an uncommitted zero-drift op-amp (Figure 1), while the ISL2863x offers a fully differential output (Figure 2).

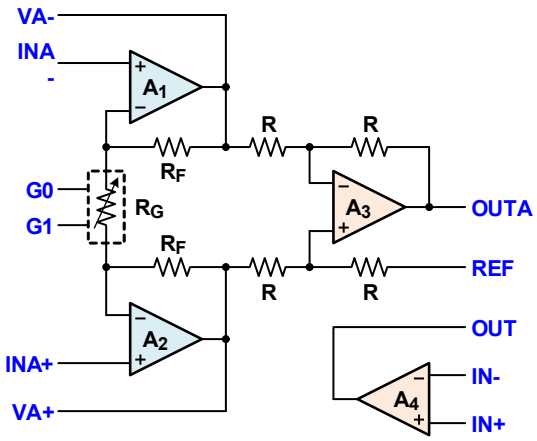

Figure 1. ISL2853x with Single Output and Uncommitted Zero-Drift Op-Amp

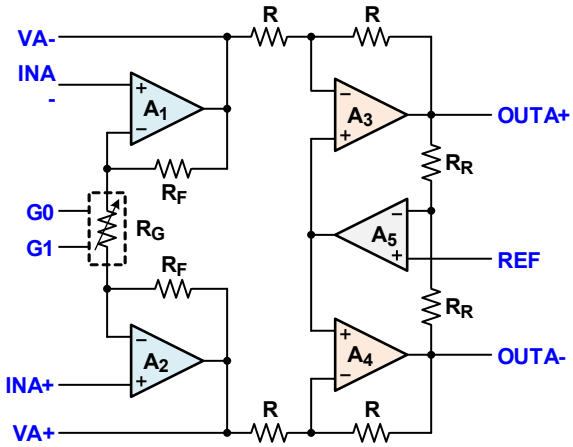

Figure 2. ISL2863x with Differential Output

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Related Literature

For a full list of related documents, visit our website:

- ISL28533, ISL28534, ISL28535, ISL28633, ISL28634, ISL28635 device pages

1. The Input Stage

An instrumentation amplifier amplifies a small differential input signal, V_{ID}, that is superimposed on a much larger common-mode voltage, V_{CM}. To avoid output saturation, its differential input stage must have two distinguished gain factors, one for common-mode signals, G_{CM}, and one for differential signals, G_{Diff}.

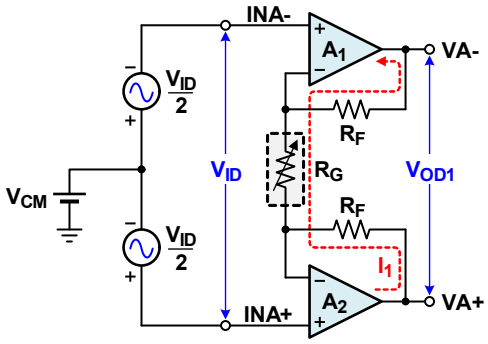

Figure 3. Differential Input Stage

Signal convention assigns each input the common-mode component and half the differential signal component:

(EQ. 1) $$V_{INA+} = V_{CM} + V_{ID}/2 \quad \text{and} \quad V_{INA-} = V_{CM} - V_{ID}/2$$

The difference between the input voltages is the differential input voltage, V_{ID}:

(EQ. 2) $$V_{INA+} - V_{INA-} = V_{CM} + V_{ID}/2 - (V_{CM} - V_{ID}/2) = V_{ID}$$

Due to op-amp action, the signals at the non-inverting inputs of the amplifier also appear at their inverting inputs. If V_{ID} = 0V, V_{CM} appears at the inverting inputs across R_G, which means no current is flowing through the R_F-R_G resistor network. This also means that V_{CM} is present at VA+ and VA-, indicating zero differential output.

The input gain for common-mode signals is therefore 1: G_{CM} = 1.

If V_{INA+} is larger than V_{INA-}, the resulting positive V_{ID} also occurs across R_G, causing a current, I_1, to flow from VA+ to VA-:

(EQ. 3) $$I_1 = \frac{V_{INA+} - V_{INA-}}{R_G} = \frac{V_{ID}}{R_G}$$

The differential output voltage due to this current is:

(EQ. 4) $$V_{OD1} = V_{VA+} - V_{VA-} = I_1(R_G + 2R_F)$$

Inserting Equation 3 into Equation 4 and solving for differential output-to-input change gives the differential gain:

(EQ. 5) $$\frac{V_{OD1}}{V_{ID}} = G_{DIFF} = 1 + \frac{2R_F}{R_G}$$

While standard instrumentation amplifiers require the use of precision resistors to minimize gain error, the ISL2853x and ISL2863x provide up to nine on-chip programmable gain settings, listed in Table 1.

Table 1. Programmable Gain Settings

G1	G0	Gain (V/V)		
		ISL28533 ISL28633	ISL28534 ISL28634	ISL28535 ISL28635
0	0	1	1	1
0	Z	2	2	100
0	1	4	10	120
Z	0	5	50	150
Z	Z	10	100	180
Z	1	20	200	200
1	0	40	300	300
1	Z	50	500	500
1	1	100	1000	1000

Note: Ground = 0, VCC = 1, and Z = floating.

The three states of the gain setting logic can be accomplished through pin-strapping the G0 and G1 inputs to either of the supply rails (Ground for 0, VCC for 1) and floating for Z (high-impedance). Internal high-impedance pull-up and pull-down resistors ensure the validity of the high-impedance state. If G0 and G1 are controlled by a microcontroller, the high-impedance state is accomplished by switching an output port into input mode while disabling the internal pull-up and pull-down resistors of the controller.

1.1 Internal Saturation Caution

To prevent instrumentation from internal saturation, it is good to know the absolute voltages at VA+ or VA-. This allows for determining the available signal headroom, which is the distance between the common-mode potential and the upper and lower supply rails, and therefore the calculation of the maximum allowable gain setting.

The absolute voltages at VA+ and VA- are easily found when considering their corresponding input voltages, V_{INA+} and V_{INA-} in Equation 1 on page 3. The common-mode component, V_{CM}, is amplified by the common-mode gain, G_{CM} = 1, and the differential signal component, $V_{ID}/2$, is amplified by the differential gain, G_{Diff}, which results in:

(EQ. 6) $$V_{VA+} = V_{CM} + \frac{V_{ID}}{2} G_{Diff} \quad \text{and} \quad V_{VA-} = V_{CM} - \frac{V_{ID}}{2} G_{Diff}$$

To avoid internal saturation, the voltage at VA+ must equal to or smaller than the positive supply voltage, V+, and the voltage at VA- must be equal to or greater than the negative supply voltage, V-. Then, substituting V_{VA+} and V_{VA-} in Equation 6 with V+ and V- respectively, and solving for G_{Diff}, yields the maximum allowable gain setting:

(EQ. 7) $$G_{Diff} \leq 2\frac{V_+ - V_{CM}}{V_D} \quad \text{and} \quad G_{Diff} \leq 2\frac{V_{CM} - V_-}{V_D}$$

Calculation Example 1:

Figure 4 depicts a symmetrical strain gauge sensor with 1kΩ base resistance with a maximum change in resistance of ΔR = ±10Ω. Due to bridge symmetry, the V_{CM} of the bridge = 1.65V.

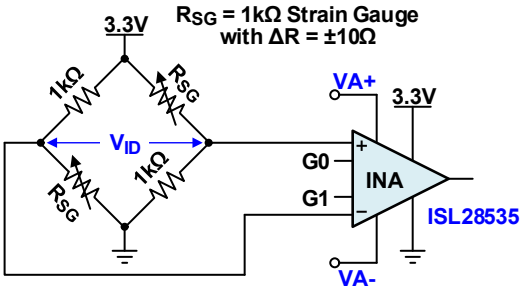

Figure 4. 1kΩ Symmetrical Strain Gauge Sensor

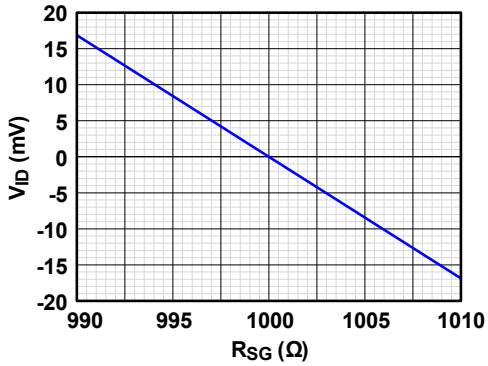

Figure 5. V_{ID} = ±17mV Over ±10Ω Resistance Change

Powered by a single 3.3V system supply, the ±10Ω span creates a V_{ID} span of ±17mV (Figure 5). Using Equation 7, the maximum gain setting is:

$$G_{Diff} \le 2\frac{3.3V - 1.65V}{17mV} = 194\,V/V$$

Table 1 shows that of the three single-output instrumentation amplifiers, the amplifier with the closest lower gain setting is the ISL28355 with 180V/V. This gain setting allows G0 and G1 to be floating.

Using Equation 6, we can calculate the absolute voltages at VA+ and VA- to ensure they are within the supply rails:

$$V_{VA+} = 1.65V + \frac{17mV}{2}\cdot 180 = 3.18V \quad \text{and} \quad V_{VA-} = 1.65V - \frac{17mV}{2}\cdot 180 = 0.12V$$

2. The Single Output Stage of the ISL2853x

The output stage of the ISL2853x is a difference amplifier that removes the input common-mode voltage, V_{CM}, amplifies the differential output of the input stage, and then adds a common-mode voltage in the form of V_{REF} to the output voltage at OUTA (Figure 6).

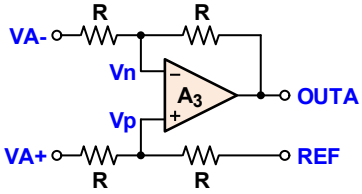

Figure 6. ISL2853x Output Stage

To derive its transfer function, we derive the voltages at the inverting and non-inverting of the inputs op-amp with:

$$V_n = \frac{V_{A-} + V_{OUTA}}{2} \quad \text{and} \quad V_p = \frac{V_{A+} + V_{REF}}{2}$$

Due to op-amp action, $V_n = V_p$, it follows that $V_{A-} + V_{OUTA} = V_{A+} + V_{REF}$, and solving for V_{OUTA} gives:

(EQ. 8) $$V_{OUTA} = V_{A+} - V_{A-} + V_{REF}$$

From Equation 5 we derive that $V_{VA+} - V_{VA-} = G_{DIFF} \cdot V_{ID}$ and inserting this term into Equation 8 gives:

(EQ. 9) $$V_{OUTA} = G_{DIFF} \cdot V_{ID} + V_{REF}$$

Therefore, the INA output voltage is the differential input voltage amplified by the differential gain setting plus the added common-mode voltage, V_{REF}.

In dual supply applications, REF is usually connected to ground (Figure 7). In a single-supply design however, V_{REF} should be set to $V_{CC}/2$ to allow for a symmetrical output swing of V_{OUTA} (Figure 8).

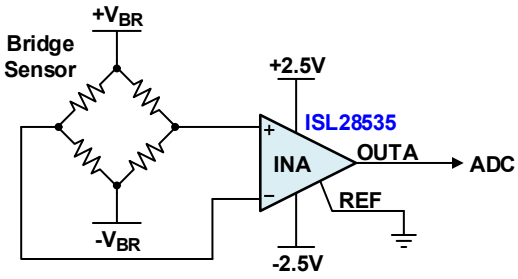

Figure 7. In a Dual-Supply Design Connect REF to GND

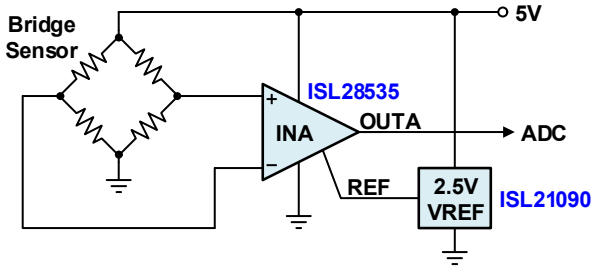

Figure 8. In a Single-Supply Design Make $V_{REF} = V_{CC}/2$

Note: For clarity, any decoupling capacitors have been omitted. With regards to Figure 8, some applications show the output of a voltage reference IC (VREF) buffered by an op-amp. This is usually not necessary but only required if the reference circuit lacks current drive or the capability of sinking current. VREFs are specially designed to provide a stable, low-noise voltage source with low source impedance.

However, there are applications where the reference input of the INA is not driven by a VREF, but with an op-amp in various amplifier configurations. In these cases, the uncommitted op-amp, A4, of the ISL2853x is extremely useful.

3. Applications Utilizing the Uncommitted Op-Amp

3.1 Buffer for Weak Voltage Reference ICs

Figure 9 depicts the op-amp as a buffer for weak voltage reference ICs. Here, weak means the IC lacks in output current drive, or in the ability of sinking current.

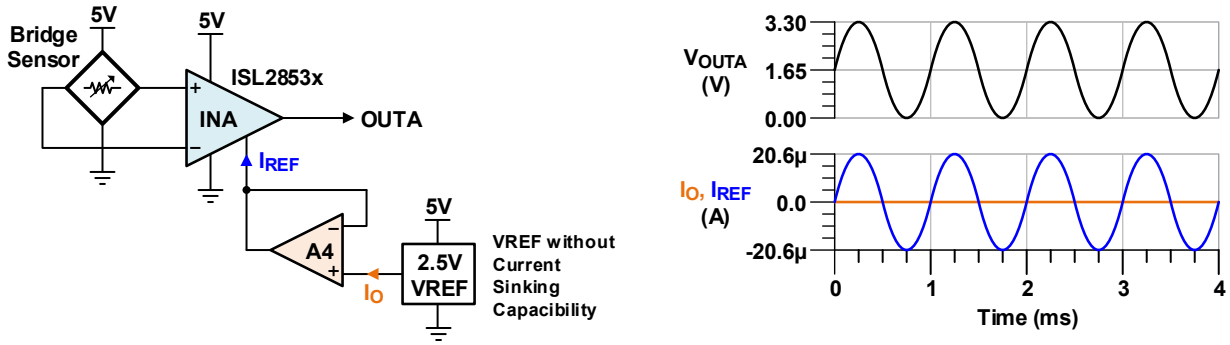

Figure 9. Buffering a Voltage Reference that Lacks Current Sinking Capability

The signal diagram on the right in Figure 9 shows that the input current to the REF terminal of the INA changes with the output voltage. A robust VREF can supply this current directly into the REF terminal. In the case of a weak VREF however, the op-amp provides the required current drive as well as sinking capability, while the output current of the VREF is reduced to leakage level.

3.2 Buffer for a Supply-Derived Reference Voltage

Ratio-metric circuits derive their reference voltage from the system supply to ensure that $V_{REF} = V_S/2$, independently of the absolute supply voltage. Figure 10 shows the level of V_{REF} being established with a high-impedance voltage divider to minimize current loading on the supply.

To maintain a high PSRR, a large 100µF capacitor, C_{IN}, is connected parallel to R_2. This capacitor, in combination with the parallel circuit of R_1 and R_2, forms a low-pass filter for the supply voltage ripples. Its -3dB frequency is calculated with $f_{-3dB} = 1/(2\pi R_1 \| R_2 C_{IN})$. For the circuit below, f_{-3}dB = 32mHz.

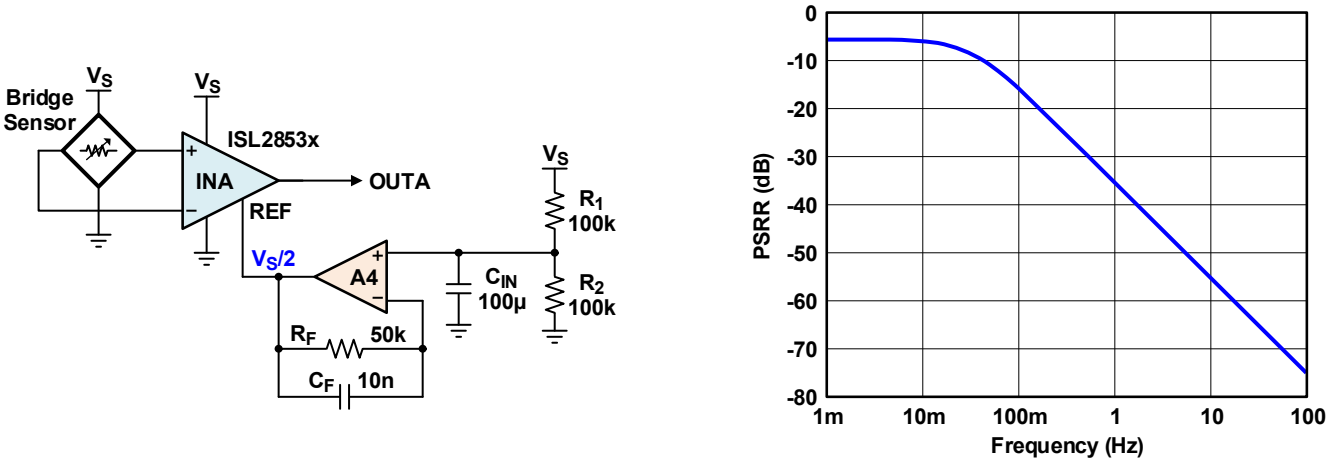

Figure 10. Proper Reference Buffering for High PSRR in Ratio-Metric Applications

Although the op-amp operates at unity-gain, a feedback resistor, R_F, is required to minimize the input offset due to bias currents. Its value should match the parallel combination of R_1 and R_2: $R_F = R_1 \| R_2$. The small capacitor, C_F, minimizes resistor noise.

3.3 Active Filter Buffer for a Supply-Derived Reference Voltage

A more elegant solution, using much smaller capacitor values, is the second-order active low-pass filter in Figure 11. Making $C_2 = 2\ C_1$ increases the quality factor to $Q = \sqrt{C_2/4C_1} = 0.707$, generating a sharper pass-to-stop band transition. Despite the large difference in capacitance, both circuits provide a PSRR of about -60dB at 20Hz.

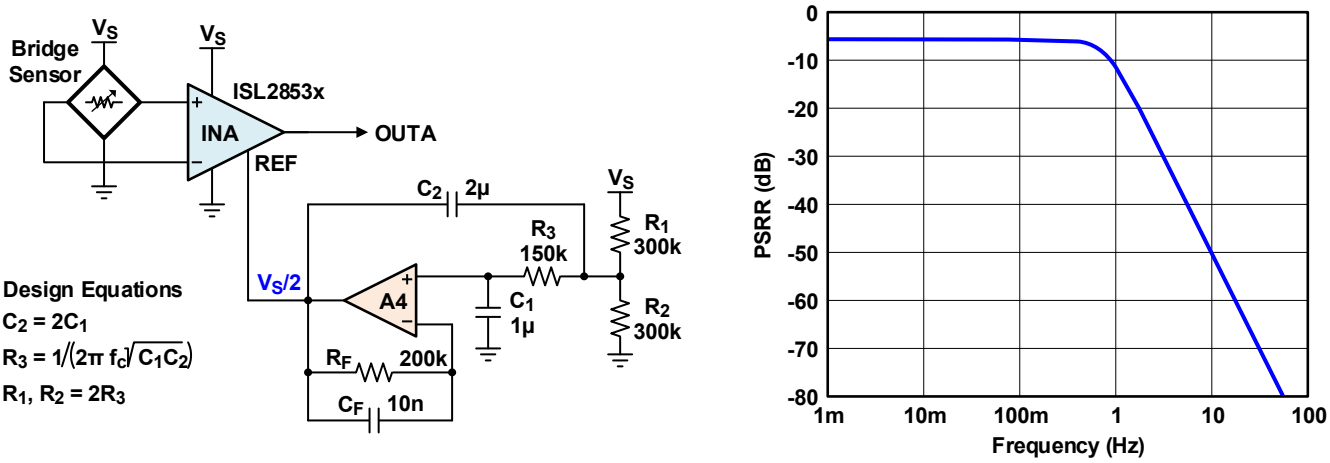

Figure 11. Improved Reference Buffering with Second-Order Active Low-Pass Filter

3.4 Feedback Integrator for Ultra-Low Input Bandwidth Limit

Medical sensors often require the lower bandwidth limit of less than 0.2Hz. Configuring A4 as a simple integrator and placing it into the feedback loop between the output of INA, OUTA, and its reference terminal, REF, transforms the lower bandwidth limit of the inputs of INA to very low frequencies (Figure 12). The -3dB cutoff frequency is determined by the R-C time constant of the integrator with $f_{-3dB} = 1/(2\pi R_F C_F)$.

Note: In this 5V application, the DC-bias voltage of the integrator is $V_B = V_{CC}/2 = 2.5V$.

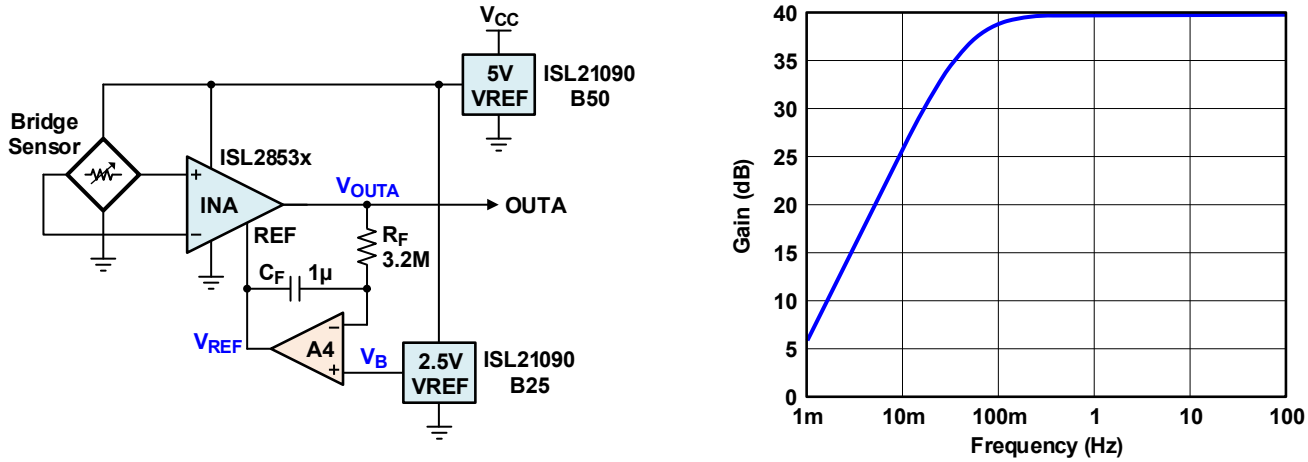

Figure 12. Feedback Integrator with A4 Achieves Extremely Low Cut-Off Frequencies with DC-Coupled Inputs

In the standard single-supply configuration of Figure 8, the output voltage of the INA is $V_{OUTA} = V_{ID} \cdot G_{DIFF} + V_{REF}$, (see Equation 9) with $V_{REF} = V_S/2$ as a fixed DC-bias potential. In this application however, V_{REF} is the output voltage of the integrator and therefore, frequency dependent: $V_{REF} = V_B(1 + X_{CF}/R_F) - V_{OUTA} X_{CF}/R_F$. Inserting this new V_{REF} term into Equation 9 and solving for V_{OUTA} gives:

$$V_{OUTA} = V_{ID} \cdot G_{DIFF} + V_B(1 + X_{CF}/R_F) - V_{OUTA} X_{CF}/R_F$$

Then, collecting terms yields:

$$V_{OUTA}(1 + X_{CF}/R_F) = V_{ID} \cdot G_{DIFF} + V_B(1 + X_{CF}/R_F)$$

And solving for V_{OUTA} results in:

$$V_{OUTA} = V_{ID} \cdot \frac{G_{DIFF}}{1 + X_{CF}/R_F} + V_B \cdot \frac{1 + X_{CF}/R_F}{1 + X_{CF}/R_F}$$

or

$$V_{OUTA} = V_{ID} \cdot G_{DIFF} \cdot \frac{1}{1 + X_{CF}/R_F} + V_B$$

This equation confirms that the actual DC-bias voltage (V_B), remains frequency independent.

To express the output voltage as a function of the -3dB cutoff frequency, we substitute X_{CF} with 1/(jωC), which turns the above fraction into:

$$\frac{1}{1 + X_{CF(f)}/R_F} = \frac{jf/f_C}{1 + jf/f_C} \quad \text{with} \quad f_C = \frac{1}{2\pi R_F C_F}$$

Then, insert this term into the output voltage equation:

(EQ. 10) $$V_{OUTA(f)} = V_{ID(f)} \cdot G_{DIFF} \cdot \frac{jf/f_C}{1 + jf/f_C} + V_B$$

Therefore, the total differential gain is:

(EQ. 11) $$\frac{\Delta V_{OUTA(f)}}{\Delta V_{ID(f)}} = G_{DIFF} \cdot \frac{jf/f_C}{1 + jf/f_C}$$

or in dB terms:

(EQ. 12) $$\left| \frac{V_{OUTA(f)} - V_B}{V_{ID(f)}} \right| (dB) = 20 \log_{10} \left(G_{DIFF} \cdot \frac{f/f_C}{\sqrt{1 + (f/f_C)^2}} \right)$$

Plotting Equation 12 over frequency yields the gain response of Figure 12. This shows that the total differential signal gain is 0V/V at DC, and only the bias voltage, V_B, is present at OUTA. Then, with rising frequency, the gain increases until it reaches the initial G_{DIFF} value at f_C.

The benefit of this solution is that it requires only small capacitor values to achieve extremely low input bandwidth limits, while leaving the INA inputs DC-coupled. The conventional approach of AC-coupling the inputs, requires much larger capacitor values of 100µF and more to achieve the same low-frequency cutoff.

3.5 Single-Ended to Differential Output Converter

Configuring A4 as a simple integrator and placing it into the feedback loop between the output of INA, OUTA, and its reference terminal, REF, converts an INA with a single output into an INA with a differential output. The purpose of this solution is to double the dynamic output signal range of the INA; therefore increasing the resolution of the amplified input signal (Figure 13).

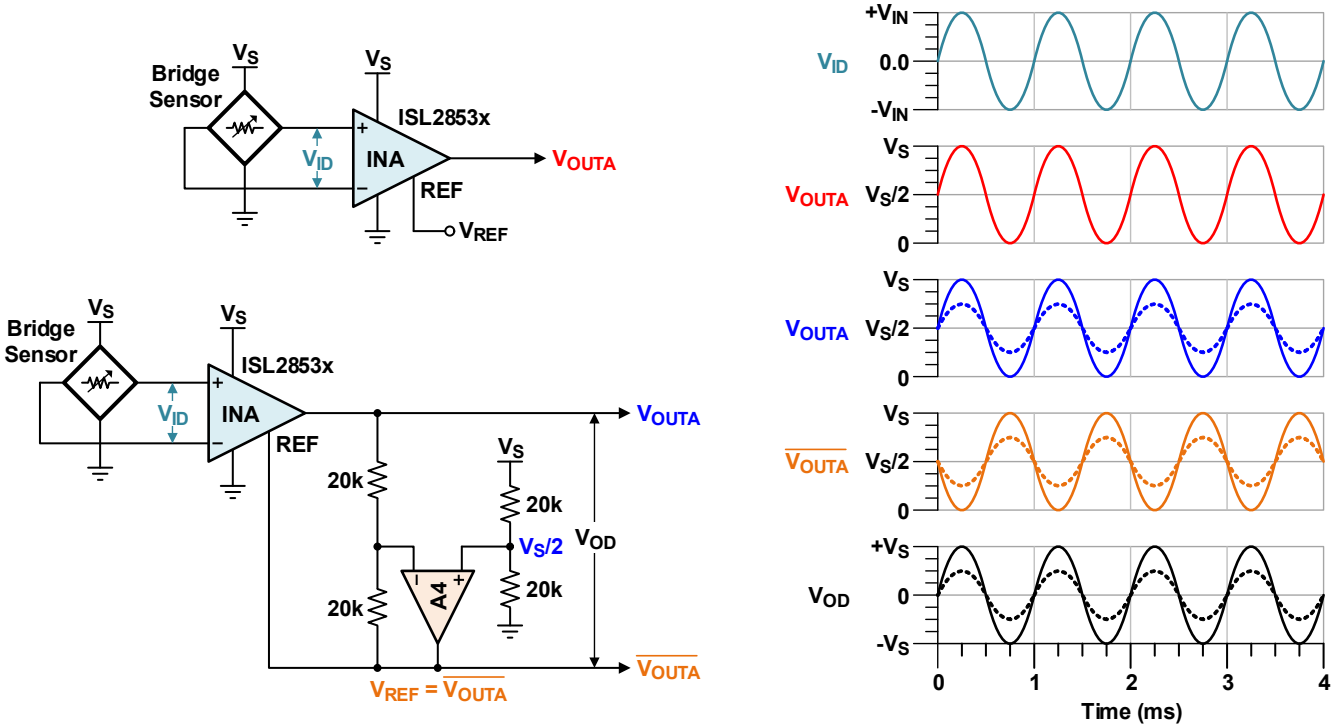

Figure 13. Differential Output Configuration with A4 Doubles Signal Dynamic Range

For better understanding, we compare the output dynamic range of the single output with the one of the differential output solution. The output dynamic range of the INA with single output is:

(EQ. 13) $$V_{OUTA} = G_{DIFF} \cdot V_{ID} + V_{REF}$$

Figure 13 depicts the positive terminal of the differential output as V_{OUTA}, and the negative terminal as $\overline{V_{OUTA}}$. The difference amplifier, operating at unity gain, buffers the difference between V_{OUTA} and V_S and drives the REF terminal of the INA and the negative output terminal:

(EQ. 14) $$V_{REF} = \overline{V_{OUTA}} = V_S - V_{OUTA}$$

Inserting this V_{REF} term into the single output equation and solving for V_{OUTA} gives:

(EQ. 15) $$V_{OUTA} = \frac{G_{DIFF} \cdot V_{ID}}{2} + \frac{V_S}{2}$$

Due to Equation 14, this makes the negative output voltage:

(EQ. 16) $$\overline{V_{OUTA}} = -\frac{G_{DIFF} \cdot V_{ID}}{2} + \frac{V_S}{2}$$

Equations 15 and 16 show that the signal dynamic of both, V_{OUTA} and $\overline{V_{OUTA}}$, is only half that of the single output amplifier; therefore, yielding only half of the possible output differential range, V_{OD}. This is indicated by the dotted waveforms in Figure 13, in comparison to the red waveform of the single output INA.

To use the full dynamic range of each output, the programmable gain, G_{DIFF}, must be doubled to yield:

(EQ. 17) $$V_{OUTA} = \frac{V_S}{2} + G_{DIFF} \cdot V_{ID} \quad \text{and} \quad \overline{V_{OUTA}} = \frac{V_S}{2} - G_{DIFF} \cdot V_{ID}$$

The resulting differential output voltage is twice the dynamic range of the single output INA:

(EQ. 18) $$V_{OD} = V_{OUTA} - \overline{V_{OUTA}} = 2G_{DIFF} \cdot V_{ID}$$

4. Summary

The uncommitted op-amp of (A4) of the ISL2853x family of single output INAs is a nice little tool, which, as demonstrated, can help satisfy a wide variety of signal conditioning requirements.

5. The Differential Output Stage of the ISL2863x

Figure 14 depicts the differential output stage of the ISL2863x family of INAs with programmable gain settings. The output of the first stage, V_{OD1}, is the input for the differential output stage. To find the equations for the differential and the individual output voltages, we define the three key voltages, Vn3, Vn4, and Vn5:

$$V_{n3} = \frac{V_{A-} + V_{OUTA+}}{2} \qquad V_{n4} = \frac{V_{A+} + V_{OUTA-}}{2} \qquad V_{n5} = \frac{V_{OUTA+} + V_{OUTA-}}{2}$$

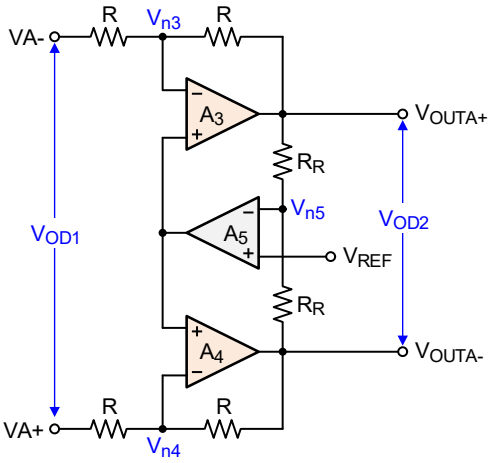

Figure 14. Differential Output Stage of ISL2863x

Due to op-amp action, $V_{n3} = V_{n4}$ and $V_{n5} = V_{REF}$, which results in:

(EQ. 19) $$\frac{V_{A-} + V_{OUTA+}}{2} = \frac{V_{A+} + V_{OUTA-}}{2}$$

and

(EQ. 20) $$V_{REF} = \frac{V_{OUTA+} + V_{OUTA-}}{2}$$

Solving Equation 19 for the differential output voltage gives:

(EQ. 21) $$V_{OUTA+} - V_{OUTA-} = V_{A+} - V_{A-}$$

Because V_{OUTA+} - V_{OUTA-} = V_{OD2} and V_{A+} - V_{A-} = V_{OD1} = $G_{DIFF} \cdot V_{ID}$, the differential output voltage is:

(EQ. 22) $$V_{OD2} = G_{DIFF} \cdot V_{ID}$$

To determine the actual voltage at OUT+, we solve Equation 20 for V_{OUTA-}, insert the result into Equation 21, and solve for V_{OUTA+}:

(EQ. 23) $$V_{OUTA+} = V_{REF} = \frac{V_{A+} - V_{A-}}{2} = V_{REF} + G_{DIFF} \cdot \frac{V_{ID}}{2}$$

Applying the same steps to V_{OUTA-} yields:

(EQ. 24) $$V_{OUTA-} = V_{REF} - G_{DIFF} \cdot \frac{V_{ID}}{2}$$

As a final check, we calculate the difference between the two output voltages and receive:

$$V_{OUTA+} - V_{OUTA-} = V_{OD2} = V_{REF} + G_{DIFF} \cdot \frac{V_{ID}}{2} - \left(V_{REF} - G_{DIFF} \cdot \frac{V_{ID}}{2} \right) = G_{DIFF} \cdot V_{ID}$$

This result confirms the correctness of Equation 22.

6. Conclusion

The ISL2853x and ISL2863x are high-performance low-noise auto-zero instrumentation amplifiers with on-chip programmable gain settings. The ISL2853x family offers a single output and an uncommitted op-amp that can be configured either as a reference buffer for ratio-metric applications, as a feedback integrator enabling ultra-low cutoff frequencies for DC-coupled inputs, or as a single-to-differential output converter. The ISL2863x family has a differential output, providing you with the widest possible output dynamic range for a high signal resolution.

Hardware circuit development is supported by the ISL2853xEV2Z and ISL2863xEV2Z evaluation boards with associated user guides and board design files. Figure 15 shows the evaluation board schematic.

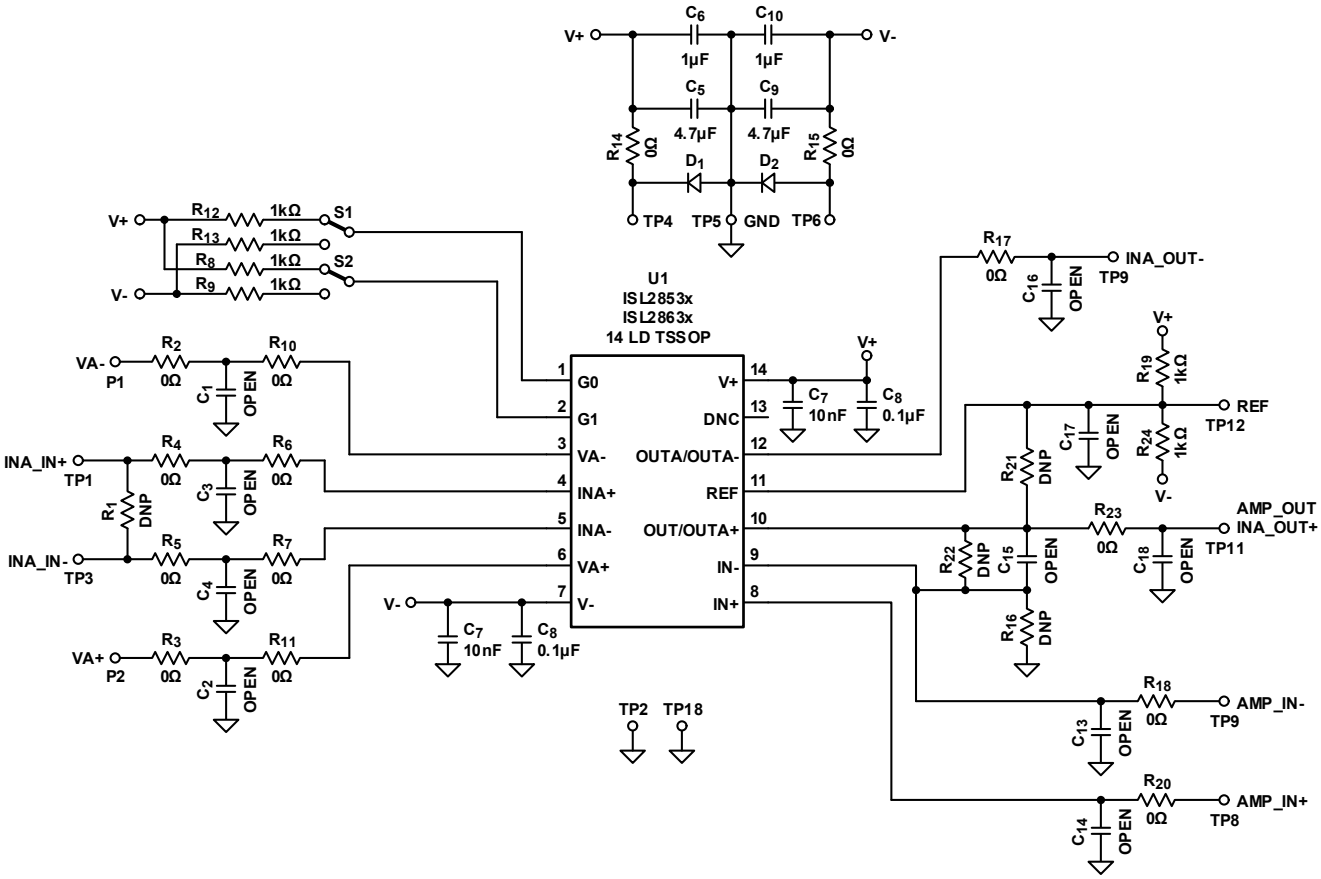

Figure 15. Evaluation Board Schematic

7. Revision History

Rev.	Date	Description
1.00	Apr.7.20	Initial release

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