Operational Amplifiers

How to Bias Op-Amps Correctly

Abstract

The inputs of an operational amplifier (op-amp) must be DC-biased to ensure proper device operation. A basic requirement that many textbooks neglect to discuss in detail. Consequently, engineers new to op-amps might overlook this important requirement, which can lead to malfunctioning circuits.

This application note tries to rectify this shortcoming by explaining the need for input biasing and suggesting practical solutions that ensure proper circuit operation.

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1. The Need for Input Biasing

Figure 1 shows the differential input stage of an op-amp. The base terminals of transistors Q_1 and Q_2 form the non-inverting and inverting op-amp inputs, IN+ and IN-, respectively. For the op-amp to operate correctly, these inputs must be DC biased. That is, the DC bias currents (I_{B+} and I_{B-}), must be able to flow into or out of the input terminals. The direction of the bias currents depends on the type of transistors. For NPN transistors and N-channel enhancement MOSFETs, the currents flow into the inputs, for PNPs and P-channel enhancement MOSFETs, the currents flow out of the inputs.

DC biasing is achieved by connecting the inputs via resistors to a reference potential, V_{mid}, which is the mid potential of the positive and negative supply voltages (V_{S+} and V_{S-}) (Figure 1).

The biasing resistors (R_{B+} and R_{B-}), represent equivalent resistances, because they can consist of one or more resistors as depicted in the DC-coupled amplifier circuits of Figure 2.

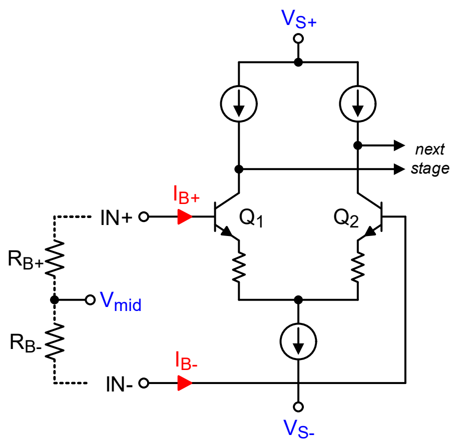

Figure 1. Input Biasing Principle

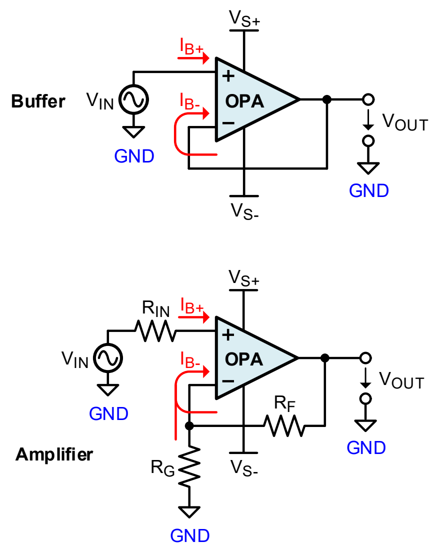

Figure 2. DC-Coupled Buffer and Amplifier

In the DC-coupled buffer of Figure 2, I_{B+} flows through the signal source and its low source impedance into the noninverting input, while I_{B-} flows from the output of the op-amp into the inverting input.

In the DC-coupled amplifier, I_{B-} flows through R_F and R_G; therefore changing the DC voltage at the inverting input by $I_{B-} \cdot (R_F||R_G)$. This introduces a DC offset voltage between the inputs. To minimize this offset, the DC potential at the non-inverting input must be adjusted by about the same amount. This is achieved by inserting a resistor (R_{IN}), in series whose value matches the parallel combination of R_F and R_G, $R_{IN} = R_F||R_G$.

2. AC-Coupled Amplifiers with Dual Supplies

While DC-coupled op-amp circuits receive their biasing through the signal source impedance, AC-coupled circuits have this bias path blocked by the input coupling capacitor (C_{IN}). Figure 3 shows an AC-coupled amplifier without a path for the DC bias current to flow. In this case, I_{B+} charges the coupling capacitor until the common-mode voltage rating of the input circuit is exceeded, or its output is driven into saturation. Depending on the polarity of the bias current, the capacitor charges towards the positive or negative supply rail, with the resulting bias voltage being amplified by the closed-loop DC gain of the amplifier, $1 + R_F/R_G$.

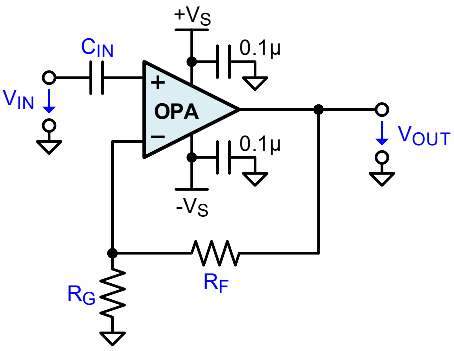

Figure 3. A Malfunctional AC-Coupled Amplifier with Missing DC Bias Path

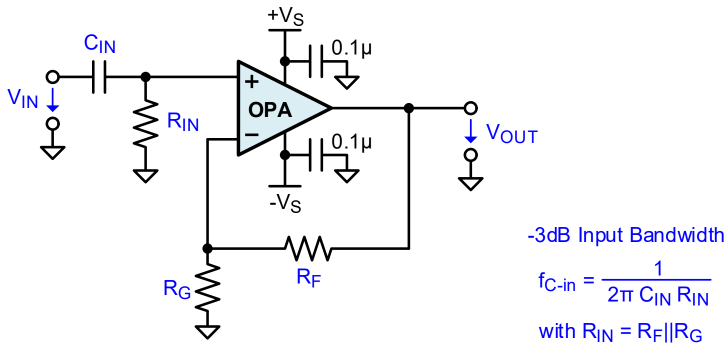

Figure 4. Correctly AC-Coupled Amplifier for Dual-Supply Operation

For a small bias current, such as 1pA, this process can take hours. Therefore, a casual lab test with an AC-coupled scope is more than likely to miss this problem, and the circuit does not fail until much later. Obviously, this problem must be avoided.

Figure 4 shows a simple solution by connecting the noninverting input through R_{IN} to ground. This forms a new DC path for the bias current. Like in the DC-coupled case before, minimizing the offset due to bias currents requires $R_{IN} = R_F \| R_G$.

Note: AC-coupling forms a high-pass filter with a cutoff at $f_C = 1/(2\pi\ C_{IN}\ R_{IN})$, which sets the minimum input bandwidth of the amplifier. With the circuit gain being defined by the application, R_F and R_G can be determined. Their parallel value defines R_{IN}, which then allows the calculation of the input capacitor: $C_{IN} = 1/(2\pi\ f_C\ R_{IN})$.

Similar input biasing methods must be applied to the differential input stages of three-amp Instrumentation Amplifiers (INAs). Figure 5 shows INA circuits that are AC-coupled using either two capacitors or a transformer, without providing a DC bias path.

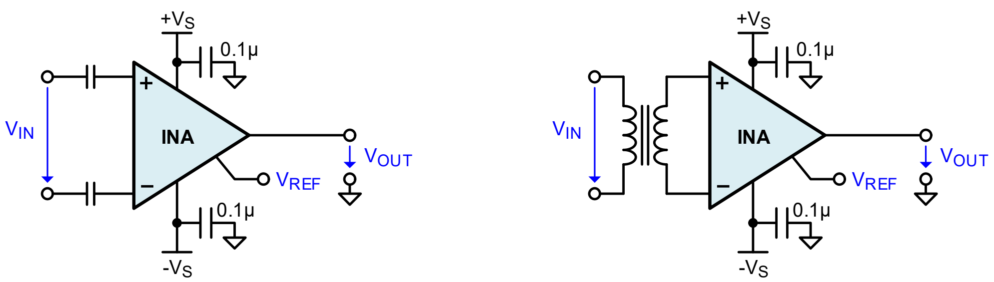

Figure 5. Examples of Non-Functional AC-Coupled Instrumentation Amplifiers

Correct biasing solutions for these circuits are shown in Figure 6, where a high-value resistor (R_{IN}) is added between each input and ground.

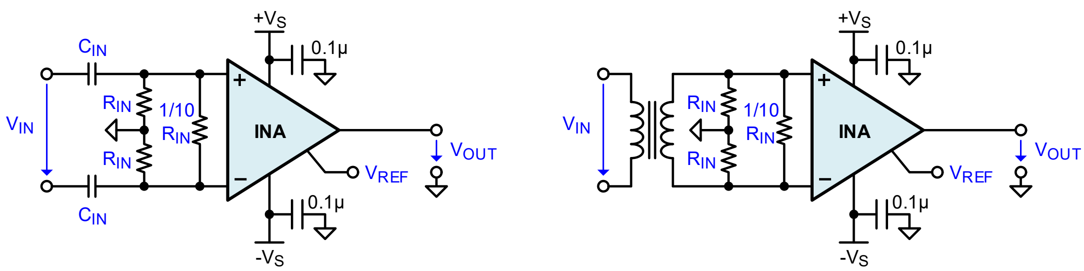

Figure 6. Correctly Biased INA Inputs use High-Value Input Resistors Between Each Input and Ground

There is a small offset-voltage error due to mismatches between the input resistors and the input bias currents. To minimize this error, a third resistor, about 1/10th their value (yet still large compared to the differential source resistance), can be connected between the two in-amp inputs, therefore bridging both resistors.

3. AC-Coupled Amplifiers with Single Supply

The DC biasing of AC-coupled single-supply amplifiers also requires an input resistor connecting the noninverting input to the reference potential, V_{mid}. In single supply circuits however, V_{mid} is derived from V_S as $V_S/2$ to ensure a symmetrical, maximum dynamic range for both, input and output signals. This can make $V_S/2$ susceptible to supply noise.

The ideal design approach is to use an integrated voltage-reference chip (VREF) with high power-supply rejection ratio (PSRR). A VREF also provides low output impedance, allowing to provide $V_S/2$ potential to multiple reference locations within a larger circuit design (Figure 7).

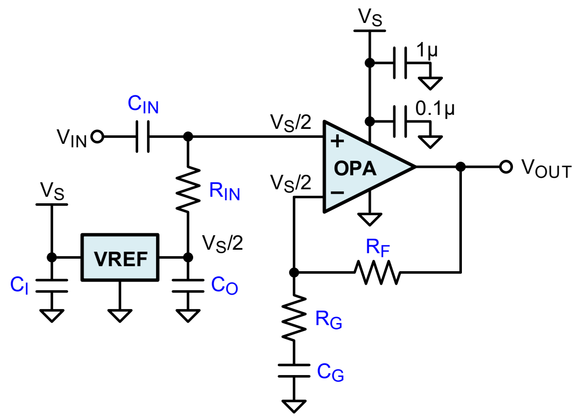

Figure 7. Input Biasing with Voltage Reference for Highest PSRR

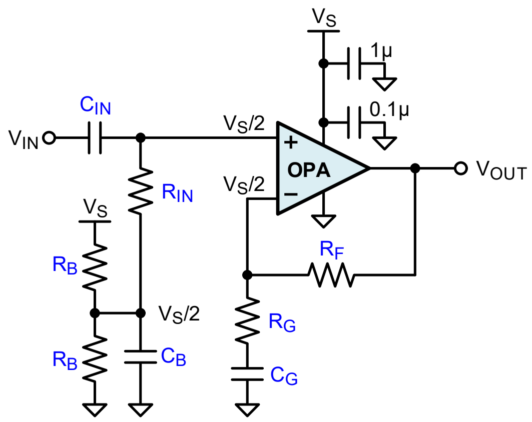

Figure 8. Input Biasing with Buffered Voltage Divider to Maintain High PSRR

For biasing a single-supply op-amp, a more convenient low-cost method exists in form of a voltage divider, whose output must be buffered with a large capacitor (C_B), to make $V_S/2$ less sensitive to supply noise, thus maintaining a high PSRR (Figure 8).

AC-coupled single-supply amplifiers also require the capacitive decoupling of the feedback path to ensure 0dB gain at DC. This prevents the $V_S/2$ potential at the noninverting input from being amplified by the passband gain, therefore saturating the output.

To calculate the component values, it is important to understand the interactions of the various time constants: R_B-C_B, R_{IN}-C_{IN}, and R_G-C_G. For clarity, their frequency responses are depicted in Figure 9, Figure 10, and Figure 11.

To the V_S supply, the biasing voltage divider presents a low-pass filter whose frequency response is:

$G_{SN} = \dfrac{\Delta V_{CC}/2}{\Delta V_{CC}} = \dfrac{1}{2} \cdot \dfrac{1}{1 + j\omega C_B R_B/2}$, with a cutoff frequency of $f_{CB} = \dfrac{1}{2\pi\, C_B\, R_B/2}$. Here, G_{SN} denotes the supply-noise gain.

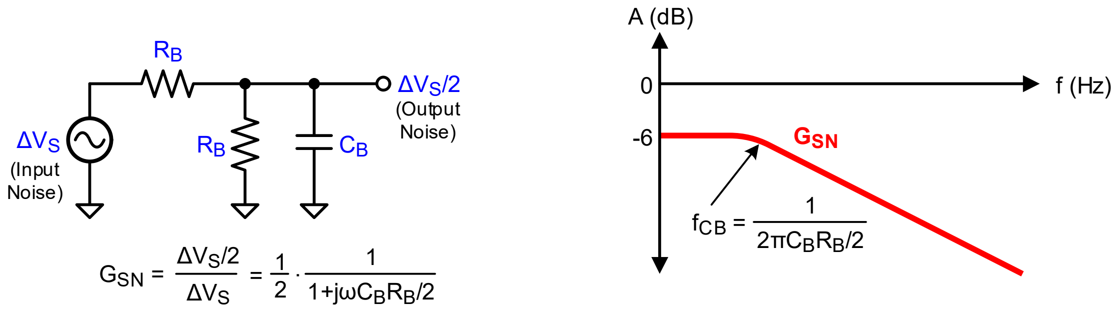

Figure 9. Transfer Function and Frequency Response of the Supply-Noise Gain of the Voltage Divider

The R_{IN}-C_{IN} circuit has a high-pass response $G_{IN} = \frac{j\omega C_{IN} R_{IN}}{1 + j\omega C_{IN} R_{IN}}$ with pole at $f_{CI} = \frac{1}{2\pi C_{IN} R_{IN}}$. This pole and the pole of the closed-loop gain, f_{pG}, determine the minimum input bandwidth of the amplifier circuit, f_{CT}.

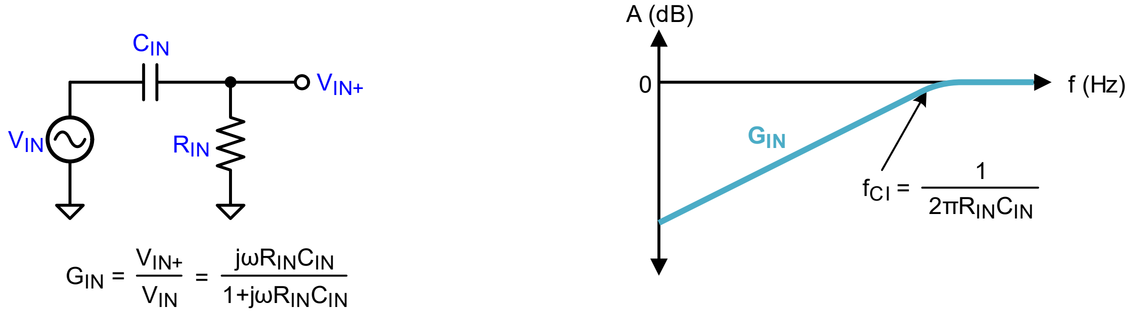

Figure 10. Transfer Function and Frequency Response of the AC-Coupled Input Stage

The closed-loop gain of the op-amp is given with $A_{CL} = \frac{1 + j\omega C_G (R_G + R_F)}{1 + j\omega C_G R_G}$.

It has a pole and a zero-location due to the decoupling effect of C_G. The zero frequency, $f_{zG} = \frac{1}{2\pi C_G (R_G + R_F)}$, is the +3dB corner frequency above unity gain. This zero ensures that DC voltages at the noninverting input, such as $V_S/2$ and any offset errors, are amplified at a gain of 1V/V (0dB). The pole frequency, $f_{pG} = \frac{1}{2\pi C_G R_G}$,

defines the -3dB cutoff of A_{CL}. This pole and the pole of the input stage, f_{CI}, determine the minimum input bandwidth of the amplifier circuit, f_{CT}.

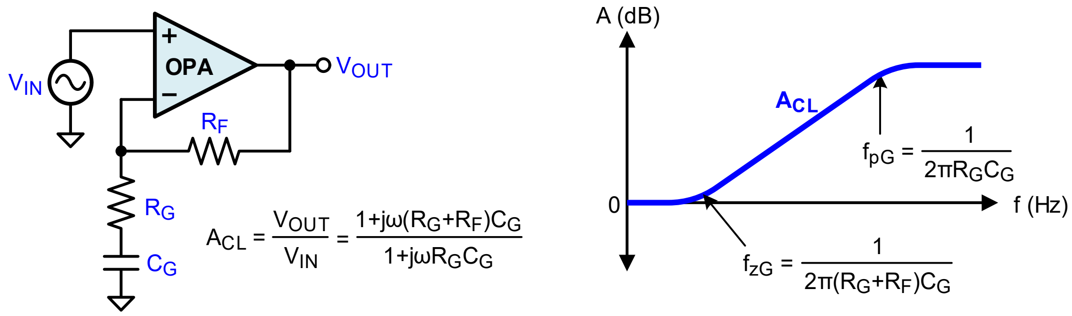

Figure 11. Transfer Function and Frequency Response of the Closed-Loop Gain of the Op-Amp, A_{CL}

Depicting all discussed frequency responses, Figure 12 shows how G_{IN} and A_{CL} define the total gain (G_T), of the AC-coupled amplifier using $G_T = G_{IN} \cdot A_{CL}$, therefore moving the new -3dB cutoff, f_{CT}, to a higher frequency.

To ensure enough supply-noise suppression at this new cut-off frequency, practical experience suggests that the corner frequency of the voltage divider should be at least $1/10^{th}$ of f_{CT}: $f_{CB} = 0.1 \cdot f_{CT}$.

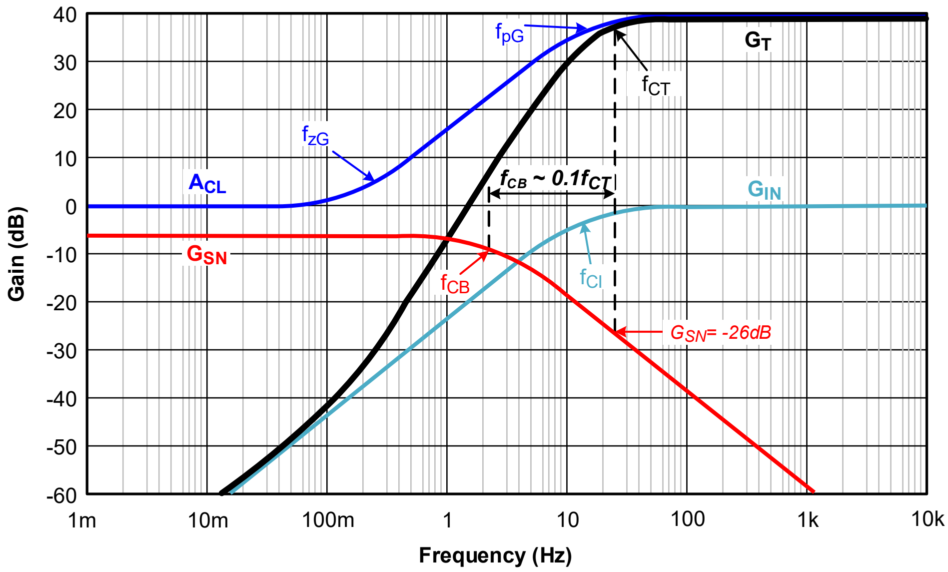

Figure 12. Frequency Responses of the Various R-C Units of the Circuit in Figure 7 on page 4

3.1 Design Example

This section discusses the practical design of an actual amplifier circuit. As previously mentioned, with regard to component selection there are always compromises to be made between power consumption, resistor noise contribution, and supply noise rejection.

The design goal is to build an AC-coupled noninverting amplifier, operating from a single 5V supply, with an overall passband gain of 100V/V (40dB) and a minimum bandwidth of f_{CT} = 16Hz.

This requires the corner frequency of the voltage divider to be $f_{CB} \leq 1/10^{th}\ f_{CT}$ = 1.6Hz. To preserve the power in the voltage divider, a DC quiescent current of 50µA is allowed. This makes the value of R_B.

(EQ. 1) $$R_B = \frac{V_S}{2I_q} = \frac{5V}{2 \cdot 50\mu A} = 50\,k\Omega$$

The buffer capacitor, C_B, can therefore be calculated with:

(EQ. 2) $$C_B = \frac{1}{2\pi f_{CB} R_B/2} = \frac{1}{2\pi \cdot 1.6Hz \cdot 25k\Omega} = 4\mu F$$

To ensure an earlier rather than later supply-noise roll-off, chose the next higher standard value with C_B = 4.7µF.

Aiming for equal corner frequencies for the input R_{IN}-C_{IN} stage and the closed-loop gain of the op-amp (A_{CL}), demands that $f_{CI} \sim f_{pG}$. These frequencies are derived from f_{CT} using:

(EQ. 3) $$f_{CI} = f_{pG} = \frac{f_{CT}}{\sqrt{1+\sqrt{2}}} = \frac{16\,Hz}{1.554} = 10.3\,Hz \approx 10\,Hz$$

To see the detailed derivation of Equation 3, see “Appendix” on page 8.

For the noninverting amplifier, a passband gain of 100V/V requires the ratio R_F/R_G = 99. Here, the compromise between the feedback path loading, noise contribution from R_F, and the capacitor size of C_G lead to resistor values of R_F = 100kΩ and R_G = 1.01kΩ.

The capacitance (C_G), required to place the A_{CL} pole at 10.3Hz can now be calculated with:

(EQ. 4) $$C_G = \frac{1}{2\pi f_{pG} R_G} = \frac{1}{2\pi \cdot 10.3\,Hz \cdot 1.01k\Omega} = 15\mu F$$

To calculate R_{IN}, the offset due to bias current flow must be considered. While I_{B-} flows through R_F only, as the DC path through R_G is blocked by C_G, I_{B+} flows through R_{IN} and the parallel circuit of the two R_B resistors. To minimize this offset, the sum of R_{IN} and $R_B/2$ must equal R_F. R_{IN} is the difference between R_F and $R_B/2$:

(EQ. 5) $$R_{IN} = R_F - R_B/2 = 100k\Omega - 25k\Omega = 75k\Omega$$

Then, the input capacitance that produces the corner frequency derived in Equation 3 on page 6 is calculated with:

(EQ. 6) $$C_{IN} = \frac{1}{2\pi f_{CI} R_{IN}} = \frac{1}{2\pi \cdot 10.3Hz \cdot 75k\Omega} = 206nF$$

Again, to make the roll-off occur slightly earlier, chose the next higher standard value with C_{IN} = 220nF.

Figure 13 shows the final amplifier circuit and its corresponding frequency responses.

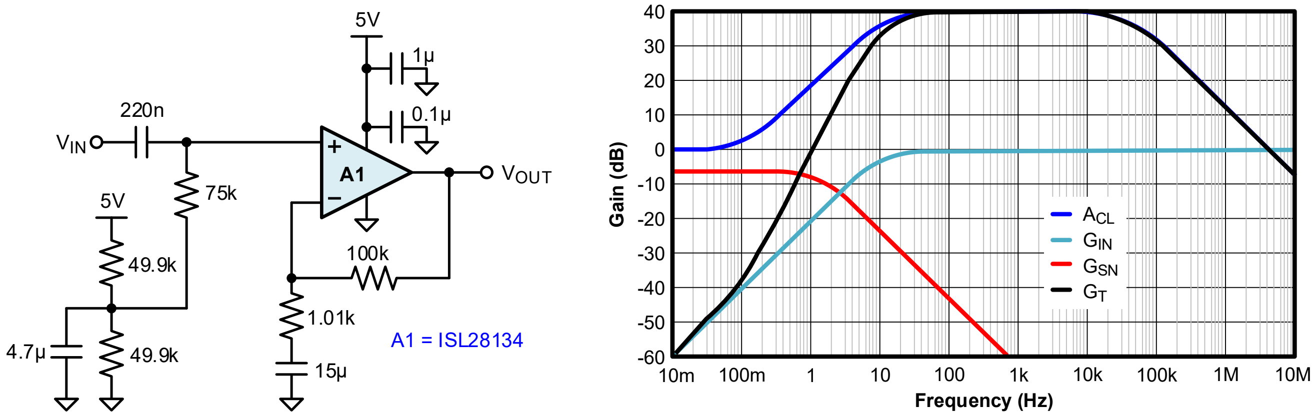

Figure 13. AC-Coupled Noninverting Amplifier with ISL28134

In the case of the inverting amplifier in Figure 14, the biasing voltage divider remains the same as in the noninverting case. The $V_S/2$ potential at the noninverting input also appears at the inverting input due to feedback action.

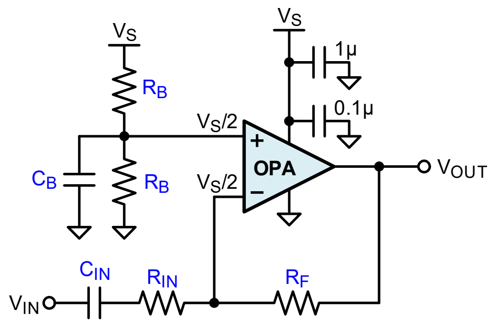

Figure 14. AC-Coupled Inverting Amplifier

Note: The gain setting resistor (R_G), also represents the input resistance (R_{IN}). With that, the closed-loop gain of the amplifier becomes the overall circuit gain. Its pole frequency is the cutoff frequency of the input stage and therefore, the minimum input bandwidth of the circuit. This simplifies the calculation of component value enormously.

The main difference is, I_B+ only flows through the parallel circuit of the two bias resistors. Therefore, reducing the offset due to bias current forces R_F to drop in value to match $R_B/2$. For high gain applications with low input bandwidth, this necessitates a much smaller R_G value, which in turn requires the increase of C_{IN}.

The simple design procedure would be to:

- Make $R_F = R_B/2$ for offset reduction,
- Then deriving the gain resistor with $R_G = R_F/G$
- And finally, calculating the input capacitor with $C_{IN} = 1/(2\pi\ f_{IN}\ R_G)$

Applying the above equations to an AC-coupled inverting amplifier with passband gain of G = 100V/V and minimum input bandwidth of f_{IN} = 16Hz, while maintaining R_B = 49.9kΩ, results in R_F = 24.9kΩ, R_G = 249Ω, and C_{IN} = 47µF.

Setting the supply-noise roll-off of the voltage divider to 1/10th of f_{IN} makes f_{CB} = 1.6Hz, which yields a capacitor value of $C_B = 1/(2\pi\ f_{CB}\ R_B/2)$ = 4µF. Again, chose the next higher standard value of 4.7µF.

Figure 15 shows the actual circuit with its corresponding frequency responses.

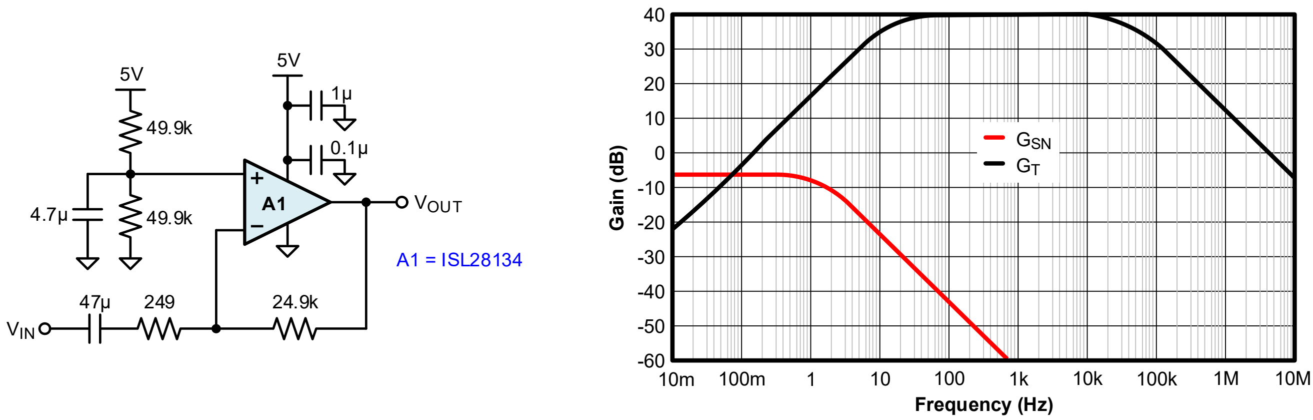

Figure 15. AC-Coupled Inverting Amplifier with ISL28134

4. Appendix

4.1 Deriving the -3dB Frequency (f_{CT}), of the Overall Circuit Gain (G_T)

Figure 16 shows the AC-signal equivalent schematic of the noninverting amplifier in Figure 8 on page 4 and its individual and overall gain responses.

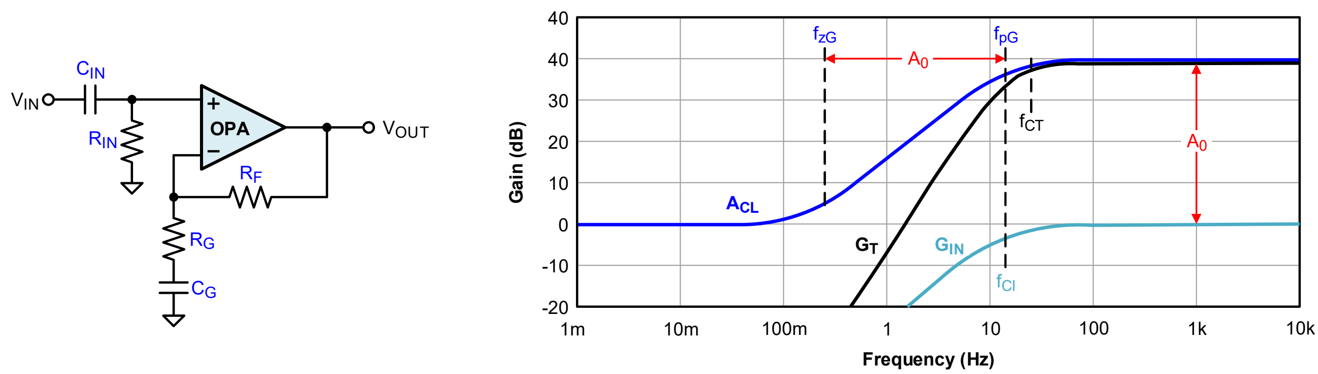

Figure 16. AC-Signal Equivalent Circuit of Figure 8 and its Frequency Responses

The gain responses for G_{IN} and A_{CL} are:

$$G_{IN} = \frac{j\omega C_{IN} R_{IN}}{1 + j\omega C_{IN} R_{IN}} \text{ with pole frequency } f_{CI} = \frac{1}{2\pi C_{IN} R_{IN}}.$$

$$A_{CL} = \frac{1 + j\omega C_G (R_G + R_F)}{1 + j\omega C_G R_G} \text{ with pole frequency } f_{pG} = \frac{1}{2\pi C_G R_G}, \text{ zero frequency } f_{zG} = \frac{1}{2\pi C_G (R_G + R_F)}, \text{ and}$$

passband gain $A_0 = \frac{R_G + R_F}{R_G}$.

Because the ratio of pole to zero frequency is: $\frac{f_{pG}}{f_{zG}} = \frac{R_G + R_F}{R_G} = A_0$, it follows that $f_{pG} = \frac{f_{zG}}{A_0}$.

Expressing the transfer functions in their generic forms gives:

$$G_{IN} = \frac{j\omega/\omega_{CI}}{1 + j\omega/\omega_{CI}} = \frac{jf/f_{CI}}{1 + jf/f_{CI}} \text{ and } A_{CL} = \frac{1 + j\omega/\omega_{zG}}{1 + j\omega/\omega_{pG}} = \frac{1 + jf/f_{zG}}{1 + jf/f_{pG}}$$

This makes the overall gain: $G_T = G_{IN} \cdot A_{CL} = \frac{jf/f_{CI}}{1 + jf/f_{CI}} \cdot \frac{1 + jf/f_{zG}}{1 + jf/f_{pG}}$

And its magnitude function: $|G_T| = \sqrt{\frac{(f/f_{CI})^2}{1 + (f/f_{CI})^2} \cdot \frac{1 + (f/f_{zG})^2}{1 + (f/f_{pG})^2}}$

By making $f_{CI} = f_{pG}$ and replacing f_{zG} with f_{pG}/A_0 the magnitude function becomes:

$$|G_T| = \sqrt{\frac{(f/f_{pG})^2}{1 + (f/f_{pG})^2} \cdot \frac{1 + (f \cdot A_0/f_{pG})^2}{1 + (f/f_{pG})^2}} \,.$$

To find f_{CT}, |GT| is set $A_0/\sqrt{2}$ (the -3dB magnitude of A_0) and the generic frequency, f, is replaced with f_{CT}:

$$\frac{A_0}{\sqrt{2}} = \sqrt{\frac{\left(\frac{f_{CT}}{f_{pG}}\right)^2 \cdot \left[1 + \left(\frac{f_{CT} \cdot A_0}{f_{pG}}\right)^2\right]}{\left[1 + \left(\frac{f_{CT}}{f_{pG}}\right)^2\right] \cdot \left[1 + \left(\frac{f_{CT}}{f_{pG}}\right)^2\right]}} \quad \Rightarrow \quad \frac{A_0^2}{2} = \frac{\frac{f_{CT}^2}{f_{pG}^2} \cdot \left(1 + \frac{f_{CT}^2 A_0^2}{f_{pG}^2}\right)}{1 + 2\frac{f_{CT}^2}{f_{pG}^2} + \frac{f_{CT}^4}{f_{pG}^4}}$$

Then, solving for f_{CT} results in:

$f_{CT} = f_{pG}\sqrt{1 - 1/A_0^2 + \sqrt{1 + \left(1 - 1/A_0^2\right)^2}}$ Therefore, for $A_0 > 10$, $f_{CT} = f_{pG} \cdot \sqrt{1 + \sqrt{2}} = 1.55 f_{pG}$.

Using 1.55 for $A_0 \geq 2$V/V, yields less than 9% deviation from the theoretical f_{CT} value.

Plotting the factor of f_{pG} over A_0, one might simply use an average factor of 1.5.

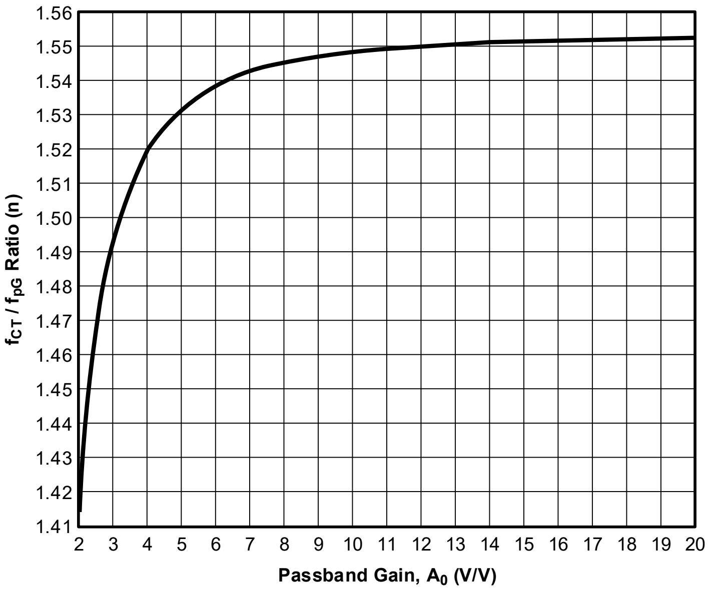

Figure 17. F_{CT}/F_{pG} Ratio vs Passband Gain

5. Revision History

Rev.	Date	Description
0.00	Dec.13.19	Initial release

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