

R-IN32M4 series

R18AN0044EJ0102

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R-IN32M4-CL3 Driver/Middleware Release Note

Summary

Thank you for using Driver/Middleware Set for R-IN32M4-CL3 evaluation board.

This document describes the package contents and operating environment of this product.

Please be sure to read before use.

For details on how to use each sample software, middleware etc, please refer to the related documents below.

Related documents

R18UZ0043EJ****	R-IN32M4 Series Startup Manual CC-Link IE Field
R18UZ0072EJ****	R-IN32M4-CL3 Programming Manual (OS edition)
R18UZ0076EJ****	R-IN32M4-CL3 Programming Manual (Driver edition)
R18UZ0071EJ****	R-IN32M4-CL3 User's Manual CC-Link IE Field
R18UZ0073EJ****	R-IN32M4-CL3 User's Manual Hardware
R18UZ0075EJ****	R-IN32M4-CL3 User's Manual Gigabit Ether PHY
R18UZ0074EJ****	R-IN32M4-CL3 User's Manual Board Design

Last four digits of document number (described as ****) indicate version information of each document.

Please download the latest document from our web site and refer to it.

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1. Introduction

Driver/Middleware Set for R-IN32M4-CL3 evaluation board is a software package that collects various sample applications, libraries, middleware, peripheral function drivers that can be used for developing applications using R-IN32M4-CL3.

2. Package contents

This package is including the below.

- Sample application

No.	Sample application name
1	CAN sample
2	CC-Link IE Field (intelligent device)
3	CC-Link IE Field (remote device)
4	Interval timer sample
5	OS sample
6	OS-less sample
7	TCP/IP BSD Socket API sample
8	TCP/IP MAC Control sample
9	TCP/IP nonblock API sample
10	TCP/IP Network App sample
11	TCP/IP SNMP sample
12	Version get sample

- Library

No.	Library name
1	HW-RTOS library
2	EtherPHY library
3	TCP/IP stack library

- Middleware

No.	Middleware name
1	Parallel flash ROM control
2	Serial flash ROM control
3	TCP/IP stack control

- Peripheral function driver

No.	Driver name
1	CAN
2	CSI
3	DMAC
4	Ether Switch
5	IIC
6	Serial Flash MEMC
7	TAUD (16bit timer TAUD)
8	Timer (32bit timer TAUJ2)
9	UART
10	WDT

3. Folder structure

Folder structure of this package is shown below.

```

TOP
|
+-- CMSIS << Cortex Microcontroller Software Interface Standard >>
|   +-- include
|
+-- Device << Device dependent files >>
    +-- Renesas
        +-- RIN32M4 << R-IN32M4 dependent files >>
            +-- Include << Include directory >>
            +-- Library << Library directory >>
            +-- Source << Source directory >>
                |
                +-- Driver      << Driver directory >>
                +-- Middleware << Middleware directory >>
                +-- Project     << Project directory >>
                    | |
                    | +-- TS-R-IN32M4-CL3
                    |   +-- can_sample
                    |   +-- cie_intelligent_device
                    |   +-- cie_remote_device
                    |   +-- interval_timer
                    |   +-- os_sample
                    |   +-- osless_sample
                    |   +-- uNet3_bsd
                    |   +-- uNet3_mac
                    |   +-- uNet3_nonblock
                    |   +-- uNet3_sample
                    |   +-- uNet3_snmp
                    |   +-- version_get_sample
                    |
                +-- Templates << Startup file and others >>
                    +-- IAR      << IAR compiler dependent files >>

```

4. Operating environment

The operating environment of this package is shown below.

- Target device
R-IN32M4-CL3

- Target board
SBEV-RIN32M4CL3 (Shimafuji Electric Incorporated.)
TS-TCS07908 (Tessera Technology Inc.)

- Development environment
 - Compiler
IAR Embedded Workbench for Arm 8.42.1(IAR Systems)
 - Debugger
IAR Embedded Workbench for Arm 8.42.1 (IAR Systems)
 - ICE
I-jet / I-jet Trace for Arm Cortex-M (IAR Systems)

5. Change history

Version	Changes
V1.0.0 (Nov 11, 2019)	First release
V1.0.1 (Apr 30, 2020)	- Update of sample application
V1.0.2 (Nov 10, 2020)	- Support for new evaluation board : SBEV-RIN32M4CL3

6. Website and Support

Renesas Electronics Website

<http://www.renesas.com/>

Inquiries

<http://www.renesas.com/contact/>

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

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