Introduction

This document summarizes how to set a given R-Car device when using the reduced gigabit media independent interface (RGMII) for connection with an external PHY device or switch and points to note when doing this to realize Ethernet functionality for R-Car H3, R-Car M3-W, and R-Car M3-N products in board design or driver development. The document is intended to help users to resolve unclear points and realize the appropriate connections and settings of the device in designing or developing their own boards or drivers.

The document consists of the following three major sections.

1. Specifications of the RGMII in outline
2. Specifications of the RGMII of R-Car H3, R-Car M3-W, and R-Car M3-N devices in outline
3. Notes on connecting external PHY devices and switches

Target Device

- R-Car H3
- R-Car M3-W
- R-Car M3-N
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1. Specifications of the RGMII in Outline

The reduced gigabit media independent interface (RGMII) is a specification for use in connection between the MAC and PHY layers of an Ethernet communications interface. The RGMII is intended to reduce the number of signals required for Ethernet communications at 10, 100, or 1000 Mbps compared to the earlier media independent interface (MII) described in the IEEE802.3u standard and gigabit media independent interface (GMII) described in the IEEE802.3z standard.

People generally refer to version 1.3 (released in December, 2000) or version 2.0 (released in April, 2002) of the RGMII specification. The latest specification is version 2.0. Note that version 2.0 is the result of major changes relative to version 1.3 in terms of two approaches: a) changes to the IO specification and b) extension of the timing specification. The following summarizes the differences between versions 1.3 and 2.0.

a) Change to the IO specification
   - Version 1.3: 2.5-V CMOS interface voltages (defined by JEDEC EIA/JESD8-5) are used with all IO pins.
   - Version 2.0: 1.5-V HSTL interface voltages (defined by JEDEC EIA/JESD8-6) are used with all IO pins.

b) Change to the timing specification
   - Version 1.3: A single timing specification is stipulated. This specification states a delay on the board, and is referred to as original RGMII in version 2.0.
   - Version 2.0: Two timing specifications are stipulated. The RGMII-ID specification newly added to version 2.0 states a delay inside the device.

1.1 Signal Line Specification in the RGMII

The RGMII uses fourteen signals to connect the MAC and PHY layers. With an RGMII, the contents of the data and control signals for transmission and reception change on both edges of the respective clock signals. This allows reduction of the number of signals compared to the GMII standard without changing the clock speed (125 MHz).

<table>
<thead>
<tr>
<th>Signal</th>
<th>Source</th>
<th>Sink</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXC</td>
<td>MAC</td>
<td>PHY</td>
<td>Reference clock for use in transmission. It runs at 125, 25, or 2.5 MHz, depending on the link speed.</td>
</tr>
<tr>
<td>TD[3:0]</td>
<td>MAC</td>
<td>PHY</td>
<td>Data being transmitted. The meanings of the signals differ with the edge of the TXC signal. Specifically, they contain bits 3:0 on ↑ of TXC and bits 7:4 on ↓ of TXC.</td>
</tr>
<tr>
<td>TX_CTL</td>
<td>MAC</td>
<td>PHY</td>
<td>Control signal for transmission. The meaning of the signal differs with the edge of the TXC signal. Specifically, it represents TXEN on ↑ of TXC and TXERR on ↓ of TXC.</td>
</tr>
<tr>
<td>RXC</td>
<td>PHY</td>
<td>MAC</td>
<td>Reference clock for use in reception. It runs at 125, 25, or 2.5 MHz, depending on the link speed.</td>
</tr>
<tr>
<td>RD[3:0]</td>
<td>PHY</td>
<td>MAC</td>
<td>Data being received. The meanings of the signals differ with the edge of the RXC signal. Specifically, they contain bits 3:0 on ↑ of RXC and bits 7:4 on ↓ of RXC.</td>
</tr>
<tr>
<td>RX_CTL</td>
<td>PHY</td>
<td>MAC</td>
<td>Control signal for reception. The meaning of the signal differs with the edge of the RXC signal. Specifically, it represents RXDV on ↑ of RXC and RXERR on ↓ of RXC.</td>
</tr>
<tr>
<td>MDIO</td>
<td>MAC or PHY</td>
<td>MAC or PHY</td>
<td>IO signal for control over the PHY layer. The specification is the same as that for an MII.</td>
</tr>
<tr>
<td>MDC</td>
<td>MAC</td>
<td>PHY</td>
<td>Clock signal for control over the PHY layer. The specification is the same as that for an MII.</td>
</tr>
</tbody>
</table>

Sources: References 1 and 2 in section 4
**Figure 1-1** System Diagram when an RGMII is in Use

Sources: References 1 and 2 in section 4
1.2 Timing Specification: Original RGMII Timing

The RGMII specification defines two types of timing specification, referred to as original RGMII and RGMII-ID timing. RGMII-ID timing was newly added in version 2.0. Original RGMII is the previous timing specification.

Original RGMII

Clock signals must be delayed by from 1.5 ns to 2.0 ns relative to the data signals. These delays are assumed to be a product of board design.

RGMII-ID

Clock signals must be delayed by at least 1.2 ns relative to the data signals. These delays are assumed to be a product of the internal design of devices that output the signals.
1.2.1 Timing Specification: Original RGMII Timing

“Original RGMII timing specification” refers to that used in v1.3 and earlier versions.

Though a transmitter changes data and clock signals at the same time, the transmitted signals must satisfy the conditions $T_{skewT}$ and $T_{skewR}$ at a receiver as shown in the table and figure below. This indicates that 1.5- to 2.0-ns delays need to be produced in board design.

Table 1-2 Timing Specification for Original RGMII Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{skewT}$</td>
<td>Data to Clock output Skew (at Transmitter)</td>
<td>-500</td>
<td>0</td>
<td>500</td>
<td>ps</td>
</tr>
<tr>
<td>$T_{skewR}$</td>
<td>Data to Clock input Skew (at Receiver)</td>
<td>1</td>
<td>1.8</td>
<td>2.6</td>
<td>ns</td>
</tr>
<tr>
<td>$T_{cyc}$</td>
<td>Clock Cycle Duration</td>
<td>7.2</td>
<td>8</td>
<td>8.8</td>
<td>ns</td>
</tr>
<tr>
<td>Duty_G</td>
<td>Duty Cycle for Gigabit</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>Duty_T</td>
<td>Duty Cycle for 10/100T</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>$T_{r/f}$</td>
<td>Rise/Fall Time (20-80%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Sources: References 1 and 2 in section 4

Figure 1-2 Timing Diagram for Signals when Original RGMII is in Use

Figure 2 (Multiplexing & Timing Diagram - Original RGMII)

Sources: References 1 and 2 in section 4
1.2.2 Timing Specification: RGMII-ID Timing (Where the Required Delays are Internal)

The RGMII-ID timing specification was added in version 2.0.

With RGMII-ID timing, the delays are produced within the device, whereas with original RGMII timing this is done in board design. A transmitter adds delays to the signals to satisfy the conditions $T_{\text{setupT}}$ and $T_{\text{holdT}}$.

### Table 1-3 Timing Specification for RGMII-ID Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{\text{setupT}}$</td>
<td>Data to Clock output Setup (at Transmitter-integrated delay)</td>
<td>1.2</td>
<td>2.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{\text{holdT}}$</td>
<td>Data to Clock output Hold (at Transmitter-integrated delay)</td>
<td>1.2</td>
<td>2.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{\text{setupR}}$</td>
<td>Data to Clock input Setup (at Receiver-integrated delay)</td>
<td>1.0</td>
<td>2.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{\text{holdR}}$</td>
<td>Data to Clock input Hold (at Receiver-integrated delay)</td>
<td>1.0</td>
<td>2.0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{\text{cyc}}$</td>
<td>Clock Cycle Duration</td>
<td>7.2</td>
<td>8</td>
<td>8.8</td>
<td>ns</td>
</tr>
<tr>
<td>$\text{Duty}_G$</td>
<td>Duty Cycle for Gigabit</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>$\text{Duty}_T$</td>
<td>Duty Cycle for 10/100T</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>$Tr/Tf$</td>
<td>Rise/Fall Time (20-80%)</td>
<td></td>
<td></td>
<td>0.75</td>
<td>ns</td>
</tr>
</tbody>
</table>

Sources: References 1 and 2 in section 4
Guide to Using RGMII in Making an EthernetAVB-IF Connection

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FIGURE 3 (Multiplexing & Timing Diagram - RGMII-ID)

Sources: References 1 and 2 in section 4

Figure 1-3  Timing Diagram for Signals when RGMII-ID is in Use
1.3 I/O Specification in the RGMII Specification

A definition in the I/O specification of the RGMII specification was changed in updating of the version from 1.3 to 2.0.

In version 1.3, all signals including MDIO and MDC are defined as operating with 2.5-V CMOS interface voltages. In version 2.0, on the other hand, they are defined as operating with 1.5-V HSTL interface voltages.

Table 1-4 Interface Specifications

<table>
<thead>
<tr>
<th>RGMII Version</th>
<th>Interface</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.3</td>
<td>2.5-V CMOS</td>
<td>JEDEC EIA/JESD8-5</td>
</tr>
<tr>
<td>2.0</td>
<td>1.5-V HSTL</td>
<td>JEDEC EIA/JESD8-6</td>
</tr>
</tbody>
</table>
2. Specifications for the RGMII in R-Car Series Devices

2.1 Specifications for the RGMII in R-Car Series Devices

This subsection describes the specifications of the RGMII for use with the EthernetAVB-IF module in R-Car H3, R-Car M3-W, and R-Car M3-N devices.

The correspondence between pins of R-Car devices and RGMII signals is given in table 2-1. All R-Car signals except for the AVB_TXCREFCLK have the same meanings as the respective RGMII signals.

The AVB_TXCREFCLK is the transmission reference clock and is used as the transmission clock in the EthernetAVB-IF module. It’s also used for output of the internal TXC signal of the EthernetAVB-IF module. The clock cycle is 125 MHz ± 50 ppm.

<table>
<thead>
<tr>
<th>RGMII Signal</th>
<th>R-Car Signal</th>
<th>Input/Output</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXC</td>
<td>AVB_TXC</td>
<td>Output</td>
<td>2.5 V</td>
</tr>
<tr>
<td>TD[3:0]</td>
<td>AVB_TD[3:0]</td>
<td>Output</td>
<td>2.5 V</td>
</tr>
<tr>
<td>TX_CTL</td>
<td>AVB_TX_CTL</td>
<td>Output</td>
<td>2.5 V</td>
</tr>
<tr>
<td>RXC</td>
<td>AVB_RXC</td>
<td>Input</td>
<td>2.5 V</td>
</tr>
<tr>
<td>RD[3:0]</td>
<td>AVB_RD[3:0]</td>
<td>Input</td>
<td>2.5 V</td>
</tr>
<tr>
<td>RX_CTL</td>
<td>AVB_RX_CTL</td>
<td>Input</td>
<td>2.5 V</td>
</tr>
<tr>
<td>MDIO</td>
<td>AVB_MDIO</td>
<td>Output</td>
<td>3.3 V</td>
</tr>
<tr>
<td>MDC</td>
<td>AVB_MDC</td>
<td>Input/Output</td>
<td>3.3 V</td>
</tr>
<tr>
<td>—</td>
<td>AVB_TXCREFCLK</td>
<td>Input</td>
<td>3.3 V</td>
</tr>
</tbody>
</table>
2.2 Timing Specifications

The timing specification of R-Car devices can be changed by the settings of bits 14 (TDM) and 13 (RDM) in the AVB-DMAC product specific register (APSR, at H’E680008C) of the EthernetAVB-IF module. The values of these bits after a reset are 0, which is the setting for original RGMII timing. Setting either of the bits to 1 causes delaying of TXC or RXC inside the R-Car device.

**APSR.TDM** (bit 14): Tx clock internal delay mode

0: Normal mode
1: Delayed mode: A 2.0-ns (typ.) delay is imposed on TXC.

**APSR.RDM** (bit 13): Rx clock internal delay mode

0: Normal mode
1: Delayed mode: A 1.8-ns (typ.) delay is imposed on RXC.
2.2.1 Timing Specification: RGMII Normal Mode

The normal mode corresponds to original RGMII timing in the RGMII specification. This timing specification is selected by setting APSR.TDM and APSR.RDM to 0.

Table 2-2 Control over the Timing of Ethernet Transfer with an R-Car Device (in RGMII 1-Gbps Mode)

| Table 87.15.2 Ethernet Control Timing (RGMII 1Gbps Mode) |
| Conditions: |
| VDDQ33 = 3.3V ±0.2V, VDDQ25_ETH = 2.5 ± 0.1V [R-Car H3/M3-W] |
| Tc = -40 to +115°C [R-Car H3/M3-W] |
| GND = VSS = 0V, CL = 30pF |

Recommend: Connection of series 25Ω as damping resistor to RGMII output buffer. [R-Car H3/M3-W]

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Figures</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVB_TXCREFCLK cycle time</td>
<td>—</td>
<td>—</td>
<td>125-50ppm</td>
<td>—</td>
<td>125+50ppm MHz</td>
<td>—</td>
</tr>
<tr>
<td>AVB_TXC cycle time</td>
<td>Tcyc</td>
<td>7.2</td>
<td>8</td>
<td>8.8</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>AVB_TXC duty cycle</td>
<td>Duty_G</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
<td>—</td>
</tr>
<tr>
<td>AVB_TX_CTL to clock output skew</td>
<td>TskewT</td>
<td>-500</td>
<td>0</td>
<td>500</td>
<td>ps</td>
<td>Figure 87.15.3</td>
</tr>
<tr>
<td>AVB_TD[3:0] to clock output skew</td>
<td>TskewT</td>
<td>-500</td>
<td>0</td>
<td>500</td>
<td>ps</td>
<td>Figure 87.15.3</td>
</tr>
<tr>
<td>AVB_RXC cycle time</td>
<td>Tcyc</td>
<td>7.2</td>
<td>8</td>
<td>8.8</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>AVB_RXC duty cycle</td>
<td>Duty_G</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
<td>—</td>
</tr>
<tr>
<td>AVB_RX_CTL to clock input skew</td>
<td>TskewR</td>
<td>1</td>
<td>1.8</td>
<td>2.6</td>
<td>ns</td>
<td>Figure 87.15.4</td>
</tr>
<tr>
<td>AVB_RD[3:0] to clock input skew</td>
<td>TskewR</td>
<td>1</td>
<td>1.8</td>
<td>2.6</td>
<td>ns</td>
<td>Figure 87.15.4</td>
</tr>
</tbody>
</table>

Source: Reference 4 in section 4

Figure 87.15.3 RGMII 1Gbps Mode Transmission Timing

Source: Reference 4 in section 4

Figure 2-1 Timing in Transmission by an R-Car Device (in RGMII 1-Gbps Mode)
Guide to Using RGMII in Making an EthernetAVB-IF Connection

Figure 87.15.4 RGMII 1Gbps Mode Reception Timing
Source: Reference 4 in section 4

Figure 2-2 Timing in Reception by an R-Car Device (in RGMII 1-Gbps Mode)
2.2.2 Timing Specification: RGMII Internal Delay on TXC

This timing specification is selected by setting APSR.TDM to 1.

This mode enables delaying of the AVB_TXC signal within the given R-Car device, with the delay being 2.0 ns (typ.).

### Table 2-3 Control over Timing of Ethernet Transfer by an R-Car Device (in RGMII Tx Clock Internal Delay Mode)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Figures</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVB_TXCREFCLK cycle time</td>
<td>—</td>
<td>125-50ppm</td>
<td>—</td>
<td>125+50ppm</td>
<td>MHz</td>
<td>—</td>
</tr>
<tr>
<td>AVB_TXC cycle time*</td>
<td>Tcyc</td>
<td>7.2</td>
<td>8</td>
<td>8.8</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>AVB_TXC duty cycle (in 1Gbps)</td>
<td>Duty_G</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>AVB_TXC duty cycle (in 100Mbps)</td>
<td>Duty_T</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>AVB_TX_CTL setup time</td>
<td>TsetupT</td>
<td>1.2</td>
<td>2.0</td>
<td>—</td>
<td>ns</td>
<td>Figure 87.15.5</td>
</tr>
<tr>
<td>AVB_TX_CTL hold time</td>
<td>TholdT</td>
<td>1.2</td>
<td>2.0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>AVB_TD[3:0] setup time</td>
<td>TsetupT</td>
<td>1.2</td>
<td>2.0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>AVB_TD[3:0] hold time</td>
<td>TholdT</td>
<td>1.2</td>
<td>2.0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Note* For 100Mbps, Tcyc will scale to 40ns+4ns respectively.

Source: Reference 4 in section 4
2.2.3 Timing Specification: RGMII Internal Delay on RXC

This timing specification is selected by setting APSR.RDM to 1.

This mode enables delaying of the AVB_RXC signal within the given R-Car device, with the delay being 1.8 ns (typ.).

Table 2-4 Control over Timing of Ethernet Transfer by an R-Car Device (in RGMII Rx Clock Internal Delay Mode)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Figures</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVB_RXC cycle time*</td>
<td>Tcyc</td>
<td>7.2</td>
<td>8</td>
<td>8.8</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>AVB_RXC duty cycle (in 1Gbps)</td>
<td>Duty_G</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>AVB_RXC duty cycle (in 100Mbps)</td>
<td>Duty_T</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>AVB_RX_CTL to clock input skew</td>
<td>TskewR</td>
<td>-500</td>
<td>0</td>
<td>500</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>AVB_RD[3:0] to clock input skew</td>
<td>TskewR</td>
<td>-500</td>
<td>0</td>
<td>500</td>
<td>ps</td>
<td>Figure 87.15.6</td>
</tr>
</tbody>
</table>

Note* For 100Mbps, Tcyc will scale to 40ns+-4ns respectively.
Source: Reference 4 in section 4

Figure 87.15.6 RGMII Delay Mode Reception Timing
Source: Reference 4 in section 4

Figure 2-4 Timing in Reception by an R-Car Device (in RGMII Delay Mode)
3. Notes on Connection with External Devices

3.1 External Devices
We assume that two types of device, PHY devices and switches, may be externally connected to the RGMII of an R-Car device. Note that the RGMII connections to both types of device are handled in the same way.

- PHY device
  This type of device is used for systems with a single port directly connected to an Ethernet cable.

![Diagram of a System with an R-Car Connected to a PHY Device](image)

- Switch
  Switches are used for systems with multiple ports connected to multiple Ethernet cables.

![Diagram of a System with an R-Car Connected to a Switch](image)
The following summarizes the points to confirm in connecting an R-Car device with an external device.

- The external device needs to support the RGMII. If this is not so, direct connection is impossible. You will need to prepare a bridge circuit.
- The I/O specification of the external device will ideally support operation at 2.5 V. If it does not, solve the problem by using a level shifter.
- When the external device employs original RGMII timing (the device does not have an internal delay function):
  Set APSR.TDM and APSR.RDM to 1 so the delay is produced within the R-Car device.
- When the external device employs RGMII-ID timing (the device has an internal delay function):
  A device that supports RGMII-ID timing can generally make changes to timing, such as enabling or disabling delays and handling fine adjustment of the delay settings. Select the appropriate combination of settings.

The timing specification is on the assumption that the requirements for board design include the conditions below.

- The wiring lengths for RXC, RD[3:0], and RX_CTL must be the same. In this case, the delay time to be added for RXC must not be less than the values for the other signals (namely, the wiring length for RXC must not be shorter than the lengths for the other signals).
- The wiring lengths for TXC, TD[3:0], and TX_CTL must be the same. In this case, the delay time to be added for TXC must not be less than the values for the other signals (namely, the wiring length for TXC must not be shorter than the lengths for the other signals).

Additionally, whether the external device has a delay function or not affects the settings for delay in the R-Car device.

### Table 3-1  Settings for the Delay of the R-Car Device

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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Values for the R-Car device</td>
<td>APSR.TDM</td>
<td>0 or 1</td>
<td>0 or 1</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>APSR.RDM</td>
<td>0 or 1</td>
<td>1</td>
<td>0 or 1</td>
<td>1</td>
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</tr>
</tbody>
</table>
3.1.1 External Devices Unable to Delay RXC or TXC

The description here is for the case where the external device does not have the ability to delay RXC or TXC. In such cases, the delay function of an R-Car device is used for timing control. After the application of the delay, confirm that this satisfies the specifications of both devices.

- Set APSR.TDM to 1. This delays TXC by 2.0 ns (typ.).
- Set APSR.RDM to 1. This delays RXC by 1.8 ns (typ.).
3.1.2 External Devices Able to Delay RXC

The description here is for cases where the external device is able to delay RXC. In such cases, either the R-Car or the external device applies the delay to RXC. As long as the specifications are satisfied, which device you use to apply the delay to RXC does not matter. After the application of the delay, confirm that this satisfies the specifications of both devices.

- When using the delay function of the external device:
  - Set APSR.RDM to 0 and use the delay function of the external device to apply the delay.
- When not using the delay function of the external device:
  - Set APSR.RDM to 1 to select use of the delay function of the R-Car device to delay RXC by 1.8 ns (typ.).
3.1.3 External Devices Able to Delay TXC

The description here is for cases where the external device is able to delay TXC. In such cases, either the R-Car or the external device applies the delay to TXC. As long as the specifications are satisfied, which device you use to apply the delay to TXC does not matter. After the application of the delay, confirm that this satisfies the specifications of both devices.

- When using the delay function of the external device:
  Set APSR.TDM to 0 and use the delay function of the external device to apply the delay.

- When not using the delay function of the external device:
  Set APSR.TDM to 1 to select use of the delay function of the R-Car device to delay TXC by 2.0 ns (typ.).
4. References

1. Reduced Gigabit Media Independent Interface (RGMII) Version 1.3, 12/10/2000
2. Reduced Gigabit Media Independent Interface (RGMII) Version 2.0, 4/1/2002
4. R-Car Series, 3rd Generation Electrical Characteristics Rev. 0.54, May. 2017
5. Electrical Characteristics Manual Errata for R-Car Gen3 Rev.0.54 on July 05, 2017
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>May, 2017</td>
<td>— First edition issued.</td>
</tr>
<tr>
<td>1.01</td>
<td>July, 2017</td>
<td>Updated references #3,#4 and #5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Modified Figure 2-1, Figure 2-2, Figure 2-3, Figure 2-4, Table 2-2, Table 2-3 and Table 2-4</td>
</tr>
</tbody>
</table>
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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