LVCMOS Terminations

Figure 1. LVCMOS Series Termination

![Diagram of LVCMOS Series Termination](image)

Ro+Rs = Zo = 50 Ohm

Figure 2. LVCMOS to 2.5V LVCMOS

![Diagram of LVCMOS to 2.5V LVCMOS](image)

Ro+Rs ~17 Ohm

Figure 3. LVCMOS to 1.8V

![Diagram of LVCMOS to 1.8V](image)

Ro+Rs = 43 Ohm
**Figure 4. LVCMOS Signal to Differential Input**

Ro + Rs = Zo

**Figure 5. LVCMOS Overdrive XTAL Input**

Ro+Rs ~50 Ohm

Increase Rs to reduce the amplitude

**Figure 6. LVCMOS to 1.0V LVCMOS**

Ro+Rs =75 Ohm

The Rs may need to be slightly adjusted to obtain proper logic high level at the receiver.
Figure 7. LVCMOS to 1.25V LVCMOS

The Rs may need to be slightly adjusted to obtain proper logic high level at the receiver.

Figure 8. LVCMOS to 3.3V LVCMOS, Series Termination

Figure 9. LVCMOS to 3.3V LVCMOS, Parallel Termination
Figure 10. LVCMOS to Differential Input with built-in Termination and DC Bias

Figure 11. Alternative LVCMOS to Differential Input with Built-in Termination and DC Bias

Increase Rs if amplitude reduction is necessary.

Figure 12. LVCMOS to 1V BCM56700
Figure 13. LVCMOS Tie N Outputs Together to Drive M Receivers

Figure 14. 3.3V LVPECL Standard Termination

Rs = Zo - (Ro x M)/(N)

LVPECL Terminations
Figure 15. 3.3V LVPECL Equivalent Termination

![Diagram of 3.3V LVPECL Equivalent Termination]

Figure 16. 3.3V LVPECL Equivalent Termination

![Diagram of 3.3V LVPECL Equivalent Termination]

Figure 17. 3.3V LVPECL Offset to VCC - 2V

![Diagram of 3.3V LVPECL Offset to VCC - 2V]
Figure 18. 3.3V LVPECL Offset to VCC - 1.3V

Figure 19. 3.3V LVPECL Driver to 1.5V SSTL

Figure 20. 3.3V LVPECL Driver to 1.8V SSTL
Figure 21. 3.3V LVPECL Driver to 1.8V SSTL, Thevenin Termination

Figure 22. 3.3V LVPECL Termination Amplitude Reduction

Larger R3/R4 resistance further reduces the amplitude.

Figure 23. 3.3V LVPECL to 2.5 Differential Input with High DC Offset Requirement
Figure 24. 3.3V LVPECL to LVDS, Option 1

Figure 25. 3.3V LVPECL to LVDS, Option 2
Figure 26. LVPECL to HSTL, Receiver VCC=1.5V and V_REF=0.75V, Option 1

Use this option if there is 0.75V rail available.

Figure 27. LVPECL to HSTL, Receiver VCC=1.5V and V_REF=0.75V, Option 2
Figure 28. LVPECL to HSTL, Receiver VCC=3.3V

Figure 29. LVPECL to HCSL (DCM)

Figure 30. 3.3V LVPECL to Broadcom BCM5785
Figure 31. LVPECL to Differential 100ohm DC, 10K Bias

Figure 32. LVPECL to 2.5 LVCMOS

Figure 33. 3.3V LVPECL to 2.5V Different Input with LVDS DC Offset Level Requirement
Figure 34. 3.3V LVPECL to PCML, Option 1

![3.3V LVPECL to PCML, Option 1 Diagram]

Figure 35. 3.3V LVPECL to PCML, Option 2

![3.3V LVPECL to PCML, Option 2 Diagram]

Figure 36. 3.3V LVPECL Driving Receiver with Built-in Termination and Built-in Self Bias

![3.3V LVPECL Driving Receiver Diagram]
Figure 37. 3.3V LVPECL to HCSL

![Diagram of 3.3V LVPECL to HCSL interface.]

Figure 38. 3.3V LVPECL to 1.8V LVCMOS Interface

![Diagram of 3.3V LVPECL to 1.8V LVCMOS interface.]

Figure 39. 3.3V LVPECL to 1.8V Differential Interface, Option 1

![Diagram of 3.3V LVPECL to 1.8V Differential interface, Option 1.]
Figure 40. 3.3V LVPECL to 1.8V Differential Interface, Option 2

Figure 41. 3.3V LVPECL to 0.65V DC Offset

Figure 42. 3.3V LVPECL to CML
Figure 43. 3.3V LVPECL to 2.5V SSTL 2 Interface with VDD/2 Voltage Source

Figure 44. 3.3V LVPECL to 2.5V SSTL 2 Interface without VDD/2 Voltage Source
Figure 45. 2.5V LVPECL Standard Termination

![Diagram of 2.5V LVPECL Standard Termination]

VCCO = 2.5V

Figure 46. 2.5V LVPECL Equivalent Termination

![Diagram of 2.5V LVPECL Equivalent Termination]
Figure 47. 2.5V LVPECL Equivalent Termination

![Diagram of 2.5V LVPECL Equivalent Termination]

Figure 48. 2.5V LVPECL Termination, No Receiver

![Diagram of 2.5V LVPECL Termination, No Receiver]
Figure 49. 2.5V LVPECL to Differential Input (CLK/nCLK) Interface, Option 1

Figure 50. 2.5V LVPECL to Differential Input (CLK/nCLK) Interface, Option 2

Figure 51. 2.5V LVPECL to Differential Input (CLK/nCLK) Interface, Option 3
Figure 52. 2.5V LVPECL to 0.8V DC offset Receiver

Figure 53. LVPECL, AC-Coupled to Receiver with no DC Offset Requirement

Figure 54. LVPECL to XTAL
Figure 55. LVPECL Short Trace Termination

Figure 56. LVPECL to Single-Ended LVPECL, Option 1

Figure 57. LVPECL to Single-Ended LVPECL, Option 2
Figure 58. LVPECL to Single-Ended LVPECL with VBB Bias, Option 1

Re-biasing positive side of input to Vcc - 1.3V to match VBB

Figure 59. LVPECL to Single-Ended LVPECL with VBB Bias, Option 2

Figure 60. LVPECL to Single-Ended LVPECL with VBB Bias, Option 3
Re-biasing both sides of the input using VBB.

Figure 62. LVPECL to HCSL (DCM)
Figure 63. LVPECL Drives Two Receivers

Figure 64. 3.3V LVPECL to AMD8132
Figure 65. 2.5V LVPEC to AMD8132

![Diagram of 2.5V LVPEC to AMD8132]

Figure 66. 3.3V LVPECL to AMD K8 CPU CLK Input

![Diagram of 3.3V LVPECL to AMD K8 CPU CLK Input]

Figure 67. 2.5V LVPECL to AMD K8 CPU CLK Input

![Diagram of 2.5V LVPECL to AMD K8 CPU CLK Input]
LVDS Terminations

Figure 68. LVDS Termination

Figure 69. LVDS AC-Coupling, Option 1
Figure 70. LVDS AC-Coupling, Option 2

Figure 71. 3.3V LVDS to 2.5 LVDS

Figure 72. LVDS to CML
Figure 73. LVDS AC-Coupled to Built-In Termination

![Diagram of LVDS AC-Coupled to Built-In Termination]

Figure 74. LVDS (Voltage Source) Amplitude Reduction

![Diagram of LVDS (Voltage Source) Amplitude Reduction]

Increasing R2/R3 reduces the amplitude.

Figure 75. LVDS (Current Source) Amplitude Reduction

![Diagram of LVDS (Current Source) Amplitude Reduction]

Increasing R2 reduces the amplitude.
Figure 76. LVDS (Current Source) to 1.5V VOS

![Diagram showing LVDS (Current Source) to 1.5V VOS](image)

Figure 77. LVDS to 0.6V DC Offset, Option 1

![Diagram showing LVDS to 0.6V DC Offset, Option 1](image)

Figure 78. LVDS to 0.6V DC Offset, Option 2

![Diagram showing LVDS to 0.6V DC Offset, Option 2](image)
Figure 79. LVDS to XTAL

LVDS Driver

Zo = 50 Ohm

R1
100

C1
0.1 uF

XTAL IN

XTAL OUT

Receiver_XTAL

Zo = 50 Ohm

R2
10 k

C2
0.1 uF

3.3 V or 2.5 V

LVDS

C1
0.01 uF

C2
0.01 uF

R1
100

R2
6.85 k

R3
3.9 k

Assumptions:
High Input Impedance
No Built-in Termination

Figure 80. LVDS to IDT PES24T6G2 HCSL Input Interface

100 Ohm Differential Transmission Line

Figure 81. LVDS to PCML

Z_diff=100 ohm differential

Assumptions:
High Input Impedance
No Built-in Termination

Renesas
Figure 82. LVDS Differential Duty Cycle Improvement

![Diagram showing LVDS Differential Duty Cycle Improvement](image)

- **C1**: 0.1μF
- **R1**: 100
- **Zo = 50**
- **Vcc = 3.3V**
- **R2**: 1.3k
- **C2**: 0.1μF
- **R3**: 800
- **R4**: 1.3k
- **R5**: 800
- **Receiv er_dif**

---

Figure 83. LVDS to 50-ohm Scope, Non-Floating Supply

![Diagram showing LVDS to 50-ohm Scope](image)

- **R3 and R4 are required only when the Coax and the Scope are absent**
HSTL Terminations

Figure 84. HSTL Standard Termination

Figure 85. HSTL to 3.3V LVPECL

As close to DUT as possible.
Figure 86. HSTL to Xilinx Spartan 1.8V HSTL II, Option 1

Figure 87. HSTL to Xilinx Spartan 1.8V HSTL II, Option 2

Figure 88. HSTL to LVDS
Figure 89. HSTL to 1.8V SSTL, Option 1

Termination for 50-ohm transmission line

Figure 90. HSTL to 1.8V SSTL, Option 2

Termination for 60 ohm transmission line

Figure 91. HSTL to 1.5V HSTL, DC-Couple
Figure 92. HSTL to 1.5V HSTL, AC-Couple

Figure 93. 1.5V HSTL Push-Pull Driver to Differential Input with 0.75V Bias

Figure 94. 1.5V HSTL Push-Pull Driver Differential Input Voltage Divider Bias
Figure 95. HSTL to DDR2

HCSL Terminations

Figure 96. HCSL to Differential Input Interface with Pulldown at the Driver

Suggest spare footprint
R5=100 for option of improving signal quality

Figure 97. HCSL to Differential Input Interface with Pulldown at the Receiver
Figure 98. HCSL to LVPECL

![HCSL to LVPECL](image)

Figure 99. HCSL to IDT Differential PCLK/nPCLK, Option 1

![HCSL to IDT Differential PCLK/nPCLK, Option 1](image)

Figure 100. HCSL to IDT Differential PCLK/nPCLK, Option 2

![HCSL to IDT Differential PCLK/nPCLK, Option 2](image)
Figure 101. HCSL to IDT Differential PCLK/nPCLK, Option 3

Figure 102. HCSL to IDT Differential PCLK/nPCLK, Option 4

Figure 103. HCSL to 400mV Swing

Reduce R5/R6 values to further reduce the amplitude.
Figure 104. HCSL to 1.5V Differential HSTL Interface

Figure 105. HCSL to 1.8V LVCMOS

Figure 106. HCSL to Xilinx Vertex 5
Figure 107. HCSL PCIE Source Termination

Recommended termination for applications which require the receiver and driver to be on a separate circuit board.

Figure 108. HCSL PCIE Receiver Termination

Recommended termination for applications which require a point to point connection and driver and receiver are on the same board.

CML Terminations

Figure 109. CML Standard Termination
Figure 110. CML to Differential CLK/nCLK

![CML to Differential CLK/nCLK Diagram](image1)

Figure 111. CML to HCSL - Receiver with High Input Impedance

![CML to HCSL Diagram](image2)

Figure 112. Receiver with Built-in 100 ohm Across

![Receiver with Built-in 100 ohm Across Diagram](image3)
**SSTL Terminations**

Figure 113. CML to HCSL - Receiver with Built-in 50 ohm to Ground

Figure 114. SSTL 1.8V to Differential PCLK/nPCLK with VBB

Figure 115. SSTL 1.8V to Differential PCLK/nPCLK, Option 1
Figure 116. SSTL 1.8V to Differential PCLK/nPCLK, Option 2

Figure 117. SSTL 1.8V to Differential PCLK/nPCLK, Option 3
Low-Power-HCSL

Figure 118. Universal Network

The above schematic uses a LP-HCSL driver with integrated termination resistors (RS). When using a driver where the termination is not integrated, please add RS=33Ω in series with each pin externally to complete the driver output impedance to 50Ω.

Equations for Figure 118

The Common Mode Voltage depends upon RN, RP and VDD: \( V_{CM} = \frac{V_{DD} \times RN}{RN + RP} \)

The following equation calculates the single-ended swing at the receiver input pins:

\[ V_{SWING} = 800\text{mVpp} \times \frac{RT}{50 + RT} \]

Figure 119. Universal Network with Amplitude Attenuation

Equations for Figure 119

Common Mode Voltage: \( V_{CM} = \frac{V_{DD} \times RN}{RN + RP} \)

Receiver Input Single-ended Voltage Swing: \( V_{SWING} = 800\text{mVpp} \times RT \times (50 + RT) \)

Rewriting to find RT for the required VSWING: \( RT = \frac{50 \times V_{SWING}}{(800\text{mVpp} - V_{SWING})} \)
Figure 120. Terminating LP-HCSL to LVPECL with Network

Also add RS=33Ω in series when not integrated in the LP-HCSL driver.

* Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver.

<table>
<thead>
<tr>
<th>VDD</th>
<th>RP</th>
<th>RN</th>
<th>CS*</th>
<th>VSWING**</th>
<th>VCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>2200Ω</td>
<td>3300Ω</td>
<td>0.1μF</td>
<td>771mVpp</td>
<td>1.98V</td>
</tr>
<tr>
<td>2.5V</td>
<td>2700Ω</td>
<td>2400Ω</td>
<td>0.1μF</td>
<td>770mVpp</td>
<td>1.18V</td>
</tr>
</tbody>
</table>

Figure 121. Terminating LP-HSCL to LVDS without Integrated RD

Also add RS=33Ω in series when not integrated in the LP-HCSL driver.

** CD is optional for filtering common mode noise in the clock.

*** Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver.

<table>
<thead>
<tr>
<th>VDD</th>
<th>RP</th>
<th>RN</th>
<th>RT</th>
<th>CS*</th>
<th>CD**</th>
<th>VSWING***</th>
<th>VCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>3000Ω</td>
<td>1800Ω</td>
<td>50Ω</td>
<td>0.1μF</td>
<td>0.1μF</td>
<td>400mVpp</td>
<td>1.24V</td>
</tr>
<tr>
<td>2.5V</td>
<td>2200Ω</td>
<td>2200Ω</td>
<td>50Ω</td>
<td>0.1μF</td>
<td>0.1μF</td>
<td>400mVpp</td>
<td>1.25V</td>
</tr>
<tr>
<td>1.8V</td>
<td>1500Ω</td>
<td>3300Ω</td>
<td>50Ω</td>
<td>0.1μF</td>
<td>0.1μF</td>
<td>400mVpp</td>
<td>1.24V</td>
</tr>
</tbody>
</table>
**Figure 122. Terminating LP-HCSL to LVDS with Integrated RD**

* Also add RS=33Ω in series when not integrated in the LP-HCSL driver.

** RD is integrated in the receiver so we don't have to assemble it.

*** Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver.

<table>
<thead>
<tr>
<th>VDD</th>
<th>RP</th>
<th>RN</th>
<th>RD**</th>
<th>CS*</th>
<th>VSWING***</th>
<th>VCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>3000Ω</td>
<td>1800Ω</td>
<td>100Ω</td>
<td>0.1µF</td>
<td>391mVpp</td>
<td>1.24V</td>
</tr>
<tr>
<td>2.5V</td>
<td>2200Ω</td>
<td>2200Ω</td>
<td>100Ω</td>
<td>0.1µF</td>
<td>391mVpp</td>
<td>1.25V</td>
</tr>
<tr>
<td>1.8V</td>
<td>1500Ω</td>
<td>3300Ω</td>
<td>100Ω</td>
<td>0.1µF</td>
<td>391mVpp</td>
<td>1.24V</td>
</tr>
</tbody>
</table>

** Figure 123. Terminating LP-HCSL to a CML Receiver**

* RT is only needed when not integrated in the CML receiver input.

** Also add RS=33Ω in series when not integrated in the LP-HCSL driver.

*** Single ended voltage swing, based upon 800mVpp at the LP-HCSL driver.

**** VDD is the value used for the CML receiver and does not need to be the same as for the LP-HCSL driver.

<table>
<thead>
<tr>
<th>RT*</th>
<th>CS**</th>
<th>VSWING***</th>
<th>VCM ****</th>
</tr>
</thead>
<tbody>
<tr>
<td>50Ω</td>
<td>0.1µF</td>
<td>400mVpp</td>
<td>VDD</td>
</tr>
</tbody>
</table>
In this case, we can connect the LP-HCSL output directly to the receiver input pins without any additional components. The swing at the receiver input is 400mVpp single ended or 800mVpp differential. Receivers often specify the swing differential.

The receiver datasheet may recommend RP and RN values. If not, use the equation on page 2 to find RP and RN values for the required common mode voltage. Make sure that the resistance value for RN and RP in parallel is at least 1KΩ to not load the signal lines too much.

When VDD is for the receiver and the IC’s datasheet does not specify a common mode voltage, a good $V_{\text{CM}}$ value is 50%VDD. In this case RP and RN can have the same value, for example 2200Ω each.

The swing at the receiver input is 391mVpp single ended with $RN = RP = 2200Ω$. 
Because generic differential inputs can often handle up to 1000mVpp of swing at the input pins we do not need to attenuate. For noise reasons it is beneficial to make as large a swing as possible.

For RN and RP values, see the previous circuit for a differential input with on-chip termination.
### Revision History

#### Table 1. Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>March 6, 2017</td>
<td>• Updated legal disclaimer</td>
</tr>
<tr>
<td>December 9, 2016</td>
<td>• Initial release</td>
</tr>
</tbody>
</table>
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Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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