

Application Note

PV88080-Dynamic Voltage Control (DVC)

AN-PV-006

Abstract

Dynamic Voltage Control (DVC) facilitates the increase or decrease of power rail voltages dynamically as the load increases on a processor. This functionality saves system power when the loading is low while allowing increased processor clocking when the system needs it. This application note illustrates the use of DVC using the PV88080 PMIC.

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1 Terms and Definitions

GUI	Graphical User Interface
HVBuck	High Voltage Buck Converter
LVBuck	Low Voltage Buck Converter

2 References

- [1] S. Mittal, "A survey of techniques for improving energy efficiency in embedded computing systems", IJCAET, 6(4), 440–459, 2014.

3 Introduction

The power consumed by processor cores is proportional to the operating frequency and to supply voltage. DVC is used to optimize performance, power consumption, and thermal performance of processor devices. DVC increases voltage to increase processor performance, and decreases voltage to save power. This technique, initially used in laptops and mobile devices [1], is now becoming prevalent in tethered systems.

4 DVC

Traditionally, a mount of resistor divider and MOSFET, as shown in Figure 1, is used to change the divide ratio for adjusting the output voltage of the converter. It needs many components and control signals, and therefore, also a large layout area. The PV88080 provides DVC, which supports adaptive adjustment of the supply voltage dependent on the processor load, via direct register write in the I²C interface. This simplifies the schematic, as shown in Figure 2. The DVC slew rate is also adjustable in the I²C to minimize the overshoot when the output voltage overshoot level is not acceptable. For examples of how the PV88080 DVC minimizes overshoot and undershoot, see Figure 3 and Figure 4.

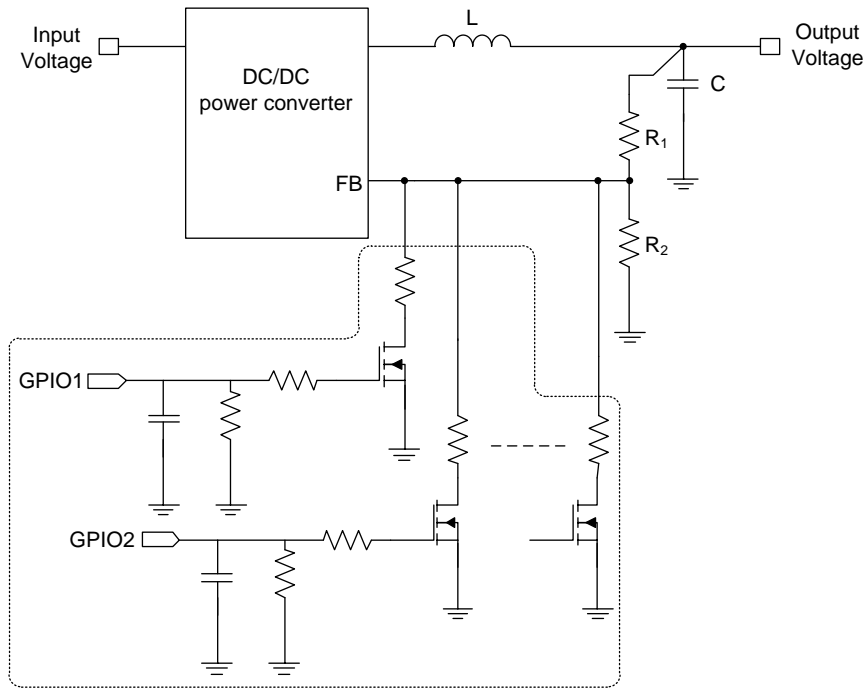


Figure 1: Traditional DVC Solution

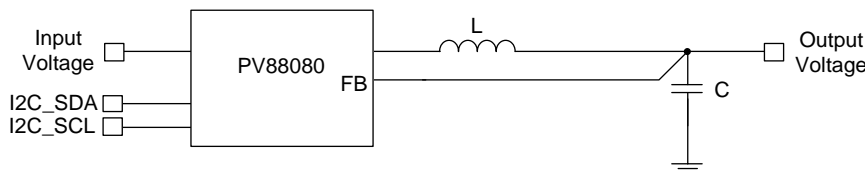


Figure 2: PV88080 Simplified Block Diagram for One Buck Stage

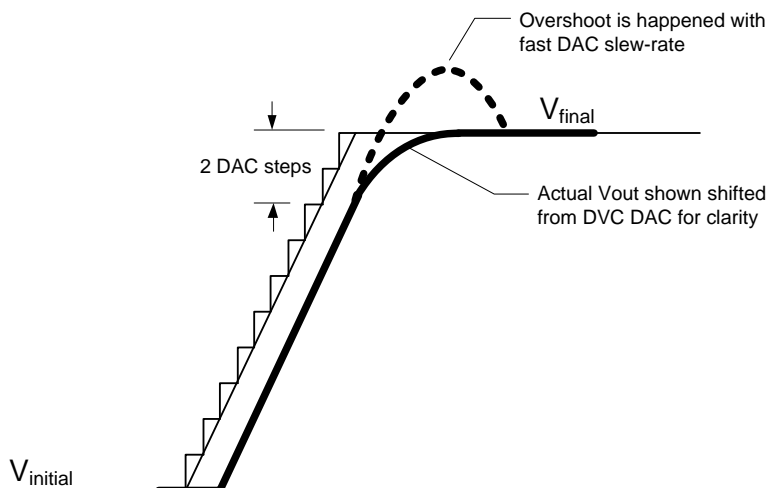


Figure 3: PV88080 DVC Up Transition Measurement Example

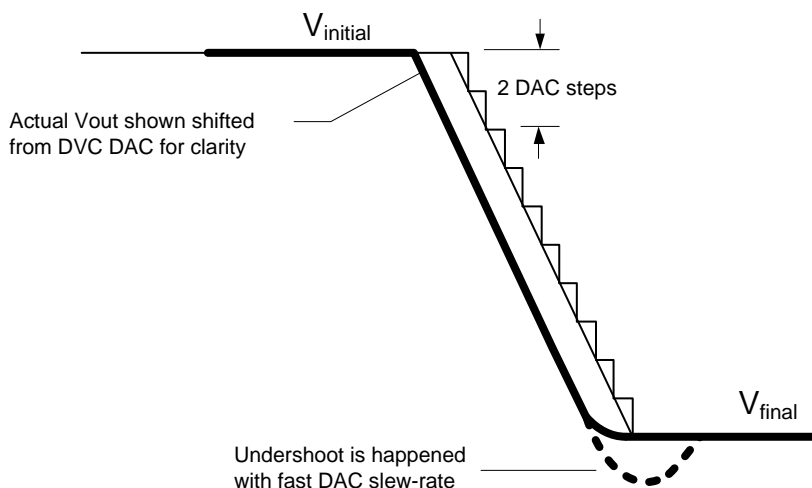


Figure 4: PV88080 DVC Down Transition Measurement Example

4.1 DVC Setting - LVBuck Converter

The LVBuck converters support DVC. The output voltage range of LVBUCK1 is 0.75 V to 3.3 V, and 0.9 V to 3.6 V for LVBucks 2 and 3, see [Table 1](#) and [Table 2](#). The typical core processor voltage is in region 1.

The target voltage is programmable to suit specific processor requirements and can be set in register BUCKx_CONF0[6:0] using **Dialog Semiconductor's** graphical user interface (GUI), see [Figure 5](#).

Table 1: LVBuck1 Output Voltage Region

Region	Min (V)	Max (V)	Step (mV)
1	0.75	1.39375	6.25
2	1.4	2.19375	6.25
3	1.2	2.7875	12.5
4	2.8	3.3	12.5

Table 2: LVBUck2/3 Output Voltage Region

Region	Min (V)	Max (V)	Step (mV)
1	0.9	1.39375	6.25
2	1.4	2.19375	6.25
3	1.2	2.7875	12.5
4	2.8	3.6	12.5

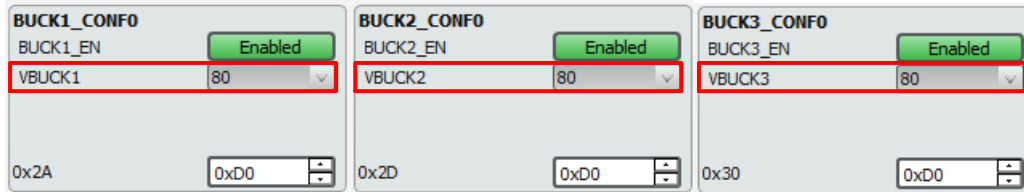


Figure 5: Dialog GUI - BUCKx_CONF0[6:0]

The DVC slew rate is adjustable to prevent overshoot or undershoot on the output voltage by setting register Buckx_CONF3[7:6] in the GUI, see Figure 6. Generally, higher slew rates are more likely to cause overshoot or undershoot. Figure 7 to Figure 10 show the DVC waveform with different slew rates. The overshoot and undershoot caused by faster slew rates are shown in Figure 9 and Figure 10.

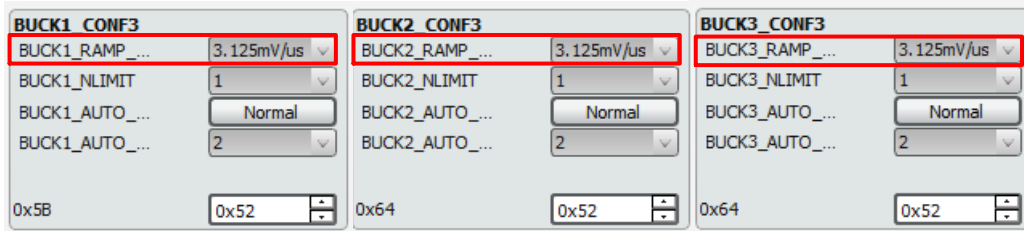


Figure 6: Dialog GUI - BUCKx_CONF3[7:6]

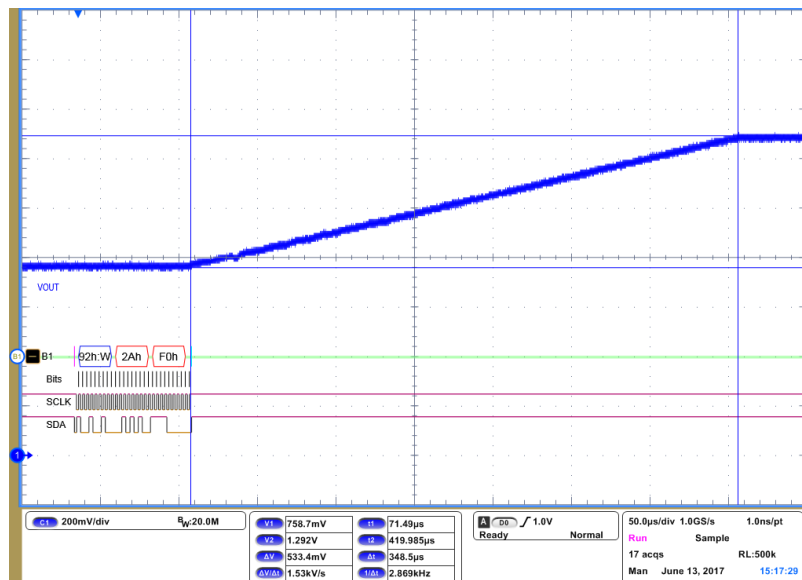


Figure 7: DVC Step-Up with 1.5625 mV/µs Slew Rate

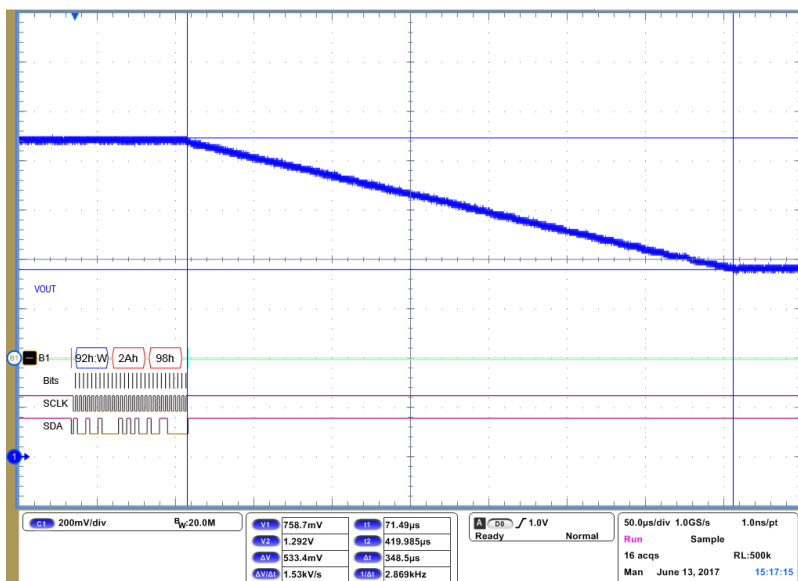


Figure 8: DVC Step-Down with 1.5625 mV/µs Slew Rate

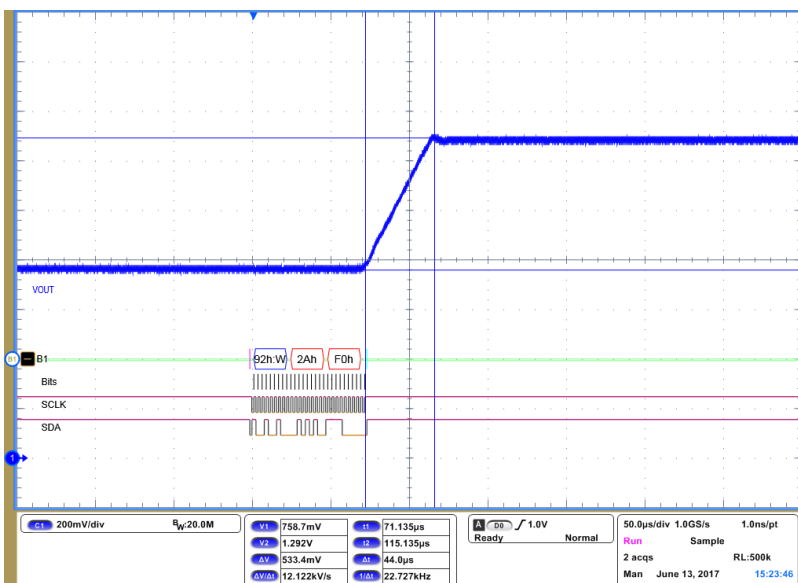


Figure 9: DVC Step-Up with 12.5 mV/µs Slew Rate

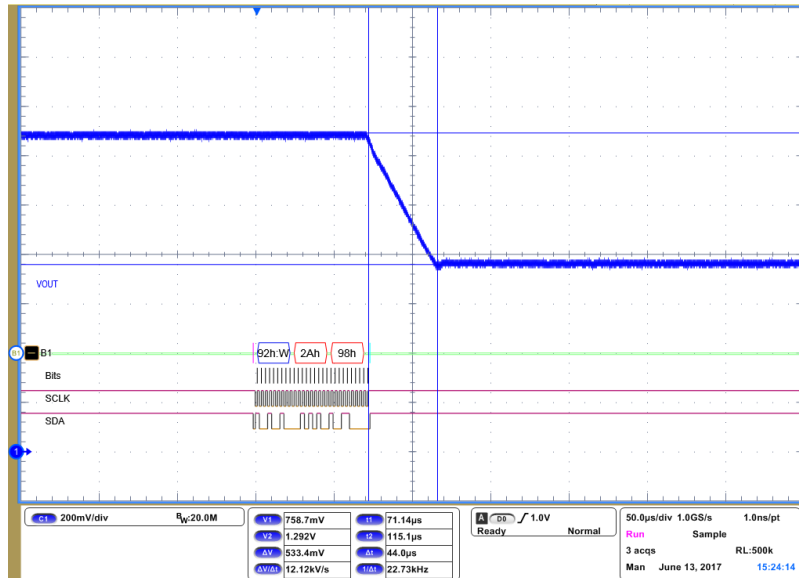


Figure 10: DVC Step-Down with 12.5 mV/µs Slew Rate

For example, a processor is supplied by the LVBuck1 for the typical 1.2 V core voltage. The LVBuck1 output voltage is in region 1, see Table 3. In idle mode, the core voltage of the process is 1.15 V to save power. The slew rate is set to 3.125mV/µs to prevent overshoot. Sending the command 0xD8 to BUCK1_CONF0(0x2A) in the I²C interface, as shown in Figure 11, results in the desired DVC step-down, see Figure 12. The output voltage is set back to 1.2 V by sending the 0xE0 command to BUCK1_CONF0(0x2A), see Figure 13 and Figure 14.

Table 3: LVBuck1 Output Voltage - Region 1

Address	Name	
0x002A	BUCK1_CONF0	
Field name	Bits	Description
BUCK1_EN	[7]	BUCK1 Enable
		Value Description
		0x0 0:Disabled
		0x1 1:Enabled
VBUCK1	[6:0]	Buck1 Target Voltage. $V_{OUT} = 0.6 + 0.00625 * V_{Buck1}[6:0]$
		Value Description
		0x18 $V_{OUT} = 0.6 + 0.00625 * 24 = 0.75 \text{ V}$
	
		0x7F $V_{OUT} = 0.6 + 0.00625 * 127 = 1.39375 \text{ V}$

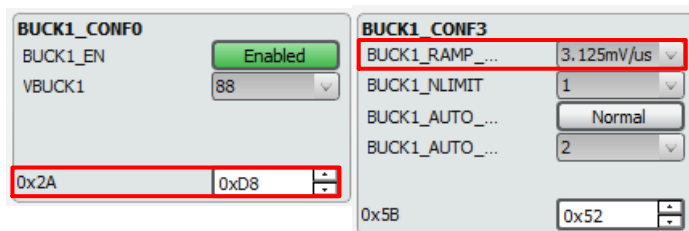


Figure 11: Sending 0xD8 to BUCK1_CONF0 in Dialog GUI

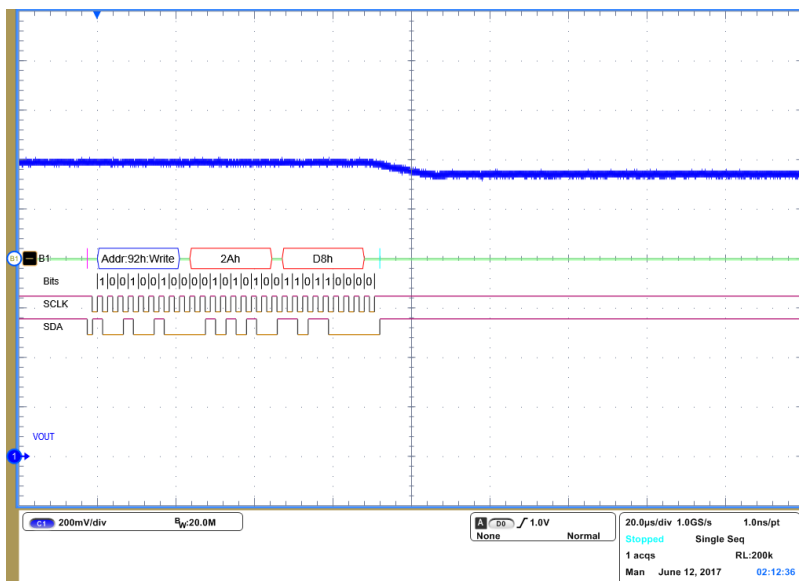


Figure 12: DVC Step-Down from 1.2 V to 1.15 V

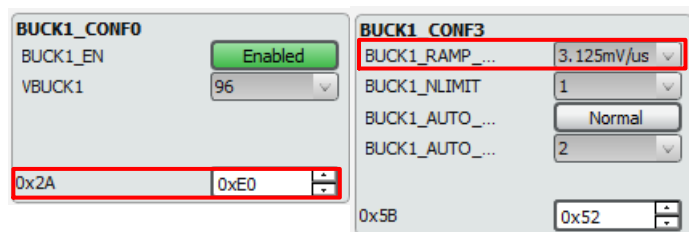


Figure 13: Sending 0xE0 to BUCK1_CONF0 in Dialog GUI

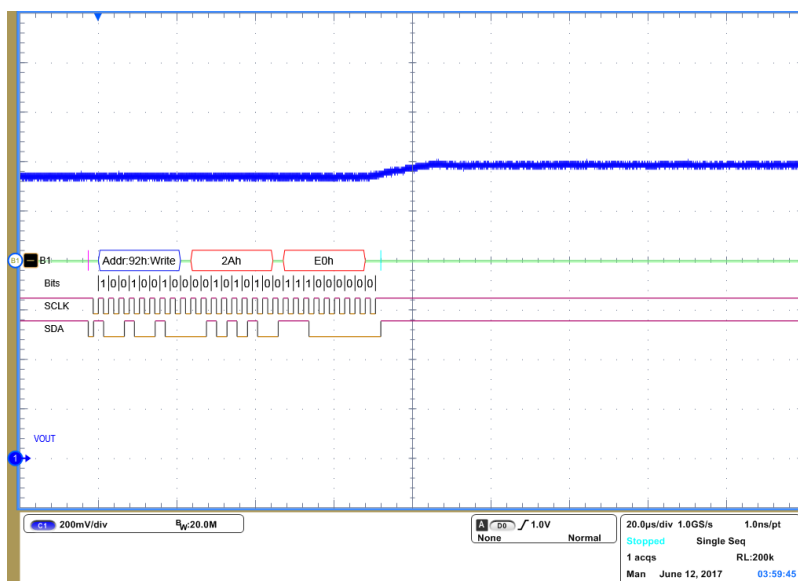


Figure 14: DVC Step-Up from 1.15 V to 1.2 V

4.2 DVC Setting - HVBUck Controller

The HVBUCK controller supports DVC in the 0.8 V to 1.275 V output voltage range with 5 mV, see Table 4. Set register HVBUCK_CONF1[7:0] to the target voltage according to the processor requirement. The HVBUCK DVC slew rate is also adjustable to prevent overshoot or undershoot on the output voltage by setting register HVBUck_CONF2[3:1].

For example, a processor is supplied by the HVBUCK for the typical 1.05 V core voltage. In idle mode, the core voltage of the process is 1.0 V to save power. The slew rate is set to 3.125 mV/μs to prevent overshoot. Sending the command 0xC8 to HVBUCK_CONF1(0x33) in the I²C interface, as shown in Figure 15, results in the desired DVC step-down, see Figure 16. The output voltage is set back to 1.05 V by sending the command 0xD2 to HVBUCK_CONF1(0x33), see Figure 17 and Figure 18.

Table 4: HVBUck Output Voltage

Address	Name		
0x0033	HVBUCK_CONF1		
Field name	Bits	Description	
VHBUCK	[7:0]	HVBUck Target Voltage. $V_{OUT} = 0.005 * VBuck1[6:0]$	
		Value	Description
		0xA0	$V_{OUT} = 0.005 * 160 = 0.8V$
		0xFF	$V_{OUT} = 0.005 * 255 = 1.275 V$

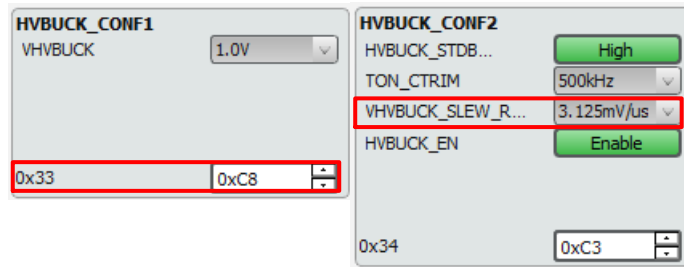


Figure 15: Sending 0xC8 to HVBUCK in Dialog GUI

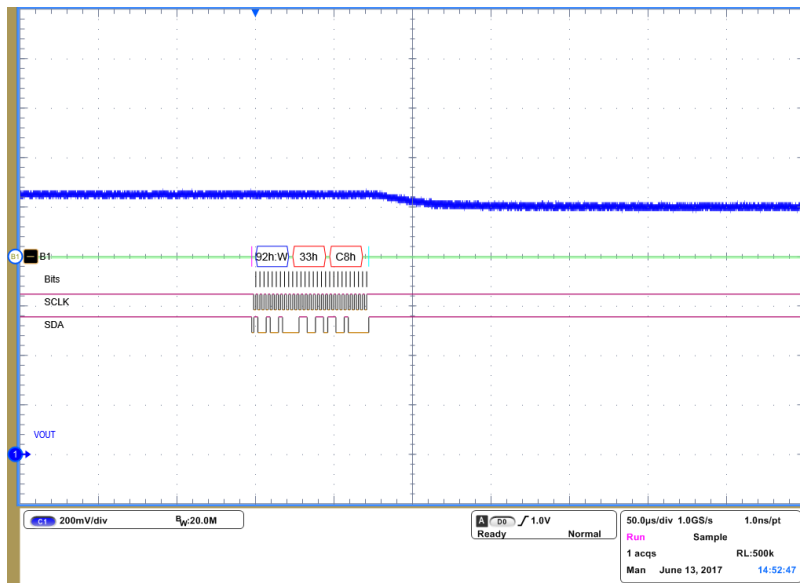


Figure 16: DVC Step-Down from 1.05 V to 1.0 V

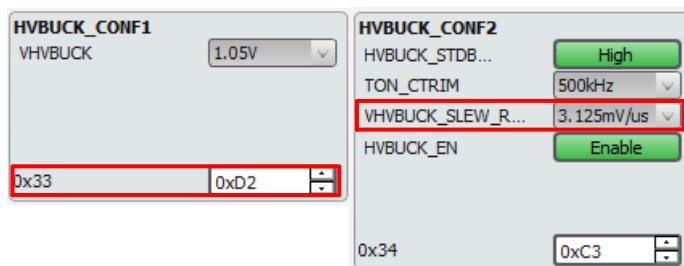


Figure 17: Sending 0xD2 to HVBUCK in Dialog GUI

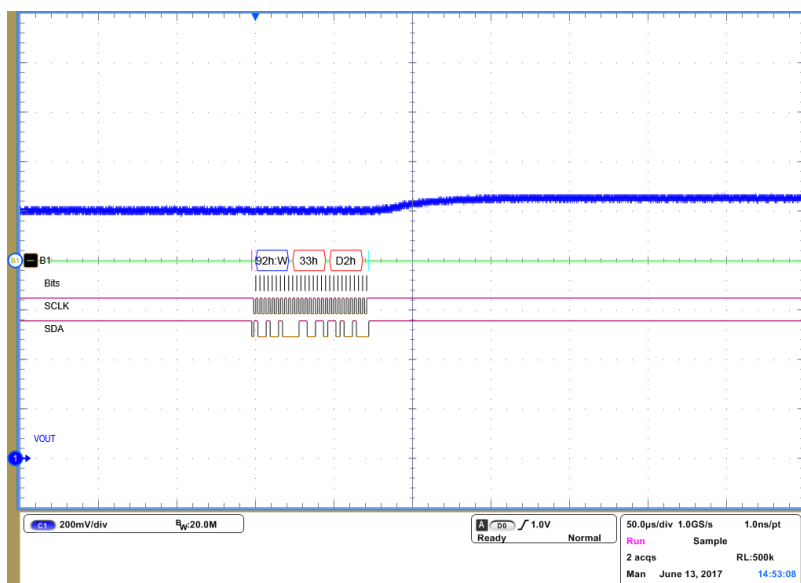


Figure 18: DVC Step-Up from 1.0 V to 1.05 V

5 Conclusions

Both the LVBUCK and HVBUCK in PV88080 support DVC function. The flexible DVC slew rate prevents overshoot and undershoot in different applications. The I²C interface provides a standard and flexible way to control this feature.

Revision History

Revision	Date	Description
1.0	17-Aug-2017	Initial version.

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