Application Note

Dynamically Changing the PV88080 Output Voltage

AN-PV-004

Abstract

Modern SOC controlled systems have to power many subsystems which require multiple power supplies in the platform, for example core, DDR interfaces, and peripheral interfaces. The start-up and sequencing for these supplies have also become more complex in applications. In addition, the increase in leakage current due to the evolution of technologies has become an issue. For that reason, we have introduced a method for power supply start/interrupt sequence design and for reducing leakage current using a power management integrated circuit (PMIC) with I²C communication functionality.

Contents

Figures

Tables

1 Terms and Definitions

DSP	Digital signal processor
DVC	Dynamic voltage control
DVS	Digital voltage scaling
GUI	Graphical user interface
I^2C	Inter-integrated circuit
IC	Integrated circuit
PMIC	Power management IC
SoC	System on (a) chip

2 Introduction

In portable applications, digital voltage scaling (DVS) is becoming increasingly important to reduce energy consumption by adapting the supply voltage of DSPs and microcontrollers depending on the upcoming loading. Power supplies for DVS applications are usually set up with VID pins or I^2C which come with PMICs specifically designed for such applications. These digitally-controlled mechanisms are used to change the reference voltage of the controller IC, generating a programmable output voltage. Changing the regulated output voltage is accomplished by modifying the feedback pin circuitry.

In principle, there are many different ways to change the output voltage by influencing the feedback pin. This application note describes the most important methods.

3 Direct Serial Resistor Connection using the Feedback Divider

This method of adjusting the output voltage adds an additional resistor in parallel, or in series, to the feedback resistors.

Transistors have to be used in the signal path and the signal controlling the output voltage has to be able to turn the transistors on and off. Figure 1 shows the additional resistor and transistors in the feedback path of a power supply to modify the output voltage.

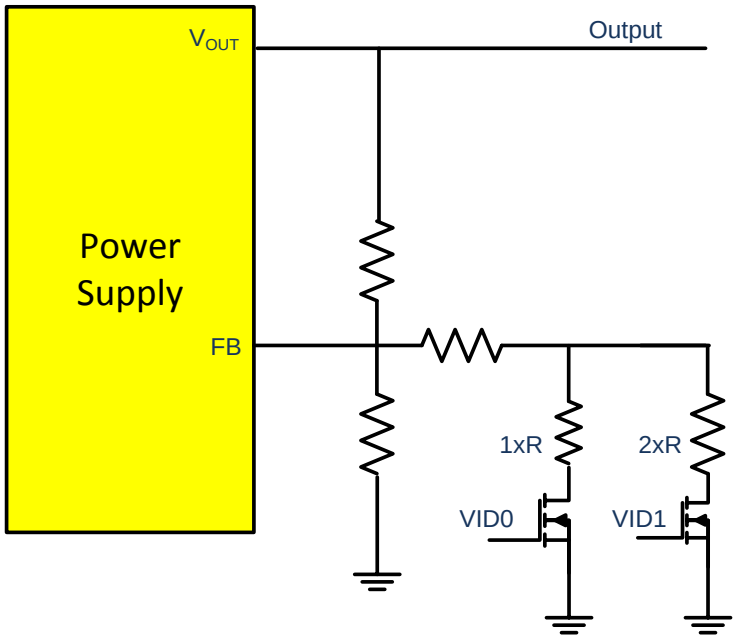

Figure 1: Additional Resistors and Transistors in the Feedback Pin

4 Adjustable Voltage Connection using the Feedback Divider

The output voltage of the regulator can be adjusted using a voltage control signal which is fed through a second resistive voltage divider into the feedback pin. The output voltage can be set to multiple voltages and can be changed in continuous transitions, see Figure 2.

Only two additional resistors are required which makes this a lower cost alternative. The downside of this method is that the programming voltage (Vcontrol) is restricted. The control signal must be able to drive the resistive dividers and every bit of this control voltage's behavior is used by the FB pin to alter V_{OUT} in a purely analog manner.

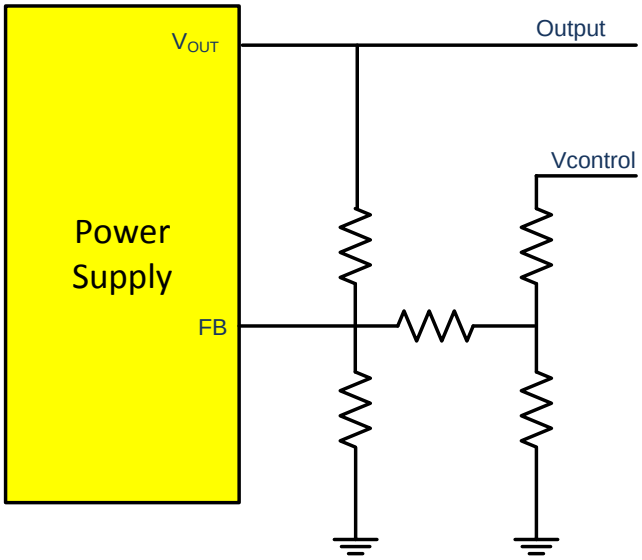

Figure 2: Voltage Control with Possible Voltage Divider

A power supply with a changing output voltage must be stable under all output voltage conditions. When using a voltage mode or a current mode PWM switching regulator, the feedback divider network has an effect on the gain of the control loop. Buck regulators have a linear transfer function and, generally, the compensation does not have to be optimized for different output voltages. When power supplies with a variable output voltage are designed, loop stability tests must be performed for the complete output voltage range.

There is a difference in the gain depending on whether the power supply's output voltage is changed by modifying the low-side feedback resistor or by injecting a current into the feedback node. Changing the low-side feedback resistor will not change the gain of the circuit if the error amplifier is a conventional opamp.

In some designs, an amplifier with a wide supply range or an additional supply for the bias voltage of the amplifier might be needed. Since the current required for the supply rails of the amplifier is very small, often the supply is only a resistive divider with a zener diode limiting the supply rail.

5 Digital Voltage Scaling by I²C

PV88080 provides an easy way to change the regulated output voltage of the buck via an I²C bus. PV88080 can be configured for a specific microprocessor's DVS requirements. All bucks in PV88080 support DVS for maximum system efficiency. The DVS method is a powerful technique that supports the optimization of power consumption for modern processors. DVS allows strict system requirements for the power dissipation of the processor to be met.

In order to implement DVS, both the processor and the power supply must be carefully designed for communication and regulation in order to account for the device operating point or process variation. PV88080 is a highly integrated device that enables and simplifies this function, see Figure 3.

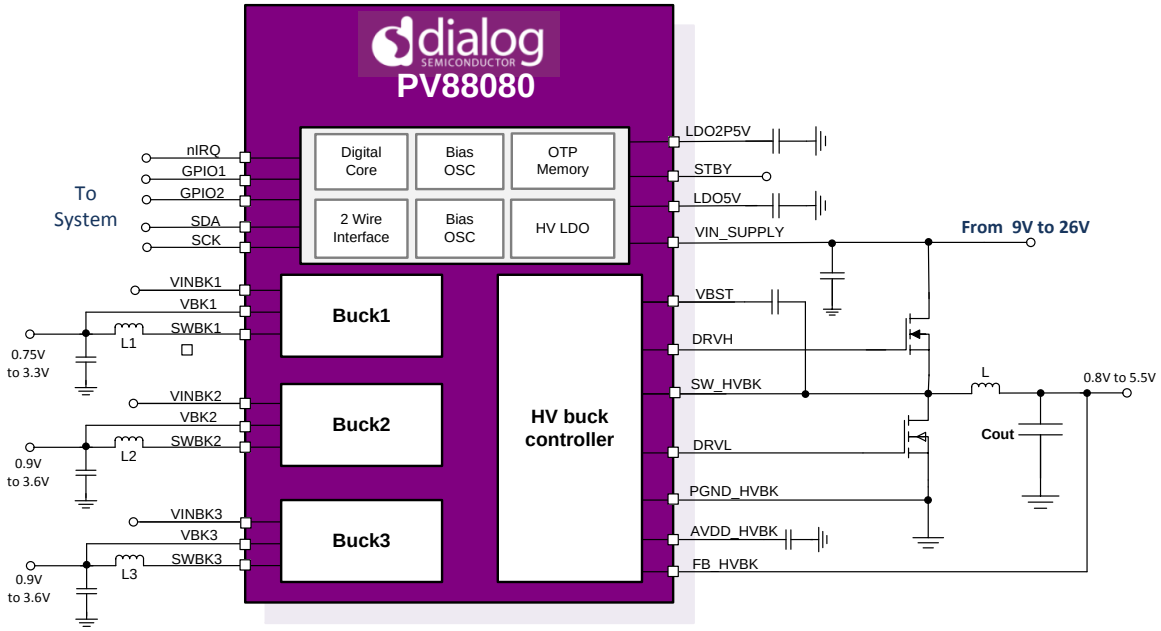

Figure 3: PV88080 Provides Digital Voltage Control by I²C Bus

6 PV88080 Power Supply Enable using GPIO Pins

The PV88080 designer is a software tool provided for configuring the device. This PC-based graphical user interface (GUI) offers an intuitive I²C interface to the device. It allows the design engineer to configure the system operating parameters for the application without directly using I²C commands, store the configuration to on-chip non-volatile memory, and observe system status (voltage, and so forth).

The PV88080 can sequence and enable or disable up to three power supplies through the GPIO1 and GPIO2 signals. These signals can be configured active-high or active-low, supporting power supplies with either polarity. The enable signals must be pulled up or down on the board according to the desired default power supply state (enabled or disabled). The buck's output voltage settings are configured by the user through the GUI, see Figure 4. The GPIO settings are stored in on-chip program memory to control each buck output's enable and disable. The GPIO_VBUCK_CONF register can be used to select the digital GPIO status on which to base the output voltage.

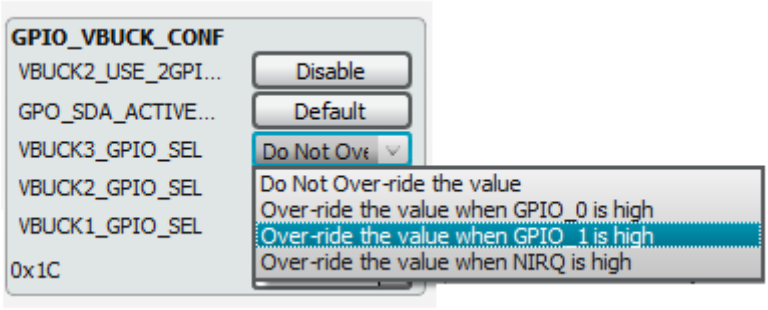

Figure 4: PV88080 GUI Rail Configuration for GPIO Enable Setting

7 Select Buck2 Voltage using GPIO Pins

The output voltage of Buck2 can be changed using the digital pins GPIO1 and GPIO2 without changing the OTP setting, see Table 1.

Table 1: Buck2 Output Voltage Selection Function Summary

	GPIO1 Pull Low	GPIO1 Pull High
GPIO2 Pull Low	VBuck2	VBuck2_ALT
GPIO2 Pull High	VBuck1_ALT	VBuck3_ALT

For systems without an I²C interface, PV88080 can provide flexible power sequencing and adjustable buck output voltages. In the example in Figure 5, the nIRQ pin is configured to enable all the bucks, and the Buck2 output voltage is selectable using GPIO pins.

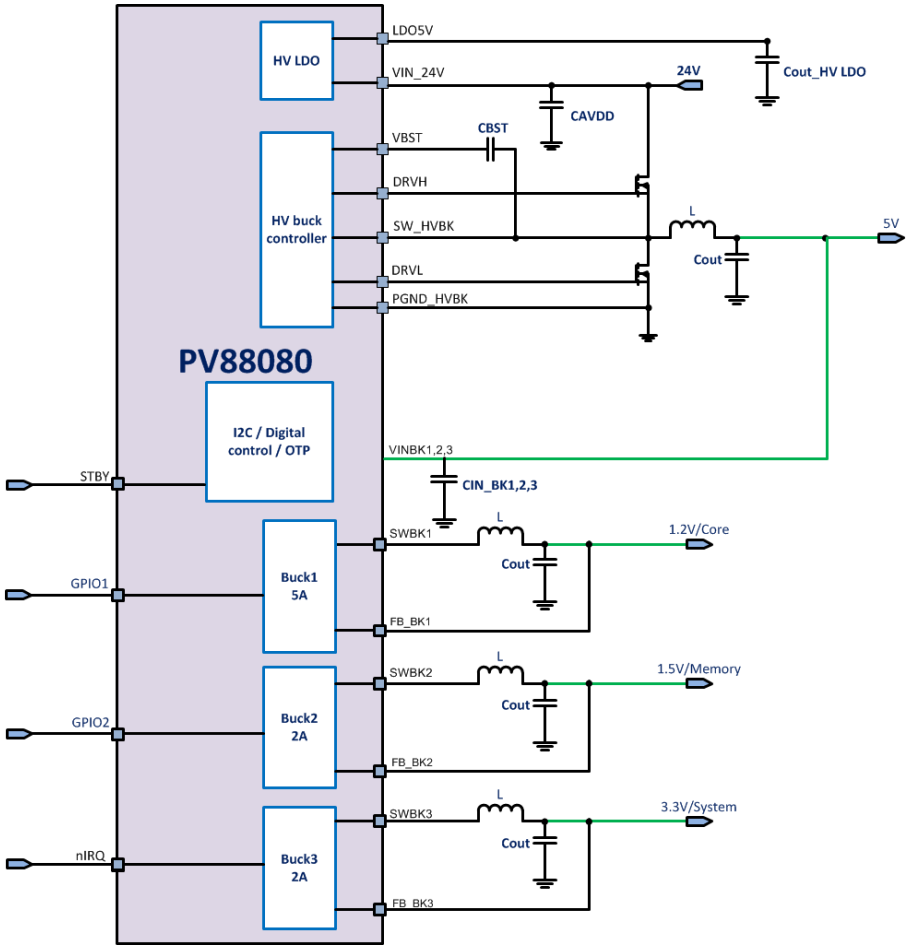

Figure 5: Flexible Output Voltage Setting by PV88080 without I²C Interface

8 Select HVBuck Voltage using STBY Pin

To achieve long battery life standby or suspend mode operation, a platform must be able to operate at a very low hardware power floor. The term power floor describes the hardware power state in which all devices are idle and inactive, and power consumption is dominated by hardware static leakage. To reliably operate at the power floor, each device outside the System on a Chip (SoC) must enter a very low standby power state when it is unused. Power to a device might be controlled autonomously by the device based on commands from the SoC that controls power management hardware using the external GPIO.

For example in a TV platform, the CPU reduces power to unneeded subsystems and places the RAM into the minimum power state for retaining sufficient data. Because of the large power saving, the platform automatically enters this mode when the computer is running. The CPU must consume some energy while sleeping in order to power the RAM and to be able to respond to a wake-up event.

The typical platform with PV88080 switched mode power supplies are dimensioned to support a supply diagram based on Figure 6.

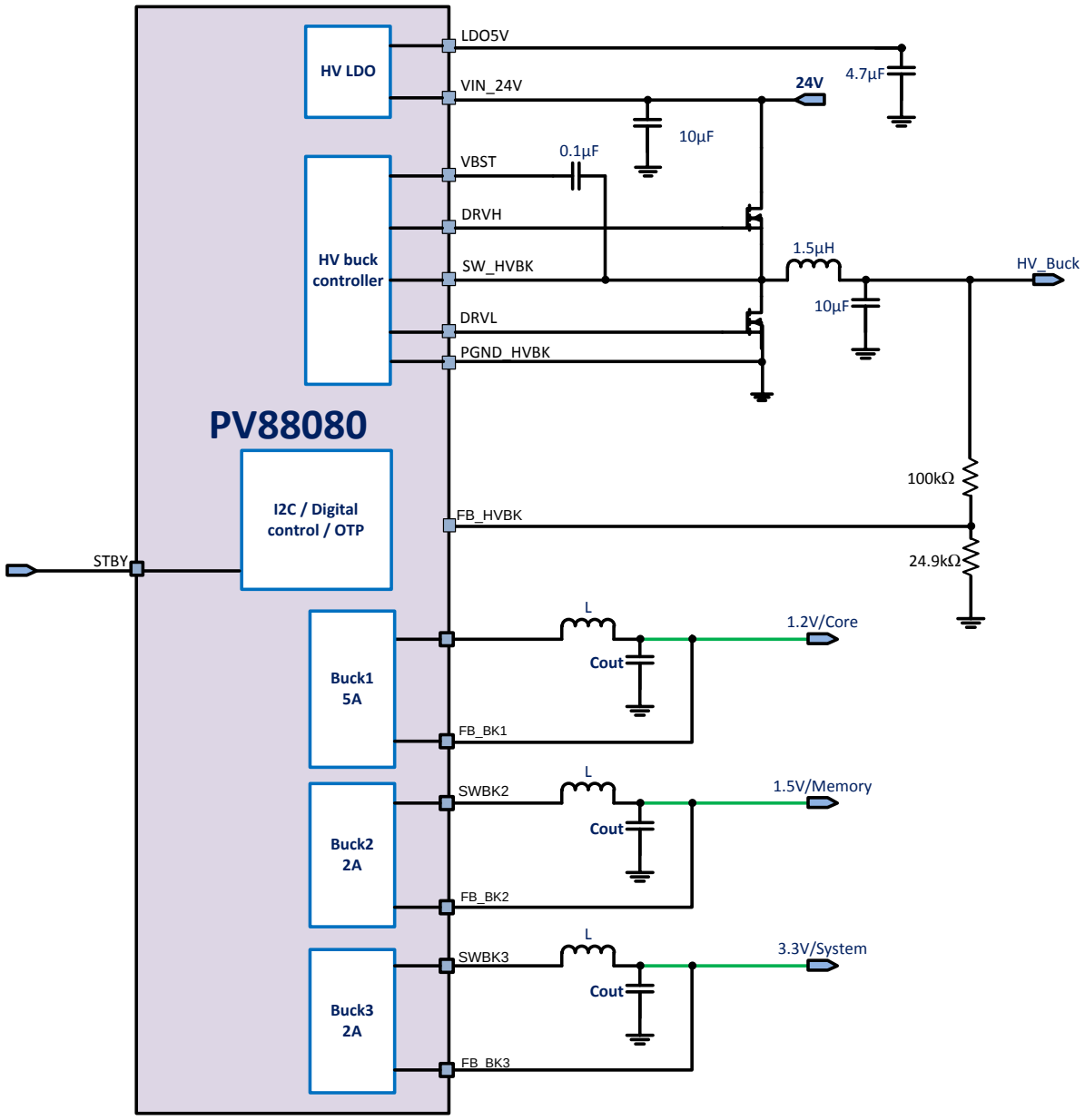

Figure 6: PV88080 Power Supply Distribution in Platform

While maintaining the specified performance, the minimum operating voltage for the HVBuck supply tree is 5 V. PV88080 can help reduce the overall platform current by lowering the switcher output voltage, disabling some regulators, or forcing some GPOs low in standby mode. This can be obtained by I²C configuration of the standby response of the circuits along with control of the STBY pin. The behavior of PV88080 can be configured in internal OTP memory.

Table 2: Output Voltages in Normal and Standby Mode

Supply	Typical Application	Output Voltage (V) in Normal Mode (STBY=Low)	Output Voltage (V) in Standby Mode (STBY=1)
Buck1	Processor core	1.2	Turn off
Buck2	Processor memory or DDR	1.5	Turn off
Buck3	I/O and peripheral	3.3	3.0
HVBuck	System 5 V	5	4.5

To implement the STBY power setting in Table 2, use the GUI to configure the registers as shown in Figure 7 and Figure 8.

Power STBY mode reduces power consumption at the cost of increased data transfer latency. Power STBY mode is expected to always be enabled when the platform is running on battery power, unless low-latency connections in a network are required.

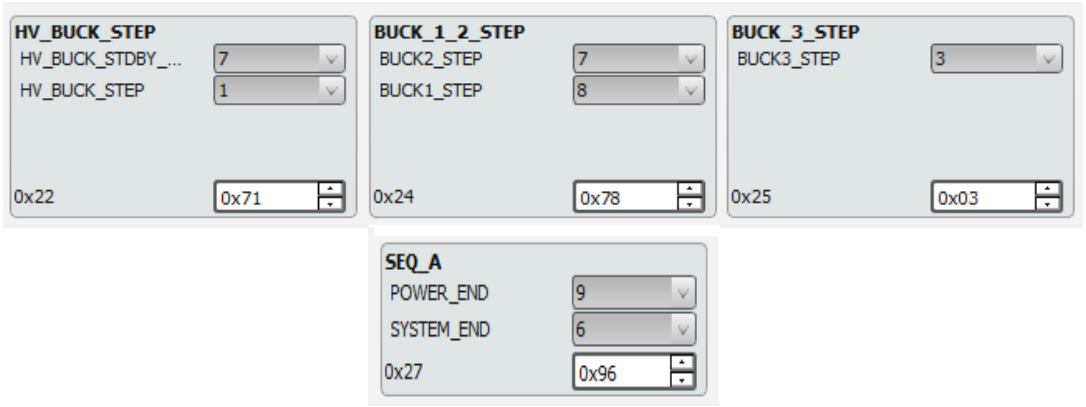

Figure 7: Internal Register Settings in STBY Mode

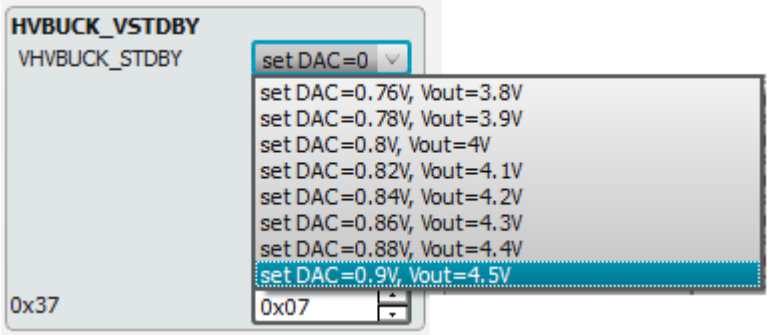

Figure 8: Set the VHVBUCK_STDBY Register to 4.5 V

A Wi-Fi device platform is a good example and must support power management features to reduce power consumption. Other examples include Wi-Fi devices in a modern standby platform that are either connected to the SoC over the digital input/output (I/O) or I²C bus, or physically integrated into the SoC itself. In PV88080, it is easy to implement voltage reduction to downgrade the Wi-Fi CPU voltage using the STBY pin.

In Figure 9, the HVBuck in PV88080 configures 1.0 V to connect the CPU terminal in normal operation. The HVBuck output voltage changes to 0.9 V for power saving request in STBY mode.

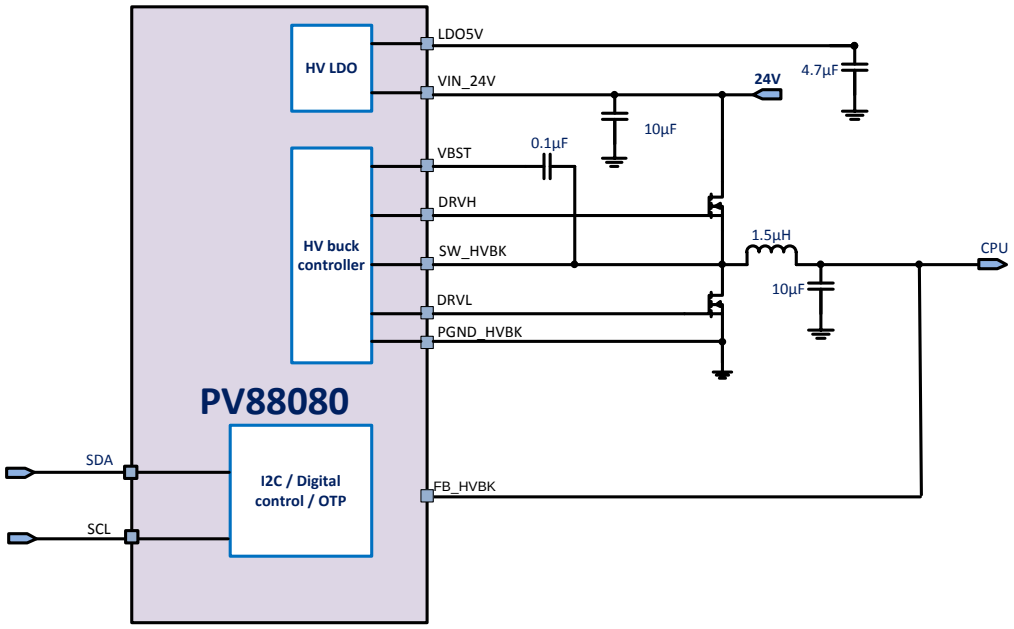

Figure 9: Connect PV88080 HVBuck for Wi-Fi CPU Application

9 Dynamic Voltage Scaling

In the core power supply of an SoC, higher voltages are required due to the voltage drop from parasitic resistance in the substrate and power wiring resistance within the SoC. Because the voltage drop is reduced in a state with light load, such as standby mode, it is possible to lower the power voltage in comparison to a state in which there is constantly a heavy load.

With systems that cannot change the PMIC output voltage, excess voltage continues to be applied to the SoC when in standby mode (light load). Power consumption due to leakage is dependent on voltage, so this results in excess consumption of power. Therefore, by using a PMIC that varies the output voltage according to the state of operation, it is possible to set an optimal voltage for the operational mode. In this way, it is possible to minimize the power consumption due to leakage. This is especially effective in systems that have long standby times, see Figure 10.

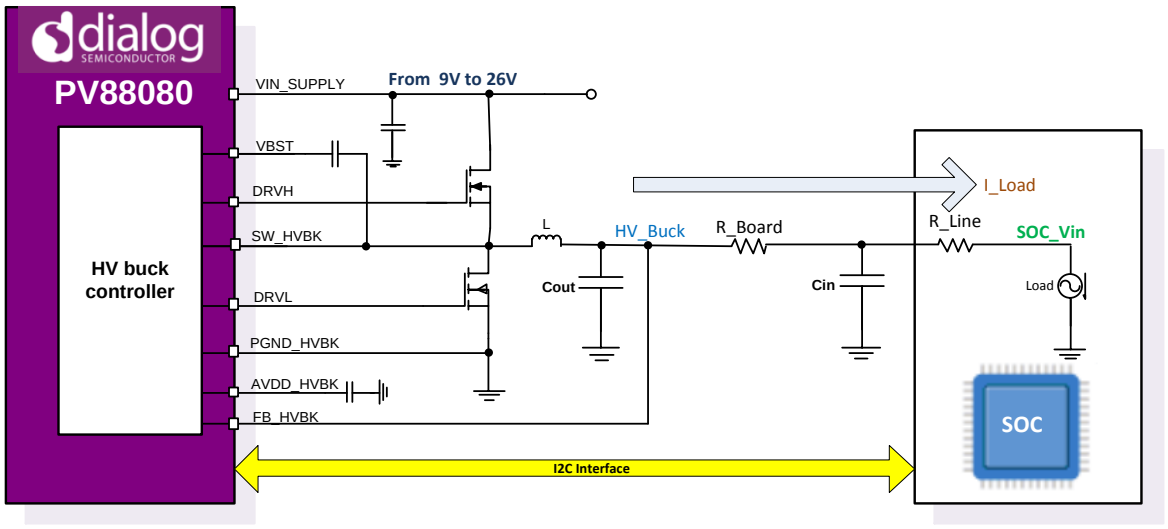

Figure 10: SoC Operational Diagram with PV88080

To optimize system performance without excessive power consumption, the CPU supply voltage is dynamically changed depending on operating conditions. In idle mode where CPU speed is lower, the CPU supply voltage is lowered to reduce power consumption, but when CPU activity suddenly needs to increase, the CPU supply is quickly increased to ensure stable CPU performance in computing intensive conditions, see Figure 11.

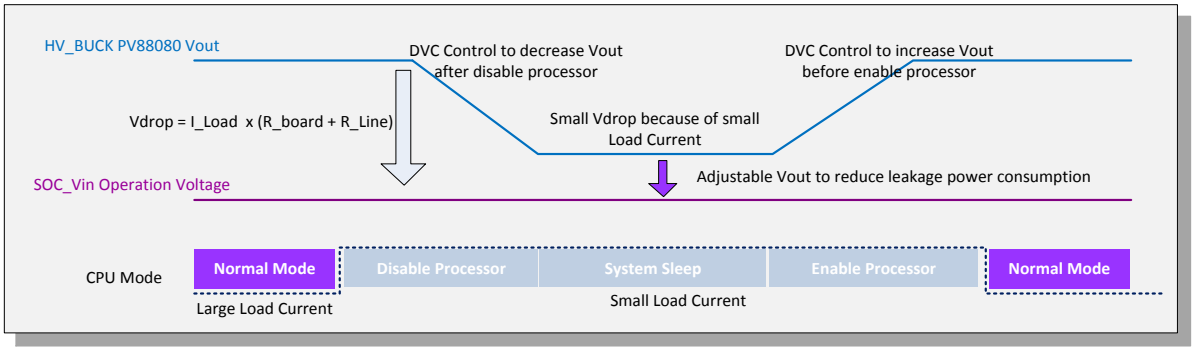

Figure 11: DVS Operational Concept Diagram with PV88080

Figure 12 shows dynamic behavior controlled by PV88080. The CPU sends the DVC command (from 1.4 V to 0.9 V, ramping down, slowly in this case) by I²C interface, the regulator then ramps down the output voltage with the requested speed.

Figure 12: DVC Behavior with Loading Current in PV88080

Figure 13 illustrates the use of the PV88080 GUI to support a flexible and easily configured DVS output setting. The minimum DVC step in PV88080 is 5 mV with 1 % accuracy.

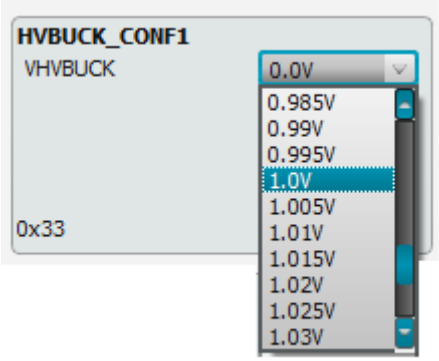

Figure 13: DVC Configuration in PV88080 GUI

10 Conclusion

This document has introduced the approach of using a PMIC with communications control to dynamically alter the power supply voltage which reduces power consumption.

Although the market is changing with increasing speed, the ability to design an adaptable power supply by changing only the software, contributes to shortening development time. Moreover, increased SoC functionality and decreased power consumption were formerly targeted as future technical developments but DVS offers an immediate solution.

Proper design of PMIC subsystems to support modern SoC-based systems reduces power consumption for these systems without the cost increases that accompany the evolution of technology.

As a final note, with increasing leakage current, DVS can optimize power solutions at the system level which will be increasingly important going forward.

Revision History

Revision	Date	Description
1.0	15-Aug-2017	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

Disclaimer

Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5425 4567

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Singapore
Dialog Semiconductor Singapore
Phone: +65 64 8499 29

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 3769 5200

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.